5101 FAMILY
256 X 4 BIT STATIC CMOS RAM

P/N	Typ. Current @ 2V (μA)	Typ. Current @ 5V (μA)	Max Access (ns)
5101L	0.14	0.2	650
5101L-1	0.14	0.2	450
5101L-3	0.70	1.0	650
5101-8	—	10.0	800

- **Single +5V Power Supply**
- **Ideal for Battery Operation (5101L)**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Three-State Output**

The Intel® 5101 is an ultra-low power 1024-bit (256 words X 4 bits) static RAM fabricated with an advanced ion-implanted silicon gate CMOS technology. The device has two chip enable inputs. Minimum standby current is drawn by this device when CE2 is at a low level. When deselected the 5101 draws from the single 5-volt supply only 10 microamps. This device is ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

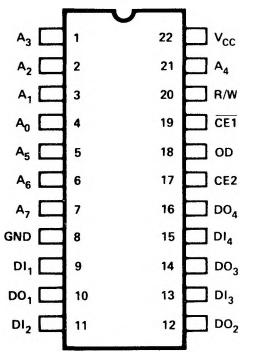
The 5101 uses fully DC stable (static) circuitry; it is not necessary to pulse chip select for each address transition. The data is read out non-destructively and has the same polarity as the input data. All inputs and outputs are directly TTL compatible. The 5101 has separate data input and data output terminals. An output disable function is provided so that the data inputs and outputs may be wire OR-ed for use in common data I/O systems.

The 5101L has the additional feature of guaranteed data retention at a power supply voltage as low as 2.0 volts.

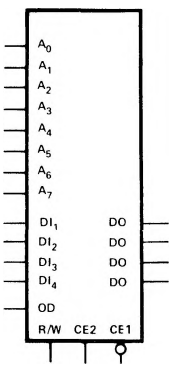
A pin compatible N-channel static RAM, the Intel® 2101A, is also available for low cost applications where a 256 X 4 organization is needed.

The Intel ion-implanted, silicon gate, Complementary MOS (CMOS) process allows the design and production of ultra-low power, high performance memories.

PIN CONFIGURATION



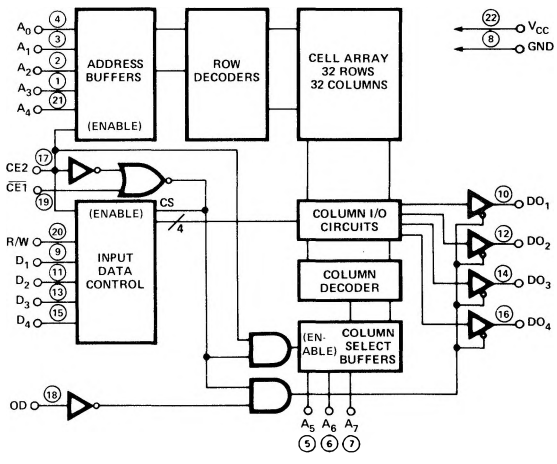
LOGIC SYMBOL



TRUTH TABLE

$\overline{CE_1}$	CE_2	OD	R/W	D_{IN}	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D_{IN}	Write
L	H	L	H	X	D_{OUT}	Read

BLOCK DIAGRAM



Absolute Maximum Ratings *

Ambient Temperature Under Bias . . . . .–10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . -0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage . . . . . +7.0V
Power Dissipation . . . . . 1 Watt

**COMMENT:*

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	5101L and 5101L-1 Limits Min.	Typ.[1]	Max.	5101L-3 Limits Min.	Typ.[1]	Max.	5101-8 Limits Min.	Typ.[1]	Max.	Units	Test Conditions
I_{L2}[2]	Input Current		5			5			5		nA	
$\|I_{LO}\|$[2]	Output Leakage Current			1			1			2	μA	$\overline{CE1}$=2.2V, V_{OUT}= 0 to V_{CC}
I_{CC1}	Operating Current		9	22		9	22		11	25	mA	V_{IN}=V_{CC}, Except $\overline{CE1}$ ⩽ 0.65V, Outputs Open
I_{CC2}	Operating Current		13	27		13	27		15	30	mA	V_{IN}=2.2V, Except $\overline{CE1}$ ⩽0.65V, Outputs Open
I_{CCL}[2]	Standby Current			10			200			500	μA	CE2 ⩽ 0.2V, T_A= 70° C
V_{IL}	Input Low Voltage	-0.3		0.65	-0.3		0.65	-0.3		0.65	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.4	V	I_{OL}=2.0 mA
V_{OH}	Output High Voltage	2.4			2.4			2.4			V	I_{OH}= -1.0 mA

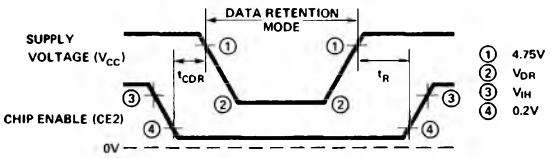
Low V_{CC} Data Retention Characteristics (For 5101L, 5101L-1 and 5101L-3) T_A = 0° C to 70° C

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V		
I_{CCDR1}	5101L or 5101L-1 Data Retention Current		0.14	10	μA	CE2 ⩽ 0.2V	V_{DR}=2.0V, T_A=70° C
I_{CCDR2}	5101L-3 Data Retention Current		0.70	200	μA		V_{DR}=2.0V, T_A=70° C
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[3]			ns		

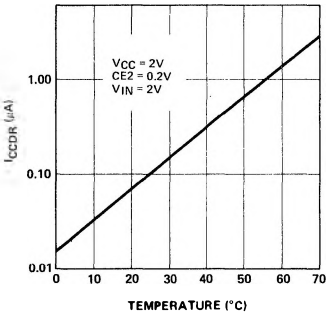
NOTES:

1. Typical values are T_A = 25°C and nominal supply voltage.
2. Current through all inputs and outputs included in I_{CCL} measurement.
3. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform



Typical I_{CCDR} Vs. Temperature



A.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

READ CYCLE

Symbol	Parameter	5101L-1 Limits (ns) Min.	5101L-1 Limits (ns) Max.	5101L and 5101L-3 Limits (ns) Min.	5101L and 5101L-3 Limits (ns) Max.	5101-8 Limits (ns) Min.	5101-8 Limits (ns) Max.
t_{RC}	Read Cycle	450		650		800	
t_A	Access Time		450		650		800
t_{CO1}	Chip Enable ($\overline{CE}$ 1) to Output		400		600		800
t_{CO2}	Chip Enable (CE 2) to Output		500		700		850
t_{OD}	Output Disable to Output		250		350		450
t_{DF}	Data Output to High Z State	0	130	0	150	0	200
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0		0		0	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0	

WRITE CYCLE

t_{WC}	Write Cycle	450	650	800
t_{AW}	Write Delay	130	150	200
t_{CW1}	Chip Enable ($\overline{CE}$ 1) to Write	350	550	650
t_{CW2}	Chip Enable (CE 2) to Write	350	550	650
t_{DW}	Data Setup	250	400	450
t_{DH}	Data Hold	50	100	100
t_{WP}	Write Pulse	250	400	450
t_{WR}	Write Recovery	50	50	100
t_{DS}	Output Disable Setup	130	150	200

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

Output Load: 1 TTL Gate and C_L = 100pF

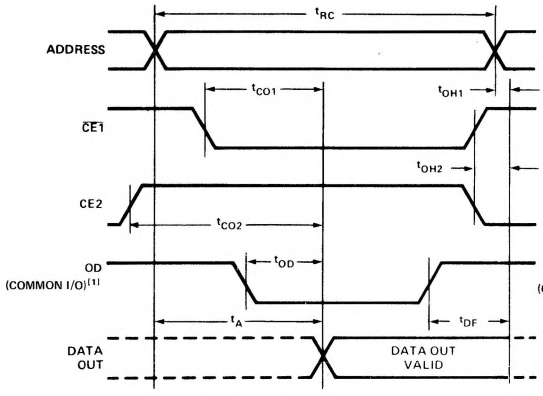
Capacitance[2] T_A = 25°C, f = 1MHz

Symbol	Test	Limits (pF) Typ.	Limits (pF) Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

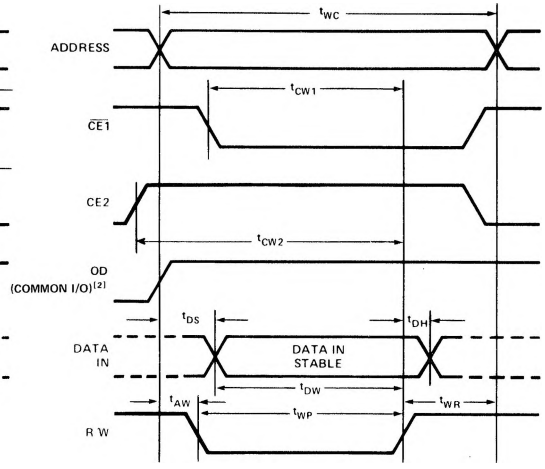
NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

Waveforms

READ CYCLE



WRITE CYCLE



NOTES:

1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.