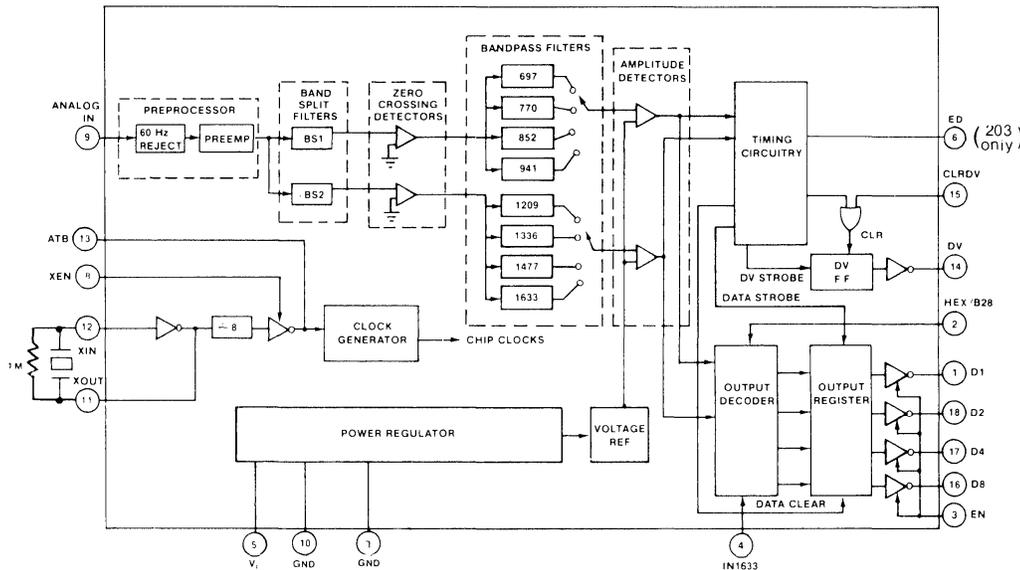
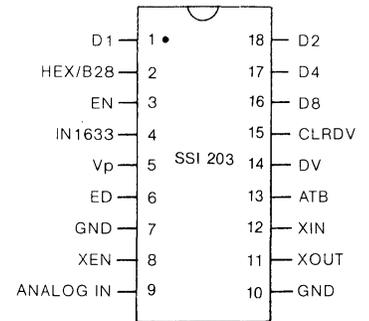
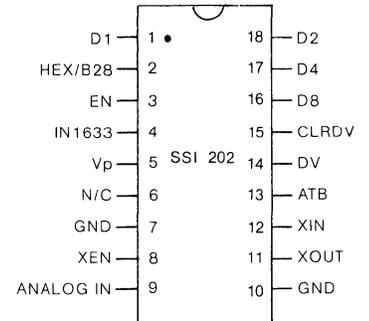


Data Sheet



SSI 202/203 Block Diagram



SSI 202/203 Pin Out
 (Top View)

FEATURES

- Central office quality
- NO front-end band-splitting filters required
- Single, low-tolerance, 5-volt supply
- Detects either 12 or 16 standard DTMF digits
- Uses inexpensive 3.579545-MHz crystal for reference
- Excellent speech immunity
- Output in either 4-bit hexadecimal code or binary coded 2 of 8

- 18-pin DIP package for high system density
- Synchronous or handshake interface
- Three-state outputs
- Early detect output (SSI 203 only)

SPECIAL OPTIONS

- Industrial temperature range available, -40°C to +85°C

DESCRIPTION

The SSI 202 and 203 are complete Dual Tone Multiple Frequency (DTMF) receivers detecting a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.58-MHz television "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is made possible by using the clock output of a crystal connected SSI 202 or 203 receiver to drive the time bases of additional receivers. Both are monolithic integrated circuits fabricated with low-power, complementary symmetry MOS (CMOS) processing. They require only a single low tolerance voltage supply and are packaged in a standard 18 pin plastic DIP.

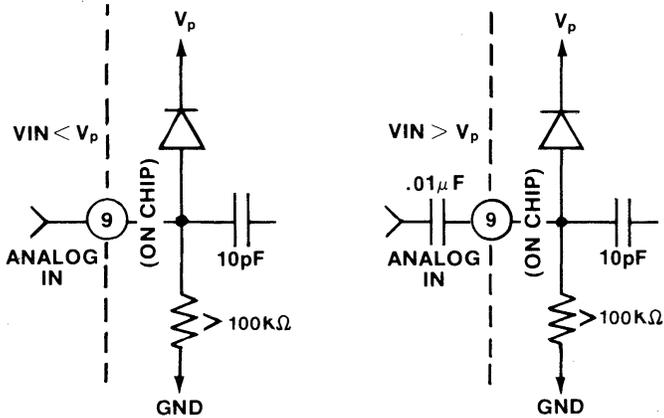
The SSI 202 and 203 employ state-of-the-art circuit technology to combine digital and analog functions on the same CMOS chip using a standard digital semiconductor process. The analog input is pre-processed by 60-Hz reject and band splitting filters and then hard-limited to provide AGC. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

5V Low-Power DTMF Receiver

SSI 202/203

ANALOG IN

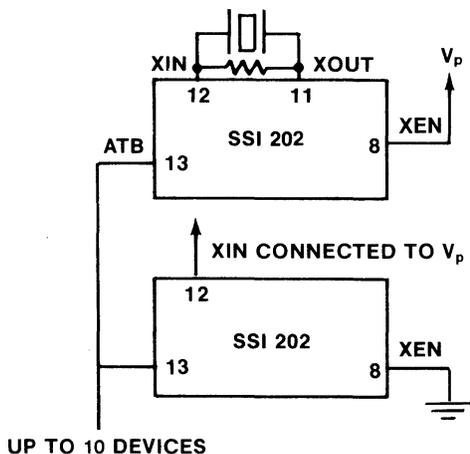
This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated below.



The SSI 202 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than 20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 202 and 203 contain an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 202's (or 203's) may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected SSI 202 or 203 as shown below.



HEX/B28

This pin selects the format of the digital output code. When HEX/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2 of 8. The table below describes the two output codes.

Digit	Hexadecimal				Binary Coded 2 of 8			
	D8	D4	D2	D1	D8	D4	D2	D1
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
0	1	0	1	0	1	1	0	1
*	1	0	1	1	1	1	0	0
#	1	1	0	0	1	1	1	0
A	1	1	0	1	0	0	1	1
B	1	1	1	0	0	1	1	1
C	1	1	1	1	1	0	1	1
D	0	0	0	0	1	1	1	1

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633-Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the code corresponding to the detected digit in the format programmed by the HEX/B28 pin. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed.

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, D8. DV remains high until a valid pause occurs or the CLRDV is raised high, whichever is earlier.

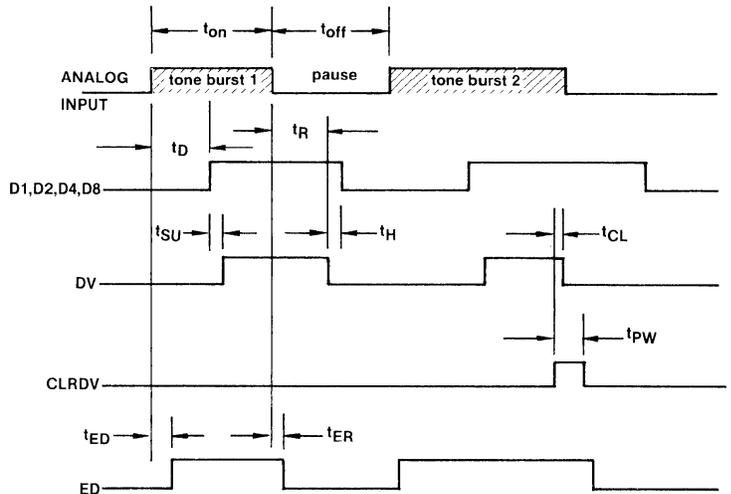
ED (SSI 203 only)

The ED output goes high as soon as the SSI 203 begins to detect a DTMF tone pair and falls when the 203 begins to detect a pause. The D1, D2, D4, and D8 outputs are guaranteed to be valid when DV is high, but are not necessarily valid when ED is high.

N/C PINS

These pins have no internal connection and may be left floating.

SSI 202/203 TIMING



DTMF DIALING MATRIX

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

Note: Column 3 is for special applications and is not normally used in telephone dialing.

DETECTION FREQUENCY

Low Group f_o	High Group f_o
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
TONE TIME: for detection	t_{ON}	40	—	—	mS
for rejection	t_{ON}	—	—	20	mS
PAUSE TIME: for detection	t_{OFF}	40	—	—	mS
for rejection	t_{OFF}	—	—	20	mS
DETECT TIME	t_D	25	—	46	mS
RELEASE TIME	t_R	35	—	50	mS
DATA SETUP TIME	t_{SU}	7	—	—	μ S
DATA HOLD TIME	t_H	4.2	—	5.0	mS
DV CLEAR TIME	t_{CL}	—	160	250	nS
CLR DV pulse width	t_{PW}	200	—	—	nS
ED Detect Time	t_{ED}	7	—	22	mS
ED Release Time	t_{ER}	2	—	18	mS
OUTPUT ENABLE TIME	—	—	200	300	nS
$C_L = 50\text{pF}$ $R_L = 1\text{K}\Omega$					
OUTPUT DISABLE TIME	—	—	150	200	nS
$C_L = 35\text{pF}$ $R_L = 500\Omega$					
OUTPUT RISE TIME	—	—	200	300	nS
$C_L = 50\text{pF}$					
OUTPUT FALL TIME	—	—	160	250	nS
$C_L = 50\text{pF}$					

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ABSOLUTE MAXIMUM RATINGS*

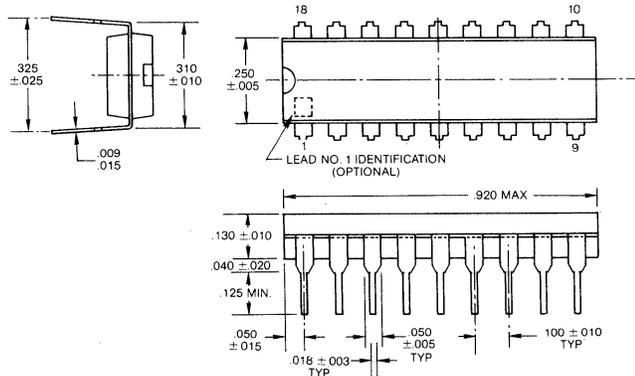
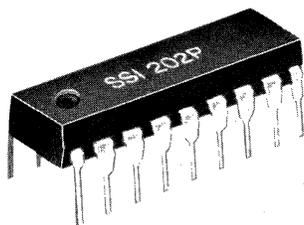
DC Supply Voltage V_p +7 Volts
 Operating Temperature..... 0°C to 70°C Ambient
 Storage Temperature..... -65°C to 150°C
 Power Dissipation (25°C) 65 mW
 (Derate above $T_A = 25^\circ\text{C}$ @ 6.25 mW/°C)

Input Voltage ($V_p + .5\text{V}$) to $- .5\text{V}$
 (All inputs except ANALOG IN)
 ANALOG IN Voltage ($V_p + .5\text{V}$) to ($V_p - 10\text{V}$)
 DC Current into any Input..... $\pm 1.0\text{mA}$
 Lead Temperature 300°C
 (soldering, 10 sec.)

*Operation above absolute maximum ratings may damage the device
 Note: All SSI 202/203 unused inputs must be connected to V_p or Gnd, as appropriate.

ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, $V_p = 5\text{V} \pm 10\%$)

Parameter	Conditions	Min	Typ	Max	Units
Frequency Detect Bandwidth		$\pm(1.5 + 2 \text{ Hz})$	± 2.3	± 3.5	% of f_o
Amplitude for Detection	each tone	-32		-2	dBm referenced to 600 Ω
Minimum Acceptable Twist	twist = $\frac{\text{high tone}}{\text{low tone}}$	-10		+10	dB
60-Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	"precise" dial tone			0dB	dB referenced to lower amplitude tone
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs (except XOUT)	"0" level, 400 μA load "1" level, 200 μA load	0 $V_p - 0.5$		0.5 V_p	Volts Volts
Digital Inputs	"0" level "1" level	0 $0.7V_p$		$0.3V_p$ V_i	Volts Volts
Power Supply Noise	wide band			10	mV p-p
Supply Current	$T_A = 25^\circ\text{C}$		10	16	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB referenced to lowest amplitude tone
Input Impedence	$V_p \geq V_{in} \geq V_p - 10$	100 k Ω //15pF			



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