

**779A TOOL 25-BIT PLUG-IN MATCHER**  
**METHOD OF OPERATION AND TESTS**  
**NO. 1 ELECTRONIC SWITCHING SYSTEM**

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**1. GENERAL**

**1.01** This section describes the procedure for using the 779A tool 25-bit plug-in matcher (bit matcher) in 2-wire and 4-wire No. 1 Electronic Switching Systems (ESS).

**1.02** This section is reissued for the following reasons:

- (a) To add ØFL-MØDE-05 in paragraph 4.02 (7) and (14).
- (b) To make minor changes.
- (c) To delete reference to No. 1 ESS ADF.

**1.03** The bit matcher (Fig. 1) is a manual testing tool. It is used with an oscilloscope to diagnose hardware faults not located by the maintenance program in the system.

**1.04** The bit matcher contains 25 toggle switches and one reset (RST) button (Fig. 1 and 2). The self-contained bit matcher is used to determine the time at which the contents of a flip-flop or register in any logic frame [for example, central control (CC)] reaches a predetermined state. The contents of any register or flip-flop are matched against the state set up manually on its 25 toggle switches. A sync pulse and a match indication

\*\*Reprinted to comply with modified final judgment.

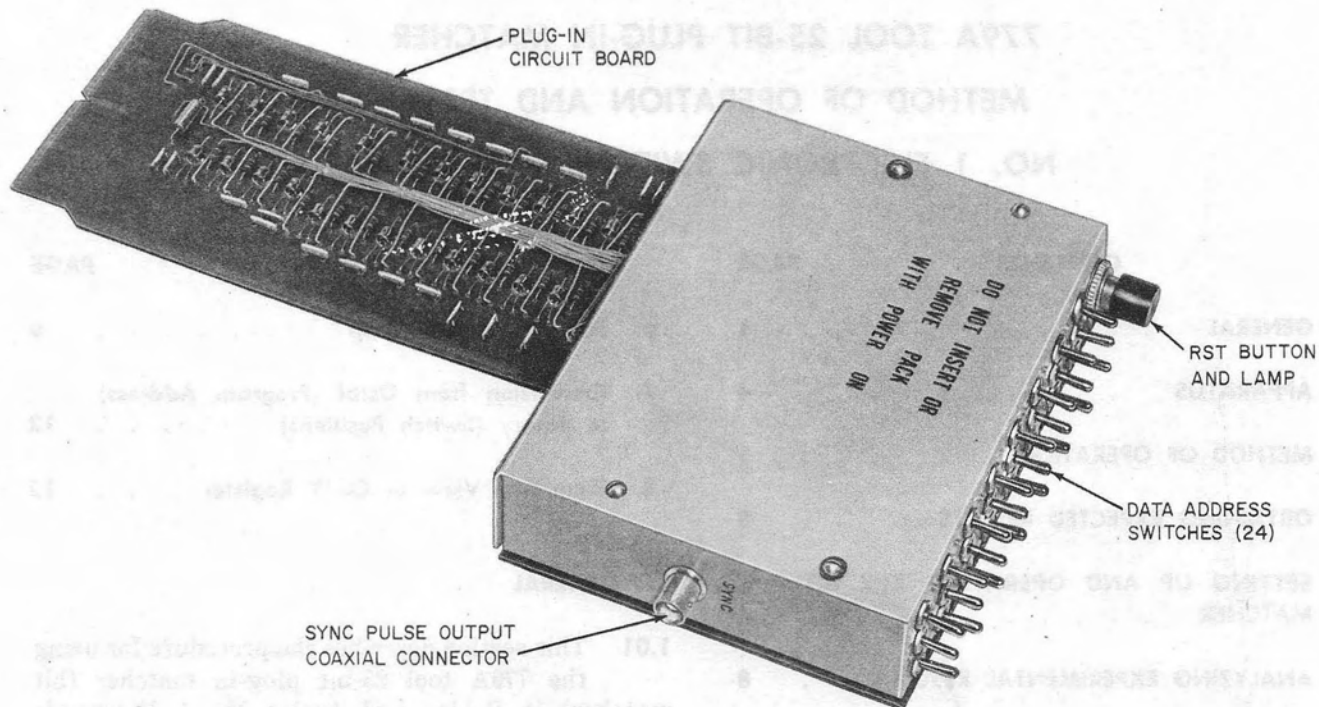


Fig. 1—779A Tool 25-Bit Plug-In Matcher

(lighting of the RST lamp) are generated when a match occurs.

**1.05** Toggle switches 0 through 24 represent 25 bits of information—present on the test connector input pins 0 through 11 and 15 through 27. Each bit can be matched to one of three conditions selected by the switches on the front panel of the bit matcher: one (up), zero (down), or don't care (center). When the 24 bits of information coming into the bit matcher correspond to the setting of the 24 toggle switches, the RST lamp lights. In addition, when the preset conditions are met, a sync pulse is available at the sync pulse output coaxial connector on the bottom of the bit matcher. The sync pulse will be present for the duration of the match condition.

**1.06** The bit matcher plugs into test connectors on the front of the logic frame (Fig. 2). These test connectors normally have access to the zero side of all registers and flip-flops in the logic frame. The bit matcher is most commonly used for troubleshooting with the CC PAR (CC test position 124-27; see SD-1A105-1, B85, C1) and the

CC index adder output register (IAOR) (CC test position 114-13; see SD-1A105-1, B74, H1) test connectors. The PAR test connector (124-27) is provided with one-half microsecond clock signals on pin 27 (6T8) and or pin 26 (14T16) to permit the match condition to be sampled.

**1.07** By sampling the match condition at either 6T8 or 14T16, the possibility of developing a false match condition during the time that the PAR is changing is eliminated. Normally, the 6T8 clock pulse (key 24) should be used. It should be noted that key 24 is set to zero rather than one to provide the 6T8 sample pulse. This is necessary because the PAR test connector pins 26 and 27 are high rather than low when the clock signal is present.

**1.08** To match a program store address, the bit matcher keys should be set up as follows:

- (a) Key 24 should be set to zero.
- (b) Keys 23 through 20 should be set to the dn't-care position.

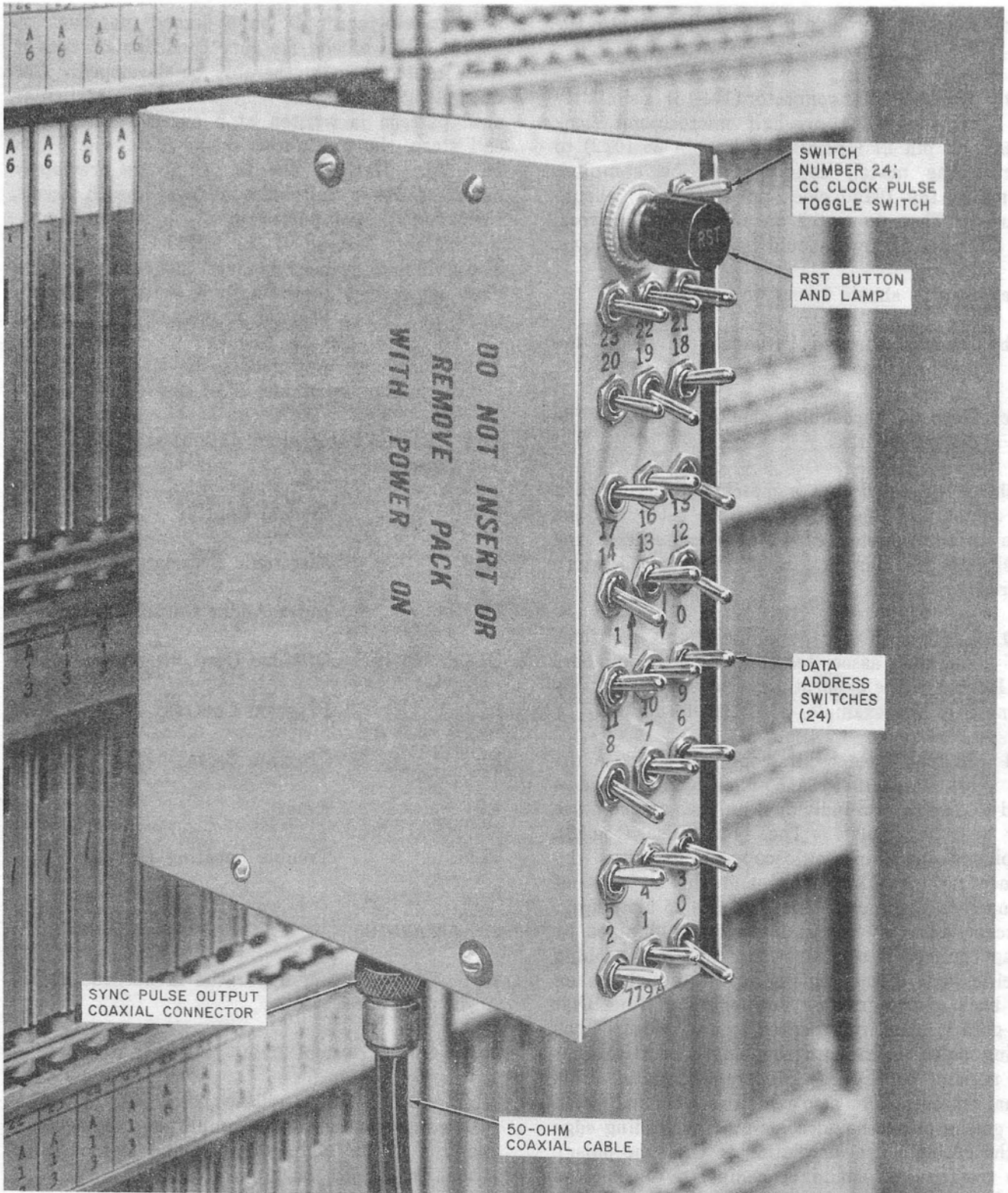


Fig. 2—779A Tool 25-Bit Plug-In Matcher (Example Location on CC)

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- (c) Keys 19 through 0 should be set to the desired address.

1.09 The IAOR test connector (114-13) is similarly provided with one-half microsecond clock signals on pin 27 (18T20) and on pin 26 (OT2) to permit the match condition to be sampled. Normally, the 18T20 clock pulse (key 24) should be used. Thus, to match on a call store address, the bit matcher keys should be set up as follows.

- (a) Key 24 should be set to zero.
- (b) Keys 23 through 18 should be set to the don't-care position.
- (c) Keys 17 through 0 should be set to the desired address.

It should be noted that a match will occur when the contents of the IAOR equal the setting of the keys on the matcher even if the contents of the IAOR are used for data rather than a call store address.

1.10 Listings of other registers and flip-flops and their associated test connector numbers are located in the apparatus indexes of the various frame SDs (for example, SD-1A105-01 for CC).

1.11 A dual trace oscilloscope connected to the bit matchers by a 50-ohm coaxial cable is used to display two individual pulses: a sync pulse and a gating pulse. The sync pulse (Fig. 3), displayed on the oscilloscope, is obtained by connecting the EXT SYNC and the Y input of channel A of the oscilloscope to the 25-bit plug-in matcher (Fig. 4). The gating pulse is obtained by using channel B of the oscilloscope and probing specific logic frame register or flip-flop leads on the back of the frame. The length of time that the gate is open, represented by the width of the gating pulse, represents the length of time that the register or flip-flop can transfer data. This visual representation also exhibits the time at which the gating pulse should come-up (the leading edge of the gating pulse in relation to the sync pulse). The test results should be compared to expected results obtained from interpretation of source material.

1.12 When desired, the output of one matcher can be used as the input to another matcher by connecting the output of the first matcher to

an *unused* input pin on a second matcher. A logical AND of the matcher condition of two or more matchers can, thereby, be developed. For example, if a sync pulse is needed when a particular data pattern is written at a specific location in call store, the configuration shown in Fig. 5 can be used. Matcher one is set up as previously described for a call store address match except that the OT2 clock pulse (key 23) is used to sample the matcher instead of the 18T20 clock (key 24). The OT2 clock is used because the buffer register does not receive the data to be written into call store until T0 on register to memory instructions.

1.13 Reference may need to be made to the bit matcher schematic SD-1A298-01.

1.14 The following abbreviations are used in this section:

CC	Central Control
ESS	Electronic Switching System
IAOR	Index Adder Output Register
OLCP	Off-Line Card Program
PC	Program Control
PS	Program Store
RST	Reset
TLM	Trouble Locating Manual

## 2. APPARATUS

2.01 The following apparatus is needed in this procedure:

- (a) One 779A tool 25-bit plug-in matcher
- (b) An E09-180A oscilloscope kit with an 1801A dual channel vertical amplifier, or equivalent, and a 10005A voltage probe and 10-foot cable that is part of the kit
- (c) One 50-ohm coaxial cable (RG 58/U or RG 58/UA) 8 feet long terminated on each end with a UG-88 B/U male connector
- (d) One T connector (UG-274 B/U).

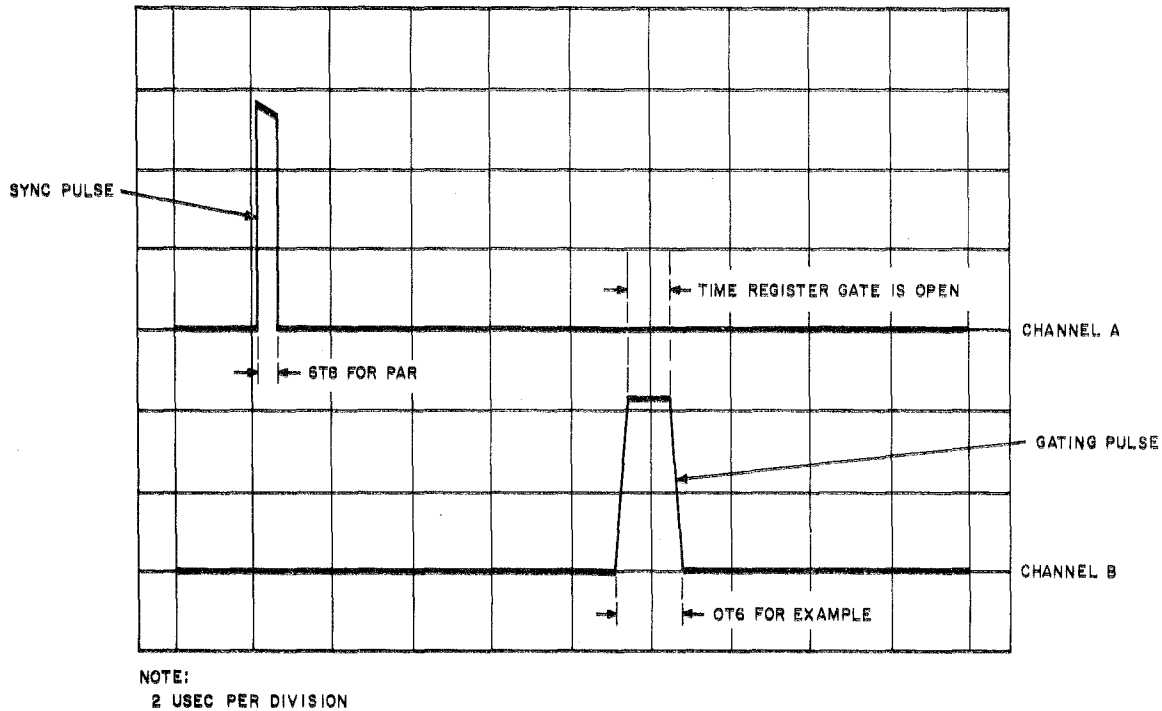


Fig. 3—Oscilloscope Representation of Sync Pulse and Gating Pulse

### 3. METHOD OF OPERATION

**3.01** There are a number of ways to use the bit matcher. The general procedure can be divided into three parts: obtaining expected results from source material, setting up and operating the bit matcher, and analyzing experimental results. Certain other operations have to be performed in the procedure to supplement the operation of the bit matcher, such as removing and restoring the frame power and placing the frame in an off-line configuration. A specific example for using the bit matcher is given in paragraph 3.09.

**3.02** This procedure does not attempt to explain how troubleshooting should be carried out. These techniques are left up to the individual office.

#### OBTAINING EXPECTED RESULTS

**3.03** Information that is needed for setting up and operating the bit matcher and for making a comparative analysis with experimental

results may be obtained from the following source material:

- SD and CD for the faulty frame
- Generic Program Map PK-1A002 (2-wire) and PK-2A002 (4-wire)
- Section 231-117-301 (2-wire) or 231-417-301 (4-wire) (Off-Line Operations)
- Diagnostic program documents (PD and PF) for the specified frame.

Any other source material may be used, if needed, to supplement office troubleshooting techniques.

**3.04** The following data or information must be obtained before using the bit matcher:

- (a) The frame that is faulty
- (b) The register or flip-flop and associated terminal leads to be probed

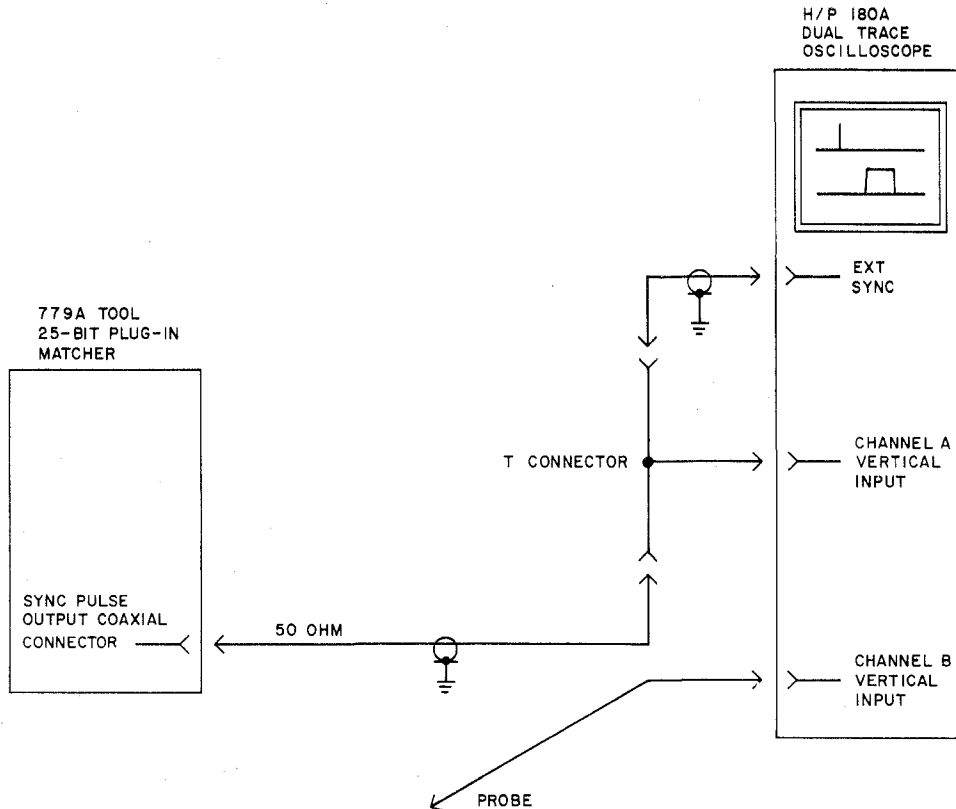


Fig. 4—Connecting Diagram for 779A Tool 25-Bit Plug-In Matcher and Dual Trace Oscilloscope

- (c) The test connector location that accesses the specified register or flip-flop (the PAR and IAOR test connectors in the CC are used most commonly)
- (d) The time at which a sync pulse and gating pulse occur when a specific lead is to be probed
- (e) A series of program addresses that use the specific register or flip-flop being tested
- (f) The lower and upper program address limits that can be used in a program loop
- (g) The program address that is to be matched (address set up on the bit matcher switches)
- (h) The program store, program store bus, call store, and call store bus to be put in off-line configuration.

#### SETTING UP AND OPERATING THE BIT MATCHER

3.05 Use the following general procedure for the bit matcher.

- (1) Remove faulty frame from service and then remove frame power. For the procedure to take the equipment out of service, refer to the following sections:
  - (a) Section 231-405-302 in 4-wire No. 1 ESS offices.
  - (b) Section 231-105-302 in 2-wire No. 1 ESS offices.
- (2) Plug bit matcher into proper frame test connector as determined from information listed in paragraph 3.03.

**Caution:** Do not insert or remove bit matcher when frame power is on.

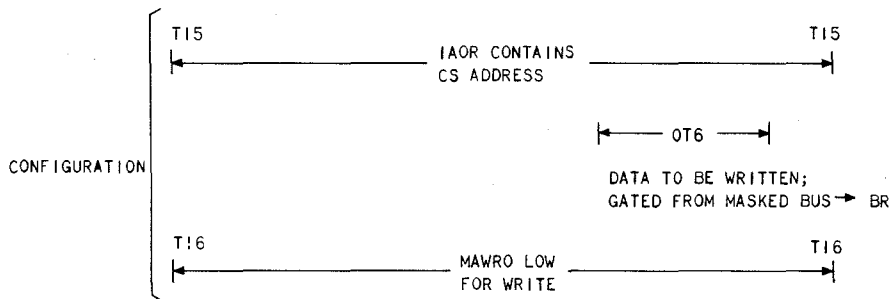
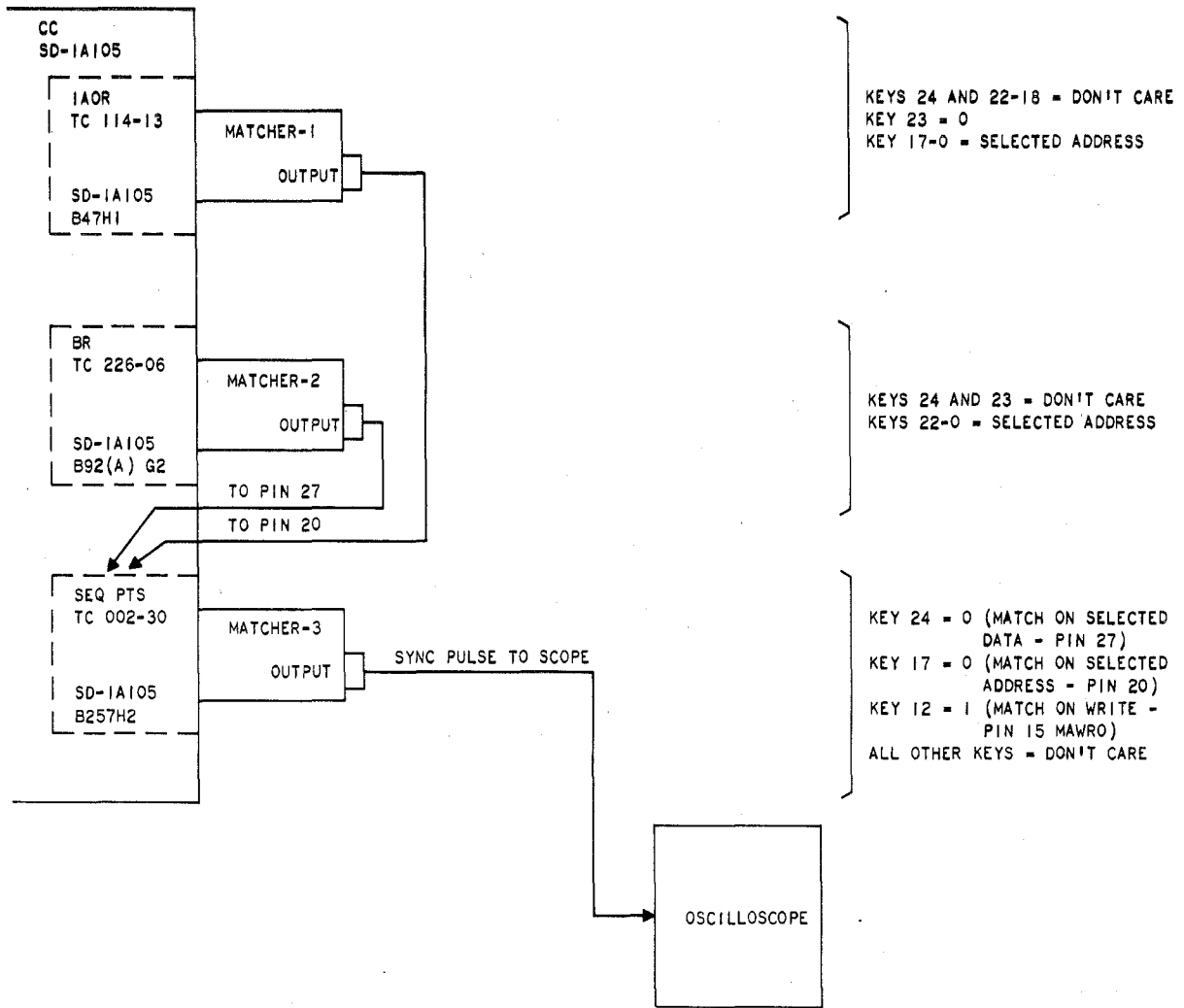


Fig. 5—Matchers Used for Logical AND Gate of Match Condition

- (3) Restore frame power by using procedures in the sections listed in (1).
- (4) Set standby (faulty) frame in off-line configuration. Refer to Section 231-117-301 (2-Wire) or 231-417-301 (4-wire).
- (5) Set up program loop between two program store addresses. Refer to Section 231-117-301 (2-wire) or 231-417-301 (4-wire).
- (6) Start off-line loop. Refer to Section 231-117-301 (2-wire) or 231-417-301 (4-wire).



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- (7) Set desired program address on bit matcher toggle switches.

**Note:** As the program passes through the program address that is set up on toggle switches of bit matcher, RST lamp lights. This switch (RST switch-lamp combination) must be operated before it indicates further matching.

- (8) Connect channel A and EXT SYNC terminals of dual trace oscilloscope to sync pulse output connector on bit matcher using 50-ohm coaxial cable.
- (9) Connect a probe to channel B of dual trace oscilloscope.
- (10) Trigger oscilloscope so that sync pulse is displayed on oscilloscope screen.
- (11) Probe predetermined lead or terminals in the back of faulty or suspected frame.

### ANALYZING EXPERIMENTAL RESULTS

- 3.06** Use the following procedure to analyze the signals displayed on the oscilloscope.

- (1) Determine which pulse is the sync pulse. (Sync pulse is to be used as reference pulse.)
- (2) Determine the time at which the sync pulse occurs by using the CD or SD for that specific register or flip-flop.
- (3) Compare sync pulse to gating pulse as displayed on oscilloscope. Determine the following:
  - Time duration of gating pulse
  - Amplitude of gating pulse
  - The time at which gating pulse occurs in relation to sync pulse

- 3.07** Compare test results to expected results obtained in 3.04. If any discrepancies occur, troubleshoot the equipment and make corrections. The procedure for using the bit matcher may be repeated until the fault has been located and repaired.

- 3.08** Restore system to normal operation by using the following procedure.

- (1) Remove frame from off-line operation. Refer to Section 231-117-301 (2-wire) or 231-417-301 (4-wire).
- (2) Request system to diagnose faulty frame. (Refer to input message manual for diagnostic message for specified frame.)
- (3) Remove frame power by using procedures in the sections listed in paragraph 3.05(1).
- (4) Remove bit matcher from frame test position.
- (5) Restore frame power and return frame to service by using the procedures in the sections listed in paragraph 3.05(1).

### SPECIFIC EXAMPLE USING THE BIT MATCHER

**3.09** This example is used to illustrate one specific use for the bit matcher. A program store (PS) test card is written to accomplish specific operations in the system registers (Fig. 6). Refer to Section 231-104-302 (2-wire) or 231-404-301 (4-wire). This PS test card is located in PS 0 at PS location MOD 1, pass 0, card 73 (1027300) since it is part of the off-line card program (OLCP). The following procedure for using the bit matcher is used.

- (1) Remove the standby CC from service by typing in

CC-REMOVE-

If the system response is OK and the OS lamp on the frame is lighted, power can be removed from the standby CC.

- (2) Remove power from the CC by using the following sequence.
  - (a) Operate FRAME CONTROL—REQ INH (request inhibit) key on CC control panel. OFF NOR and OS lamps light.

**Caution:** In 2-wire ESS do not depress the OFF key until the system prints OK to RMV PWR.



BEGINNING OF PROGRAM LOOP	PROGRAM STORE ADDRESS								
	1027300	00000	00000003	EE	3				
	1027301	00710	00000001	WX	1				
	1027302	00700	00000001	WY	1				
	1027303	00730	00000001	WZ	1				
	1027304	00720	00000001	WL	1				
	1027305	00750	37777777	WK	37777777				
	1027306	00622	00000000	WF	0				
	1027307	00722	00000000	WJ	0				
	1027310	00600	00000000	WR	0				
	1027311	05750	00000000	WK	0,X				
	1027312	00005	20000001	H	1				
	1027313	04710	00000000	WX	0,K				
	1027314	01600	00000001	WR	1,B				
	1027315	11430	00000027	CWR	27,B				
	1027316	00035	21027311	TCLF	1027311				
	1027317	06750	00000000	WK	0,Y				
	1027320	00005	20000001	H	1				
	1027321	04700	00000000	WY	0,K				
	1027322	03722	00000001	WJ	1,J				
	1027323	13430	00000027	CWR	27,J				
	1027324	00035	21027310	TCLF	1027310				
	1027325	07750	00000000	WK	0,Z				
	1027326	00005	20000001	H	1				
	1027327	04730	00000000	WZ	0,K				
	1027330	02622	00000001	WF	1,F				
	1027331	12430	00000027	CWR	27,F				
	1027332	00035	21027307	TCLF	1027307				
	1027333	00754	37777777	WK	37777777..PL				
	1027334	00005	20000001	H	1				
	1027335	04720	00000000	WL	0,K				
	1027336	00031	21027306	TCAU	1027306				
	1027337	00002	01027340	EXC	1027340				
	1027340	00000	00000000	EE	0				
	1027341	00002	01027342	EXC	1027342				
	1027342	00000	00000000	EE	0				
	1027343	00002	01027344	EXC	1027344				
	1027344	00000	00000000	EE	0				
	1027345	00002	01027346	EXC	1027346				
	1027346	00000	00000000	EE	0				
	1027347	00002	01027350	EXC	1027350				
	1027350	00000	00000000	EE	0				
	1027351	00002	01027352	EXC	1027352				
	1027352	00000	00000000	EE	0				
	1027353	00002	01027354	EXC	1027354				
	1027354	00000	00000000	EE	0				
	1027355	00002	01027356	EXC	1027356				
	1027356	00000	00000000	EE	0				
	1027357	00002	01027360	EXC	1027360				
	1027360	00000	00000000	EE	0				

(CONTINUED)

END OF PROGRAM LOOP

(CONTINUED)

Fig. 6—Sample Program Loop

- (b) Operate OFF key to remove power. PWR-OFF lamp lights.
- (3) Plug bit matcher into the standby CC test connector location 124-27 (PAR).

**Caution: Do not insert or remove bit matcher when CC frame power is on.**

- (4) Restore CC frame power by using the following sequence.
  - (a) Operate FRAME CONTROL—REQ INH key.
  - (b) Operate NOR key. OFF NOR lamp extinguishes.
  - (c) Momentarily operate ST key. PWR OFF lamp extinguishes.
  - (d) Momentarily operate CLK ST key.
- (5) Set the standby CC in off-line configuration by typing in  
 ØFL-CØNFIG-00 0 00 0. (CC offices and 4-wire ESS)  
 ØFL-CØNFIG-00 0 00 0 99 0. (SP offices)
- (6) Have standby CC repeatedly execute a program (Fig. 5) by typing in

ØFL-EXEC-03 0...0.(16 0s)

- (7) Set up specified program address (underlined PS address in Fig. 6) on toggle switches of bit matcher as shown in Fig. 7.
- (8) Connect channel A of a dual trace oscilloscope to sync pulse output connector of bit matcher via 50-ohm coaxial cable (Fig. 4). Use this same signal to trigger oscilloscope by connecting it into EXT SYNC terminal of oscilloscope.
- (9) Connect a probe to channel B of oscilloscope.
- (10) Probe MBYR1A lead terminal in the back of CC frame as shown in Fig. 8.
- (11) Analyze results displayed on oscilloscope. The following conclusions can be made.

- (a) Sync pulse is at time 6T8 (obtained from SD- and CD-1A105-01).
- (b) Gating pulse takes place at time 0T6.
- (c) Gating pulse occurs every 11 milliseconds.
- (12) Compare test results with expected results obtained from SD- and CD-1A105-01.
- (13) Remove CC from off-line operations by using the following sequence.

- (a) Type in  
 ØFL-MØDE-02.
- (b) Type in  
 ØFL-MØDE-03.

- (c) Type in  
 ✓ CS-RESTØRE-C S 00. (2-wire)  
 CS-RESTØRE-S 00. (4-wire)

- (d) Type in  
 ✓ CS-RESTØRE-C B 00. (2-wire)  
 CS-RESTØRE-B 00. (4-wire)

- (e) Type in  
 CS-RESTØRE-S 00.

- (14) Request system to diagnose standby CC by typing in

CC-DGN-CCR.

If system response ATP occurs, power can be removed from the unit.

- (15) Remove power from CC. [Refer to paragraph 3.09 (2).]
- (16) Remove bit matcher from test position.
- (17) Restore power to the standby CC. [Refer to paragraph 3.09 (4).]

- (18) Standby CC restored to service and verified by ATP response.

#### 4. TESTING THE BIT MATCHER

**4.01** Office hardware faults which require the use of the bit matcher tool for diagnosis occur infrequently. Therefore, it is recommended that the tool be tested periodically to assure its operation and availability when the need does occur. The recommended test interval is at least every 6 months, or at any time when the tool may be suspected for any reason. Care should be exercised in storing and handling the tool to prevent any physical damage.

**4.02** Much of the procedure described in paragraph 3.09 is similar to that which is used to test the bit matcher. The off-line facility is set up to test each bit of the bit matcher for the following conditions:

- (a) Match on one
- (b) Match on zero
- (c) Don't care.

The example described in paragraph 3.09 uses the bit matcher and a specific program address to verify that the sync pulse is generated upon a match condition. In the following test, the sync pulse generation is assumed operating with the RST lamp used as the visual indicator of a match condition for each bit.

- (1) Remove standby CC from service by typing in

CC-REMOVE.

If the system response is OK and the OS lamp on the frame is lighted, power can be removed from the standby CC.

- (2) Remove power from the CC by using the following sequence.

- (a) Operate FRAME CONTROL—REQ INH (request inhibit) key on CC control panel. OFF NOR and OS lamps light.

**Caution: In 2-wire ESS do not depress the OFF key until the system prints OK TO RMV PWR.**

- (b) Operate OFF key to remove power. PWR OFF lamp lights.
- (3) Plug bit matcher into standby CC test connector location 218-11 (XR).

**Caution: Do not insert or remove bit matcher when CC frame power is on.**

- (4) Restore CC frame power by using the following sequence.
  - (a) Operate FRAME CONTROL—REQ INH key.
  - (b) Operate NOR key. OFF NOR lamp extinguishes.
  - (c) Momentarily operate ST key. When ST key is operated, PWR OFF lamp extinguishes.
  - (d) Momentarily operate CLK ST key.
- (5) Set up off-line configuration by typing in

ØFL-CØNFIG-00 0 00 0. (CC Offices)

✓ ØFL-CØNFIG-00 0 00 0 99 0. (SP Offices)

ØL01 ØK response.

#### MATCH ON ZERO TEST

- ✓ (6) **2-Wire ESS only:** Set up program control (PC) keys at MCC to all zeros by releasing pushbuttons at positions zero through 22. BLCK (block) key should be released and remain released throughout the entire test procedure. Later, when all ones are entered into the PC keys and if the BLCK key is depressed, maintenance printouts will be inhibited.

- (7) **2-Wire ESS:** Set up off-line program by typing in

✓ ØFL-MØDE-05

✓ ØFL-EXEC-09 00010000 00010000

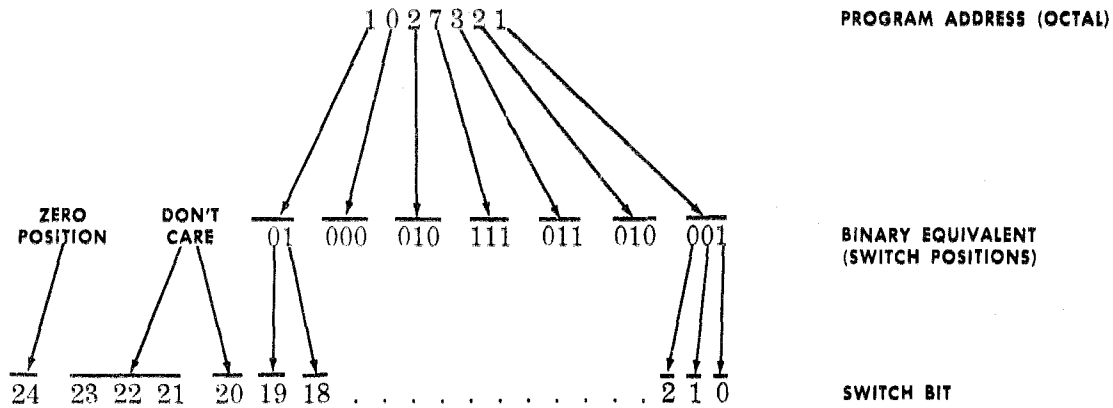


Fig. 7—Conversion From Octal (Program Address) to Binary (Switch Positions)

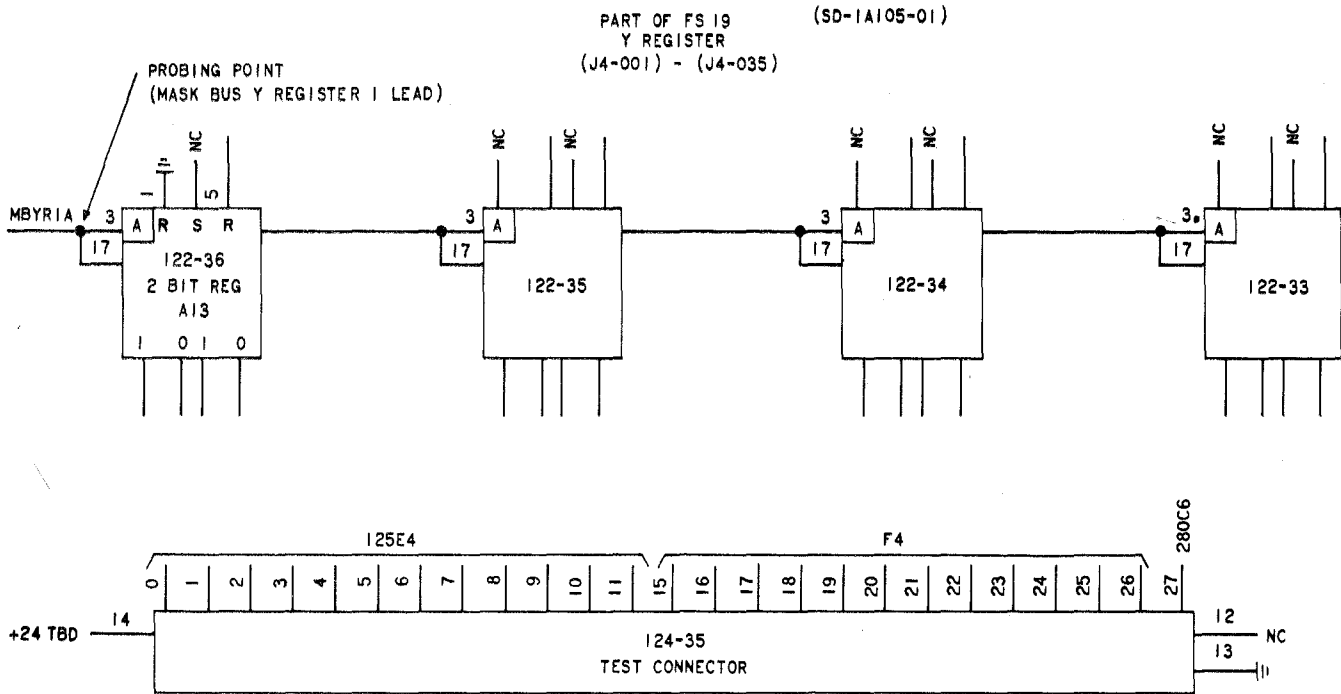


Fig. 8—Simplified View of CC Y Register

Contents of PC keys will be written into CS 0 at address 10,000 every cycle.

ØFL-EXEC-10 00010000 00010000.

**4-Wire ESS:** Set up off-line program by typing in

ØFL-MØDE-05.

(8) **2-Wire ESS and 4-Wire ESS:** Place all toggle switches on the matcher tool in the don't-care position. Operate the RST lamp/switch. RST lamp should remain on.

SEE - ADDENDUM

(9) Place toggle switch 0 in the one position. Operate RST. RST lamp should extinguish (mismatch).

ØFL-MØDE-05. 02 01 11 11

✓ ØFL-EXEC-09 00010000 00010000.

Contents of PC keys, all ones, will be written into CS 0 at address 10,000 every cycle.

(10) Place toggle switch 0 in the zero position. RST lamp should light (match). Operate RST. RST lamp should remain on. Leave toggle switch 0 in the zero position.

4-Wire ESS: Type in

ØFL-MØDE-05.

ØFL-EXEC-09 00010000 00010000.

(11) Repeat the test in Steps 9 and 10 individually for each toggle switch (1 through 22). When in the one position, lamp should extinguish; when in the zero position, lamp should light. After each test, switch is left in the zero position, eventually leading to an all zeros match.

(15) **2-Wire ESS and 4-Wire ESS:** Place all toggle switches of the matcher tool in the don't-care position, except for toggle switch 0, which should be left in the zero position. Operate RST. Lamp should extinguish (mismatch).

Bits 23 and 24 toggle switches (23 and 24) are no-connects at the XR test connector location and, because of the tool's circuitry, will represent one inputs. If these positions are suspected of match-on-zero problems, pick a convenient 4.5 V point, such as an unused 4.5V load resistor (location 218-17, unused LR terminals 2 through 11) and apply it to the following XR test connector terminals in turn: (1) terminal 26 to test switch position 23 and (2) terminal 27 to test position 24.

(16) Place toggle switch 0 in the one position; lamp should light (match). Leave toggle switch 0 in the one position.

(17) Repeat test for each toggle switch (1 through 24). Whenever in the zero position, the lamp should extinguish when RST is operated; whenever in the one position, the lamp should light and remain lighted before and after RST is operated. After each test, each switch should be left in the one position, which eventually leads to the all ones match.

**MATCH ON ONE TEST**

(12) Type in

✓ ØFL-MØDE-02.

This message stops the standby CC for next series of tests.

(13) **2-Wire ESS:** Set up MCC PC keys to the all ones position by pushing keys down at bits 0 through 22. BLCK key should remain released.

**4.03** The above test verifies each bit for the match-on-one, the match-on-zero, and the don't-care conditions. Now proceed to terminate the off-line mode and restore the system by following the sequence shown in paragraph 3.09, Steps 13 through 18. This entire test procedure requires approximately 15 minutes to complete.

(14) **2-Wire ESS:** Type in

**4.04** If the bit matcher tool fails any part of the above test, it should be sent, through normal forwarding procedures, to the WE repair control location for necessary repairs.

# GO TO PAGE 10 STEP 13 OF PAR. 3.09 FOR RESTORAL.

**779A TOOL 25-BIT PLUG-IN MATCHER**  
**METHOD OF OPERATION AND TESTS**  
**NO. 1 ELECTRONIC SWITCHING SYSTEM**

**1. GENERAL**

**1.001** This addendum supplements Section 231-001-301, Issue 6 and replaces Issue 1 of this addendum. Place this pink sheet ahead of Page 1 of the section and discard Issue 1 of this addendum.

**1.002** This addendum is reissued to correct TTY input messages for the match on one test in paragraph 4.02.

**1.003** Issue 1 of this addendum was issued to correct ØFL-EXEC-09 and ØFL-EXEC-10 input messages in paragraph 4.02.

**2. CHANGES TO SECTION**

**ISSUE 1 CHANGES**

**2.001** On Pages 11 and 12, change Step (7) to read as follows:

(7) **2-Wire ESS:** Set up off-line program by typing in

ØFL-MODE-05.  
ØFL-EXEC-09 00010000 00010001.

Contents of PC keys will be written into CS 0 at address 10,000 every cycle.

**4-Wire ESS:** Set up off-line program by typing in

ØFL-MODE-05.  
ØFL-EXEC-10 00010000 00010001.

**2.002** On Page 13, change Step (14) to read as follows:

(14) **2-Wire ESS:** Type in  
ØFL-MODE-05.  
ØFL-EXEC-09 00010000 00010001.

Contents of PC keys, all ones, will be written into CS 0 at address 10,000 every cycle.

**4-Wire ESS:** Type in  
ØFL-MODE-05.  
ØFL-EXEC-09 00010000 00010001.

**ISSUE 2 CHANGES**

**2.003** On Page 13, change step (14) to read as follows:

(14) **2-Wire ESS:** Type in  
PS-RESTORE-SOO.  
CC-REMOVE-ØK.  
Power Cycle CC-(PS power restored)  
Type in 00 000 0 990  
ØFL-CONFIG-0\_ \_ \_ \_ \_PF  
ØFL-MODE-05.ØK.  
ØFL-EXEC-09 00010000 00010001.ØK.

Contents of PC keys, all ones, will be written into CS 0 at address 10,000 of every cycle.

**4-Wire ESS:** Type in  
ØFL-MODE-05.  
ØFL-EXEC-09 00010000 00010001.

**NOTICE**

Not for use or disclosure outside the  
Bell System except under written agreement