ANALYZING AND LOCATING TROUBLE IN THE 8K CALL STORE

NO. 1 ELECTRONIC SWITCHING SYSTEM

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TABLES

1. GENERAL

1.01 This section provides an approach to locating and analyzing many of the malfunctions that can occur in the 8K call store used in 2W and 4W No. 1 ESS. Using a flowchart as a general procedure allows the detailed procedure to be referenced on the flowchart.

1.02 This section is reissued to include CTX-6 Issue 8 and later generics and to make the following changes:

(a) To make changes to Fig. 4 and 17

(b) To add Tables H and I.

1.03 The call stores (CSs) are memory units that store information related mainly to the handling of calls as they are processed. The CS is used for short term scratch pad storage of events that occur in the No. 1 Electronic Switching System (ESS). Certain long term information is also stored temporarily in the CS until enough of such information accumulates to make it worthwhile to write it into the program store memory cards.

1.04 The CSs are erasable read-write temporary memories used by the central control (CC) and the signal processor (SP). The information contained in a CS is organized in words of 24 bits. The 24th bit of each word is used for parity checking. Each word occupies one location in the memory unit of the CS and is identified by a unique address. Inputs from a CC or an SP specify the operation (reading or writing), CS address, and data (writing only). The CS responds to the order and, in the case of reading, sends the word read to the CC or SP.

1.05 The memory unit of each CS consists of four memory modules. Two of these modules are connected to make the G-half of the memory unit. The other two modules are connected to make the H-half of the memory unit. Each half has a storage capacity of 4096 words (24 bits each), and each CS memory has 8192 storage addresses. In order to achieve maximum reliability, all information stored in the H-half of one CS is duplicated in the G-half of another CS and vice-versa

(Fig. 1). The CC or SP communicates with the CSs over duplicated buses.

1.06 The number of CSs needed in each No. 1 ESS depends on the office size. For example, in a 2-wire No. 1 ESS office, a maximum of 39 CSs (78 store halves) can be used with the pair of CCs and a maximum of 8 CSs (16-store halves) can be used with each duplicated pair of SPs.

1.07 The following abbreviations are used in this section:

ASW	All Seems Well
C	Celsius Temperature
CPD	Central Pulse Distributor
CS	Call Store
CW	Control Write
CR	Control Read
ESS	Electronic Switching System
FF	Flip Flop
MCC	Master Control Center
SD	Signal Distributor
SP	Signal Processor

2. REFERENCE DOCUMENTS

CD-1A124-01	Circuit Description
IM-1A001	Input Message Manual
OM-1A001	Output Message Manual
PA-591003	Translation Specification
PD-1A018	Call Store Deferred Fault Recognition Programs Description
PD-1A019	Diagnostic Program Description
PD-1A120	Translation Program Description
PF-1A019	Program Flowchart
PK-1A019	Raw Data Analysis
PR-1A019-26	Program Listing
SD-1A124-01	Schematic Drawing
TLM-1A124	Trouble Locating Manual

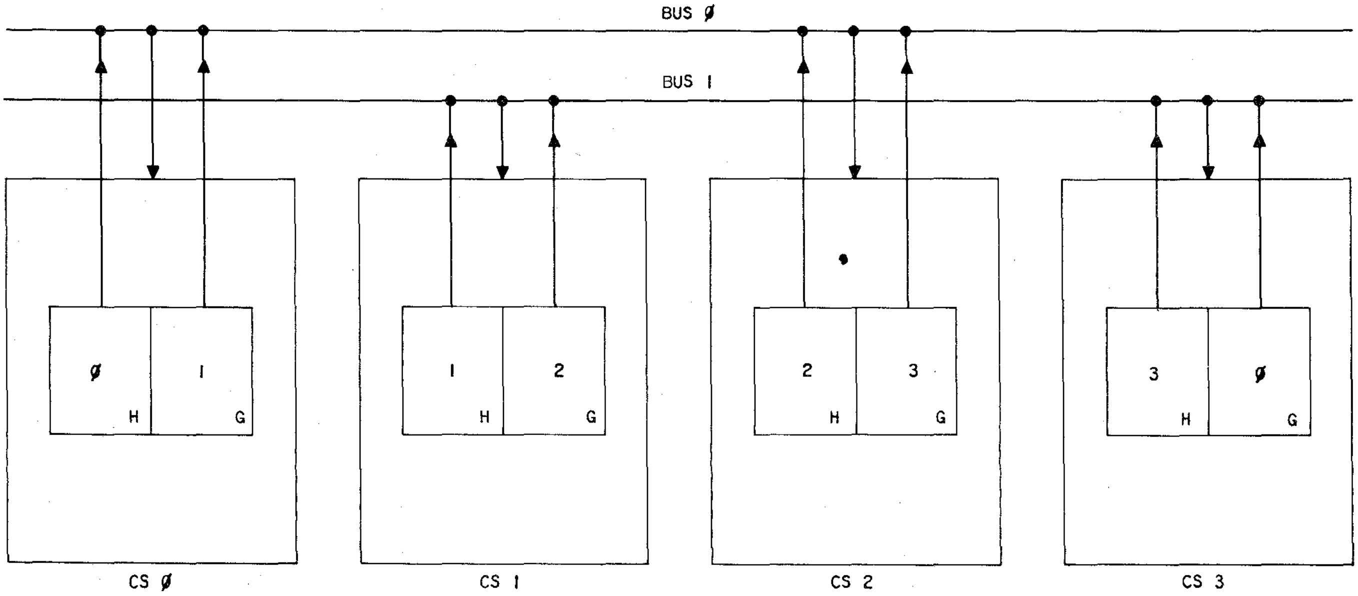


Fig. 1—Call Store Duplication and Bus Duplication

231-006-101	8K Call Store Description
231-006-501	8K Call Store Margin Checks—Using 762A Tool
231-006-801	8K Call Store Memory Assembly Replacement Procedure
231-011-102	Maintenance Program Organization Description
231-109-301	Analyzing Maintenance Interrupts
231-125-301	Master Control Center—Alarm, Display, and Control Panel—Method of Operation

3. CALL STORE TROUBLESHOOTING OVERVIEW

3.01 The flowchart in Fig. 2 gives an overall indication of the types of CS troubles that can be encountered. The flowchart also references the procedure that can be used in troubleshooting.

3.02 The basis of the flowchart layout is to deal with one type of trouble at a time.

4. DIAGNOSTIC FAILURES

NORMAL DIAGNOSTIC FAILURE

4.01 A normal diagnostic printout can be generated by the system. It can also be requested via the TTY with the CS-DGN input message (refer to IM-1A001 for complete message) or via the appropriate CS frame control. The output message is as follows:

```
DR01 DGN RES CS 2
0577 0034 6600 = universal trouble number.
```

4.02 The first line of the above message identifies the failing unit as CS 2. Line two contains the 12-digit trouble number that may be found in TLM-1A124. First, however, the maintenance personnel should request another diagnosis to insure a solid fault. The flowchart procedure is given in Fig. 3. A step-by-step procedure is given in TLM-1A124, Section B.

RAW DIAGNOSTIC FAILURE

4.03 The CS diagnostic program is comprised of a series of diagnostic tests. Basically, it divides the CS into four functional hardware blocks. The tests are run first on bus 0, then on bus 1 (Table A). Figure 4 gives a flowchart approach to troubleshooting a CS using the raw data printout.

Phase 1 and Phase 5

4.04 Phase 1 and phase 5 are used to test basic internal CS circuitry associated with routing, lockout conditions, and voltage levels. Most of the tests in these phases are carried out by operating central pulse distributor (CPD) points or relays within the CS, and scanning either the CS monitor bus or private scan points to verify expected results. A list of primary hardware tested by these phases is shown in Table B. The tests that are run are shown in Table C.

4.05 The CS monitor bus consists of eight scan points having a fixed assignment on master scanner 00, row 50, ferrods 0 through 7. These scan points are connected to all the CSs in the office. However, only the store currently being diagnosed will have relays operated to connect the monitor bus leads to the internal CS circuitry.

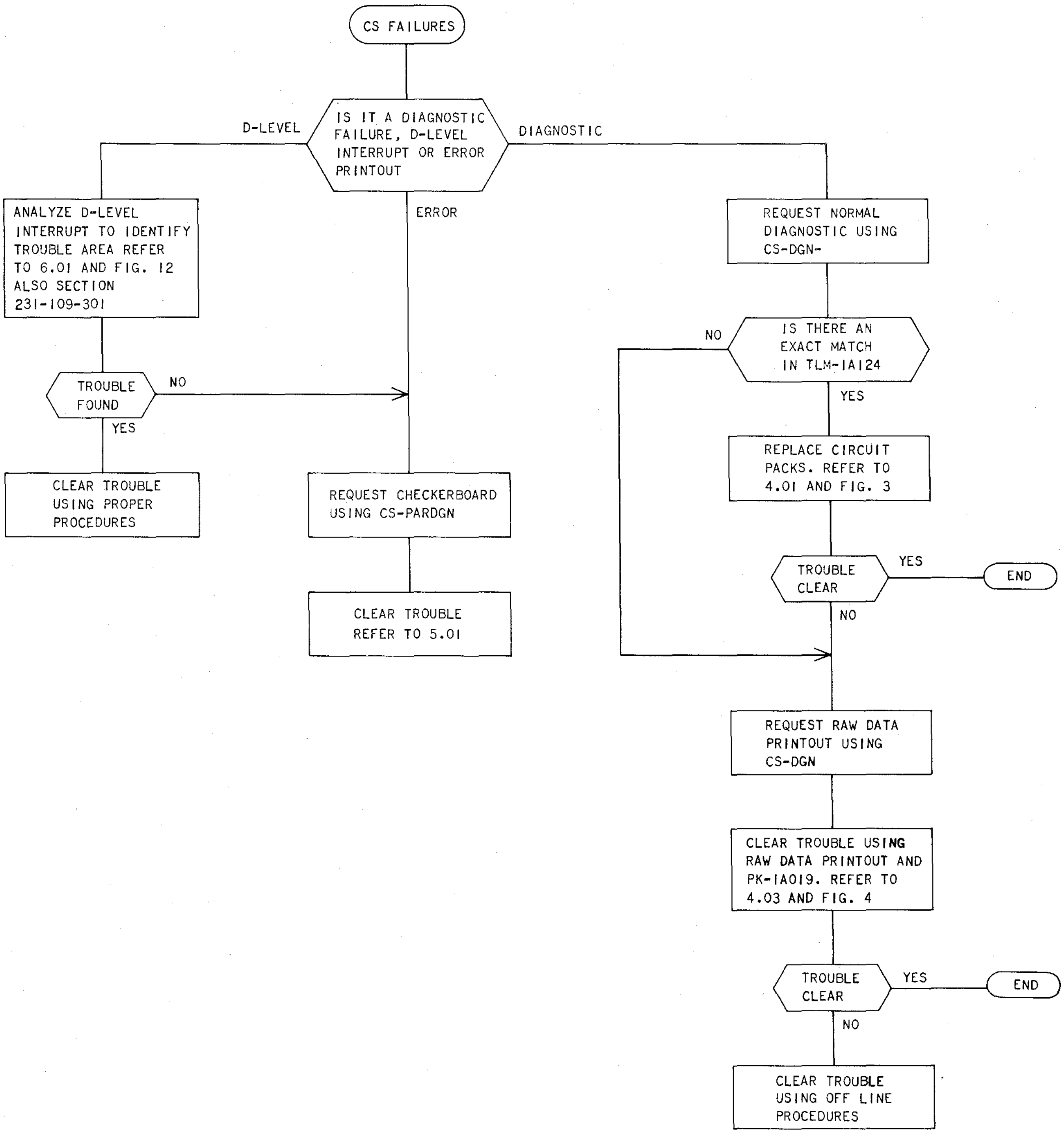


Fig. 2—General Troubleshooting Flowchart

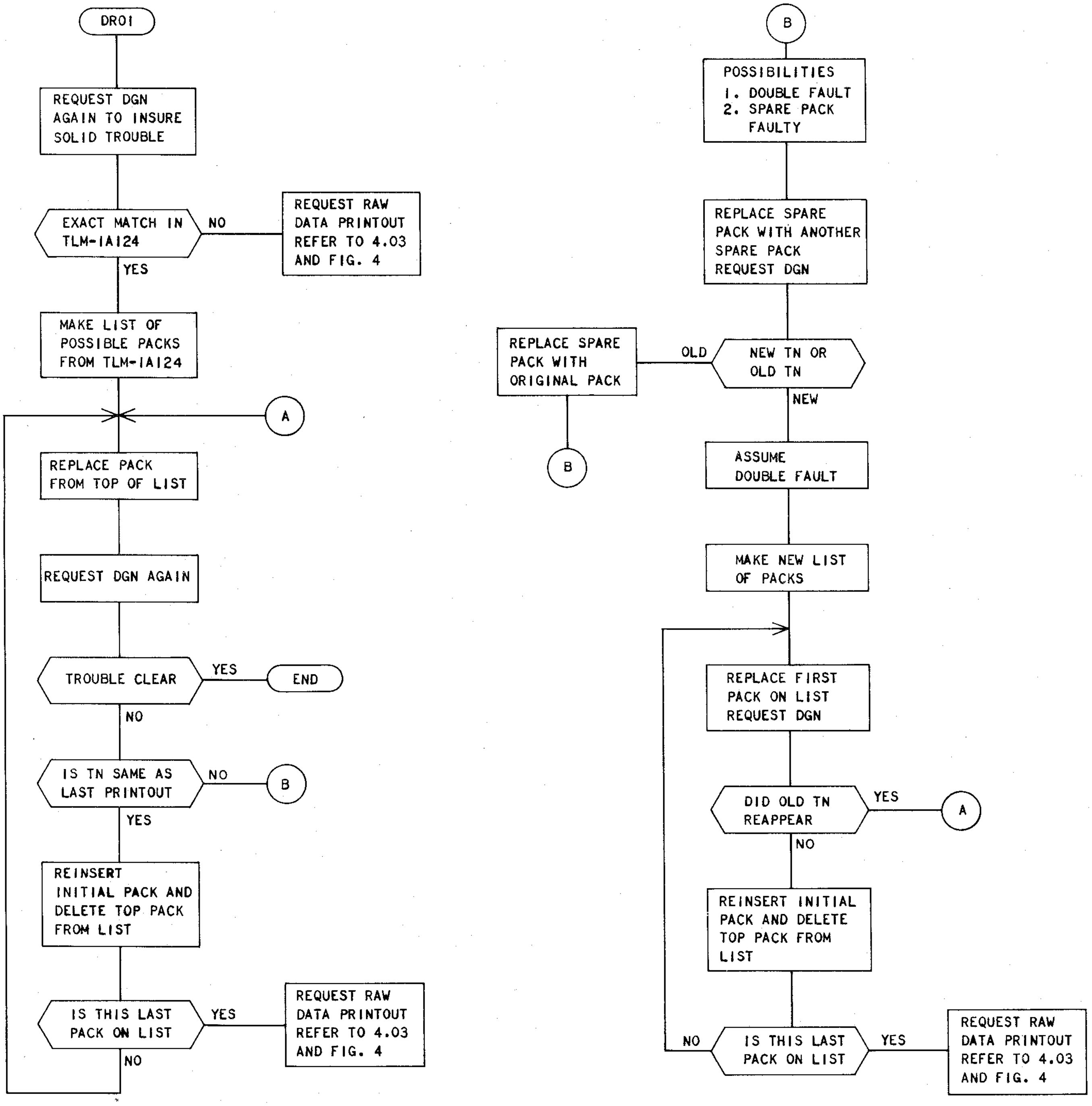
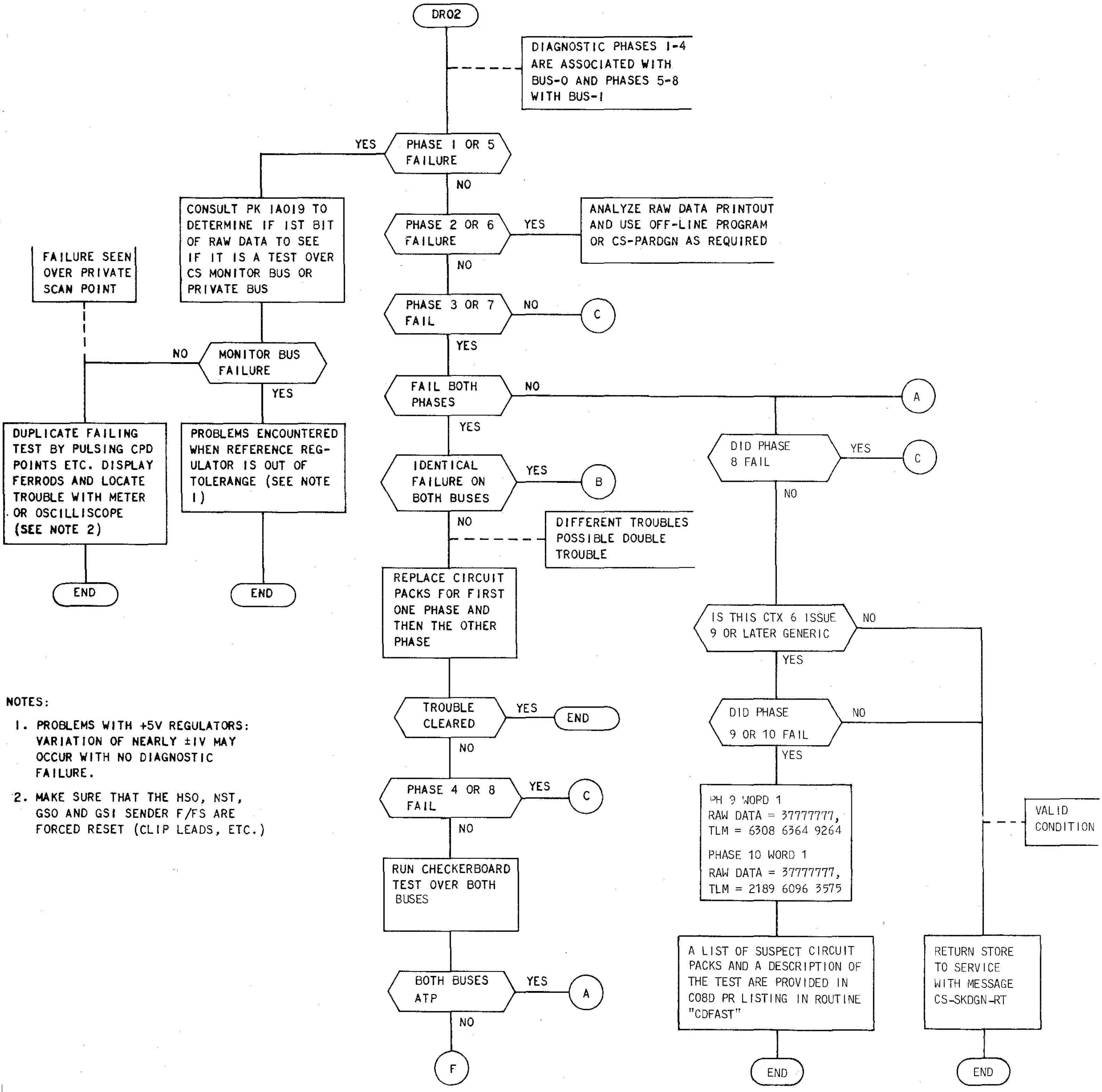


Fig. 3—Normal Diagnostic Troubleshooting Flowchart

TABLE A

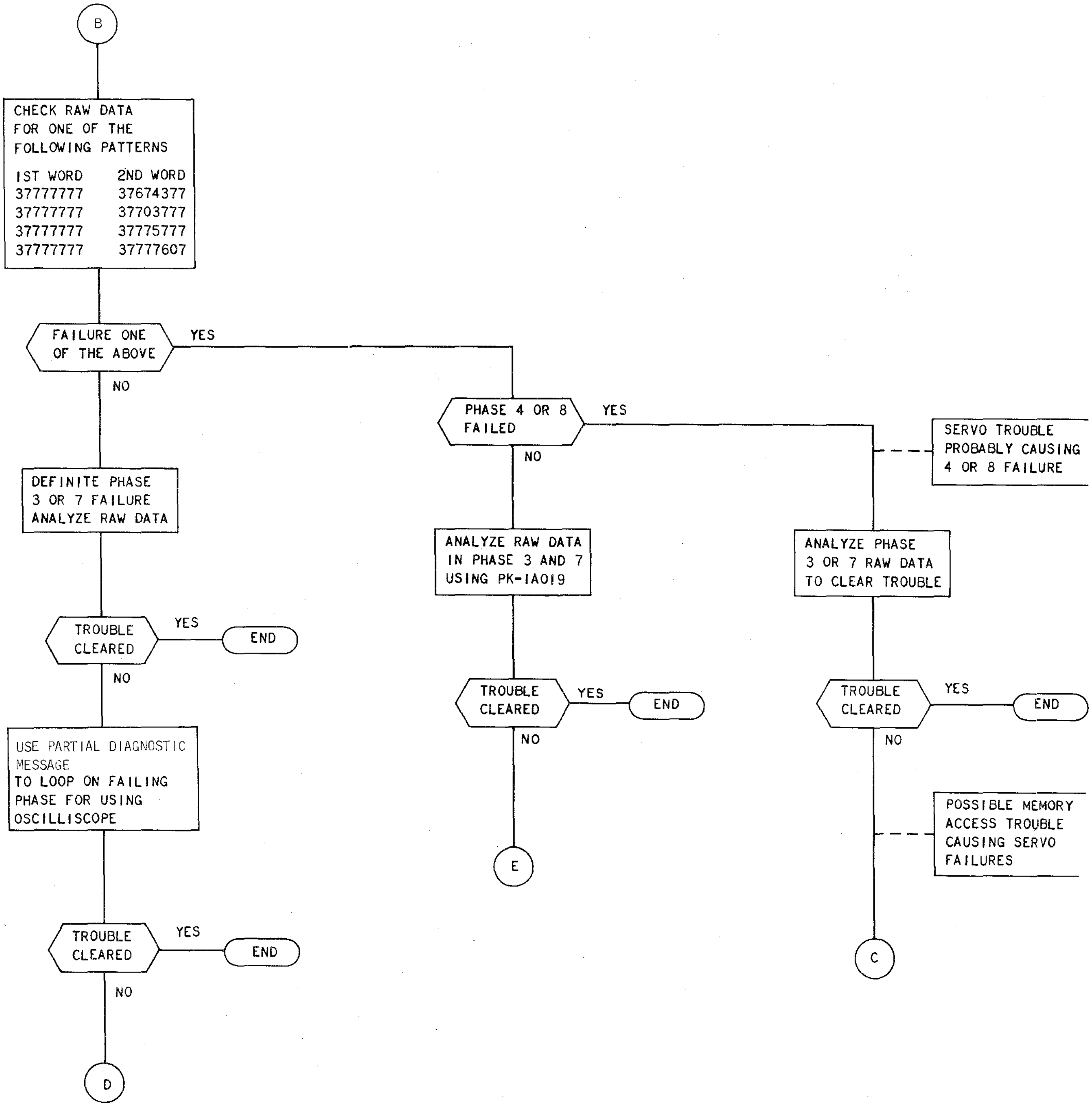
CALL STORE DIAGNOSTIC

PHASE	NO. OF WORDS OF TEST DATA GENERATED	PRIMARY HARDWARE TESTED PER PHASE
1	29	CPD, SD, and MS access to the call store via CS bus 0
2	40	Control and maintenance logic circuitry via CS bus 0
3	2	CS X and Y servo counters via CS bus 0
4	9	Memory access and logic circuitry via CS bus 0
5	29	CPD, SD, and MS access to the call store via CS bus 1
6	40	Control and maintenance logic circuitry via CS bus 1
7	2	CS X and Y servo counters via CS bus 1
8	9	Memory access and logic circuitry via CS bus 1



NOTES:

1. PROBLEMS WITH +5V REGULATORS: VARIATION OF NEARLY ±1V MAY OCCUR WITH NO DIAGNOSTIC FAILURE.
2. MAKE SURE THAT THE HSO, NST, GSO AND GS1 SENDER F/FS ARE FORCED RESET (CLIP LEADS, ETC.)


B
CHECK RAW DATA FOR ONE OF THE FOLLOWING PATTERNS
1ST WORD 2ND WORD
37777777 37674377
37777777 37703777
37777777 37775777
37777777 37777607
FAILURE ONE OF THE ABOVE
YES
NO
DEFINITE PHASE 3 OR 7 FAILURE ANALYZE RAW DATA
TROUBLE CLEARED
YES
END
NO
USE PARTIAL DIAGNOSTIC MESSAGE TO LOOP ON FAILING PHASE FOR USING OSCILLISCOPE
TROUBLE CLEARED
YES
END
NO
D
PHASE 4 OR 8 FAILED
YES
NO
ANALYZE RAW DATA IN PHASE 3 AND 7 USING PK-1A019
TROUBLE CLEARED
YES
END
NO
E
SERVO TROUBLE PROBABLY CAUSING 4 OR 8 FAILURE
ANALYZE PHASE 3 OR 7 RAW DATA TO CLEAR TROUBLE
TROUBLE CLEARED
YES
END
NO
POSSIBLE MEMORY ACCESS TROUBLE CAUSING SERVO FAILURES
C

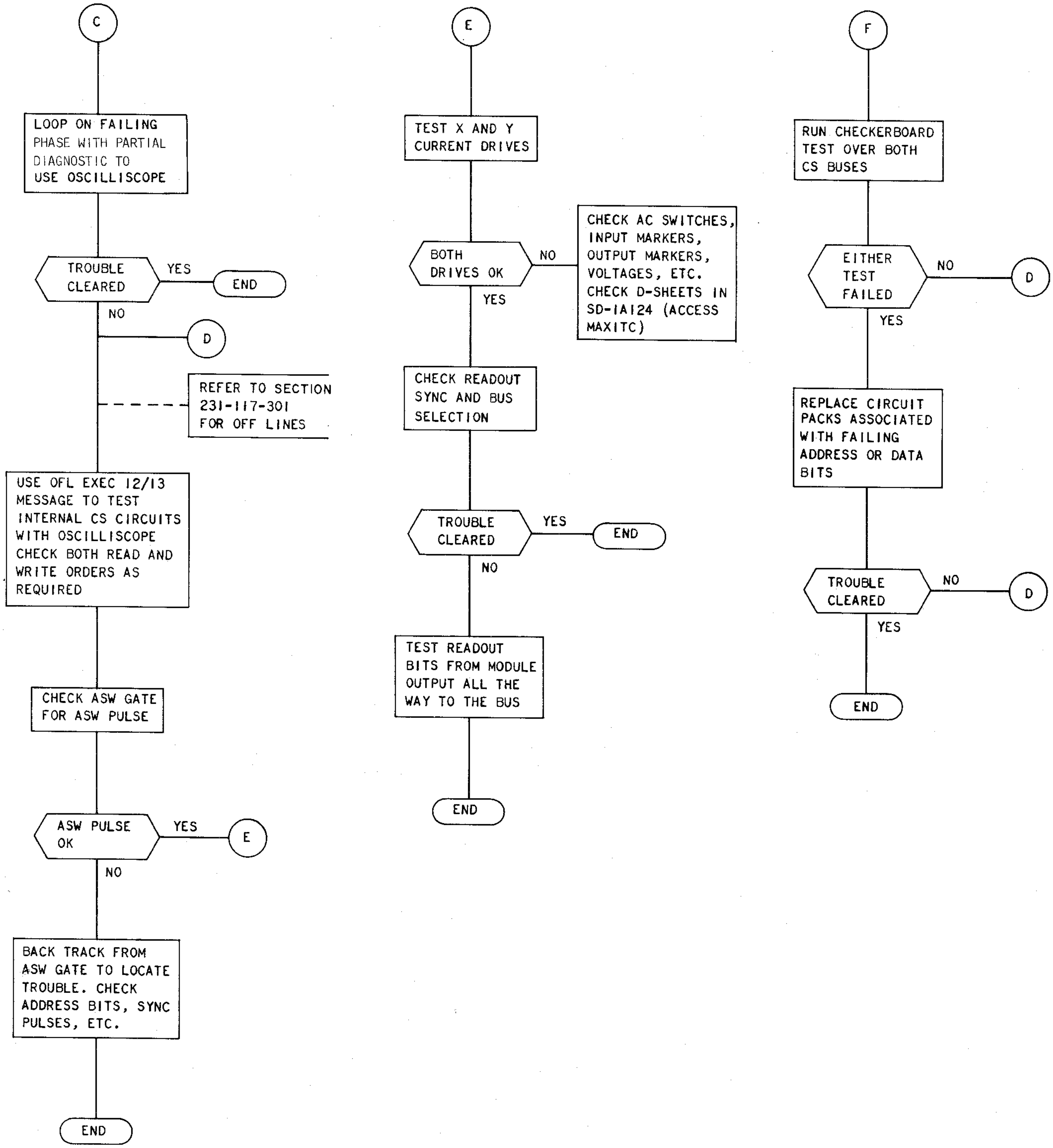


Fig. 4—Raw Data Analysis Flowchart

TABLE B

PRIMARY HARDWARE TESTED BY PHASE 1 AND PHASE 5

FS IN SD-1A124	DESCRIPTION
33	CS (i) lamp fuse
33	CS (i) manual control panel status and fuse alarm
	Lockout conditions and circuitry
24	(a) Permanent RO sync
24	(b) Permanent precharge enable
21	(c) Permanent H code enable
22	TBL0 FF, TBL1 FF, RO FF
	CS monitor bus
35	(a) Verify all CS disconnected from the CS monitor bus
	(b) Check for false currents
	(c) Check for false grounds
35	(d) CS (i) relays (primary and secondary)
34	(e) CS (i) voltage regulator

TABLE C

TEST RUN IN PHASE 1 AND PHASE 5

TEST RUN	RESULTS	REFERENCE
1. Lamp Fuse	The lamp fuse scan point is read and the result recorded. Curent should flow; thus, the lamp fuse scan point (SC2) should read 0.	PD-1A019-01 (Page 53) SD-1A124 (FS 33 Power Control LF Lead)
2. Manual Control Panel Status and Fuse Alarm Circuit	The manual control panel status scan points SC0 and SC1 are scanned and recorded. If the manual control panel is in the *normal* state, both scan points should read 0. Any non-normal state, inhibit request, manual power off, or fuse alarm will yield a non-zero reading.	PD-1A019-01 (Page 53) SD-1A124 (FS 33 Power Control SC0 and SC1 leads)
3. Permanent RO Sync, Precharge Enable, or H-code Enable Lockout Condition	Test the permanent RO output sync and precharge enable lockout conditions. Scan points 0TB and 1TB are scanned; if no lockout condition exists, scan points should read 0.	PD-1A019-01 (page 54) SD-1A124 (FS 22 System Control)
4. TBL0, TBL1, and RO FFs	Test the ability of the RO, TBL0, TBL1 FFs to be set and reset via the CPD. FFs are scanned via scan point RO0, RO1, 0TB, and 1TB. Set state will cause the scan point to read A1, reset A0.	PD-1A019-01 (Page 54) SD-1A124-01 (FS 22 System Control)
5. CS Monitor Bus for:		
A. A clear monitor bus (verify all CSs are disconnected from monitor bus)	A. SD point VPT0 is released in every CS in the office, disconnecting each CS from the monitor bus. This is verified by reading the VT scan point; if disconnected, VT scan point should read 0.	PD-1A019-01 (Page 54) SD-1A124-01 (FS 35 Voltage Regulator Test)
B. All Voltage Regulators	B. SFC 12 checks the CS voltage regulators by activating appropriate relays via SD operations, and scanning the voltage regulator monitoring scan points (CSM 0 through CSM 7).	PD-1A019-01 (Page 55-59)

4.06 In addition to the eight common scan points of the CS monitor bus, each CS has nine private scan points. To determine the scan points associated with a particular CS, use the TTY input message VFY-UNTY-1503XX. (Refer to input message manual IM-1A001 for the complete message.) The TR13 output message received from this request will yield not only the private scan point for a given CS, but the CPD and signal distributor (SD) assignments as well. The TR13 output message is shown below. (Refer to OM-1A001 for complete message format.) CS private scan points and their significance are shown in Table D.

```
TR13 30          3 = Unit type  0 = CS00

04236400         Convert octal numbers to binary
05004151         Use PA-59103, Section 030, unit
02000254         type 3 for complete breakdown
07001500         of translators.
```

4.07 Phase 1 and phase 5 failures can be located by using one of the following test methods, assuming TLM-1A124 does not aid in finding the trouble. DC test procedures can be used. This consists of displaying the CS monitor bus ferrods at the master control center (MCC) and duplicating the failing test. (Refer to Section 231-125-301 for procedures.) ***First,*** consult the raw data printout and PK-1A019 to determine the state of the hardware components. Next, block/operate the indicated relays and observe the ferrod condition. From here, the trouble can be pursued by using either a meter or an oscilloscope.

4.08 Similar steps can be followed when the trouble is detected over one of the CS private scan points. Consult the raw data printout and PK-1A019 to obtain all the circuitry involved. Using the VFY-UNTY message, obtain scanner, CPD, and SD assignments. Refer to IM-1A001 for complete input message. By displaying the proper scan row at the MCC and pulsing the CPD or SD points using the TTY input message T-CPD or T-MISD, the suspected ferrod point can be observed. Use DC test procedures to clear the trouble.

Phase 2 and Phase 6

4.09 Phase 2 and phase 6 are carried out by using control read (CR) and control write (CW) orders. These control orders have the facility of testing most internal CS circuitry without accessing the memory area. There are twelve control orders, six CR and six CW orders. Control instructions can be recognized by the nonmemory mnemonic N (NX, BN, NBTA, etc).

4.10 ***Data register*** can be written into and can also be read. This operation verifies that the CS can receive each bit from the bus and also the ability to send 24 bits of data back to the CC.

4.11 ***Name and Answer Flip Flops (FFs)*** can be both written and read. The name FFs are used to establish the K code for the G-half of a CS. The answer FFs control selection of the bus to be used for sending data back to the CC (GS0, GS1, HS0, and HS1 FFs).

4.12 ***Accumulate timing 1 and 2*** can only be written. In each case a CS FF is set. This will start the timing sequences. At proper intervals, designated timing points are interrogated and the results gated into the data register. Either of these orders will normally be followed by a CR order of the data register.

4.13 ***Servo counters*** can be read or control written to either the set or reset states. The servo counters are 3-bit binary counters designed to regulate the X and Y current drives. These counters can be control written to either all ones or all zeroes, and not to any value in between.

4.14 ***DC switches and parity:*** These 16 Y access switches and 16 X access switches can be control read. The dc switches provide the access into the memory module. They are activated by decoding bits in the address register. In addition to the dc switches, there are five points in the parity check circuit which are checked by this control read order.

4.15 ***Fault test points*** are tested with a control read of several semi-dc gate conditions which are fixed during a cycle and can be gated onto the bus. This test group includes the fault FFs.

TABLE D

CALL STORE PRIVATE SCAN POINTS

SCAN	POINT	PURPOSE
SC0	SC1	
0	0	CS control panel keys normal
0	1	Manual power off
1	0	Inhibit request
1	1	Fuse alarm
	SC2	LF scan point — current flows if the lamp fuse is good
	SC3	DC0 — Reset only via CPD operation
	SC4	TBL1 scan point Set — Inhibits CS communication via CC-CS Bus 1 Reset — Allows CS to communicate with CC via bus 1 if the RO FF is reset
	SC5	TBL0 scan point Set — Inhibits use of CC-CS Bus 0 Reset — Allows use of CC-CS Bus 0 if RO FF is set
	SC6	RO1 scan point — RO FF set allows CS to receive over Bus 0 if the TBL0 FF is reset
	SC7	RO0 Scan point — RO FF reset allows CS to receive from BUS 1 if the TBL0 FF is reset
	SC8	VT scan point — saturated indicates that the CS is disconnected from the CS monitor bus

4.16 Any failure in either phase 2 or phase 6 will result in omitting the remainder of the diagnostic phases usually run on the same CS bus. For example, if phase 2 fails, phase 3 and phase 4 will not be run. The primary hardware tested by phase 2 and phase 6 is given in Table E.

4.17 Failures in phase 2 or phase 6 can be located by using the input message CS-PARDGN and analyzing the printout. (Refer to IM-1A001 for complete message.) Also use the 0FL-EXEC message to loop on a section of the program which will duplicate the first failure in the raw data printout. (Refer to Section 231-117-301.) To accomplish this, use PF-1A019 to locate the global that can serve as a reference into PR-1A019. Once the specific test has been identified in PR-1A019, the address can be applied to the 0FF-LINE message. The trouble can be located with an oscilloscope.

Caution: The following procedure requires additional analysis and should not be considered until all other methods have failed.

4.18 The appropriate CR and CW orders can be written on a program store card and executed by means of the 0FL-EXEC-03 program (Section 231-117-301 for 2-wire and Section 231-417-301 for 4-wire). The orders to be written can be determined from analysis of the raw data and PK-1A019.

Example of Phase 2 and Phase 6 Failure

4.19 The following is a step-by-step procedure used for locating one fault in phase 2. This

TABLE E

PRIMARY HARDWARE TESTED BY PHASE 2 AND PHASE 6

FS IN SD-1A124	DESCRIPTION
6	Y access dc switches
7	X access dc switches
10	*Bus 0 receiver cores
12	*Code register (a) Bus 0 inputs and sync
13	*Mode register (C,G,H,R,W,PKA) (a) Bus 0 inputs and syncs
14	*Address register (a) Bus 0 inputs and sync
15	*Bus 0 data inputs (pulse directors) and syncs
16	Enable decoder (H and G name)
17	Mode decoder (C,G,H)
18	Order decoder (CR,CW,NBTA,NBTB, GMR,GMW,HMR,HMW,NR,NW)
19	Control address decoder
20	Test register (TT FFs and control and normal or MTCE data reg FFs reset)
21	Fault register (ASW,GH,MUM,TCF,DC0 FFs)
22	System control (code, mode, and address register bus inhibit gates and O.5T4.5 cycle lockout gates)
23	*Answer control (bus 0 routing of control and MTCE order info onto output bus 0)
24	Sequence control (CS timing chain)
25	Data register
26	Parity check (code, address, PKA parity check circuit)
27	*Bus 0 bus sending transformers (SP0) (Control mode sending only)
15	Variable G name FFs and normal mode answer routing FFs
*FOR PHASE 6 CHANGE BUS 0 TO BUS 1	

procedure will show the logic used in finding the fault.

```
CS-DGN-RCS03.PF

   08 DR02 RAW          CS  3
PH 1   ATP            PH 5   ATP
PH 2   STF            PH 6   STF
00000000              00000000
00160000              00160000
00000000              00000000
00000000              00000000
00000000              00000000
00000000              00000000
00000000              00000000
00000000              00000000
00000000              00000000
00000000              00000000
00000000              00000000
00000000              00000000
00000000              00000000
00000000              00000000
00000052              00000052
37777777              37777777
37777777              37777777
37777777              37777777
37777777              37777777
37777777              37777777
37777777              37777777
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37777777              37777777
37777777              37777777
37777777              37777777
37777777              37777777
37777777              37777777
37777777              37777777
37777777              37777777
5514 4943 0422
                      5972 1409 2404
                      UNIV TBL NO.
                      3295 7391 2760
```

4.20 The DR02 printout shows that phase 2 and phase 6 failed the same on both buses. It also shows that bits 13, 14, and 15 failed in word 2.

4.21 Use PK-1A019 to analyze failing word and bits. Word 2 in this case is testing the X dc switches. The first bit to fail was bit 13, which is looking at the state of gate XDC5C′.

4.22 Use SD-1A124, sheet index, to locate the X access FS. The sheet index shows that the X access is in FS7. The XDC5C′ gate is shown on sheet B38 and is from circuit pack 08-12, a dc switch.

4.23 Another possible failure might be circuit pack 08-10. The printout shows bits 14 and 15 failing. These two bits are gates XDC6C′ and XDC7C′.

4.24 The DR02 printout also gives a universal trouble number at the end of the printout. Use TLM-1A124 by finding the exact match; it shows circuit pack 08-12 could be the trouble.

Example of Fault in Phase 2 and Phase 6

4.25 The following is a step-by-step procedure used for locating one fault in phase 2. This procedure will show the logic used in finding the fault.

4.26 The following messages were received on the TTY. Some were machine generated and some were requested at the TTY.

```
27 MA14A
00000000 01102333 01024345 01026532 21254750 01572000

27 MA14 CC INT
01165440 01165440 10300000 01165432 00000000 00000000
00011400 01163671 03777777 00000000 36612337 01165440
00010510 00020503 02000040 03101401 00010550 00002010

27 DR01 TBL NOS CS 1
PH 2 STF
4742 3416 7205
PH 6 STF
2502 6109 3750
UNIV TBL NO.
7245 1525 8141
```

4.27 The TLM approach does not yield a solution, so the next step would be to request a cell data printout as follows:

```
  CS-DGN-CCS01.PF

**29 DR01 TBL NOS CS 1
  CELL NOS
  4295 1883 1497
  7413 4839 1617
  6998 5021 1710
  1018 6316 1755
  0107 6811 1039
  2815 3052 1280
  4485 5184 1656
  4794 0010 1130
  7549 1314 1620
  7881 2127 1940
```

4.28 Using TLM-1A124, look for an exact match in section E. In this case, there is no match that yields a solution to this fault. The next step would be to request a raw data printout as follows:

```
CS-DGN-RCS01.
```

The system responds with the following printout:

```
32 DR02 RAW CS      1
PH 1    ATP         PH 5    ATP
PH 2    STF         PH 6    STF
00000000            00000000
00000000            00000000
00000000            00000000
00000000            00000000
00000000            00000000
00000000            00000000
00000000            00000000
00000000            00000000
00000000            00000000
00000000            00000000
00000000            00000000
00000000            00000000
00000000            00000000
34036303            34036303
04036303            04036303
37777777            37777777
37777777            37777777
37777777            37777777
37777763            37777763
00000100            00000100
00000100            00000100
26374040            26374040
26365076            26365076
26305044            26305044
26074044            26074044
26374076            26374076
26374076            26374076
26374076            26374076
26374076            26374076
26374076            26374070
26374076            26374070
26374074            26374074
26374074            26374074
05416317            05416317
05411477            05411477
00000000            00000000
01360000            01360000
00000100            00000100
00260000            00260000
00000000            00000000
4742 3416 7205

        2502 6109 3750
        UNIV TBL NO.
        7245 1525 8141
```

4.29 The following procedure is used to analyze the raw data and to locate the fault. It should be noted that several documents are used in analyzing the failure.

4.30 Raw data: word 14, phase 2 and phase 6, is the first failing word. Phase 2 and phase 6 fail exactly the same. The fault is probably not in circuits associated with only one bus. PK-1A019 shows that word 14 is the result of testing address parity checker outputs PAR 1 and PAR 2.

4.31 PF-1A019 A sheets show that phase 2 and phase 6 are in SFC 13, and the E sheets show that the parity checker test begins at CDPARS. CDPARS can be found in PR-1A019-26. Using the B sheets of PF-1A019, it is found that ADRKK is the CS location where word 14 of phase 2 and phase 6 is stored. Finding ADRKK in the symbol table of PR-1A019-26 will give the page that CDPARS starts on.

4.32 Word 15 also fails: PR-1A019-26 and PD-1A019 state that if both words 14 and 15 fail, the fault is not in the parity checker circuit. The circuits for PAR 1 and 2 are independent of the circuits for PAR 3 and 4. A single fault in the parity check circuits will make one word or the other fail, but never both. If both fail, the fault must be in a circuit other than the parity checker.

4.33 The test of the next 3 raw data words (16, 17, 18) is omitted and the raw data is faked in as all 1s. The test resumes at word 19 at CDCMIT in PR-1A019-26. Word 19 points toward gates CR6′, CR5′, and CR1′ in the control address decoder. These gates are on circuit packs 26-07 and 26-09.

4.34 Words 20 and 21 point towards failure of the CS to return an all seems well (ASW) signal. Word 22 points towards no CS response to control mode operations. At this point, it might indicate a faulty mode register. Words 23 through 40 failures do not match any patterns given in PK-1A019. The list of possible circuit packs has grown quite large at this point.

4.35 Using 0FF-LINE methods to locate the fault, the following procedure was used (Section 231-117-301 for 2-wire and Section 231-417-301 for 4-wire).

```
ØFL-CØNFIG-
ØFL-MØDE-05.
ØFL-EXEC-11   00020503   00020504
```

Failing address from D-Level interrupt

4.36 Using an oscilloscope, it soon becomes apparent that nothing is happening in the store. Both TBL0 and TBL1 FFs are set. This cuts the store off from both buses. By trying to reset the TBL0 FF, it is found that it sets right away.

> ***Caution: Do not reset the TBL1 FF. As shown in the D-level interrupt, this is the active bus and will put the store back on-line.***

4.37 With the oscilloscope connected to the PD0-P′ lead (30-26 pin 20) with the TBL0 FF reset, the set pulse appears every cycle on the PD0-P′ lead. Tracing back to the GO FF with the oscilloscope, a low is found feeding back to the 1 output from the PG lead. The low was from a shorted diode on pin 4 of gate ASW′. This is an A2 pack at location 28-29. Figure 5 shows the shorted diode in the circuit.

4.38 ***What the shorted diode does:*** At the end of the CS cycle, the code mode and address registers are reset by RST1-P′. This makes leads PG and GR0′ go low. Even though GO1 also goes low at the same time, the 1 output of GO FF is locked low through the shorted diode. The 0 side is then locked high. If the next CS operation is ***not*** a control mode operation (CM′ high), the sync 2 (the sync that accompanies R, W, and PKA at 19T21) will fire the gate and set both TBL0 and TBL1. The GO FF circuit is supposed to fire in the event the CS gets a fault which makes it recognize a permanent name match.

4.39 The CS will run okay as long as a string of control mode operations is received. A normal, G, or H maintenance mode will set both TBL0 and TBL1. With both FFs set, the store is blind to anything on the buses.

4.40 The diagnostic program carefully resets both TBL0 and TBL1 FFs at the beginning of each segment. The fault does not show up as a test failure until the parity circuit test of CDPARS. The program takes a segment break and does a couple of BMAPs (normal mode). Then the program

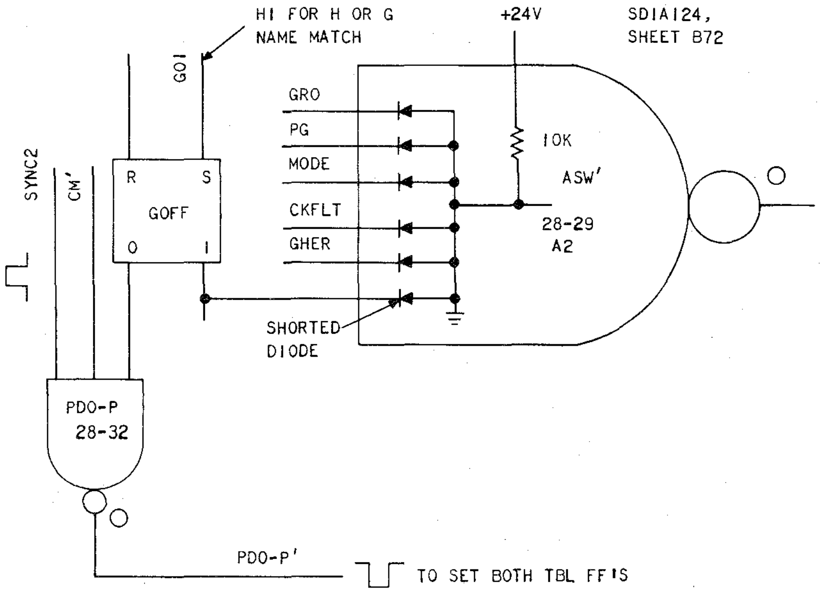


Fig. 5—Shorted Diode Causing Blind CS

does the parity circuit test. The BMAPs set TBL0 and TBL1 FFs, so the test fails whenever a 1 is expected from the CS.

Phase 3 and Phase 7

4.41 Phase 3 and phase 7 test the servo circuitry over each of the two CS address buses. Since the address bus should have no effect on the servo system, the results of phase 3 and phase 7 should be identical. If the results of these two phases differ, refer to Fig. 4 to determine some of the possible trouble causes.

4.42 Two binary counters of three bits each comprise the servo control system. These counters are used to alter the current in the X and Y current drives. During each CS cycle, the read current is monitored, and either increments or decrements the servo binary counter when the current deviates up or down from a predetermined level. This change in the binary counter causes a 4 ma change in the read current during the next CS cycle.

4.43 Under ideal conditions the three-bit servo binary counters should be stabilized at a setting of 3 or 4. This phase tests the servo circuitry by setting or resetting the binary counters to one of two extremes. Following a series of test orders, the servo counters are tested to verify that the CS circuitry has caused the binary counter to step from the extreme to a new state. Additionally, each binary counter is tested for 64 consecutive cycles to verify that an oscillation condition does not exist which will cause a change on each operation.

4.44 Since the servo system is directly related to the X and Y current drives, troubles in either of these drives can result in any invalid trouble indication in phase 3 or phase 7. In some instances, a failure in phase 3 or phase 7 does not warrant the CS being left out of service. These failures may be caused by the servo binary counter operating at one of the extremes, while the operation of the CS is not otherwise affected. Such a condition could be the result of temperature or component changes and, in some programs, is commonly encountered during the midnight routines. The primary hardware tested by phase 3 and phase 7 is shown in Table F.

Phase 4 and Phase 8

4.45 Phase 4 and phase 8 consist of testing the CS memory modules. These phases generate nine words of test data. Unlike the other CS diagnostic, these phases produce raw data which must be considered as a nine-word entity and not as individual failure bits. This means that to locate a failure point in PK-1A019, an exact match must be found for all nine words of the raw data printout.

4.46 The tests which are used to derive each of the nine test result words are as follows:

Test Word

1. H-half addresses 0.0000 through 0.0077 are written first with a test word of 0.14631463 and then read to verify the proper data. Next, the same procedure is followed using test word 0.23146314. These tests are repeated four times at each address, with any failing bit positions being marked in the test results. For example, if the first word of raw data equals 0.00002400, it indicates that bits 8 and 10 failed at least one of the 512 tests performed by this series. If no failures are detected in the 23 bits of data, the 24th bit is checked for any parity failure. This bit is the PFC FF in CC buffer bus B8SESA.

2. H-half addresses 0.4400 through 0.4477 are tested by the same methods used in test word 1.

3. G-half addresses 0.0000 through 0.0077 are tested identically to test word 1.

4. G-half addresses 0.4400 through 0.4477 are tested identically to test word 1.

TABLE F

PRIMARY HARDWARE TESTED BY PHASE 3 AND PHASE 7

FS IN SD-1A124	DESCRIPTION
7	X servo three cell FF binary counter
7	Logic stepping circuitry to X servo binary counter
6	Y servo three cell FF binary counter
6	Logic stepping circuitry to Y servo binary counter
19	Control read servos gating
6, 7	Control read servos readout circuitry
19	Control write set servos
19	Control write reset servos
24	Normal and MTCE order servos enable

5. The 64 addresses shown below are tested in the H-half of CS. Each address is tested four times, with the same test words used in test one.

TEST DATA BITS	TEST ADDRESSES			
0	0000	1010	2020	3030
1	4040	5050	6060	7070
2	0101	1111	2121	3131
3	4141	5151	6161	7171
4	0202	1212	2222	3232
5	4242	5252	6262	7272
6	0303	1313	2323	3333
7	4343	5353	6363	7373
8	0404	1414	2424	3434
9	4444	5454	6464	7474
10	0505	1515	2525	3535
11	4545	5555	6565	7575
12	0606	1616	2626	3636
13	4646	5656	6666	7676
14	0707	1717	2727	3737
15	4747	5757	6767	7777

6. This test is the same as test word 5, but with the addresses listed below.

TEST DATA BITS	TEST ADDRESSES			
0	0077	1067	2057	3047
1	4037	5027	6017	7007
2	0176	1166	2156	3146
3	4136	5126	6116	7106
4	0275	1265	2255	3245
5	4235	5225	6215	7205
6	0374	1364	2354	3344
7	4334	5324	6314	7304
8	0473	1463	2453	3443
9	4433	5423	6413	7403
10	0572	1562	2557	3542
11	4532	5522	6512	7502
12	0671	1661	2651	3641
13	4631	5621	6611	7601
14	0770	1760	2750	3740
15	4730	5720	6710	7700

7. G-half addresses are tested using the same procedures and test addresses listed in test word 5.

8. G-half addresses are tested using the same procedures and test addresses listed in test word 6.

9. Routing of both the H- and G-half of CS to the active bus is tested. This includes both sending and inhibiting CS readouts.

4.47 Failures in either phase 4 or phase 8 have to be considered in conjunction with any failures that may have been indicated in phase 3 or phase 7. This is necessary because of the relationship between the servo system and the X and Y current drives. A circuitry failure in phase 3 or phase 7 can result in meaningless data being received for phase 4 or phase 8, or vice versa. The primary hardware tested by phase 4 and phase 8 is shown in Table G.

4.48 For offices with CTX-6 Issue 8 and later generic except CTX-8, Issues 2.1 and 2.2, phases 4 and 8 have a test to detect interference on the CS answer bus. This test is run only if all previous tests have passed.

The raw data is stored in the last raw data word for phase 4 or phase 8. The raw data pattern for bits 0 through 22 will have a 1 in the bit position corresponding to the interfering bit on the A74 circuit board. No new trouble number will be produced. See Table H for pack location and corresponding raw data values.

TABLE G

PRIMARY HARDWARE TESTED BY PHASE 4 AND PHASE 8

FS IN SD-1A124	DESCRIPTION
1	Preamplifiers
2	Discriminators
2,24	Associated discr logic
3	H and G inhibit generators
24	Associated inhibit gen logic
25	Regenerate gates in data reg
27	Normal and MTCE mode SP0 (bus 0 outputs)
4,5	H and G diode matrices
6,7	H and G input markers
6,7	H and G output markers
6,7	H and G ac switches
6,7	X and Y access current drivers, cur driver trnsf, std sig ref SR3
23	H and G normal mode answer bus routing onto output bus 0
24,34	Discr strobes STB0-P′, STBE-P′, STB2-P
18	Data reg logic gates WDC1′, WDC2′

Example of Phase 4 or Phase 8 Failure

4.49 The following is an example of a phase 4 or phase 8 failure, with possible ways for finding the fault.

```
  23 MA14A
  00000000 01630164 01024345 01152306 01152726 00000000

**23 MA14  CC  INT
  00506605 11051105 00014273 01074556 00506605 00000000
  00012317 00506632 17777777 00506605 00506405 01051105
  00010510 00014273 00000000 12201401 00010550 00002010

**24 DR01 TBL NOS CS 3
  PH 4 STF
  5276  6940  6650
  PH 8 STF
  1614  7132  6793
  UNIV TBL NO.
  6891  7151  6098
```

4.50 From these messages, the following can be determined.

(1) The failing instruction

(2) The failing CS address

(3) The configuration of CS, CS buses, and CSs in effect at the time of the failure.

4.51 The TLM approach yields no match, so the next step is to request a cell data printout as follows:

```
  CS-DGN-CCS03.PF

**59 DR01 TBL NOS CS 3
  CELL NOS
  3141  2147  1379
  0621  7515  0997
  3520  1279  1306
  3533  2467  1120
  7886  0512  1030
  0000  0000  0000
  0000  0000  0000
  0000  0000  0000
  0000  0000  0000
  0000  0000  0000
```

4.52 The cell data does not yield a match, so in this case it cannot be used. The next step would be to request a raw data diagnostic as follows:

```
CS-DGN-RCS03.PF
```

```
20 DR02 RAW CS 3
PH 1 ATP
PH 2 ATP
PH 3 ATP
PH 4 STF
00125252
00125252
00125252
00125252
00000000
00000000
00000000
00000000
00000000
5276 6340 6650
PH 5 ATP
PH 6 ATP
PH 7 ATP
PH 8 STF
00125252
00125252
00125252
00125252
00000000
00000000
00000000
00000000
00000000


1614 7132 6793
UNIV TBL NO.
6891 7151 6098
```

4.53 The following procedure is used to analyze the raw data and locate the fault. It should be noted that several documents are used in analyzing the failure.

4.54 The DR02 analysis, using the PK approach, shows that the following conditions exist.

(1) Word 1 failed bits 15, 13, 11, 09, 07, 05, 03, and 01 at one time or another in the first 100 (octal) H-half locations (name +0000) through name +7777).

(2) Word 2 failed in the same manner as word 1, H-locations 4400 through 4477.

(3) Words 3 and 4 failed with the same results in G-half as failed in H-half.

(4) Phase 8 failed the same as phase 4.

4.55 The conclusions reached at this point are

(1) The fault is not bus-sensitive. Any circuitry assosciated with only one bus should be OK.

(2) The fault is not G- or H-half sensitive (affects both G- and H-half the same). Any circuitry associated with only the H-half or only the G-half should be OK.

(3) Only odd-numbered bits 15 through 01 failed. The fault appears to be a bit-associated trouble; but it is not yet possible to tell if the failure is on a write or the subsequent read, or whether it is in the accessing, writing, or readout circuits.

BIT POSITION																											
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	C.P.	FUNCTION	FS	
34–40						34–39						34–38						34–45						A18	CA. RCV. BUS 0	11	BUS SENSITIVE
34–48						34–47						34–46						34–37						A18	CA. RCV. BUS 1	11	
28–24						28–20						28–16						28–14						A72	PULSE DIR. BUS–0	15	
28–26						28–22						28–18						28–12						A72	PULSE DIR. BUS–1	15	
				32–24		32–20						32–16						32–14						A72	PULSE DIR. BUS–0	15	
				32–26		32–22						32–18						32–12						A72	PULSE DIR. BUS–1	15	
32-36				24-48	24-47		24-46	26–32				26–31				26–30				26–29				A06	CONTROL WRITE GATES	25	
24-48	24-47	24-46	24-45	24-40	24-39	24-38	24-37	24-32	24-31	24-30	24-29	24-24	24-23	24-22	24-21	24-16	24-15	24-14	24-13	24-08	24-07	24-06	24-05	A06	DATA REGISTER	25	
06-30	21-30	06-26	21-26	06-24	21-24	06-20	21-20	06-18	19-30	06-14	19-26	04-30	19-24	04-26	19-20	04-24	17-30	04-20	17-26	04-18	17-22	04-14	17-18	A89	READOUT PREAMP	01	
21-41	21-42	21-41	21-42	21-41	21-42	21-41	21-42	21-41	21-42	21-41	21-42	21-41	21-42	21-41	21-42	21-41	21-42	21-41	21-42	21-41	21-42	21-41	21-42	A08	UNCLAMP GATES	02	
06-28	21-28	06-28	21-28	06-22	21-22	06-22	21-22	06-16	19-28	06-16	19-28	04-28	19-22	04-28	17-28	04-22	17-28	04-22	17-28	04-16	17-20	04-16	17-20	A90	DISCR	02	
17–48		19–46		17–46		19–44		17–44		19–42		17–42		19–40		17–40		19–38		17–38		19–36		A96	H. INHIBIT GEN.	03	
06–46		04–44		06–44		04–42		06–42		04–40		06–40		04–38		06–38		04–36		06–36		06–34		A96	G. INHIBIT GEN.	03	
24–42				24–34				24–26				24–18				24–10				24–02				A74	SENS. PULS. ORIG. B–0	27	BUS SENSITIVE
24–44				24–36				24–28				24–20				24–12				24–04				A74	SENS. PULS. ORIG. B–1	27	
26–44								26–40								26–36								A21	C.D. BUS 0	27	
26–46								26–42								26–38								A21	C.D. BUS 1	27	

Fig. 6—Data Sensitive Troubleshooting Aid

4.56 One method for finding the fault is to use the 0FL-EXEC-09 message and the failing address from the D-level interrupt. Refer to Section 231-117-301 for 2-wire and Section 231-417-301 for 4-wire for off-line procedures.

4.57 This method is a write order, but the CS performs a readout/write-in operation. This will allow observing a readout fault in action even though the store is receiving only ***write*** commands from CC.

4.58 The scope sync should be on the sync 1 input (SD-1A019) to the CS and the probing should start at the readout circuits and work backwards towards the ferrite module.

4.59 Compare a good bit (bit 00) with a bad one having the same value (bit 01) on the 2 scope channels. It will be found in this fault where address bit X5 does not equal address bit Y5 that bit 01 never gets its unclamp signal for address. Gate UCB4-P′ on sheet B26 in SD-1A019 has 2 highs on its inputs and one high on its output; also, the output should be low. This circuit pack is an A8 in location 21-41.

4.60 Another method for locating a fault of this type is to use the bit sensitive troubleshooting aid shown in Fig. 6. Using the failing word in the phase 4/8 raw data printout, convert the octal number to binary. Put this data into the bit position on the chart. The only pack common to all the odd failing bits and none of the even bits is the ***Unclamp Gates,*** an A8 circuit pack at location 21-41.

4.61 Since it is known that the fault is not bus-sensitive, the circuit packs listed on the first six lines and the last four lines are ruled out. It could also possibly be more than the discriminator circuit pack (A90). It could not be the A96 inhibit generators since the trouble is common to both H- and G-halves.

Phase 9 and Phase 10 (CTX-6, Issue 8)

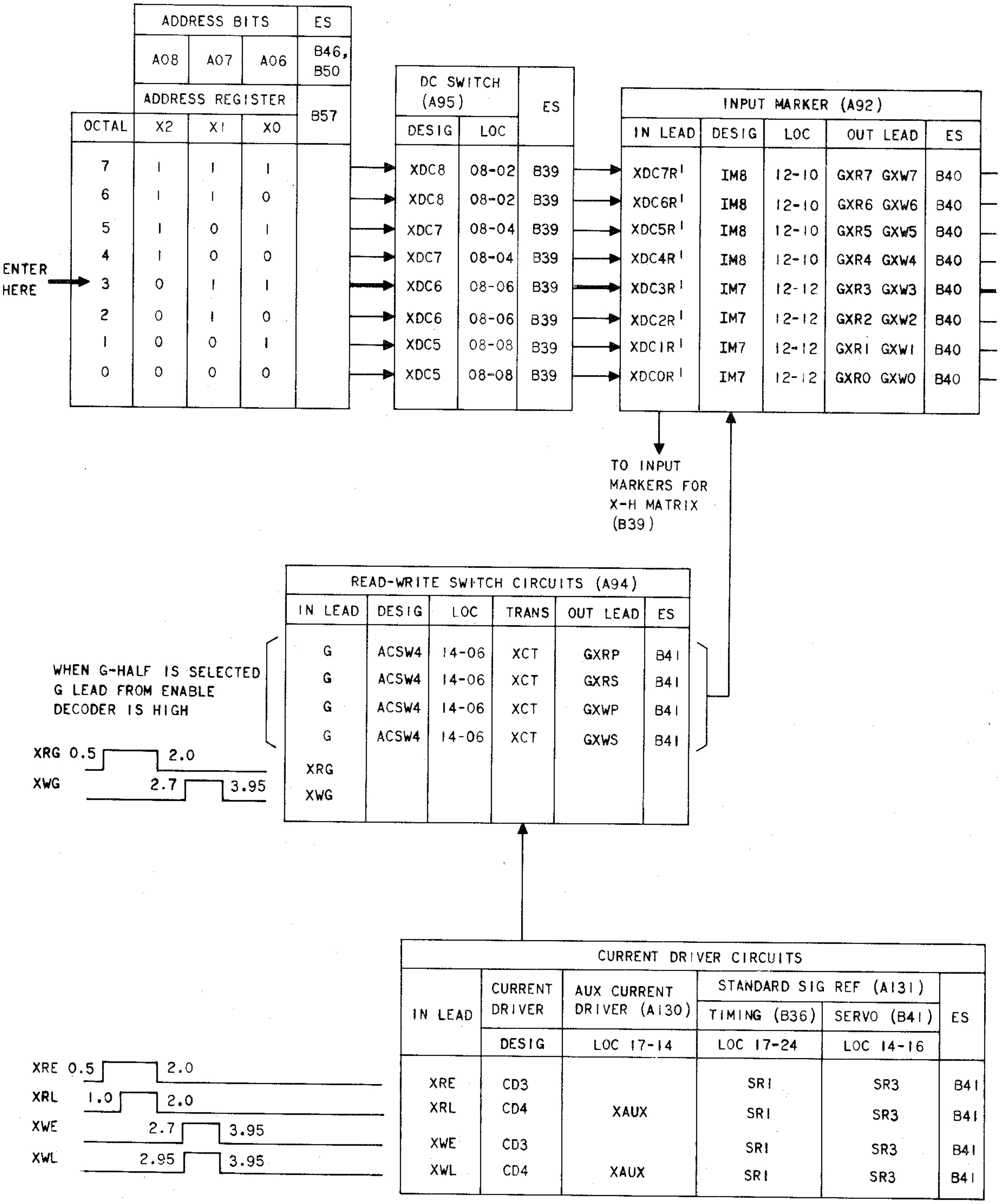
4.62 For offices with CTX-6 Issue 8 and later generics except CTX-8, Issues 2.1 and 2.2, phases 9 and 10 detect access rate dependent faults in CC or XP call stores. This functional access test run over BUS 0 (phase 9) and BUS 1 (phase 10), is primarily directed at faults in the CS timing chain and bus lockout circuitry. Depending upon the complex, either the CC or SP will be used to verify that the CS under diagnosis can be accessed at a 5.5 microsecond rate without CS errors re-read failures.

4.63 Because these tests are functional rather than diagnostic in nature, there is no meaningful raw data produced by phases 9 and 10. A test failure causes a constant raw data word (37777777) to be generated and a TLM# of 6308 6364 4264 (PH9) or 2189 6096 3575 (PH10) to be produced. Phases 9 and 10 are run ***only*** if all other tests pass.

4.64 When phases 9 or 10 fails, the faulty circuit pack can be isolated by looping on phase 9 or 10 and checking the outputs of the delay generator circuit packs with an oscilloscope. The location of these packs and their normal output pulse width are given in Table I.

5. CHECKERBOARD TEST

5.01 This test consists of multiple write-read operations at each CS address. Basically, this test walks a 1 or 0 through a field of opposite bits, and extensively exercises the CS circuitry to detect noise problems. However, when this test is requested,all checks are made over the presently active CS bus. The full value of this test can only be realized if it is run over both buses. Therefore, once a checkerboard test has been run over one bus, switch the active CS bus and request a new checkerboard test.



	ADDRESS BITS			ES
	A08	A07	A06	B46, B50
	ADDRESS REGISTER			B57
OCTAL	X2	X1	X0	
7	1	1	1	
6	1	1	0	
5	1	0	1	
4	1	0	0	
3	0	1	1	
2	0	1	0	
1	0	0	1	
0	0	0	0	

DC SWITCH (A95)		ES
DESIG	LOC	
XDC8	08-02	B39
XDC8	08-02	B39
XDC7	08-04	B39
XDC7	08-04	B39
XDC6	08-06	B39
XDC6	08-06	B39
XDC5	08-08	B39
XDC5	08-08	B39

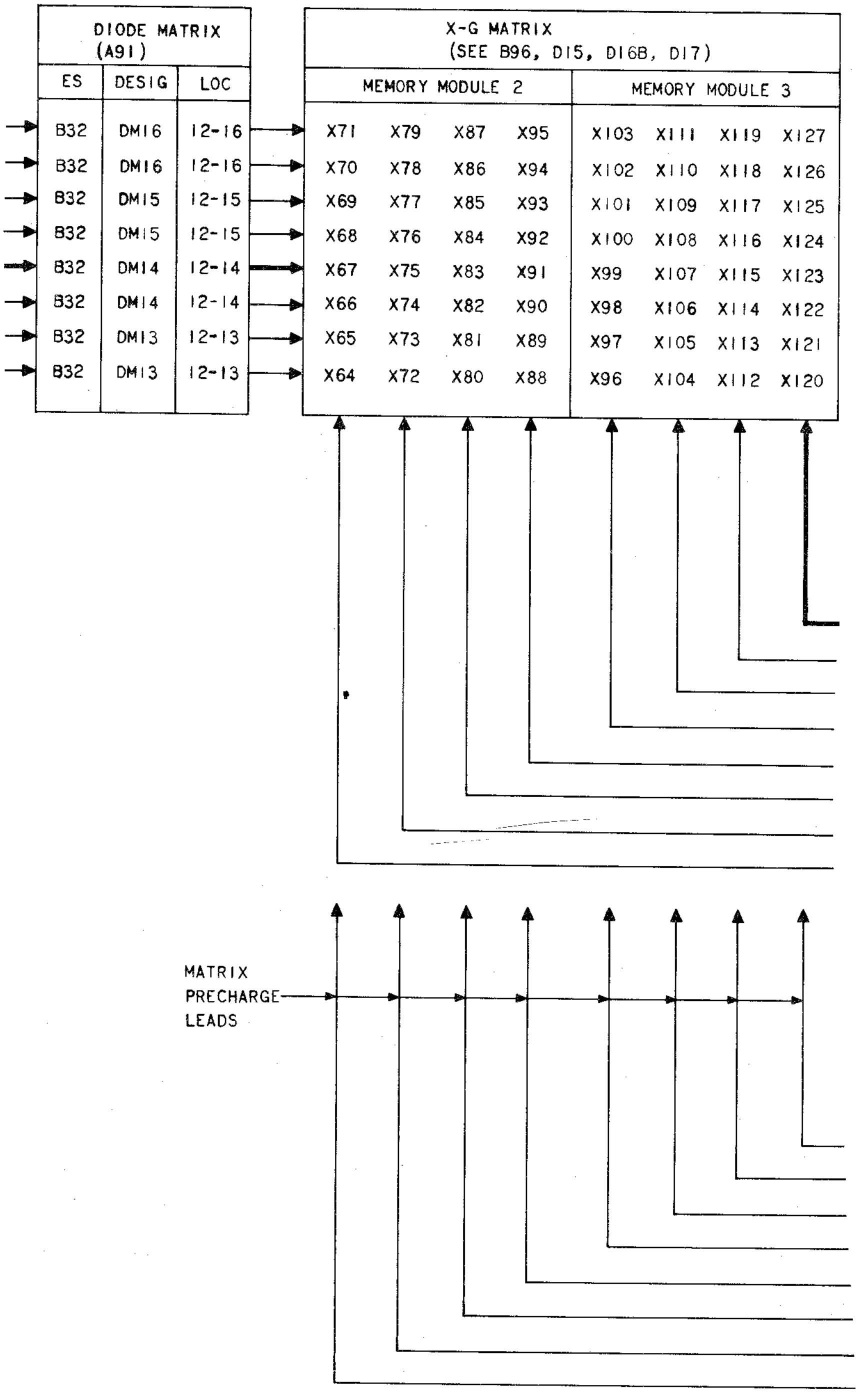
INPUT MARKER (A92)				
IN LEAD	DESIG	LOC	OUT LEAD	ES
XDC7R'	IM8	12-10	GXR7 GXW7	B40
XDC6R'	IM8	12-10	GXR6 GXW6	B40
XDC5R'	IM8	12-10	GXR5 GXW5	B40
XDC4R'	IM8	12-10	GXR4 GXW4	B40
XDC3R'	IM7	12-12	GXR3 GXW3	B40
XDC2R'	IM7	12-12	GXR2 GXW2	B40
XDC1R'	IM7	12-12	GXR1 GXW1	B40
XDC0R'	IM7	12-12	GXR0 GXW0	B40

READ-WRITE SWITCH CIRCUITS (A94)					
IN LEAD	DESIG	LOC	TRANS	OUT LEAD	ES
G	ACSW4	14-06	XCT	GXRP	B41
G	ACSW4	14-06	XCT	GXRS	B41
G	ACSW4	14-06	XCT	GXWP	B41
G	ACSW4	14-06	XCT	GXWS	B41
XRG					
XWG					

CURRENT DRIVER CIRCUITS					
IN LEAD	CURRENT DRIVER	AUX CURRENT DRIVER (A130)	STANDARD SIG REF (A131)		ES
			TIMING (B36)	SERVO (B41)	
	DESIG	LOC 17-14	LOC 17-24	LOC 14-16	
XRE	CD3		SR1	SR3	B41
XRL	CD4	XAUX	SR1	SR3	B41
XWE	CD3		SR1	SR3	B41
XWL	CD4	XAUX	SR1	SR3	B41

Q

CALL STORE SELECTIONS IN G-HALF X MATRIX
(SEE NOTE 2)



DIODE MATRIX (A91)			X-G MATRIX (SEE B96, D15, D16B, D17)							
ES	DESIG	LOC	MEMORY MODULE 2				MEMORY MODULE 3			
B32	DM16	12-16	X71	X79	X87	X95	X103	X111	X119	X127
B32	DM16	12-16	X70	X78	X86	X94	X102	X110	X118	X126
B32	DM15	12-15	X69	X77	X85	X93	X101	X109	X117	X125
B32	DM15	12-15	X68	X76	X84	X92	X100	X108	X116	X124
B32	DM14	12-14	X67	X75	X83	X91	X99	X107	X115	X123
B32	DM14	12-14	X66	X74	X82	X90	X98	X106	X114	X122
B32	DM13	12-13	X65	X73	X81	X89	X97	X105	X113	X121
B32	DM13	12-13	X64	X72	X80	X88	X96	X104	X112	X120

NOTES:
1. K-CODES AND OCTAL NUMBERS DEFINED BY BITS A17-A12 ARE SHOWN ON SHEET D25.
2. CHOOSE THE ADDRESS STATES. THEN FOLLOW THE ARROWS TO THE MATRIX INTERSECTION.

* X-G SELECTIONS ARE DEFINED ON THIS SHEET

OCTAL ADDRESS RANGE TO CALL STORES (SEE NOTE 1)																			EQUIVALENT DECIMAL RANGE
FIRST ADDRESS	0			1			0			0			0			0			004096
LAST ADDRESS	7			6			7			7			7			7			258047
BUS PAIRS	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	
CS FF	K5	K4	K3	K2	K1	K0	X5	X4	X3	X2	X1	X0	Y5	Y4	Y3	Y2	Y1	Y0	
	CS H - NAME						X-H MATRIX						Y-H MATRIX						
	CS G - NAME						X-G MATRIX *						Y-G MATRIX						

7 3 3 0 = FIRST FAILING ADDRESS

OUTPUT MARKER (A93)				
OUT LEAD	LOC	OM	IN LEAD	ES
GX7	12-08	OM7	XDC7C'	B40
GX6	12-08	OM7	XDC6C'	B40
GX5	12-08	OM7	XDC5C'	B40
GX4	12-08	OM7	XDC4C'	B40
GX3	12-06	OM7	XDC3C'	B40
GX2	12-06	OM7	XDC2C'	B40
GX1	12-06	OM7	XDC1C'	B40
GX0	12-06	OM7	XDC0C'	B40

DC SWITCH (A95)		ES
LOC	DESIG	
08-10	XDC4	B38
08-10	XDC4	B38
08-12	XDC4	B38
08-12	XDC4	B38
08-14	XDC4	B38
08-14	XDC4	B38
08-16	XDC4	B38
08-16	XDC4	B38

ADDRESS BITS			ES	
A11	A10	A09	B46, B50	
ADDRESS REGISTER			B57	
X5	X4	X3		OCTAL
1	1	1		7
1	1	0		6
1	0	1		5
1	0	0		4
0	1	1		3
0	1	0		2
0	0	1		1
0	0	0		0

ENTER HERE

TO OUTPUT MARKERS FOR X-H MATRIX (B38)

PRECHARGE SWITCH CIRCUITS (A94)						
OUT LEAD	LOC	TRANS	AC SW	LOC	IN LEAD	E
GX7	10-02	PT4	ACSW8	10-04	XDC7C'	B44
GX6	10-02	PT4	ACSW8	10-04	XDC6C'	B44
GX5	10-02	PT4	ACSW8	10-04	XDC5C'	B44
GX4	10-02	PT4	ACSW8	10-04	XDC4C'	B44
GX3	12-02	PT3	ACSW7	12-04	XDC3C'	B44
GX2	12-02	PT3	ACSW7	12-04	XDC2C'	B44
GX1	12-02	PT3	ACSW7	12-04	XDC1C'	B44
GX0	12-02	PT3	ACSW	12-04	XDC0C' XPCG-P	B44 B44

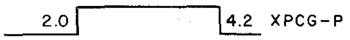
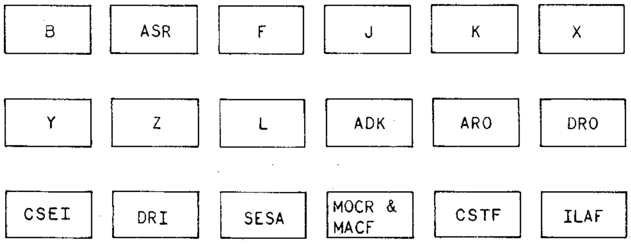


Fig. 7—Matrix Access Aid

5.02 Use the address that failed in CS03 printout to access sheets D21 through D24 in SD-1A124 to determine access circuits that failed. See the example below and in Fig. 7. Use bits that failed to determine readout circuit packs that failed.

```
        CS03 CHKBD CC 3
00007330    00000001<-┐
00007323    00000001  │
00007152    00000001  │
00007142    00000200  └-Bit 1 Failed
00007142    00000400
00007020    00000001
00006774    00000001
00006752    00000001
00006647    00000001
00006611    00000001
00006375    00000001
00005372    00000001
00005113    00000001
00004521    00000001
00002462    00000001
00001403    00000001
00007137    00000000
00004157    00000000
  ^
  │
  └-Bit 15 = 0 = G-Half
```

5.03 The printout should be analyzed to determine the possible trouble; for example, more than one bit failing might be a voltage pack, or bits failing next to each other might be a readout pack.



ARO = B REG OF STANDBY CC
DRO = PA ADDRESS AT TIME OF INTERRUPT
DRI = FAILING CALL STORE ADDRESS
CSEI = ERROR INDICATORS

Fig. 8—D-Level Interrupt Register Locations

DATA=ADDRESS

5.04 For offices with CTX 6 Issue 8 and later generics except CTX-8, Issues 2.1 and 2.2, a demand exercise has been added to verify CS memory integrity. This test is done by initialzing and then verifying every word in the call store under test with DATA=ADDRESS and DATA=ADDRESS complemented test patterns. This test can be requested via the CS partial diagnostic message. This test can be used with the checkerbord test to locate faults.

6. D-LEVEL INTERRUPTS

6.01 A D-level maintenance interrupt occurs when a reread or rewrite failure of a CS word is encountered or an invalid transfer to a CS address rather than to a PS address. When one of these failures is detected and the interrupt request is made by the system, the address that the failure occurred at is saved in the CC match registers.

6.02 The system prints out the MA14 registers for D-level interrupts as shown in Fig. 8. This layout shows the following registers:

B register	Z register
ASR register	L register
F register	addend K register
J register	ARO register (contains the complement of the B reg.)
K register	DRO register (contains the interrupted PS address)
X register	AR1 register (contains CSTF before the interrupt)
Y register	DR1 register (contains failing CS address)

MOCR and MACF register

SESA register (store error summary FFs)

ILAF register

BUFFER REGISTER BIT POSITION	NAME OF BIT	COMMENTS
0	AU	Defines active CC
1	TCC	Marks standby CC in trouble
2	PBO	
3	PBA	PS bus control
4	PBT	
5	CBO	
6	CBA	CS bus control
7	CBT	
8	CW	Control word bus selection
9	CWC	Enable standby to receive control words

PROGRAM STORE AND CALL STORE BUS SELECTION

PS BUS	PBO	PBA	PBT	ACTIVE CC		STANDBY CC	
CS BUS	CBO	CBA	CBT	SEND	REC	SEND	REC
	0	0	0	0	0	1	1
	0	1	0	1	1	0	0
	0	0	1	0	0	X	0
	0	1	1	1	1	X	1
	1	0	0	0+1	0	X	1
	1	1	0	0+1	1	X	0
	1	0	1	0+1	0	X	0
	1	1	1	0+1	1	X	1
0 = FF Reset 1 = FF Set				0 = Bus 0 1 = Bus 1 X = Neither Bus			

Fig. 9—CSTF Register Layout

6.03 The data contained in the CSTF (Fig. 9), SESA (Fig. 10), and the MOCR/MACF determines the validity of the information contained in the other registers. If (1) CBT (bit 7 of CSTF) is reset and (2) MOCR (Fig. 11) indicates routine matching by having HM, I, and X set (1401 in least significant bits), the parity failure PFC and the ASWC of the active CC and active bus determine the CS at fault. If either PFC or ASWC for the active CS bus is set and the system was in normal configuration before the interrupt occurred, the active CC recognized the problem and the even-numbered CS that contains the address specified in the DR1 register is at fault. Comparing the B registers of the two CCs (the standby CC B registers complement is in the ARO) or, depending on the instruction being performed at the time of the interrupt, the active B register and the data or the complement of the standby B register should produce the bit in error. It is the bit that disagrees in the active register. If no mismatch is present and PFC is set, the parity bit (bit 23) is at fault. (Check instruction for possible masking.) If, under the same condition of CSTF and MOCR, SESA does not have PFC or ASWC set, the failing address belongs to an odd-numbered CS. Since the standby CC recognized the mismatch, the standby B register (ARO) should contain the failing bit. If there is no mismatch, parity bit 23 is the fault.

6.04 In the case where the CSTF CBT bit is set, both CCs receive from the active bus. The failing address given in the DR1 register would belong to the H-half of the CS specified. The B register and the ARO register would not indicate the bit in error.

6.05 The signal processor (SP) CSs in the normally functioning office are configured in the same manner as the CC CSs. This means that the even-numbered CSs are on the active bus. The active CC CS bus and the SP CS bus do not have to be the same. For D-level interrupts that indicate an SP CS address in the DR1 register of the MA14 message, the same conditions apply that were previously explained with the following exceptions. D-level interrupts on write into SP CS implies that the SP saw the failure and not the SP CS. It would imply that the SP CS saw the failure on a read. If the SP CS failure is on a write, the system will generate an F-level interrupt.

6.06 In some cases, bit 11 of ILAF register is set on an interrupt, indicating an internal

BUFFER REGISTER BIT POSITION	NAME OF BIT	COMMENTS	
0	ASWPF—0	ASW failure from PS Bus 0	PS error summary flip-flops have inputs from error detection and correction circuits — gated on interrupt request or on maintenance orders
1	ASWPF—1	ASW failure from PS Bus 1	
2	ADEF	Address Error	
3	DBEF	Double Error	
4	PF	Single Error	
5	ASWC—0	ASW failure from CS Bus 0	Call store summary group, inputs controlled similar to above
6	ASWC—1	ASW failure from CS Bus 1	
7	PFC	Parity failure of CS word at buffer register	
8	X23—1	Bit 24 of K addend register	

Fig. 10—SESA Register Layout

BUFFER REGISTER BIT POSITION	NAME OF BIT	ACCESS (SEE NOTE)			COMMENTS	LOCATION IN SD
		R	W	C		
00	X	X	X	X	These bits establish matching mode	FS 85 Maintenance Control System M
01	Y	X	X	X		
02	MS	X	X	X		
03	TD	X	X	X		
04	CB	X	X	X		
05	PB	X	X	X		
06	TR	X	X	X		
07	IC	X	X	X		
08	I	X	X	X	Interrupt on abnormality	
09	HM	X	X	X	Stop match on abnormality	
10	E	X	X	X	Stop standby with execute-stop on abnormality	
11	F	X	X	X	Stop standby with fast-stop on abnormality	

Note: R — Bit position can be read with read-memory orders.
W — Bit position can be written into with write-memory orders.
C — Bit position can be written into with control-write orders.

Fig. 11—MOCR Register Layout

CS failure (CSFI). This means the CC suspected an error on the storage of the registers in the interrupt bins. The printout may or may not contain valid information and should be analyzed carefully.

6.07 To analyze a D-level maintenance interrupt printout, use the following procedure.

(1) Determine the matching mode of the CCs by examining the MOCR. This register should indicate routine matching with interrupts in effect at the time of interrupt. (The four rightmost octal digits printed out in MOCR should be 0.1401.)

(2) Determine the status of the send bus (CBO, bit 5), the bus that is active (CBA, bit 6), and the status of the standby bus (CBT, bit 7), using CSTF in the MA14 printout. Bus information can also be obtained from CSEI (Table J).

(3) Determine if the active CC recognized the problem by examining the status of PFC (parity bit 7) bit in SESA register.

TABLE H

PHASES 4 AND 8 INTERFERENCE TEST BIT FAILURES

BIT POSITION	BUS 0 PACK LOCATION	BUS 1 PACK LOCATION	RAW DATA WORD
0	24-02-08	24-04-08	00000001
1	24-02-13	24-04-13	00000002
2	24-02-20	24-04-20	00000004
3	24-02-26	24-04-26	00000010
4	24-10-08	24-12-08	00000020
5	24-10-13	24-12-13	00000040
6	24-10-20	24-12-20	00000100
7	24-10-26	24-12-26	00000200
8	24-18-08	24-20-08	00000400
9	24-18-13	24-20-13	00001000
10	24-18-20	24-20-20	00002000
11	24-18-26	24-20-26	00004000
12	24-26-08	24-28-08	00010000
13	24-26-13	24-28-13	00020000
14	24-26-20	24-28-20	00040000
15	24-26-26	24-28-26	00100000
16	24-34-08	24-36-08	00200000
17	24-34-13	24-36-13	00400000
18	24-34-20	24-36-26	01000000
19	24-34-26	24-36-26	02000000
20	24-42-08	24-44-08	04000000
21	24-42-13	24-44-13	10000000
22	24-42-20	24-44-20	20000000
Parity	24-42-26	24-44-26	25252525

TABLE I

DELAY GENERATOR CIRCUIT PACK INFORMATION

TYPE CIRCUIT PACK	FRAME LOCATION	NORMAL PULSE WITHIN μ SEC	BUS DEPENDENCY
A88	19-08	2.2	0
A88	19-10	2.2	1
A88	19-12	2.2	0
A88	19-14	2.2	1
A88	28-40	2.2	None
A83	28-42	.25	None
A86	28-44	1.0	None
A85	28-46	.5	None
A85	30-40	.5	None
A85	30-40	.5	None
A88	30-44	2.2	None
A113	30-48	.75	None
A84	32-46	.35	None

TABLE J

CSEI LAYOUT

BIT	FF OR LEAD	DESCRIPTION
0	LF = 1	Lamp fuse power failure
1	GOHI = 1	GO is high = code match
2	TBL1 = 1	Bus 1 trouble FF set
3	TBL0 = 1	Bus 0 trouble FF set
4	RO (0) = 1	RO FF reset — receive from Bus 1
5	RO (1) = 1	RO FF set — receive from Bus 0
6	VT = 1	One of the 7 voltage monitor relays is operated
7	SPARE	
8	HS0 = 1	Send normal readouts from fixed half (H) on Bus 0
9	HS1 = 1	Send normal readouts from fixed half (H) on Bus 1
10	GS0 = 1	Send normal readouts from variable half (G) on Bus 0
11	GS1 = 1	Send normal readouts from variable half (G) on Bus 1
12 and 13	SPARE	
14	DCO = 0	FF is set — decoder output FF (indicates code match)
15	ASW = 0	FF is set — ASW failure
16	GH = 0	FF is set — error G and H halves of CS selected simultaneously
17	CKGF = 0	FF is set — clock fault FF (readout sync and test point sync occurring simultaneously)
18	TC = 0	FF is set — test clock fault FF (readout sync and test point sync occurring simultaneously with a fault in 0 MEM or 1 MEM)
19	CR5′ = 1	Type 5 control read
20	PGO = 1	Permanent GO signal
21	CW3A′ = 1	Type 3 control write
22	CW4A′ = 1	Type 4 control write

(4) Determine in which CS the failure occurred and if the CS address is in-range or out-of-range by analyzing the failing CS address. Use the following procedure. (In-range address designates a hardware reread or rewrite failure; out-of-range address designates a software problem.)

(a) Drop off the four least significant CS address digits. (CS address is 6 digits.)

(b) Subtract 1 octally from the remaining 2 digits.

(c) Convert remainder to decimal number.

Example: If 0.203157 is the CS address, the 4 least significant digits (3157) are dropped. From the remaining 2 digits (20), subtract 1 octally, which leaves 17. Converting 0.17 to a decimal number results in decimal 15. This means that the CS address belongs to the H-half of CS 15, and the G-half of the preceding store (CS 14) has the same memory block address.

Note: If the resulting decimal CS number is within the limits of the office, the resulting number is the failing CS number.

(5) Compare the active B register contents with the complement of the ARO register and look for any mismatch.

6.08 A flowchart approach for analyzing D-level interrupts is given in Fig. 12. For an in-depth analysis of D-level interrupts, refer to Section 231-109-301.

Example: CC CS ERROR

6.09 Bit positions 3 and 10 of ILAF (Fig. 13) indicate that a valid D-level interrupt occurred. The MOCR has 0.1401 in the four least significant digits, indicating that both CCs are in service and in the routine matching mode. The CBT bit (bit 7 of CSTF) is 0, indicating that the standby CC was receiving on the standby bus. CBA (bit 6) is set to 1, indicating bus 1 was active. CBO (bit 5) is 0, indicating the standby CC was sending on the standby bus. PFC (bit 7 of SESA) is set to 1, indicating the active CC saw an error in the computation of the parity check over the data and address. Since the even-numbered CSs in a normal configuration are connected to the active CC, the even-numbered CS caused the interrupt. Looking at the failing CS address 0.00177743 and dropping off the four least significant digits leaves 0.17. Subtracting 1 leaves 16, which, when converted to decimal, shows that this address belongs to the H-half of CS14. Comparing the active B register with the complement of the data in the ARO register, bit 10 shows a mismatch. Since the active CC detected the error, and a 1 was received instead of a 0, the logic associated with bit 10 in the H-half of CS 14 should be checked.

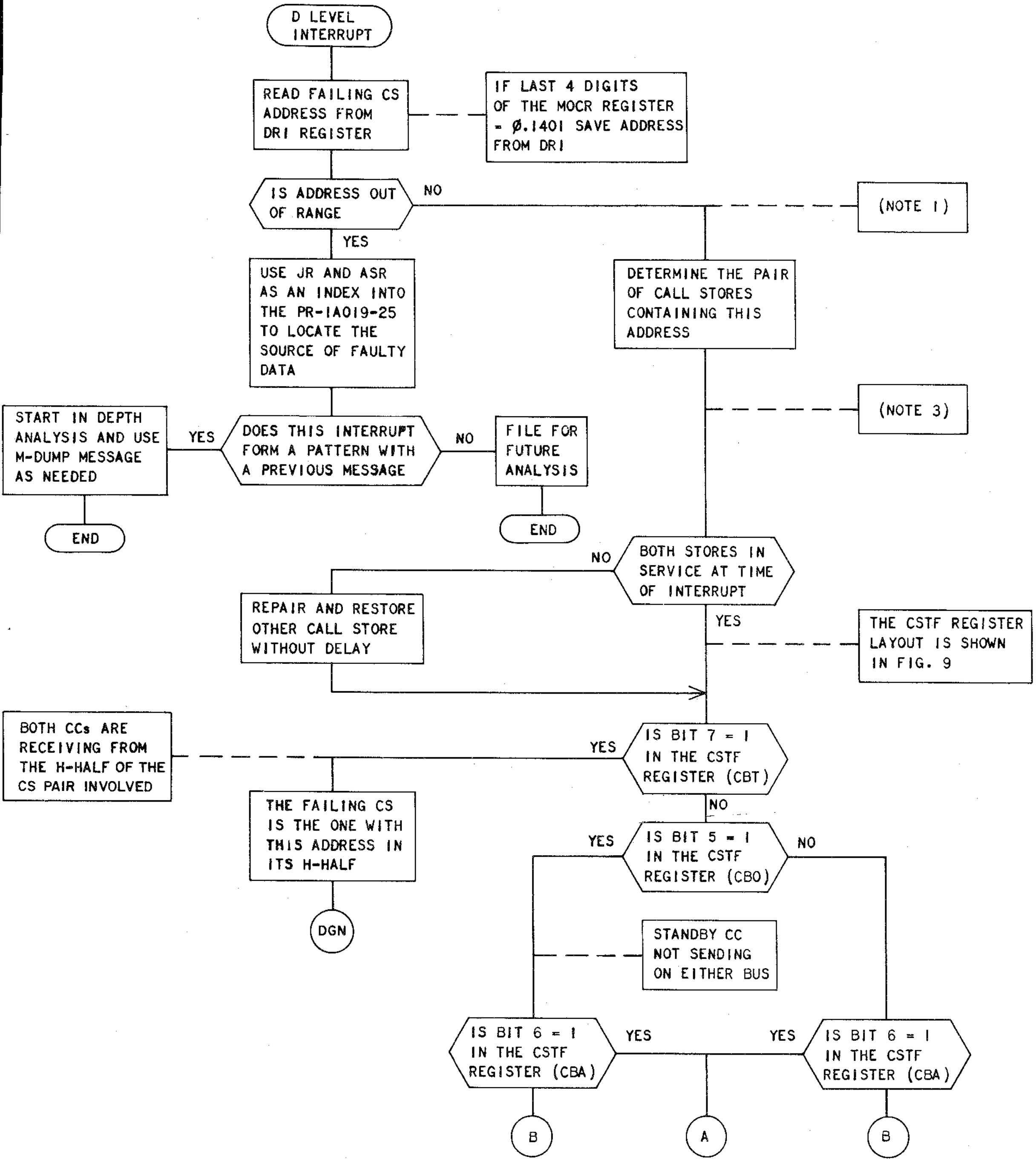
Example: SP CS ERROR

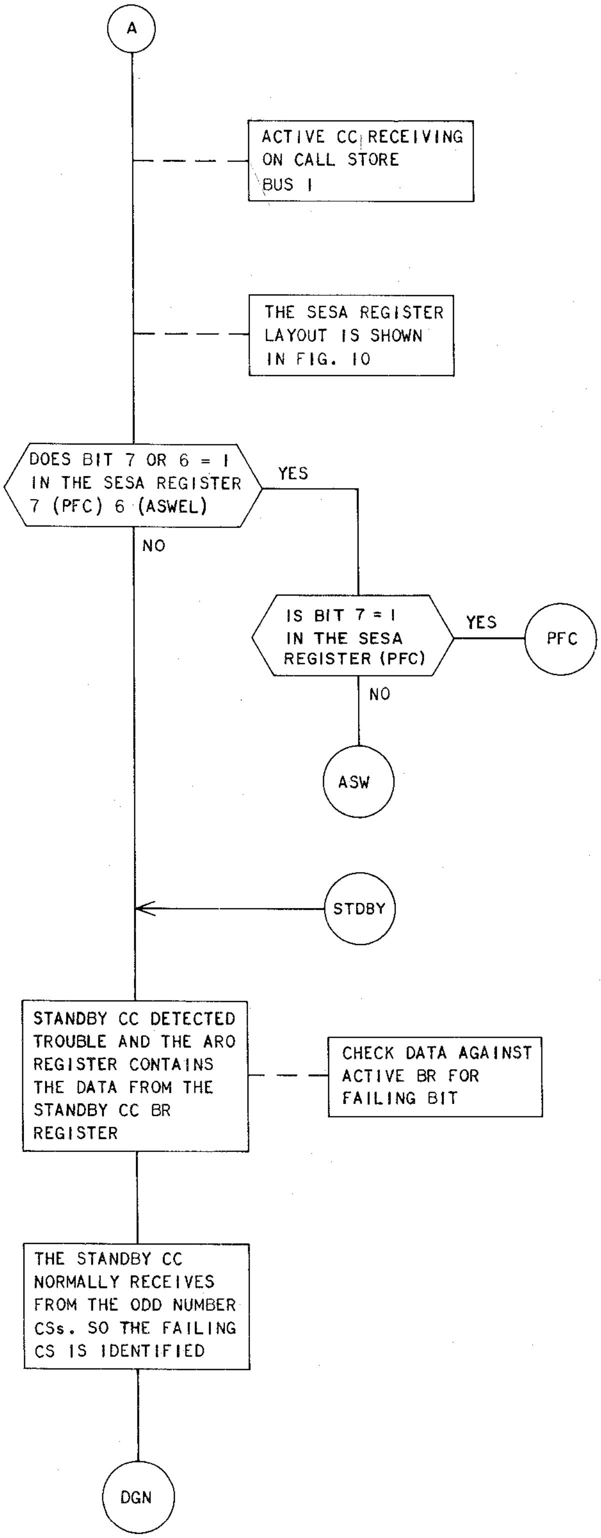
6.10 Bits 3 and 10 of ILAF register (Fig. 14) indicate a normal D-level interrupt occurred. The system was in a routine matching mode as indicated by the MOCR register (four least significant bits equal 0.1401). CBO and CBT bits are zeros (CSTF register), indicating that the standby CC was sending and receiving on the standby bus. CBA bit was set to 1, indicating bus 1 was active. PFC bit (bit 7 in SESA) is 0, indicating that the standby CC saw the error. Checking the ARO register, it shows the complement of the data in the B register. Comparing the two registers after complementing the ARO register shows that the standby CC received an extra bit in bit position 3. The failing address in the DR1 register belongs to an SP CS.

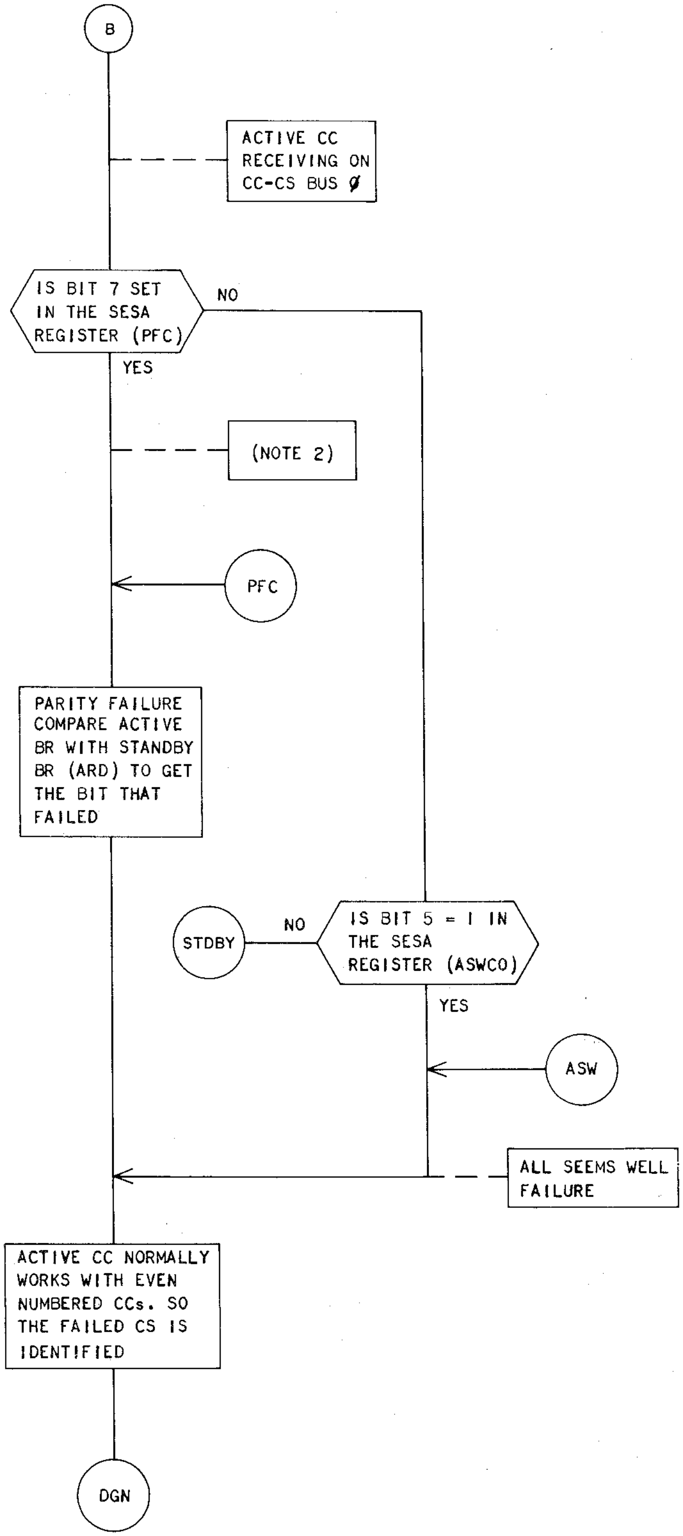
6.11 A D-level interrupt can be generated on a CC read of a faulty SP CS. On a CC write into a faulty SP CS, an SP interrupt occurs. If a D-level interrupt should occur on a write of SP CS, the SP circuitry that interfaces the CC and SP CS would be suspect.

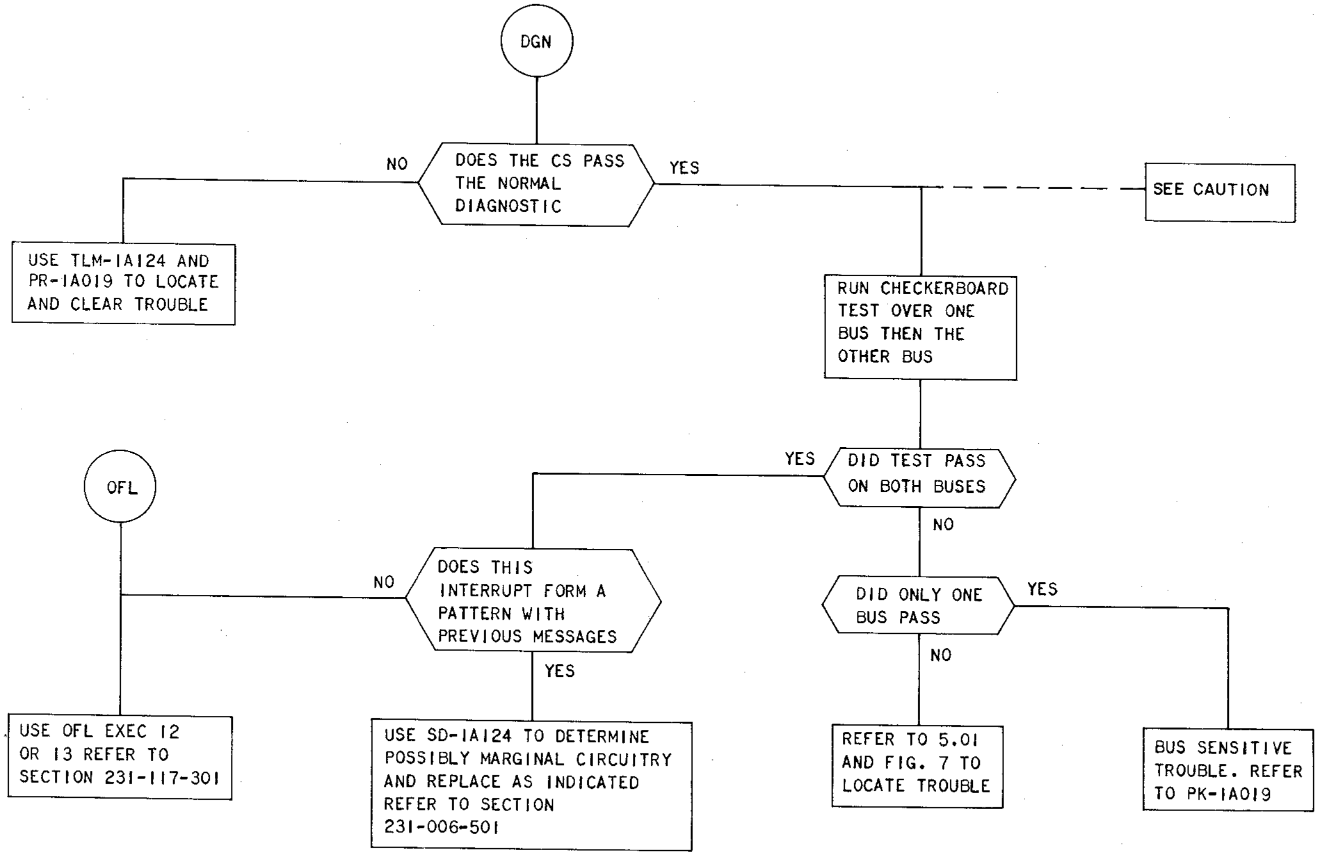
6.12 Next, check the match cycle flip-flops which are in bit positions 12 through 20 of the MOCR/MACF registers (Fig. 15). Bit position 16 indicates that a read order was being performed. Bit 19 indicates that the match cycle counter has a value of 2. Knowing that the system is performing a read instruction indicates an SP CS fault. The failing address was checked and the results corresponded to the address range of SP CS 1, H-half, an odd-numbered store.

6.13 Since the SP CSs are normally configured in the same way as the CC CSs (even-numbered to this active system), SP CS 1 and also the logic in the standby SP, which permits the CC to communicate with the SP CS, was suspected.


D LEVEL INTERRUPT
READ FAILING CS ADDRESS FROM DRI REGISTER
IF LAST 4 DIGITS OF THE MOCR REGISTER = 0.1401 SAVE ADDRESS FROM DRI
IS ADDRESS OUT OF RANGE
NO
(NOTE 1)
YES
USE JR AND ASR AS AN INDEX INTO THE PR-1A019-25 TO LOCATE THE SOURCE OF FAULTY DATA
DETERMINE THE PAIR OF CALL STORES CONTAINING THIS ADDRESS
(NOTE 3)
START IN DEPTH ANALYSIS AND USE M-DUMP MESSAGE AS NEEDED
YES
DOES THIS INTERRUPT FORM A PATTERN WITH A PREVIOUS MESSAGE
NO
FILE FOR FUTURE ANALYSIS
END
END
NO
BOTH STORES IN SERVICE AT TIME OF INTERRUPT
REPAIR AND RESTORE OTHER CALL STORE WITHOUT DELAY
YES
THE CSTF REGISTER LAYOUT IS SHOWN IN FIG. 9
BOTH CCs ARE RECEIVING FROM THE H-HALF OF THE CS PAIR INVOLVED
YES
IS BIT 7 = 1 IN THE CSTF REGISTER (CBT)
NO
THE FAILING CS IS THE ONE WITH THIS ADDRESS IN ITS H-HALF
YES
IS BIT 5 = 1 IN THE CSTF REGISTER (CBO)
NO
DGN
STANDBY CC NOT SENDING ON EITHER BUS
IS BIT 6 = 1 IN THE CSTF REGISTER (CBA)
YES
YES
IS BIT 6 = 1 IN THE CSTF REGISTER (CBA)
B
A
B


A
ACTIVE CC RECEIVING ON CALL STORE BUS 1
THE SESA REGISTER LAYOUT IS SHOWN IN FIG. 10
DOES BIT 7 OR 6 = 1 IN THE SESA REGISTER 7 (PFC) 6 (ASWEL)
YES
NO
IS BIT 7 = 1 IN THE SESA REGISTER (PFC)
YES
PFC
NO
ASW
STDBY
STANDBY CC DETECTED TROUBLE AND THE ARO REGISTER CONTAINS THE DATA FROM THE STANDBY CC BR REGISTER
CHECK DATA AGAINST ACTIVE BR FOR FAILING BIT
THE STANDBY CC NORMALLY RECEIVES FROM THE ODD NUMBER CSs. SO THE FAILING CS IS IDENTIFIED
DGN


B
ACTIVE CC RECEIVING ON CC-CS BUS 0
IS BIT 7 SET IN THE SESA REGISTER (PFC)
NO
YES
(NOTE 2)
PFC
PARITY FAILURE COMPARE ACTIVE BR WITH STANDBY BR (ARD) TO GET THE BIT THAT FAILED
STDBY
NO
IS BIT 5 = 1 IN THE SESA REGISTER (ASWCO)
YES
ASW
ALL SEEMS WELL FAILURE
ACTIVE CC NORMALLY WORKS WITH EVEN NUMBERED CCs. SO THE FAILED CS IS IDENTIFIED
DGN



NOTES:

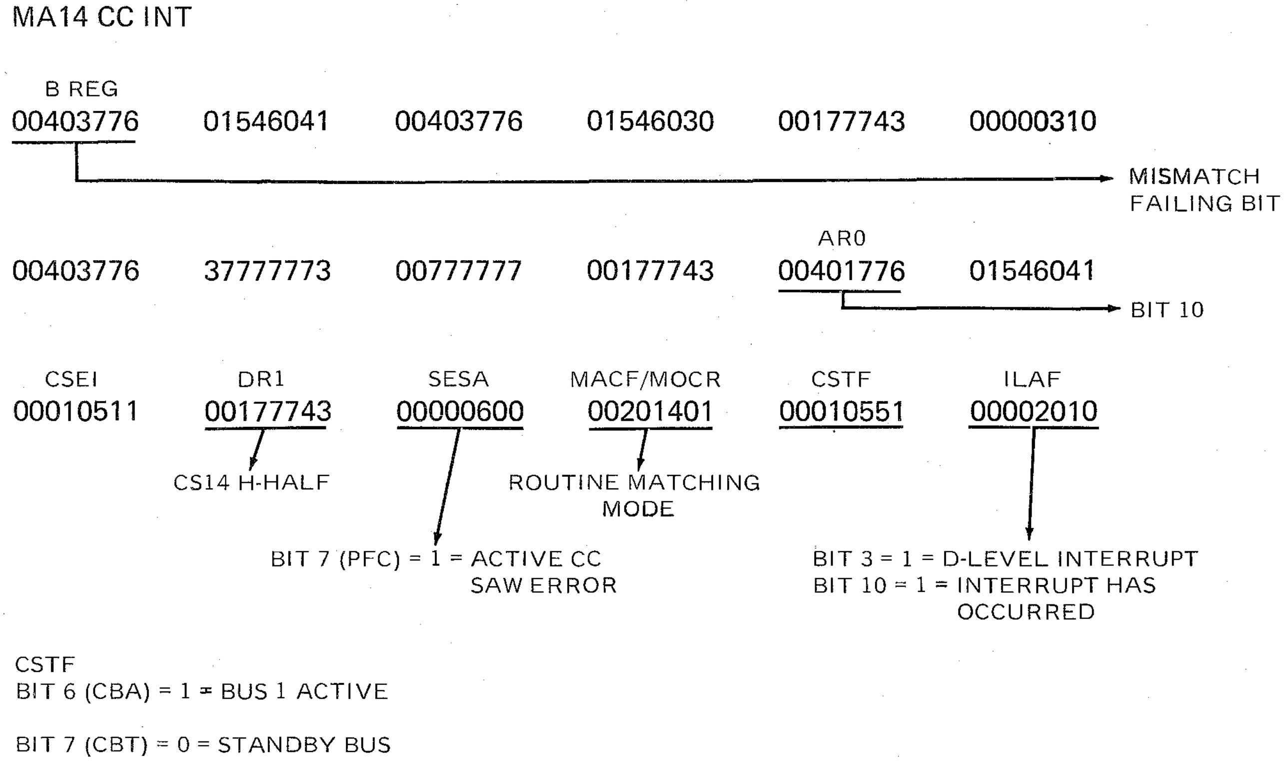
1. FROM THE FAILING ADDRESS DROP THE FOUR LEAST SIGNIFICANT DIGITS, SUBTRACT ONE FROM THE REMAINING NUMBER AND CONVERT THE RESULTS FROM OCTAL TO DECIMAL. THIS GIVES THE CS NUMBER WITH THE FAILING ADDRESS IN ITS H-HALF. THE PRECEEDING CS ALSO CONTAINS THIS ADDRESS IN ITS G-HALF.

   EX: 1 - FAILING ADDRESS = 0.126032
   2 - DROP FOUR LS DIGITS = 0.12
   3 - SUBTRACT ONE = 0.11
   4 - CONVERT TO DECIMAL = 9
   5 - THE FAILING ADDRESS IS IN THE H-HALF OF CS NO. 9 AND THE G-HALF OF CS NO. 8
2. IF NO MISMATCH IS SHOWN BETWEEN THE ACTIVE BR AND THE STANDBY BR (ARO) THE PARITY BIT 23 CAUSED THE FAILURE.
3. REVIEW THE CS STATUS PRINTOUT FROM THE PREVIOUS HOUR, AND IF THIS STORE WAS OUT OF SERVICE, DETERMINE IF IT WAS RESTORED BY THE SYSTEM AUTOMATICALLY OR MANUALLY.

CAUTION:

IF OTHER HALF GOES INTO TROUBLE THE CS WITH THE CHECKERBOARD TEST MAY BE PUT ON LINE WITH THE CHECKERBOARD INFORMATION IN THE CS. RUN THESE TEST DURING PERIODS OF LIGHT TRAFFIC.

Fig. 12—D-Level Interrupt Analysis Flowchart



```
MA14 CC INT

B REG
00403776    01546041    00403776    01546030    00177743    00000310

00403776    37777773    00777777    00177743    00401776    01546041

CSEI        DR1         SESA        MACF/MOCR   CSTF        ILAF
00010511    00177743    00000600    00201401    00010551    00002010
```

Fig. 13—Example of CC CS Error

Example: CC CS ERROR

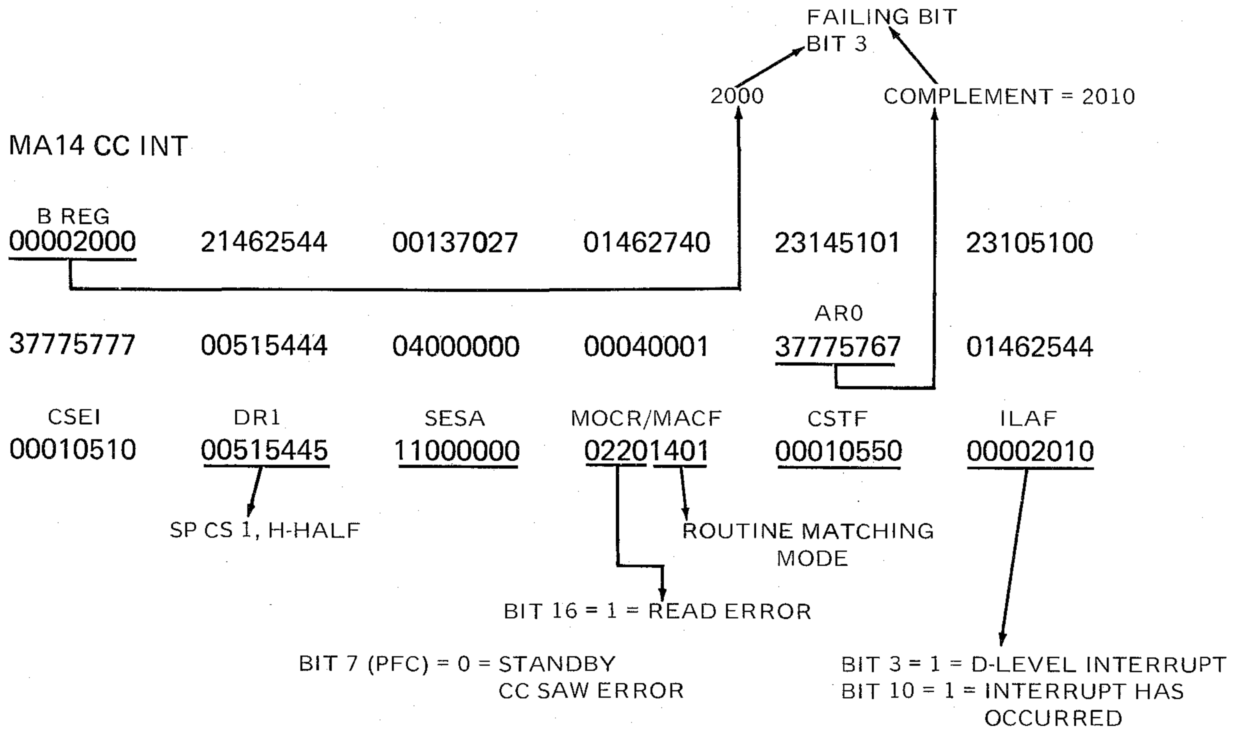
6.14 Bits 3 and 10 of ILAF register (Fig. 16) indicate that a valid D-level interrupt occurred. MOCR indicates that the system was operating in routine matching mode (0.1401 in the four least significant digits). CSTF indicates that the standby CC is sending and receiving on the standby bus (CBO and CBT reset) and that bus 1 was active (CBA set). The active CC saw the error since PFC bit (bit 7) in SESA register is set. The failing CS address (DR1) shows it to be the H-half of CS 14, an even-numbered store. Comparing the active CC B register with the complement data in the ARO register, bit 8 was found to be failing. The circuitry associated with bit position 8 is suspected.

DETECTING FAILING CALL STORE FROM D-LEVEL INTERRUPT

6.15 A brief analysis of the MA14 CC INT printout will give the failing CS. Using the contents of B8 DR1 (see example in 6.18), drop the rightmost 4 digits as shown in example. Take the remaining 2 digits, convert the octal digits to decimal, and subtract 1. This number should now equal the CS that failed, but it may be necessary to subtract 1 again from this number depending on which CC detected the error.

6.16 On CSs the active CC addresses the even-numbered CSs. The standby CC addresses the odd-numbered CSs. To determine which CC detected the trouble, refer to B8SESA on the MA14 CC INT printout. Convert the octal number to binary. If bits 5, 6, and 7 equal 0, the standby CC detected the trouble on a parity failure. If bits 5, 6, and 7 do not equal 0, the active CC detected the trouble unless the routing FFs indicate that ASW failure was on the standby bus.

6.17 As shown in the example (6.18), the active CC detected the trouble. Since the number that was obtained in 6.15 is now an odd number, subtract one again; this will give CS 22_{10} as the failing CS.



```
MA14 CC INT

B REG
00002000   21462544   00137027   01462740   23145101   23105100

                                            AR0
37775777   00515444   04000000   00040001   37775767   01462544

CSEI       DR1        SESA       MOCR/MACF  CSTF       ILAF
00010510   00515445   11000000   02201401   00010550   00002010
```

CSTF
BIT 6 (CBA) = 1 = BUS 1 ACTIVE

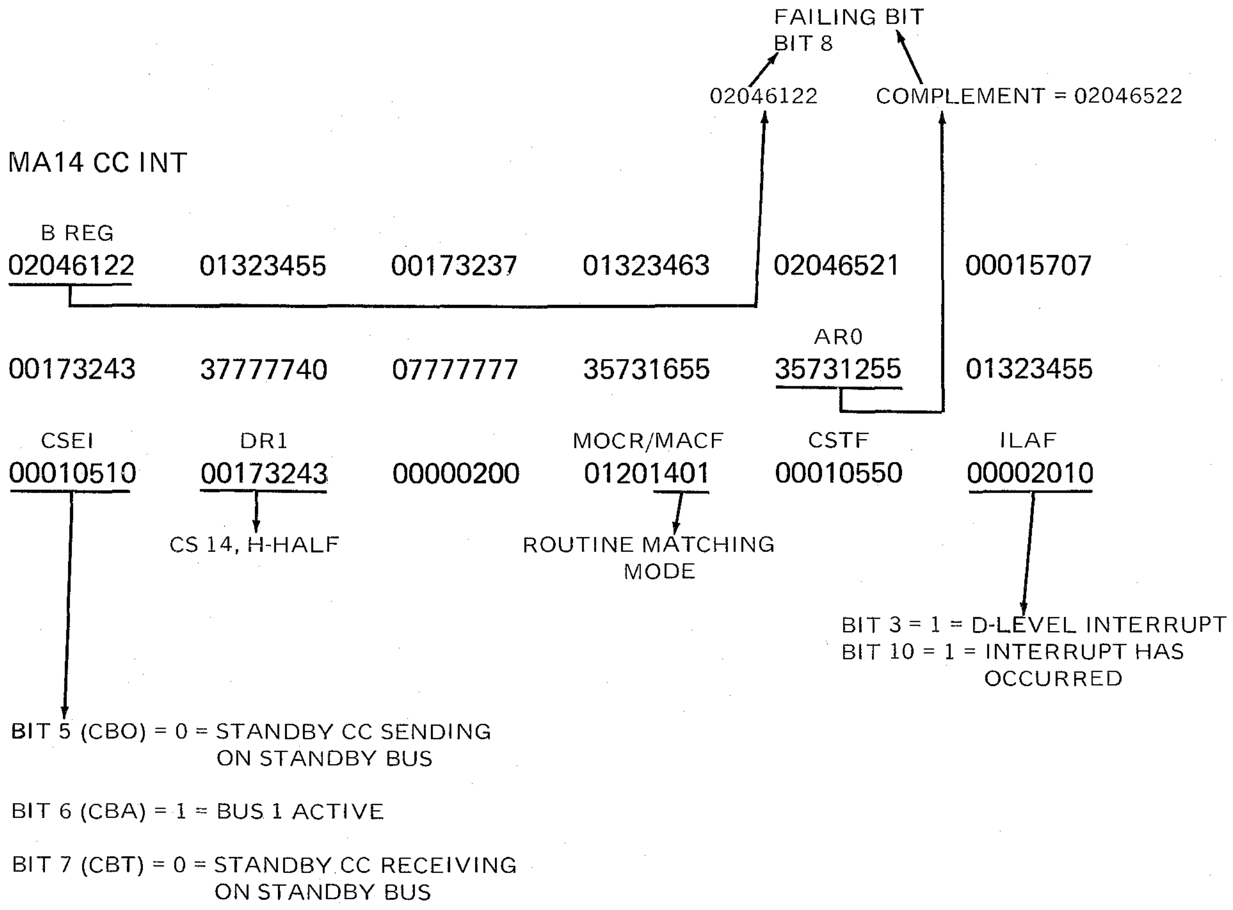
BIT 7 (CBT) = 0 = STANDBY CC RECEIVING
ON STANDBY BUS

Fig. 14—Example of SP CS Error

BUFFER REGISTER BIT POSITION	NAME OF BIT	ACCESS (SEE NOTE)			COMMENTS	LOCATION IN SD
		R	W	C		
00						
01						
02						
03						
04						
05						
06						
07						
08						
09						
10						
11						
12	M0	X			Flip-flop outputs of matchers	FS 85 Maintenance Control System M
13	M1	X				
14	PU	X	X	X	This flip-flop is set on peripheral orders	
15	WR	X	X	X	This flip-flop is set on write orders	
16	RE	X	X	X	This flip-flop is set on read orders	
17	EC	X	X	X	This flip-flop is set on error correction	
18	MC13	X	X	X	Bits of match cycle counter	
19	MC23	X	X	X		
20						
21	MRC	X	X	X	Defines which CS bus is to be used for CS maintenance and control word reception	
22	MRP	X	X	X	Defines which PS bus is to be used for PS maintenance and control word reception	

Note: R — Bit position can be read with read-memory orders.
W — Bit position can be written into with write-memory orders.
C — Bit position can be written into with control-write orders.

Fig. 15—MACF Register Layout



```
MA14 CC INT

B REG
02046122    01323455    00173237    01323463    02046521    00015707

                                                ARO
00173243    37777740    07777777    35731655    35731255    01323455

CSEI        DR1                     MOCR/MACF   CSTF        ILAF
00010510    00173243    00000200    01201401    00010550    00002010
```

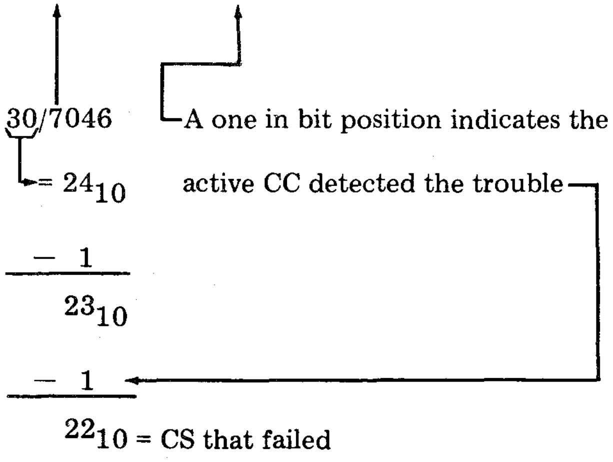
Fig. 16—Example of CC CS Error No. 2

6.18 The location of valid registers for a D-level interrupt is as shown below:

```
    MA14 CC INT

B REG ASR F REG J REG K REG X REG

Y REG Z REG L REG ADDEN K AR0 DR0

                 MACF
CSEI   DR1 SESA MOCR CSTF ILAF
```

Example

```
  21  MA14A
00000000 01565610 01267375 01531225 01573607 01232126

 **21 MA14 CC INT
00400134 01531346 00000005 01573607 00307046 00000000
00250052 00207147 00000040 00307046 37377643 01531346
00010511 00307046 02000100 01101401 00010551 00002010
```



7. ERRORS

7.01 Normally if the CS takes errors, the system will generate a D-level interrupt and request a diagnostic on the CS. Occasionally, the CS will take a random error due to a marginal circuit pack or some intermittent trouble. Figure 17 gives a flowchart approach to locating error problems.

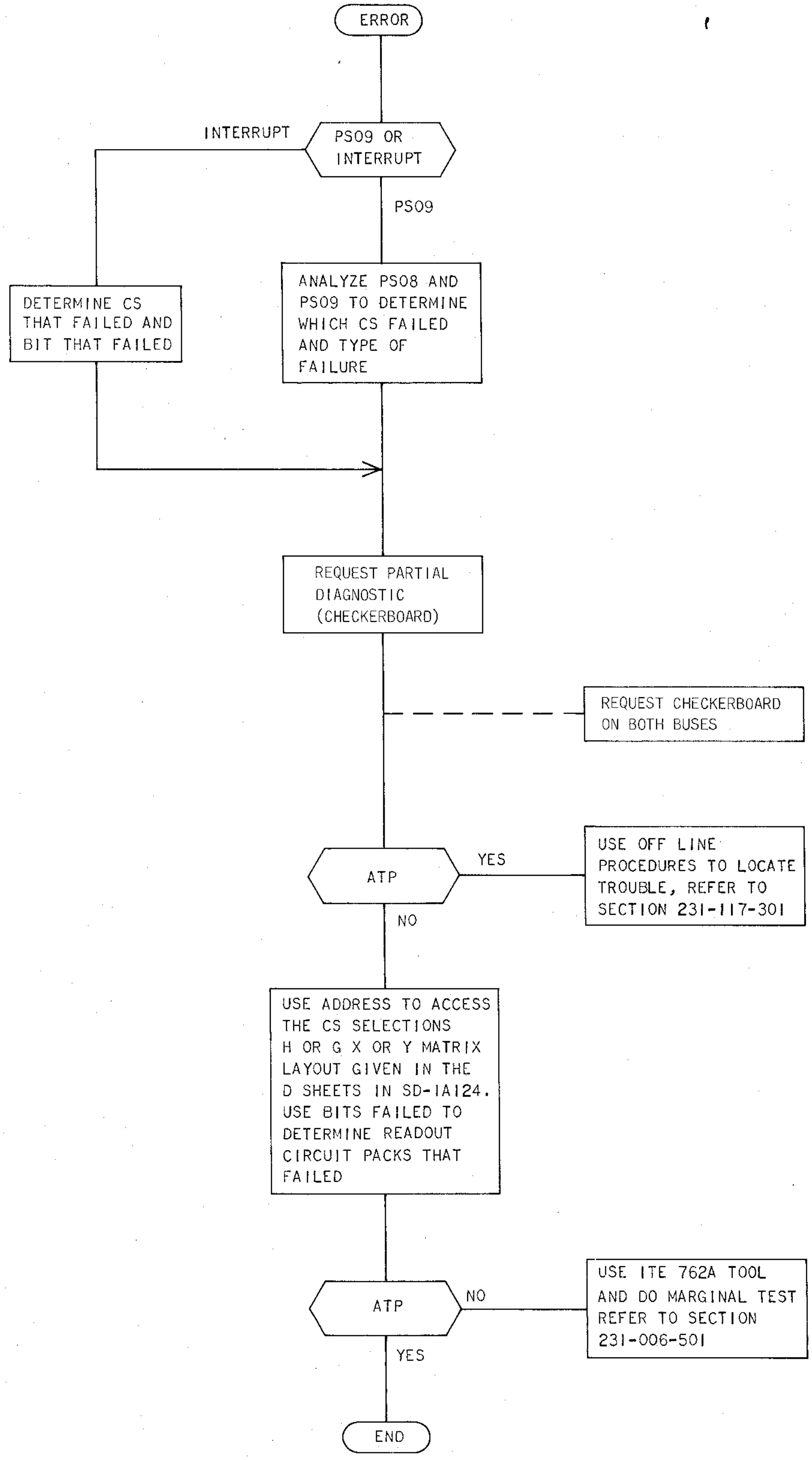
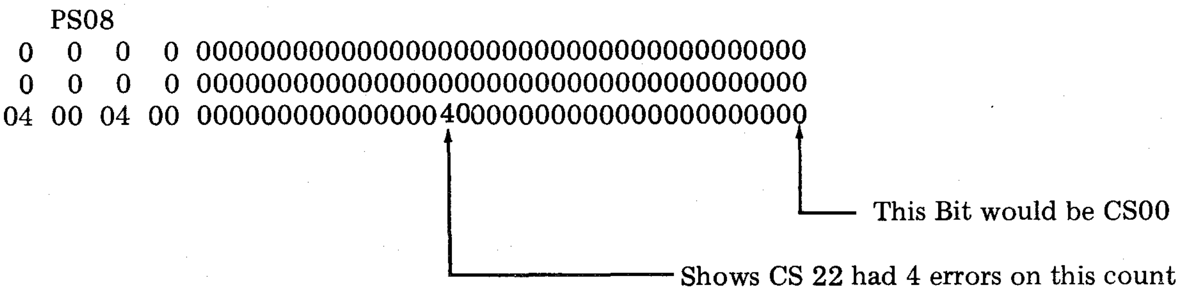
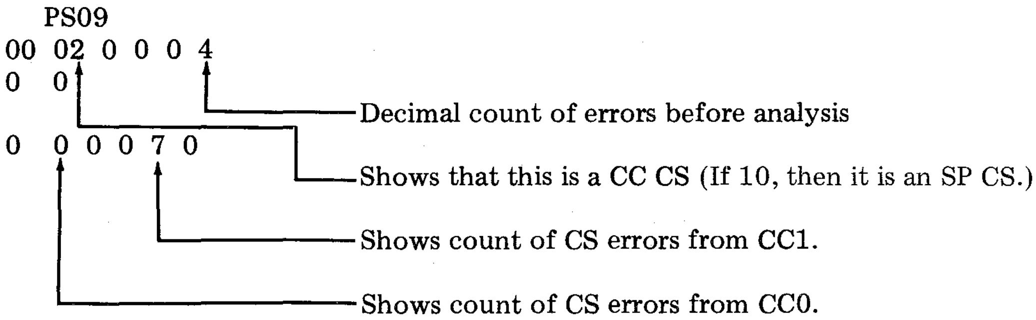


Fig. 17—Error Troubleshooting Flowchart

7.02 To trap random errors, two input messages can be used. The PCS-DUMPERR-. message will give the output messages PS08 and PS09 and a raw data dump. The PCS-TRAPERR-a. message, where a is equal to 2 for CC CSs and a is equal to 3 for SP CSs, will cause the PS08 and PS09 output messages to print on the TTY if an error is detected. This message may time out before an error is detected. The PS08 and PS09 messages are also generated automatically by the system on a routine basis. The PS08 and PS09 output messages and the procedure for breaking them down is given below. (Refer to OM-1A001 for other breakdowns.)



```
 PS08
0  0  0  0  00000000000000000000000000000000000000
0  0  0  0  00000000000000000000000000000000000000
04 00 04 00 00000000000000040000000000000000000000
```



```
 PS09
00 02 0 0 0 4
0  0
0  0 0 0 7 0
```

7.03 To locate errors caused by a marginal circuit pack, it may be necessary to run the CS margin checks. Section 231-006-501 gives the complete procedure for this test.

7.04 Another method for trapping random errors is to use the ØFL-EXEC-18 message. This off-line message causes the contents of the active CC and the buffer registers to be printed (dumped) on the TTY when a CS single error occurs. The dump is contained in the TW02 output message which consists of 32 words of 8 octal digits each.

> ***Note:*** ØFL-EXEC-18 message will cause a dump if a bad PS word is read but not if control is transferred to a bad PS word. Check word 22 of the TW02 output message to see what type of error has occurred. If a valid CS single error has occurred, words 11 and 12 of the TW02 message will show the address of the CS error, and words 13 and 14 will show the contents of the word.

7.05 After completion of the dump, use the ØFL-MODE-03. message followed by CC-RESTØRE--- message to deactivate the trapping routine.

8. MEMORY CURRENTS

A. General

8.01 This part describes the memory currents in the No. 1 ESS 8K CSs. It is intended to help locate troubles in the case of faulty memory currents.

8.02 The analysis of memory current waveforms is much more complex than the analysis of logic type voltage waveforms. For example, a slight error (in the order of 5 to 10 percent) in rise time or amplitude may be very hard to detect, but may cause the CS to malfunction. It should be noted that the memory is an analog machine as far as the currents are concerned, making their amplitude and waveshapes critical.

B. Types of Currents in the CS

Main Drive Currents

8.03 There are two identical sets of current drivers for both the X and Y access. Each set consists of two A97 circuit packs (Fig. 18). The current from both drivers can be steered into either the G-half or H-half. Each consists of 64 X coordinates and 64 Y coordinates, representing 4096 addresses (Fig. 19). The access circuitry steers the currents to the proper coordinate.

Auxiliary Drive Currents

8.04 The auxiliary drive currents are supplementary currents and are used to add or subtract correction currents to the main drive currents to compensate for drift. They are generated by two A130 circuit packs, one for each access (Fig. 18). Their variable amplitude is only a fraction of the access current amplitude. The magnitude is controlled by a servo system. Note that there is a READ as well as a WRITE auxiliary current, the magnitude of both being the same. The auxiliary currents flowing into the A130 circuit packs are four times larger than the auxiliary currents flowing through the memory modules due to a 4 to 1 turns ratio of the transformers on the A100 circuit packs. The waveforms of the primary auxiliary currents are shown in Fig. 20, representing a superposition of 16 pictures. Shown are both the READ and WRITE auxiliary currents with all possible current amplitudes corresponding to all states of the X-servo counter ranging from 0 to binary 7.

Inhibit Currents

8.05 The inhibit currents are two independent sets of inhibit drivers, one for the G-half and one for the H-half. In each set one inhibit driver is associated with one of the 24-bit planes. Two inhibit drivers are mounted on an A96 circuit pack, one driving a bit plane in the G-half, the other driving a bit plane in the H-half. Since only one half is being addressed at a time, only one driver per circuit pack may be fired. The waveforms of the inhibit currents are shown in Fig. 21.

C. Amplitude Control of the Memory Currents

Current Regulating Scheme

8.06 The readout signal of the memory module is temperature dependent. In order to keep the readout of the memory at a constant level, the currents have to be adjusted for temperature compensation. A temperature sensitive regulator provides a reference voltage to all access and inhibit current drivers whose current amplitude is proportional to this reference voltage. This regulating scheme is indicated in Fig. 22. An A98 circuit pack serves as the temperature sensitive regulator while seven A133 tracking regulators share the load.

8.07 The output of the A98 circuit pack has a temperature coefficient of -14 millivolts per degree Celsius (C). This circuit pack is factory adjusted to +5 ±.010 volts at 26 degrees Celsius. However, with an ambient of 25 degrees Celsius and the circuit pack plugged in place in the CS, its output voltage is somewhat lower due to an increased temperature within the frame of 5 degrees to 7 degrees Celsius at that particular location.

8.08 Note that the current values given in Fig. 21, 23, and 25 correspond to a memory module temperature of 25 degrees Celsius. The A98 circuit pack causes these currents to change as a function of temperature as follows:

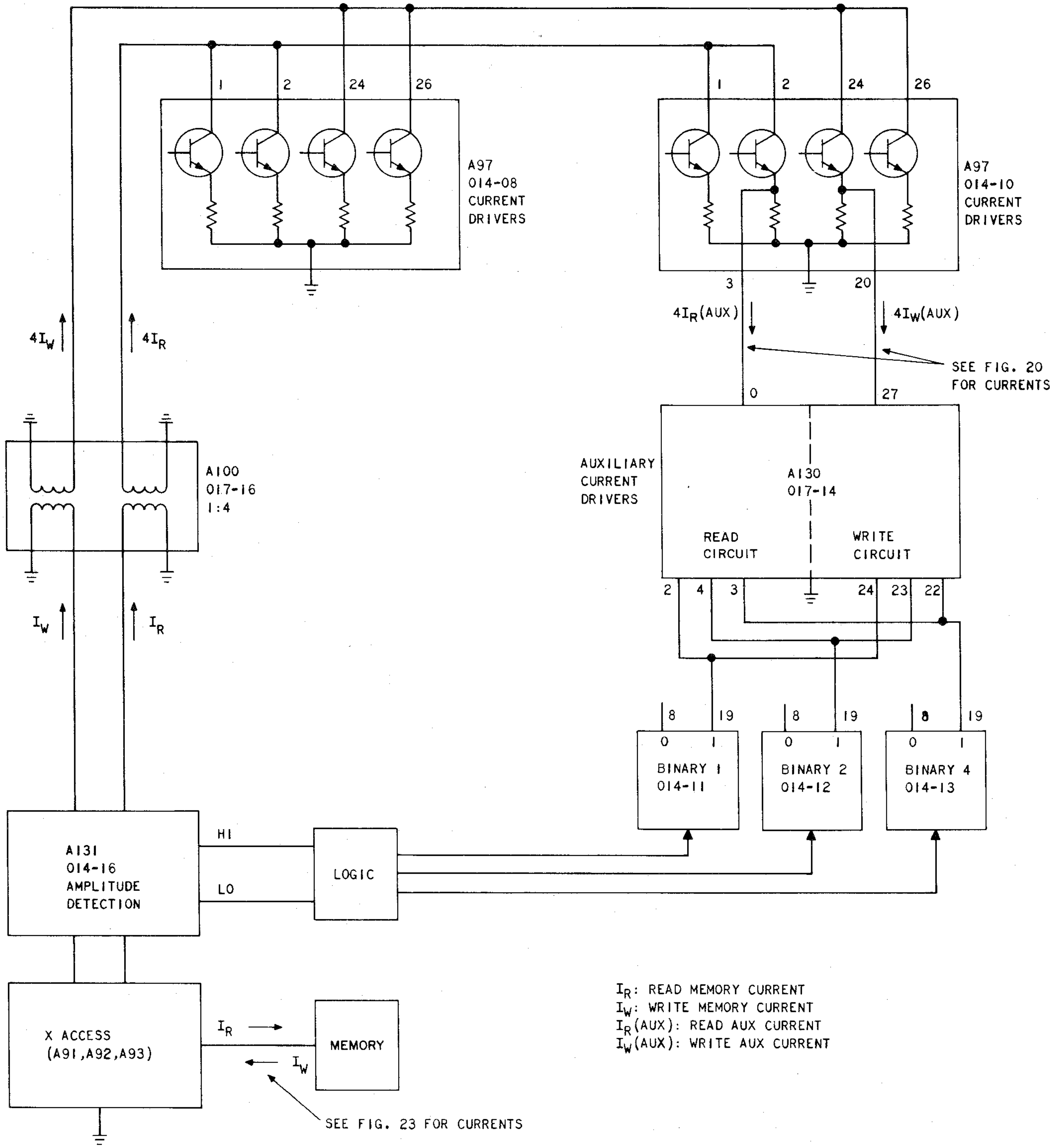
Access currents (Fig. 23 and 25): -1.0 ma/°C

Inhibit currents (Fig. 21): -0.8 ma/°C

Servo System

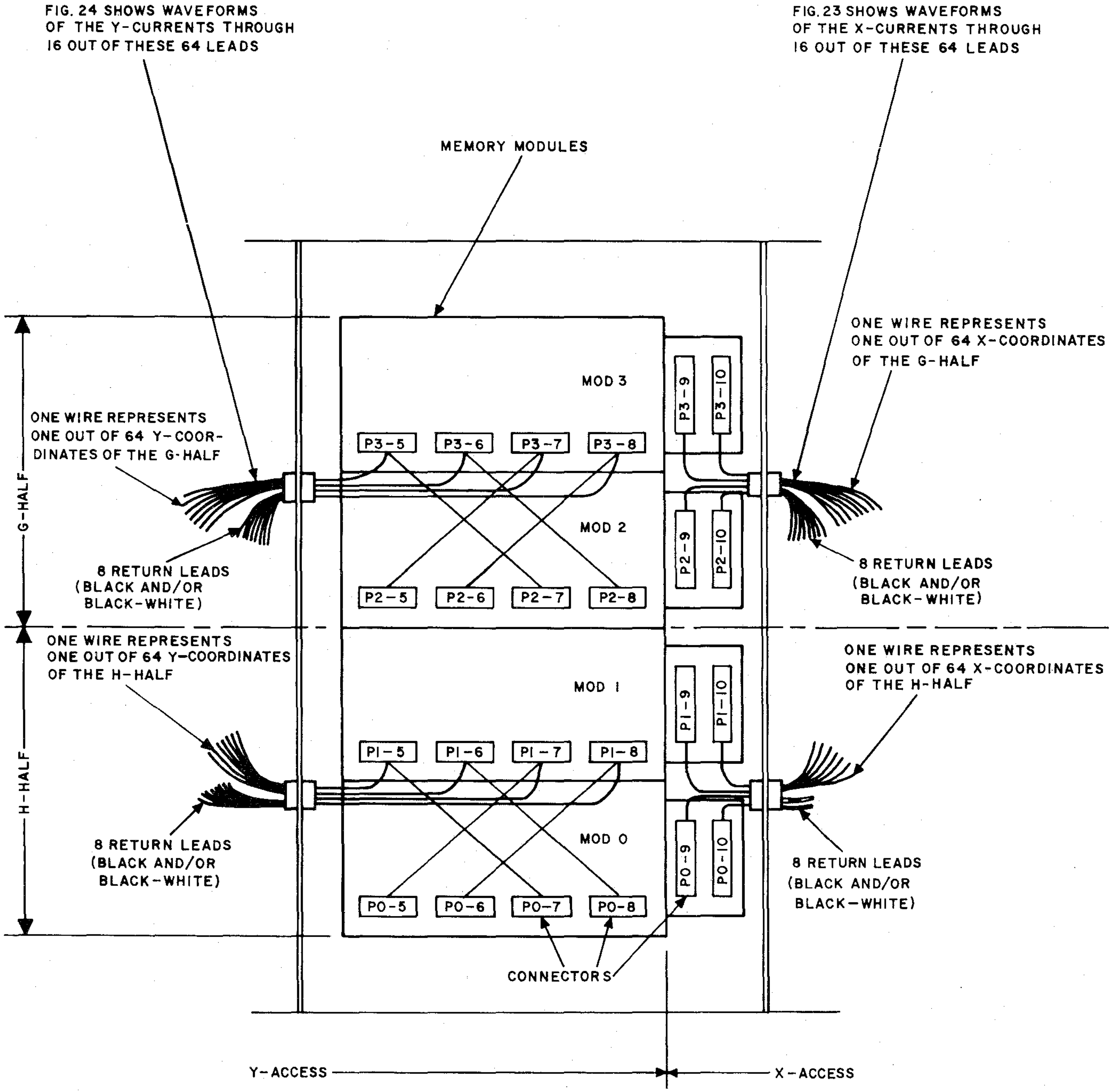
8.09 The A98 temperature coefficient, which determines the regulation, however, is not accurate enough over the operating temperature range to maintain a constant level of the memory readout signal. The servo system compensates for any additional current deviations which might occur. Separate independent acting servo systems are used for both X and Y access circuits; inhibit currents are not stabilized by a servo system. Figure 18 shows a simplified block diagram of the X-servo system.

8.10 The A131 package is a current amplitude detecting device. The two logical outputs indicate one of the following three conditions: the READ and WRITE currents are either too high,



I_R: READ MEMORY CURRENT
I_W: WRITE MEMORY CURRENT
I_R(AUX): READ AUX CURRENT
I_W(AUX): WRITE AUX CURRENT

Fig. 18—X Servo System Block Diagram



CALL STORE MEMORY BLOCK
VIEWED FROM WIRING SIDE

Fig. 19—Access Current Leads

correct, or too low. The associated logic circuitry controls a three-stage binary counter. This counter causes the binary-weighted auxiliary currents to flow through the memory module in addition to the main drive currents. One binary step corresponds to a current increment of 4 ma in the memory and an increment of 16 ma at the A130s.

8.11 If the currents of the A97 drivers have been adjusted properly and the room temperature

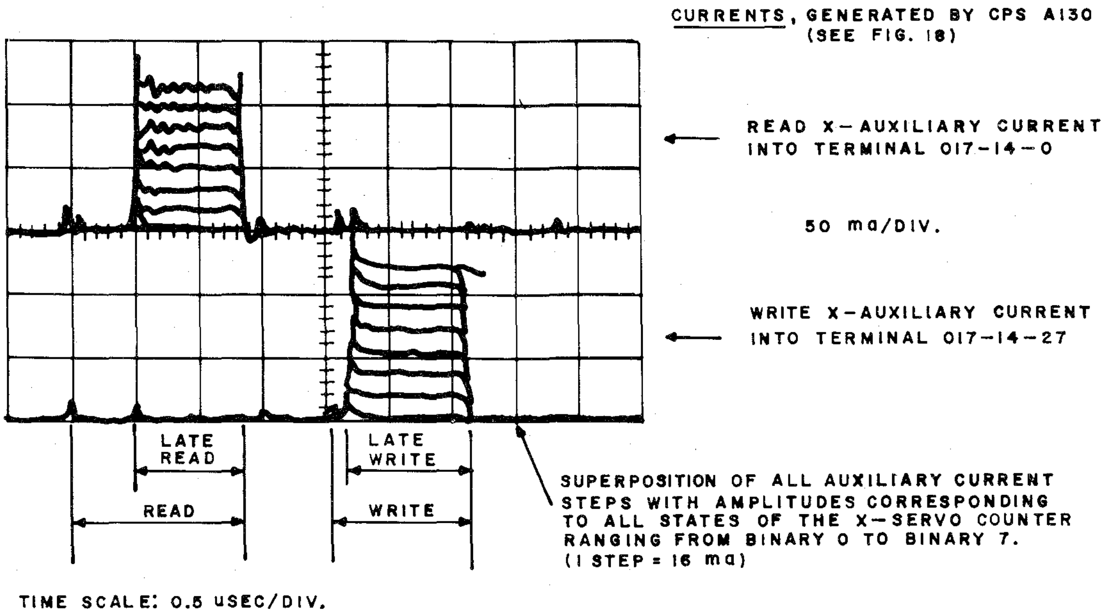


Fig. 20—Primary X Auxiliary Currents

is approximately 25 degrees Celsius, the servo counters should be in a midrange state, preferably binary 4. This means the servo system is adding 16 ma into the memory. A decrease in the drive current causes the counter to step up, and vice versa.

D. Correct Current Amplitudes

Current Measurements

8.12 In order to determine the absolute magnitude of a current, the measurement should be taken with a calibrated current probe only. Otherwise, errors in the range of ±5 percent or even larger are very likely to occur. If current standards are not available and a package must be checked (A96, A97, A130), make a relative measurement between several circuit packs.

Access Currents

8.13 Since the amplitude of the access currents is a function of the state of the servo counters, these currents should be measured under the following conditions (Fig. 24).

(a) Both X and Y servo counters clamped to state binary 4 by grounding the following points:

Y SERVO COUNTER	X SERVO COUNTER
014-36-19	014-11-19
014-37-19	014-12-19
014-38-8	014-13-8

(b) Write all 0s in all memory locations, using 0FL-EXEC- message. Refer to Section 231-117-301 for 2-wire and Section 231-417-301 for 4-wire for message for office generic.

(c) Memory temperature: 25 degrees Celsius. For different temperatures, the change is ±1.0 ma/°C.

8.14 The correct amplitudes are given in Fig. 23 and 25. Note the slight difference in waveshapes between the X and Y access currents due to impedance differences. The four A97 current driver circuit packs, however, are interchangeable.

8.15 The currents shown in Fig. 23 and 25 flow through any of the coordinate wires shown

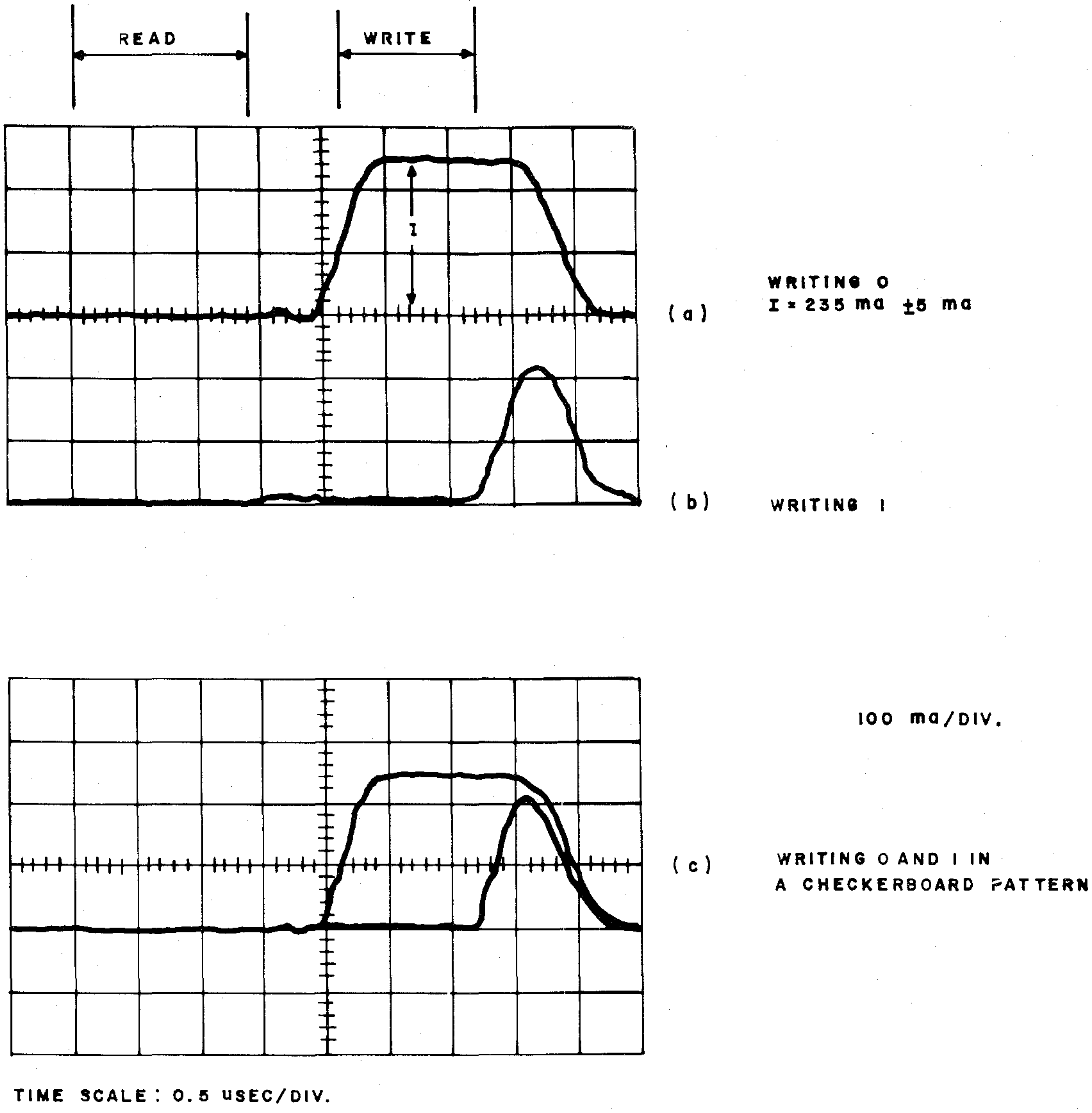


Fig. 21—Inhibit Currents

in Fig. 20. These currents do not flow through any of the black wires, however. These wires are return leads and purposely carry a considerable amount of stray capacitive discharge current.

Inhibit Currents

8.16 The amplitudes of the inhibit currents are controlled only by the reference voltages of the A133 circuit packs. These currents should be measured under the following conditions:

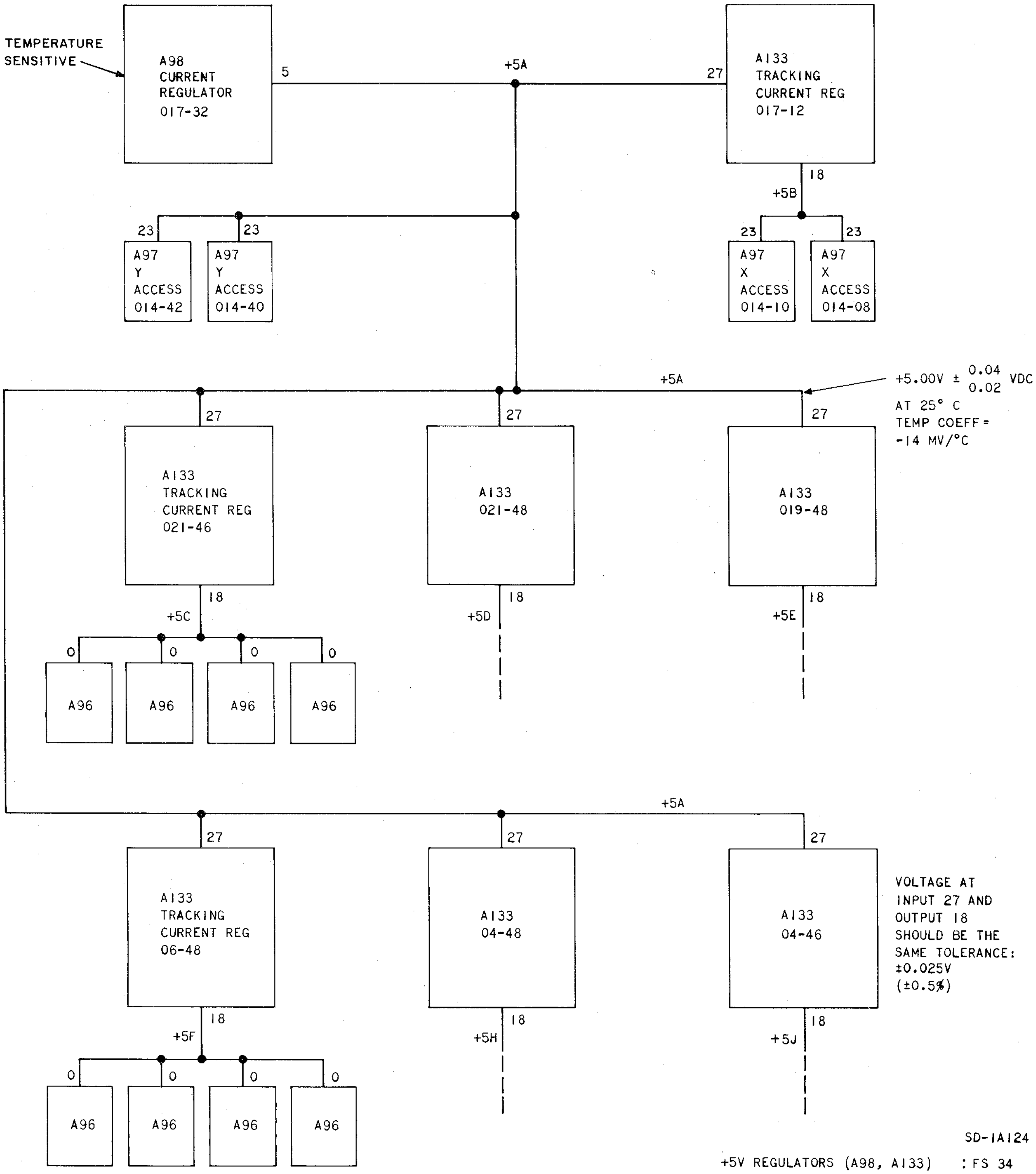
(a) Write all 0s in all memory locations.

(b) Memory temperature: 25°Celsius. For different temperatures the correction is ±0.8 ma/°C.

8.17 The correct amplitudes are given in Fig. 20. In case of writing a 1, the inhibit drivers are fired at the end of the WRITE cycle. The significance of the narrow ***post write disturb*** pulse is to reduce the shuttle noise due to nonideal properties of the magnetic material. The inhibit currents can be monitored right at the terminals of the A96 circuit packs.

E. Failures Affecting Memory Currents

8.18 The following is a list of failures affecting the memory currents in the order of likelihood of occurrence. All these failures may cause memory malfunctions.



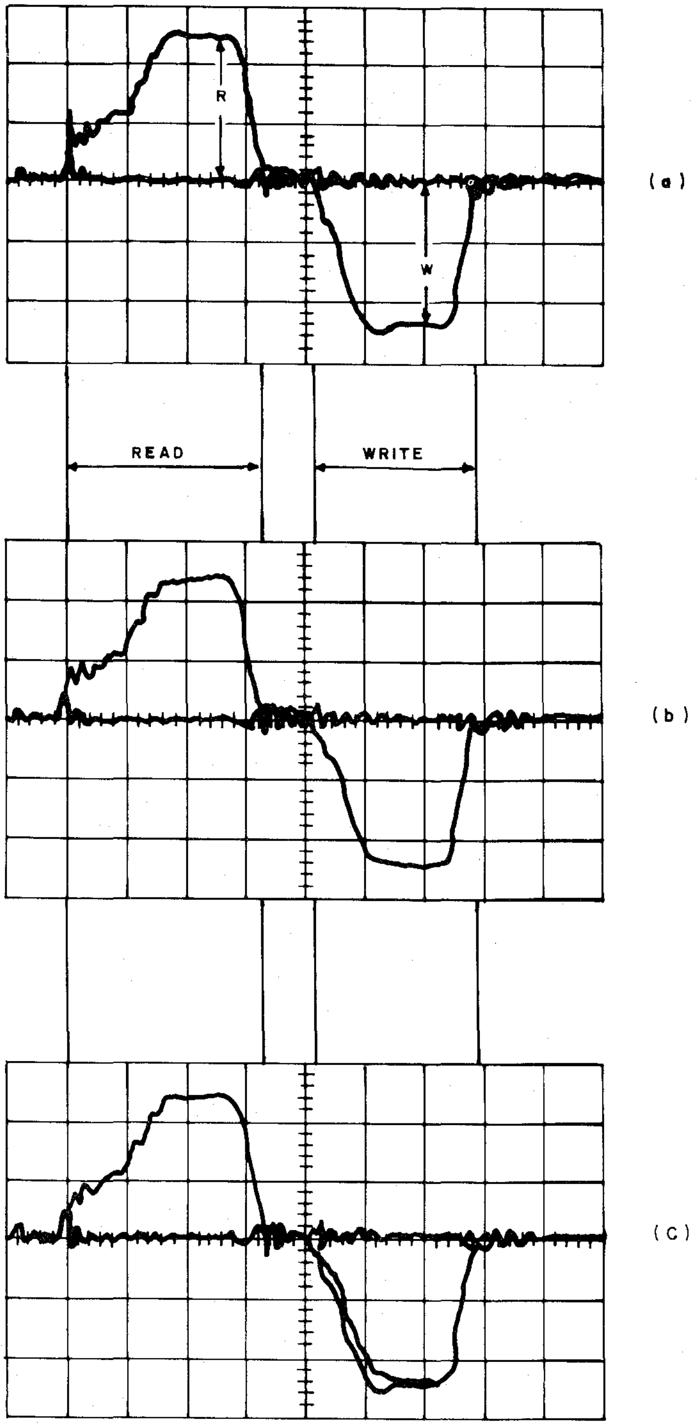
SD-1A124

+5V REGULATORS (A98, A133) : FS 34
ACCESS CURRENT DRIVERS (A97) : FS 6,7
INHIBIT CURRENT DRIVERS (A96) : FS 3

Fig. 22—Current Regulating Scheme Block Diagram

R=265 ma+5 ma
W=285 ma+5 ma

FOR MEASUREMENT CONDITIONS SEE PARAGRAPH 8.13



(a) WRITING 0 IN ALL MEMORY LOCATIONS. PICTURE SHOWS CURRENTS THROUGH A BUNDLE OF 16 OUT OF 64 Y—ACCESS LEADS. SEE FIG. 19 FOR LOCATION OF THESE LEADS.

(b) WRITING 1 IN ALL MEMORY LOCATIONS. THIS PICTURE SHOWS THE CURRENTS THROUGH THE SAME 16 LEADS.

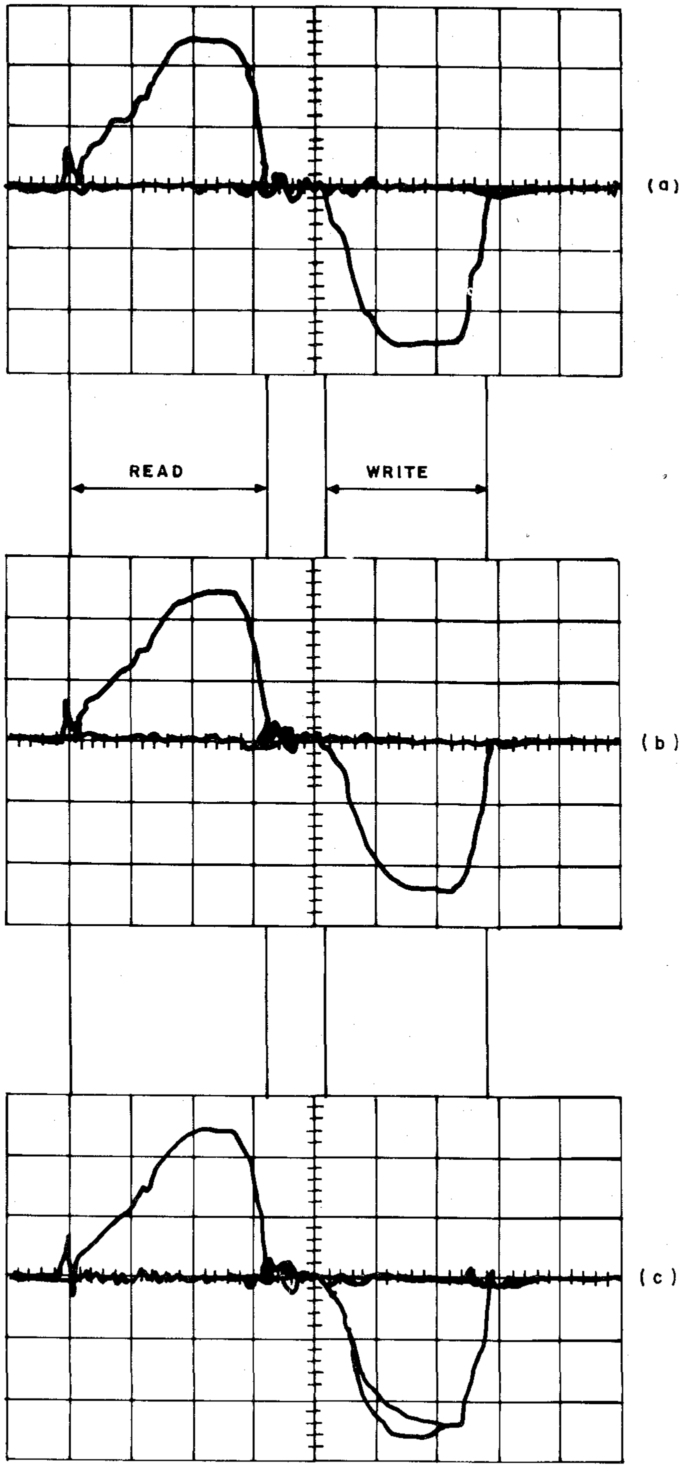
(c) WRITING 0 AND 1 IN A CHECKERBOARD PATTERN. THIS PICTURE SHOWS THE CURRENTS THROUGH THE SAME 16 LEADS AND IS A SUPERPOSITION OF THE TWO PICTURES SHOWN ABOVE.

SCALES:
HORIZONTAL: 0.5 USEC/DIV.
VERTICAL: 100 ma/DIV.

Fig. 23—X Access Currents

R = 265 ma ± 5 ma
W = 285 ma ± 5 ma

(FOR MEASUREMENT CONDITIONS SEE PARAGRAPH 8.13)



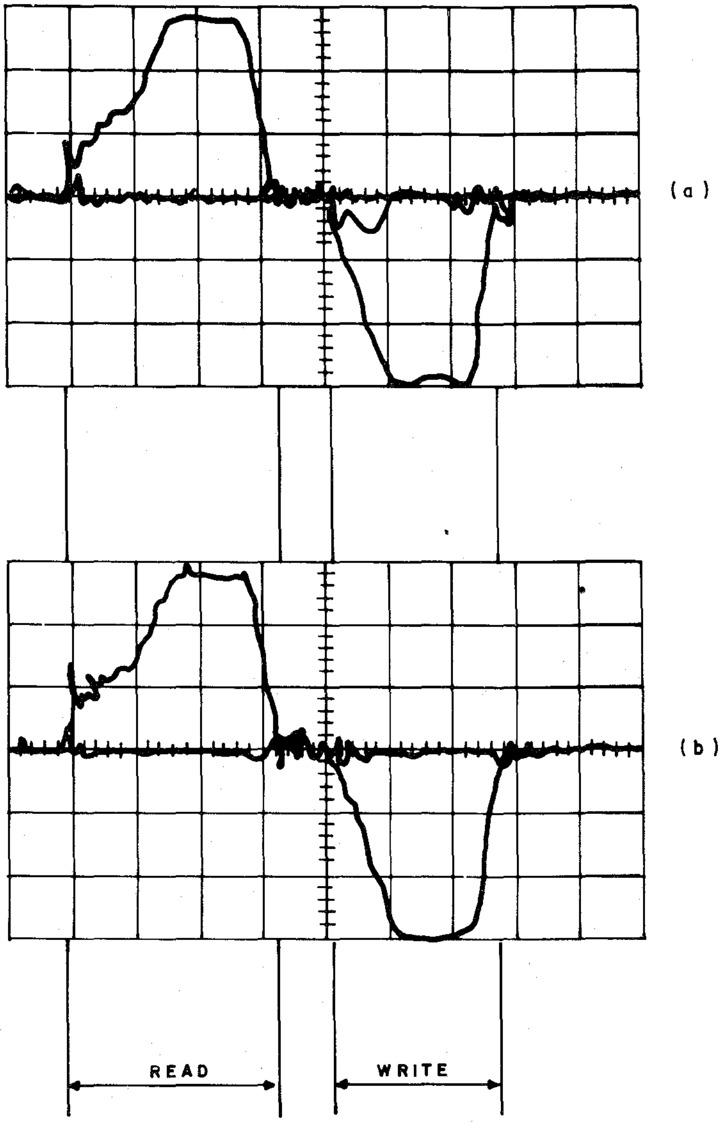
(a) WRITING 0 IN ALL MEMORY LOCATIONS PICTURE SHOWS CURRENTS THROUGH A BUNDLE OF 16 OUT OF 64 X–ACCESS LEADS. SEE FIG. 19 FOR LOCATION OF THESE LEAD.

(b) WRITING 1 IN ALL MEMORY LOCATIONS. THIS PICTURE SHOWS THE CURRENTS THROUGH THE SAME 16 LEADS.

(c) WRITING 0 AND 1 IN A CHECKERBOARD PATTERN. THIS PICTURE SHOWS THE CURRENTS THROUGH THE SAME 16 LEADS AND IS A SUPERPOSITION OF THE TWO PICTURES SHOWN ABOVE.

SCALES: HORIZONTAL: 0.5 USEC/DIV.
VERTICAL: 100 ma/DIV.

Fig. 24—Y Access Currents



CURRENTS THROUGH THE SAME 16 LEADS AS SHOWN IN FIG. 24a. ONE OF THE 8 PRECHARGE SWITCHES (CPS A94) IS NOT WORKING. RESULT: LEAKAGE THROUGH NON-SELECTED PATHS DURING THE WRITE INTERNAL ONLY AND DETERIORATION OF WRITE CURRENTS DUE TO CURRENT ROBBING.

CURRENT THROUGH A DIFFERENT SET OF 16 LEADS. NO LEAKAGE THROUGH UNSELECTED PATHS (CLEAN BASE LINE). WRITE CURRENT HAS ALMOST PERFECT WAVEFORM, HOWEVER, TOP IS SLIGHTY DETERIOR. COMPARE WITH FIG. 24a.

SCALES: HORIZONTAL: 0.5 USEC/DIV.
VERTICAL: 100 ma/DIV.

Fig. 25—Faulty Precharge Currents

Access Precharge Circuit Failures

8.19 The purpose of the precharge circuit is to prevent leakage through unselected paths of the coincident current memory system. Failures in the precharge circuit can affect the X or Y currents considerably. However, the precharge circuits are not operated during the READ interval and failures can be detected only during the WRITE interval when the precharging is activated, as shown in Fig. 25a and 25b. Figure 25a shows leakage current through unselected paths. Leakage, however, causes current robbing from selected paths, as shown in Fig. 25a and 25b. Note that the waveform appears almost perfect. The trouble can be easily located by checking the operation of the precharge switches. These are the A94 circuit packs in locations 010-04, 012-04, 010-46, and 012-46. (See SD-1A12Y, FS 8 and FS 9, B-sheets.) Fourteen of the sixteen switches are simultaneously closed during any WRITE interval; the set of closed switches is a function of memory address location and operation of all switches can be observed by sequentially addressing all 4096 words of either memory half. The black wires between the access circuitry and the memory modules are return leads and carry capacitive discharge currents supplied by the precharge circuit. These currents do not give any direct indication of the CS performance.

Open Access Lead

8.20 This trouble is most likely to occur within a memory module or in a memory connector. If a particular address wire with an open is selected, both READ and WRITE currents split and are forced into unselected paths. There they show up as leakage as illustrated in Fig. 26.

8.21 This failure is unlike a precharge fault where leakage occurs during the WRITE cycle only (Fig. 25a). Leakage as a result of an open lead occurs during both READ and WRITE intervals.

Excessive Storage Access Diodes

8.22 Figure 27a illustrates the result of a bad diode in a WRITE current path. Its reverse storage current adds to the READ current of the subsequent cycle, provided that the store is running at high speed. At low repetition rates, the diode has enough time to recover and no trouble can be detected. Figure 27b shows the effect of a bad diode in the READ path, which deteriorates the subsequent WRITE current pulse. This condition, of course, is not repetition rate sensitive. The heavy trace in both figures indicates the undisturbed currents.

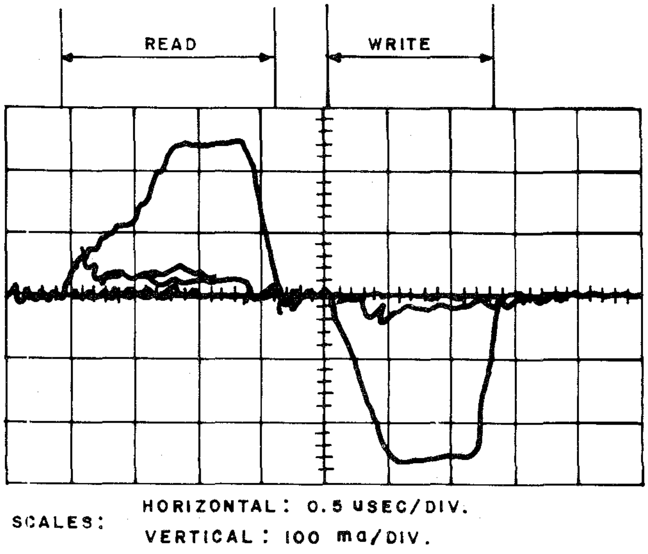
9. BLOWING FUSES

9.01 Replacing a blown fuse may not clear the trouble. If, upon replacing the fuse, it again blows, this condition is indicative of an existing fault in a circuit pack which causes the fuse to blow (Fig. 28).

9.02 To clear this type of trouble, locate the faulty pack causing the fuse to blow. The following steps should be considered and followed accordingly.

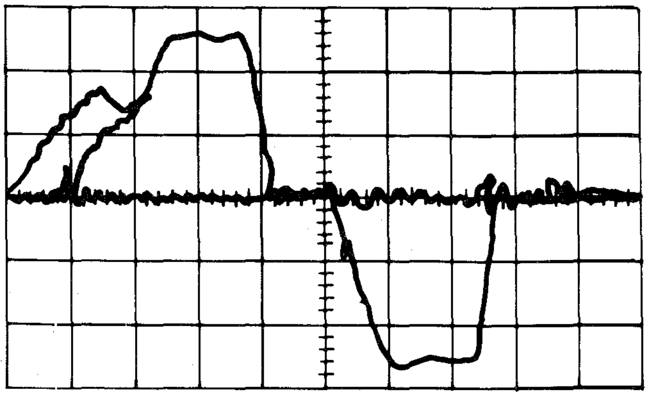
9.03 If any circuit packages are listed under the trouble number issued by the system for this blown fuse, replace each pack listed (one at a time) and the fuse simultaneously. If, upon replacing a pack, the fuse ceases to blow when power is returned to the store, this pack should be the faulty one and the trouble should be cleared.

9.04 If the above method failed to clear the trouble (fuse continues to blow) or if no circuit packages were listed under the trouble number issued by the system, remove all packs associated with this fuse. This information is supplied in SD-1A124, section D. Here are listed all circuit packs associated with each fuse. The



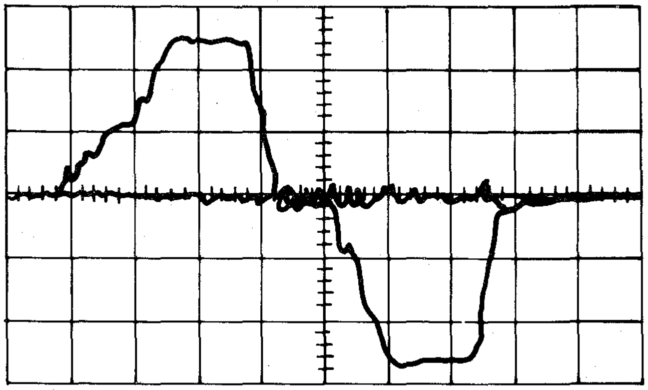
CURRENTS THROUGH THE SAME 16 LEADS AS SHOWN IN FIG. 24a. ONE LEAD IN A Y-CONNECTOR IS OPEN. NOTE "LEAKAGE" DURING BOTH READ AND WRITE INTERVALS DUE TO CURRENT SPLITTING.

Fig. 26—Faulty Module Connector



(a)

CURRENTS THROUGH 16 LEADS
AS SHOWN IN FIG. 242
BAD DIODE IN "WRITE"
CURRENT PATH OF Y ACCESS
CIRCUIT. RESULT: DEFORMED
READ CURRENT WAVEFORM
OF SUBSEQUENT CYCLE
AT HIGH REPETITION RATE
(LIGHT TRACE).



(b)

CURRENTS THROUGH 16
LEADS AS SHOWN IN FIG.
24a BAD DIODE IN
"READ" CURRENT PATH
OF Y ACCESS CIRCUIT.
RESULT: DEFORMED WRITE
CURRENT WAVEFORM
(LIGHT TRACE)

Fig. 27—Effects of Access Diodes with Large Reverse Storage Conduction

maintenance procedure for this type of trouble is as follows.

(a) Note the fuse that continues to blow and locate it in SD-1A124, section D.

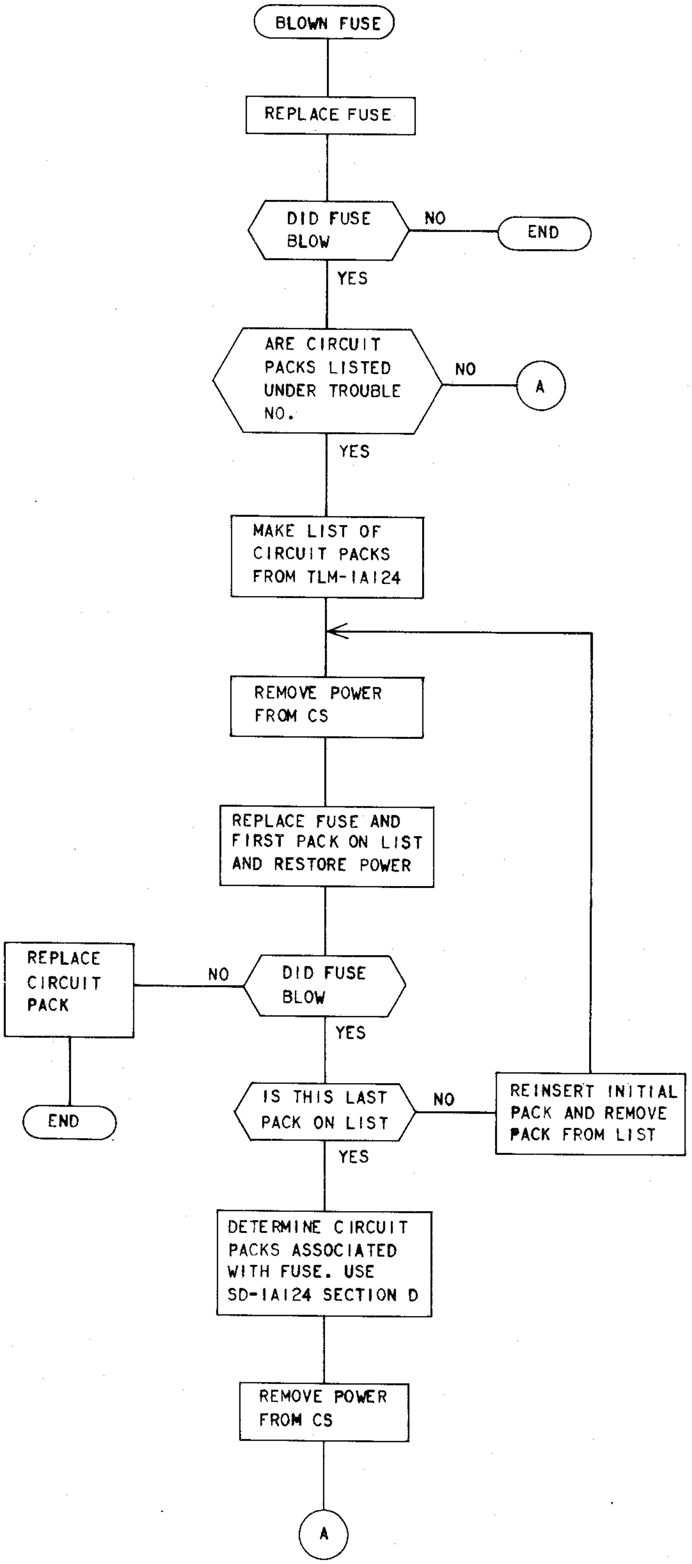
(b) Remove all circuit packs associated with that fuse.

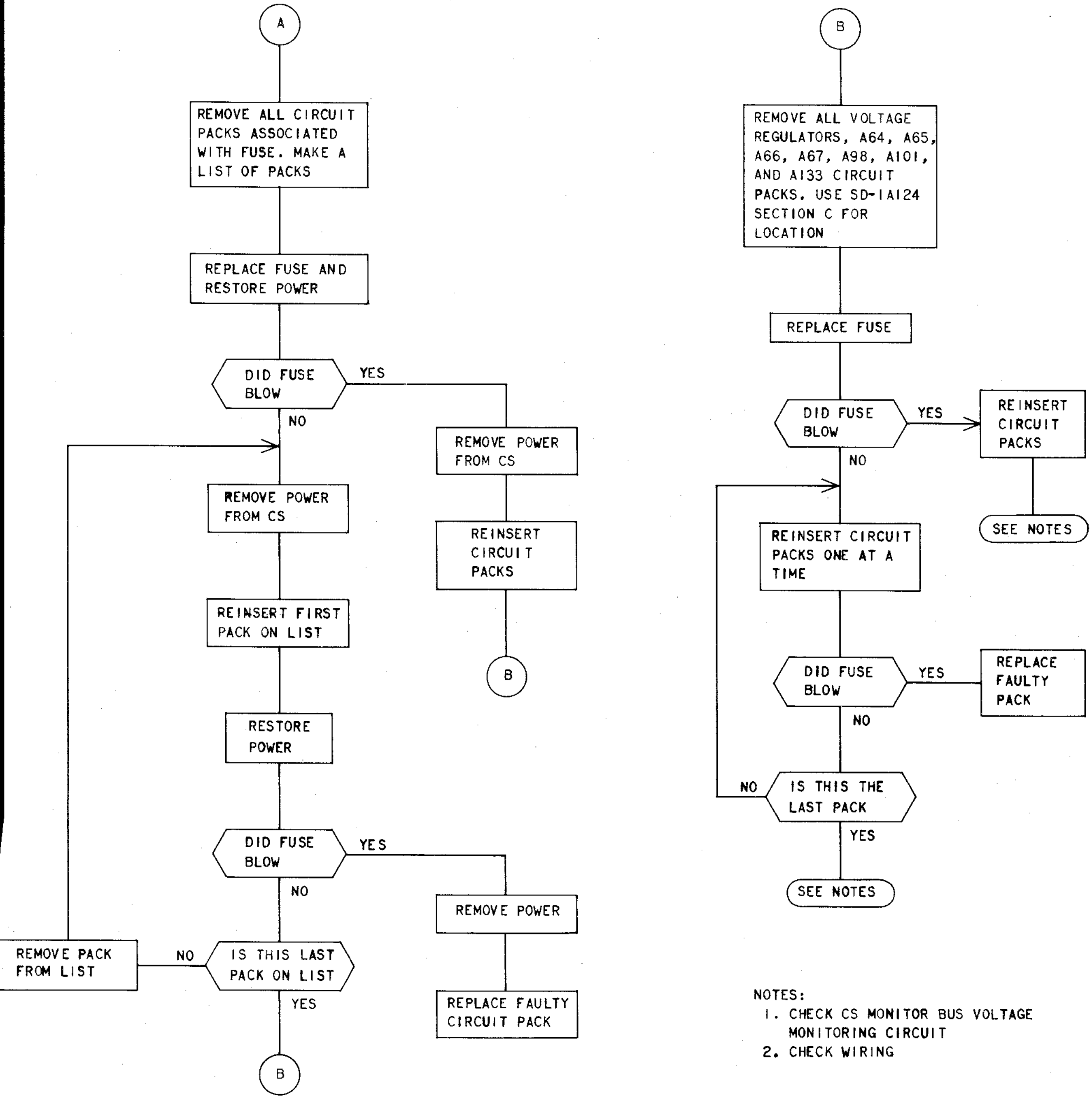
(c) Replace the fuse and return power to the CS. If the fuse again blows, go to 9.05. If the fuse does not blow, turn off power, return one pack to the store, and turn on power. Repeat until fuse blows again. The pack just replaced and caused the fuse to blow should be the faulty circuit pack.

Caution: Replacing circuit packs with power on can damage the circuit packs.

9.05 If the above method failed to clear the trouble and the fuse continues to blow, remove all voltage regulators (all A64, A65, A66, A67, A98, A101 and A133 packs), replace the fuse, and return power to the CS. If the fuse blows again, go to 9.06. If the fuse does not blow, turn off power, return one regulator pack, and turn on power. Repeat this step until fuse blows again. The pack just replaced and caused the fuse to blow should be the faulty circuit pack.

9.06 If the above method failed to clear the trouble and the fuse continues to blow, check the CS MONITOR BUS voltage monitoring circuitry in the CS. Check the monitoring circuitry relays for shorted contacts; also check behind the CS for shorted relay contact leads. If a shorted contact is found and repaired, replace all voltage regulators checked via this contact and all voltage regulators that are checked using the monitor bus lead


BLOWN FUSE
REPLACE FUSE
DID FUSE BLOW
NO
END
YES
ARE CIRCUIT PACKS LISTED UNDER TROUBLE NO.
NO
A
YES
MAKE LIST OF CIRCUIT PACKS FROM TLM-1A124
REMOVE POWER FROM CS
REPLACE FUSE AND FIRST PACK ON LIST AND RESTORE POWER
REPLACE CIRCUIT PACK
NO
DID FUSE BLOW
YES
END
IS THIS LAST PACK ON LIST
NO
REINSERT INITIAL PACK AND REMOVE PACK FROM LIST
YES
DETERMINE CIRCUIT PACKS ASSOCIATED WITH FUSE. USE SD-1A124 SECTION D
REMOVE POWER FROM CS
A



NOTES:
1. CHECK CS MONITOR BUS VOLTAGE MONITORING CIRCUIT
2. CHECK WIRING

Fig. 28—Flowchart for Locating Faults of Blown Fuses

associated with this shorted contact. This information is located in SD-1A124 on B105. If no trouble can be located in the voltage monitoring circuit, go to 9.07.

9.07 If procedures in 9.03 through 9.06 failed to clear the trouble, check behind the CS for wire strappings and other shorts in the vicinity of the packages as determined by procedures in 9.04 through 9.06.