DUPLICATION AND BUS SYSTEM DESCRIPTION NO. 1 ELECTRONIC SWITCHING SYSTEM

CONTENTS PAGE

1. GENERAL

1.01 This section describes the 2-wire No. 1 Electronic Switching System (ESS) and 4-wire No. 1 ESS bus systems and the extent of duplication of the equipment.

1.02 This section is reissued for the following reasons:

(a) To include information on peripheral units and peripheral unit parity.

(b) To make minor changes.

1.03 Abbreviations used in this section are listed in Part 5.

1.04 A group of leads providing interconnections between units is referred to as a bus. The No. 1 ESS has three major buses which connect the major units of the system. These are the call

store bus, the program store bus, and the peripheral unit bus systems. When the office is equipped with signal processors, there is also a signal processor bus system.

1.05 In addition to the buses, interconnecting leads exist over which information for individual units is relayed.

1.06 All common system units required to provide continuous service are duplicated. This duplication also extends to the bus systems.

2. DUPLICATION OF FACILITIES

2.01 Duplication of facilities is desirable primarily to establish the reliability required in a switching system to prevent an interruption of service. In addition, a check of outputs is done by comparing the output of one unit with the output of the other unit.

2.02 Both the interconnecting leads and the buses are duplicated to insure continuous service. The central control (CC) is able to communicate over either one of these buses or interconnections. Duplicated units in the No. 1 ESS may communicate with central control over either bus or interconnecting leads. Duplicated units are designated as standby and active. The active bus is defined as the bus the active CC is receiving information on. An active store block is one which is transmitting information on an active bus. Similar definitions apply to other duplicated units. The redundancy of equipment provides a way for the system to easily switch out a nonoperating unit and switch to a unit which will operate properly.

2.03 The following equipment is duplicated in the No. 1 ESS:

- Central Controls
- Signal Processors (used for 2 wire only)
- Program Stores
- Call Stores
- Central Pulse Distributors
- Switching Frame Controllers
- Signal Distributor Controllers
- Scanner Controllers
- Automatic Message Accounting Recorders
- Common Channel Interoffice Signaling (used for toll 2 wire and HILO 4 wire only)
- Ringing and Tone Plant
- Peripheral Unit Controller (used for 2 wire only)
- Peripheral Interface Units (used for 2 wire only)

CENTRAL CONTROLS

2.04 Duplicate CCs are always provided regardless of the office size. One unit is always activately exercising control of the No. 1 ESS. The other unit is usually in a standby status and ready to be switched into operation should the active unit fail. Even though one unit is in standby and not controlling peripheral units, it still processes the same information as the active unit. Certain selected internal points of the standby unit are compared with those of the active CC to insure that these points are in the same state. These comparisons provide a continuous check on the CC operations.

SIGNAL PROCESSORS

2.05 The signal processor (SP) is required only in the larger central offices. It performs those highly repetitive and time consuming input-output tasks for the CC which would severely limit the number of lines which CC could serve alone. The SP tasks include the supervisory scanning of lines and trunks for service requests, answers, disconnects, as well as the scanning of service circuits. The SP operates under the control of instructions stored in the signal processor call stores (SPCSs). The SP operates simultaneously with the CC; however, its operation is generally independent of the CC. A single pair of SPs is provided. The SPs function in a manner similar to the CCs in that one unit in each pair is active while the other unit is in a standby status. The standby checking function of the alternate SP is the same as for an alternate CC since it also does comparisons of internal points to check the SP operation.

PROGRAM STORES

2.06 Program stores (PSs) use a split type of duplication. No single store in this scheme completely duplicates the information contained in another store. The split scheme of duplication is shown in Fig. 1C. Note that the highest numbered information block is contained in PS 1 and the highest numbered PS rather than the two highest numbered stores (as with call stores).

2.07 The PSs involved in the split scheme of duplication can be compared to links of a closed chain. Each store contains two blocks of information labeled H and G that are duplicated in other stores. For example, under normal conditions while word $a_{(i}$ is read out of the G half of store 0, the duplicate word $a_{)1}$ is read out of the H half of store 2. By using the split scheme, the semipermenent memory in the PSs is allowed to grow by a single unit at a time. The number of PSs may vary from 3 to 12.

CALL STORES

2.08 The 32K or 8K call stores (CSs) use a split scheme of duplication like the PSs. The number of 32K CSs associated with the CCs may vary from 2 to 9 (2 to 10 for generic program 1E6 and later). If the office has a pair of SPs, there will be two 32K CSs associated with the SPs. The 32K CSs are divided into F (fixed) and V (variable) halves. The duplication scheme for 32K CSs is shown in Fig. 1A. There may be from 2 to 39 8K CSs associated with the CCs and up to eight 8K CSs associated with a pair of SPs. The duplication scheme for 8K CSs is shown in Fig. 1B. A single office cannot contain both 8K CSs and 32K CSs. However, an office with 8K call stores can be retrofitted to 32K call stores.

CENTRAL PULSE DISTRIBUTORS

2.09 Central pulse distributors (CPDs) are provided in pairs up to a maximum of eight pairs. The units in each pair operate independently of each other and can operate with either CC. Each CPD has a single controller.

SWITCHING FRAME CONTROLLERS

2.10 The network crosspoints in each switching frame are divided into two halves, each with its own controller. The controllers in these switching frames operate independently unless one of the halves fails. When one half fails, the controller in the other half can control the entire frame.

SIGNAL DISTRIBUTOR CONTROLLERS

2.11 Signal distributors (SDs) are divided into two halves, each with its own controller. Like the controllers for the switching frames, each half operates independently of the other half until a failure occurs. At this time one controller takes over control of all outputs.

SCANNER CONTROLLERS

2.12 Scanners contain two controllers and a number of unduplicated current-sensing devices called ferrods. Each controller has access to the ferrods. Under normal conditions one controller is active while the other controller is in standby. Unlike the standby condition for CC and SP, this standby controller is completely idle.

AUTOMATIC MESSAGE ACCOUNTING RECORDERS

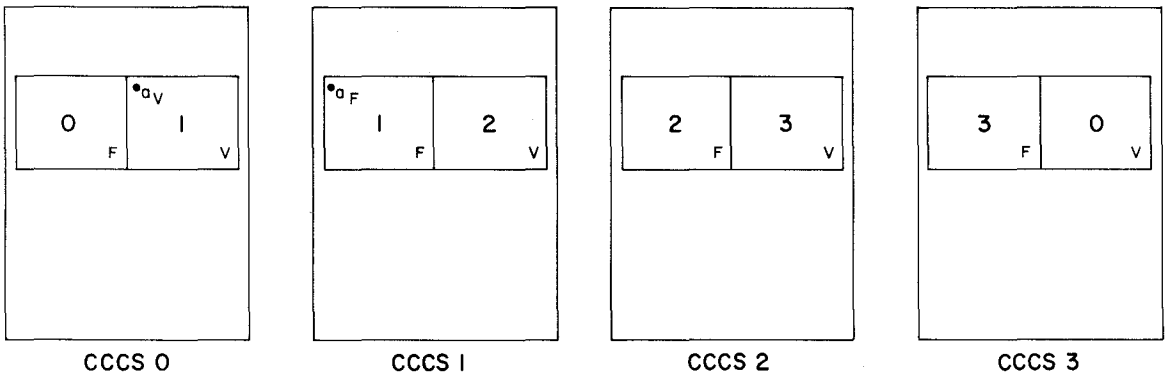
2.13 Automatic message accounting (AMA) recorders are provided in pairs at the master control center. Each AMA recorder has its own controller. During normal operation, one AMA recorder is operating while the other recorder is in a standby condition and idle.

▶TOLL COMMON CHANNEL INTEROFFICE SIGNALING

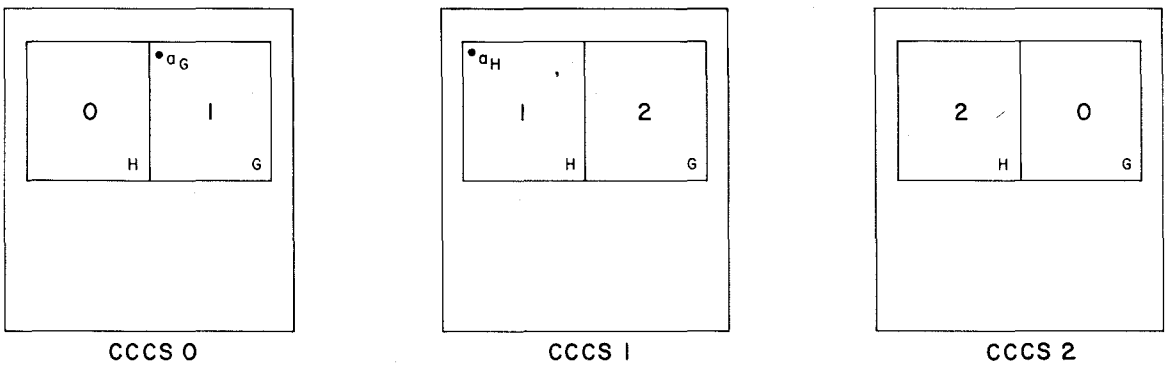
2.14 Toll common channel interoffice signaling (CCIS) is a duplicated system which routes data between CCs in different offices. The equipment required for CCIS consists of a duplicated terminal access controller, a signalling terminal, a modem, and a duplicated voice frequency link. The terminal access controller provides an interface between the processor and signalling terminal. CCIS is available with 1E5 and later generic programs. For information see Section 231-038-010.◀

▶PERIPHERAL UNIT CONTROLLER

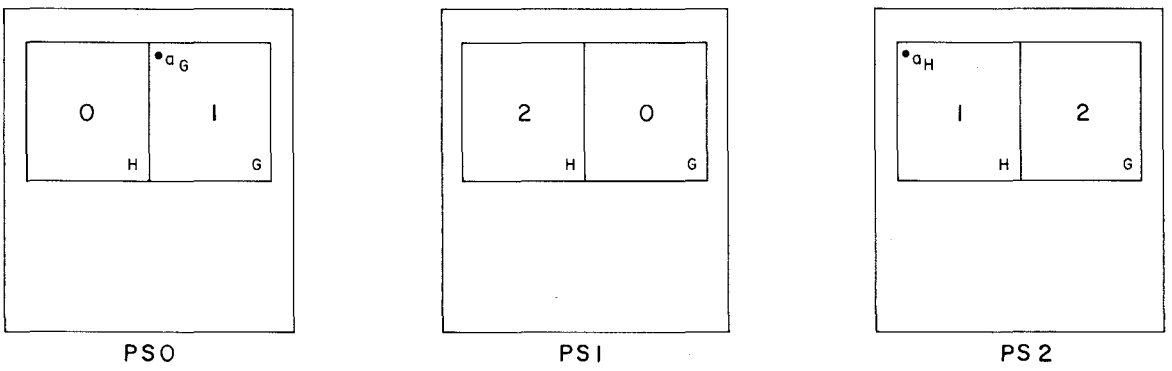
2.15 The peripheral unit controller (PUC) is a general purpose, microprocessor based controller. It is used to control peripherals such as the remote switching system (RSS) and the digital carrier trunk (DCT). The PUC is duplicated and is available with 1E6 and later generic programs. For more information see Section 231-037-020.◀



A. 32K CSs



B. 8K CSs



C. PSs

Fig. 1—Split Scheme of Duplication

▶PROCESSOR INTERFACE FRAME

2.16 There is one processor interface frame (PIF) which contains two processor interface units for duplication. The PIF provides an interface between the 3A processor and the CC. The PIF is used with 1E5 and later generic programs. ◀

RINGING AND TONE PLANTS

2.17 Ringing and tone plants are divided into two halves. During normal operation, both sets of ringing generators and tone generators are powered but only the interrupter which is active is powered. System control provides for automatic transfer in cases of failure of either group.

▶PERIPHERAL UNIT PARITY

2.18 The peripheral unit parity (PUP) feature provides parity checking on the peripheral unit (PU) reply bus (scanner answer bus) for new peripheral frames such as the peripheral unit controller (PUC). PUP is available with generic program 1E6 and later. The PUP feature requires two additional bits on the PU reply bus which is duplicated (Fig. 2). One bit is a parity bit which is pulsed whenever the parity over the 16 data bits is even. The other bit is a parity check request bit which is pulsed whenever the PU identifies itself as a circuit. Pulsing the parity check request bit causes the CCs and SPs to check the parity of the 16 data bits and the parity check bit. If the parity check indicates an error, a failure statement is printed on the TTY. This failure statement indicates which processor, peripheral units, and buses are involved and what the error is. The system will try to locate and correct the problem. A reaction statement is printed to explain what the system did to correct the problem. It will also indicate what parts of the system are faulty and if any part is out of service. Other related information may be printed depending on the problem. The CCs and SPs also compute the parity of the PU reply bus without the parity check bit and match the results. This parity match provides more immediate detection of certain classes of PU troubles before they result in C-level interrupts.◀

OPERATION WITH DUPLICATED EQUIPMENT

2.19 Operation with duplicated equipment makes it possible even with only two units to have four patterns for operation between two pairs of units communicating over a duplicated bus system. Duplication increases reliability because if one unit of a duplicated pair fails the No. 1 ESS will automatically be alerted of the failure and will automatically and quickly switch to the other unit. With this switching of units, the system also provides an alarm and a printout on the maintenance teletypewriter (TTY) so that operating personnel will be aware of the failure and take the necessary steps to repair the faulty unit. The probability of both units in a pair failing simultaneously is extremely low, and the possibility of the activated unit of a pair failing while a faulty unit is being repaired is remote.

3. ORGANIZATION OF BUS SYSTEM

3.01 The communication between system units is accomplished through groups of paired wires called buses. To keep pace with the high repetitive rate of the data processing circuitry, each pair of wires has been designed as a balanced transmission path for 0.5-microsecond signals.

3.02 A bus provides a common path for information exchange between the system units. A gating scheme allows the bus to be time shared by the different units it serves. This arrangement eliminates the need for many individual unit-to-unit interconnections. With very few exceptions, the flow of information on any particular bus lead is always in the same direction.

3.03 The bulk of information transferred between the major functional units is done by means of pulses transmitted over pairs of wires in the interconnecting buses. The following three major bus systems exist:

- Communication Bus Circuit for Peripheral Units (CC-PU)
- Call Store Interconnecting Bus Circuit (CC-CS)
- Program Store Interconnecting Bus Circut (CC-PS).

When the office is equipped with SPs, the signal processor call store interconnecting bus circuit

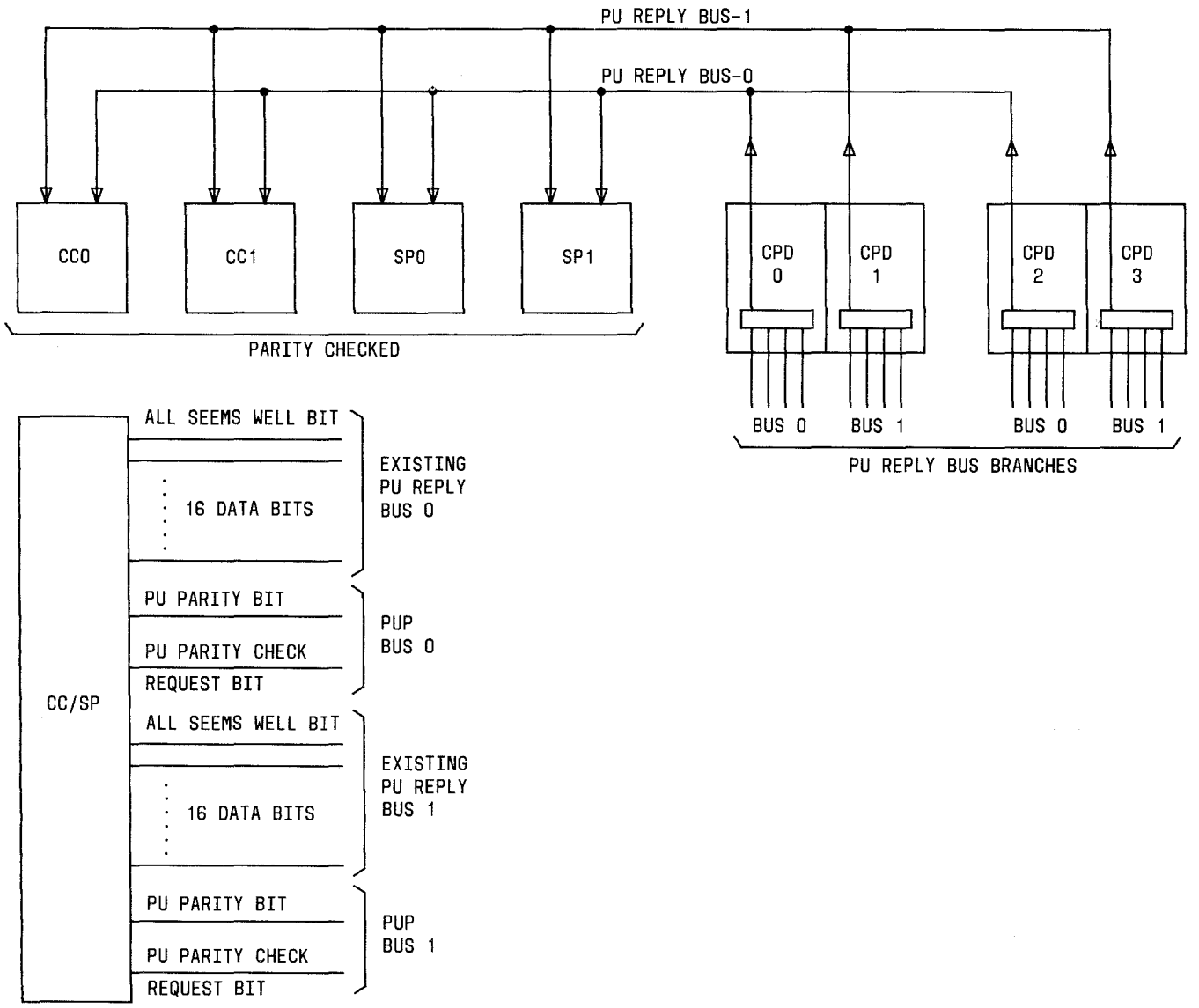
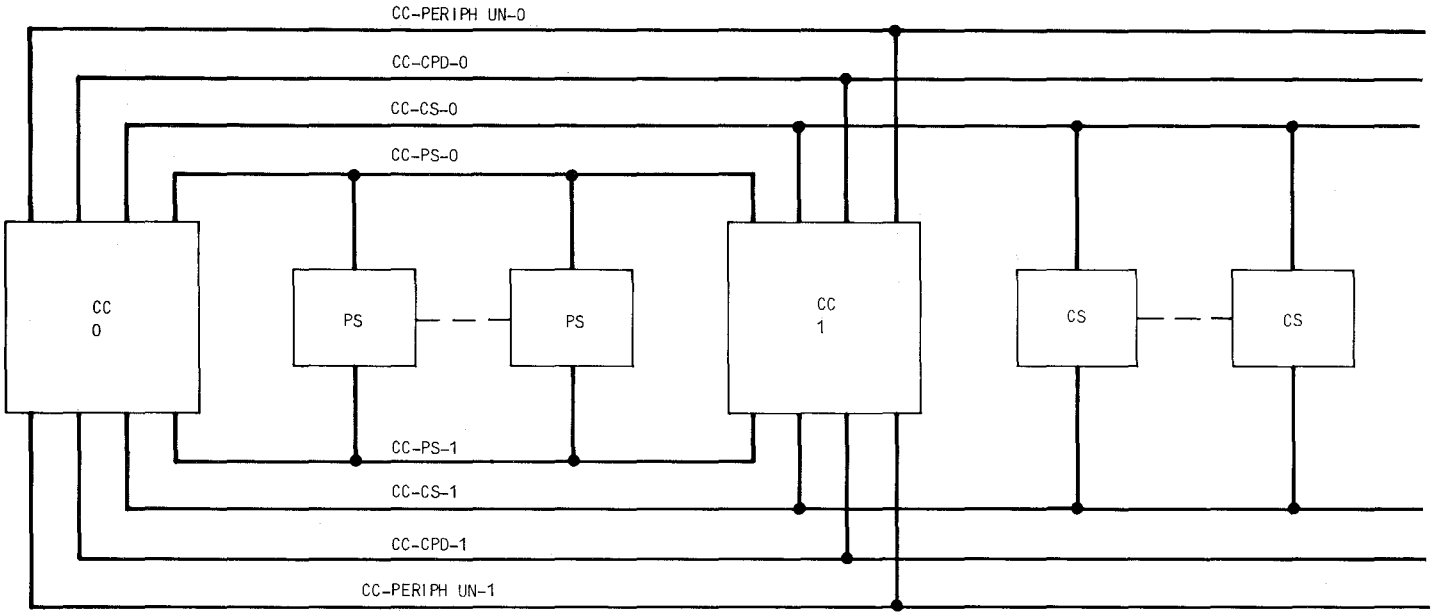


Fig. 2—Peripheral Unit Parity Feature—Simplified Diagram

(SP-SPCS) also exists. The SPs communicate with the CCs via the CC-CS bus system.

3.04 A simplified diagram of the system illustrating the interconnection of the buses covered in 3.03 is shown in Fig. 3. Also shown are duplicated units (CS and PS) which may communicate with either CC over either one of the two buses provided for this communication. The SPCSs may communicate with either SP over either of the two provided buses.

3.05 In Fig. 3 the two outputs from the CPD represent bus and interconnecting leads communication with peripheral units. All peripheral units are designed to work from the communication bus system for peripheral units. This peripheral unit bus system is expandable to a very large number of input-output units. The central processor


CC-PERIPH UN-0
CC-CPD-0
CC-CS-0
CC-PS-0
CC
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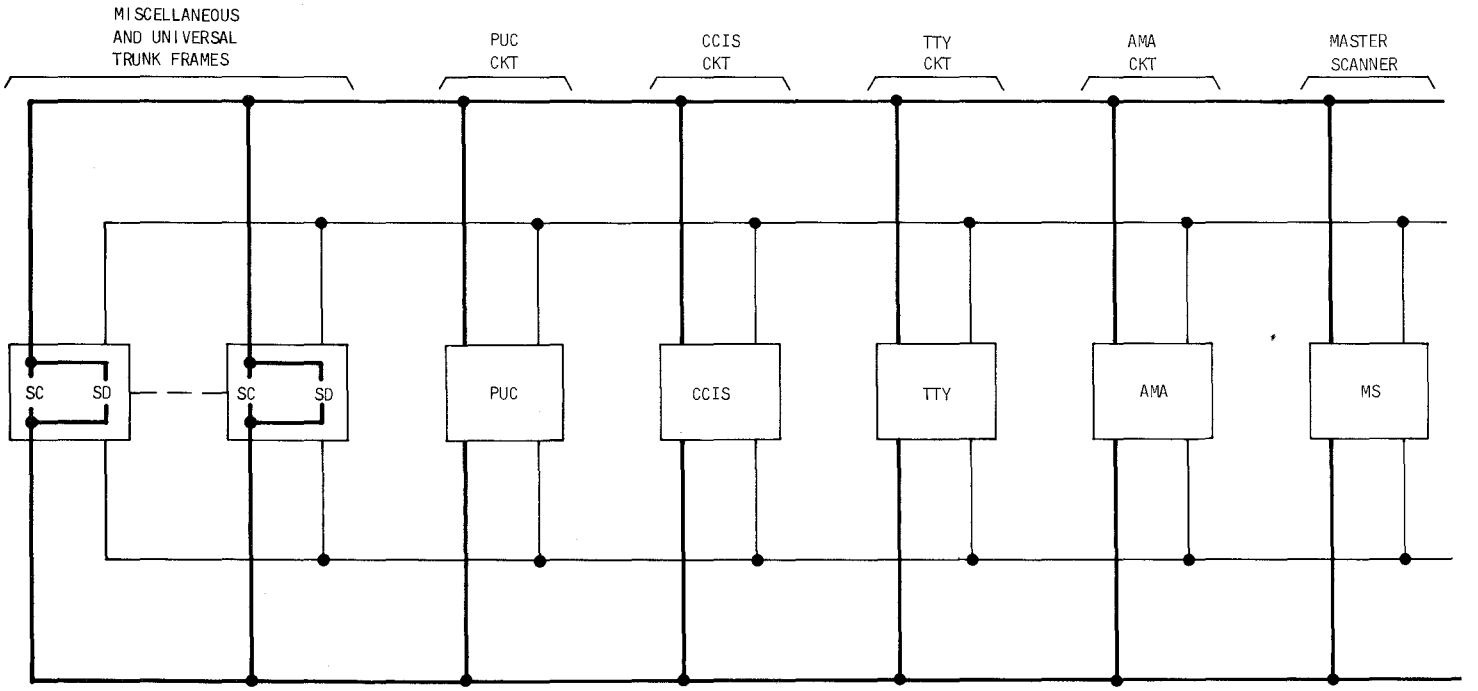
CC-CS-1
CC-CPD-1
CC-PERIPH UN-1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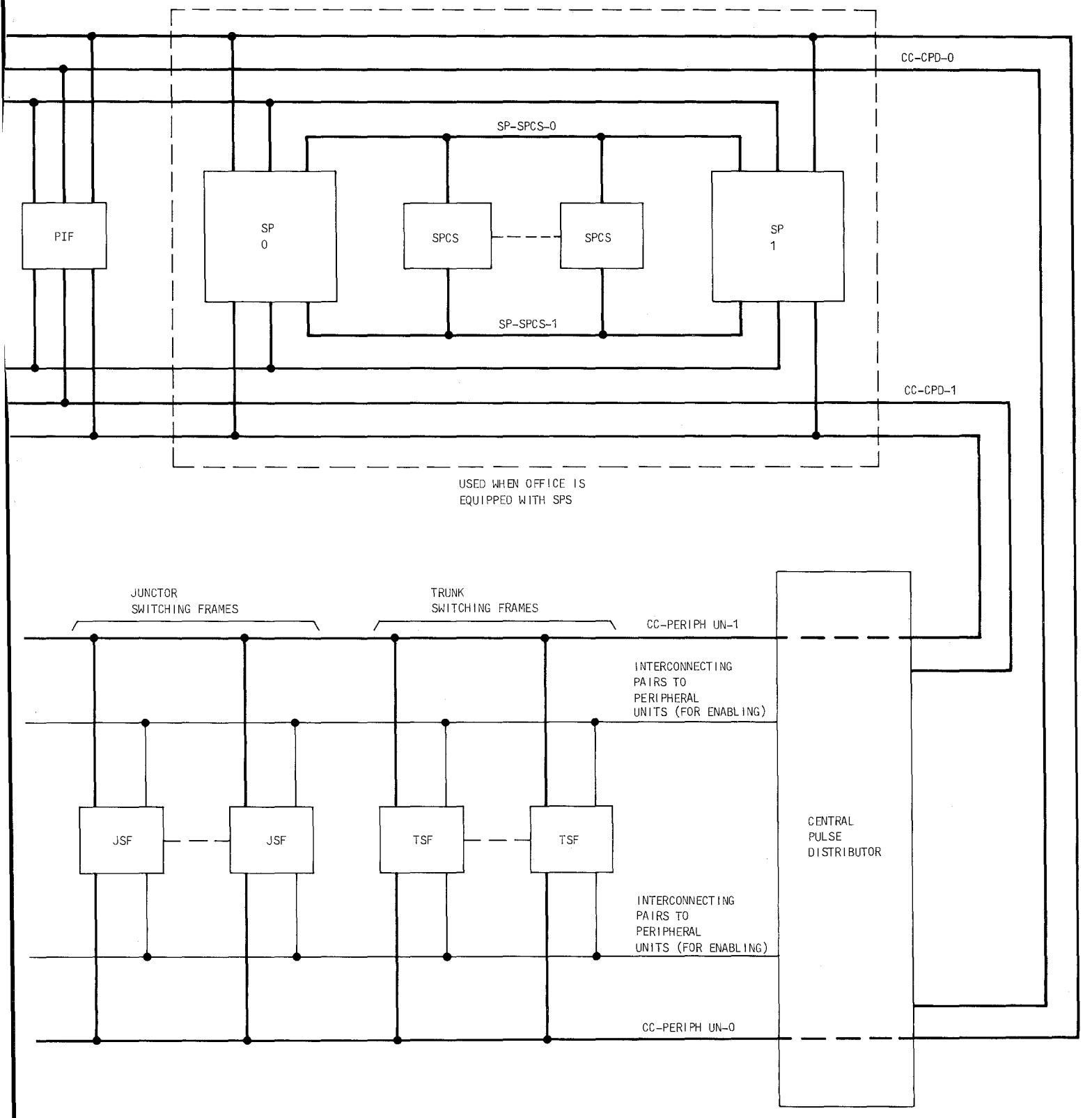


Fig. 3—Bus System and Interconnection—Simplified Diagram

is capable of only one operation over the peripheral unit bus every 11 microseconds since a peripheral unit order takes 2 machine cycles.

4. DESCRIPTION OF BUS SYSTEM

MECHANICAL FEATURES

4.01 The cable rack (Fig. 4) and cables constitute the physical make-up of the bus. Lines for the bus system utilize standard switchboard cable. This cable uses 26-gauge twisted pairs with a twist approximately every 2-1/2 inches.

4.02 In a central office, one end of the bus cable will go from the CC to the cable rack and then into a specially shielded compartment (Fig. 4). The bus cable then goes over the row of frames to an end guard at the end of the row of equipment where terminating resistors are connected to each pair. The other end of this cable goes to the other CC also via the cable rack. After going into the second CC and out again, the cable goes via the cable rack to a CPD. The cable then goes in and out of the CPDs for fan-in and fan-out purposes.

4.03 All the leads of a peripheral unit bus cable are brought to the terminal blocks located on all the peripheral unit frames. Bus transformers are incorporated into these terminal blocks (Fig. 5). The feed-through terminal assembly of the terminal block is built in a molded wire array. When an address twisted pair is used on a particular frame, the in lead goes to one end of a bus transformer

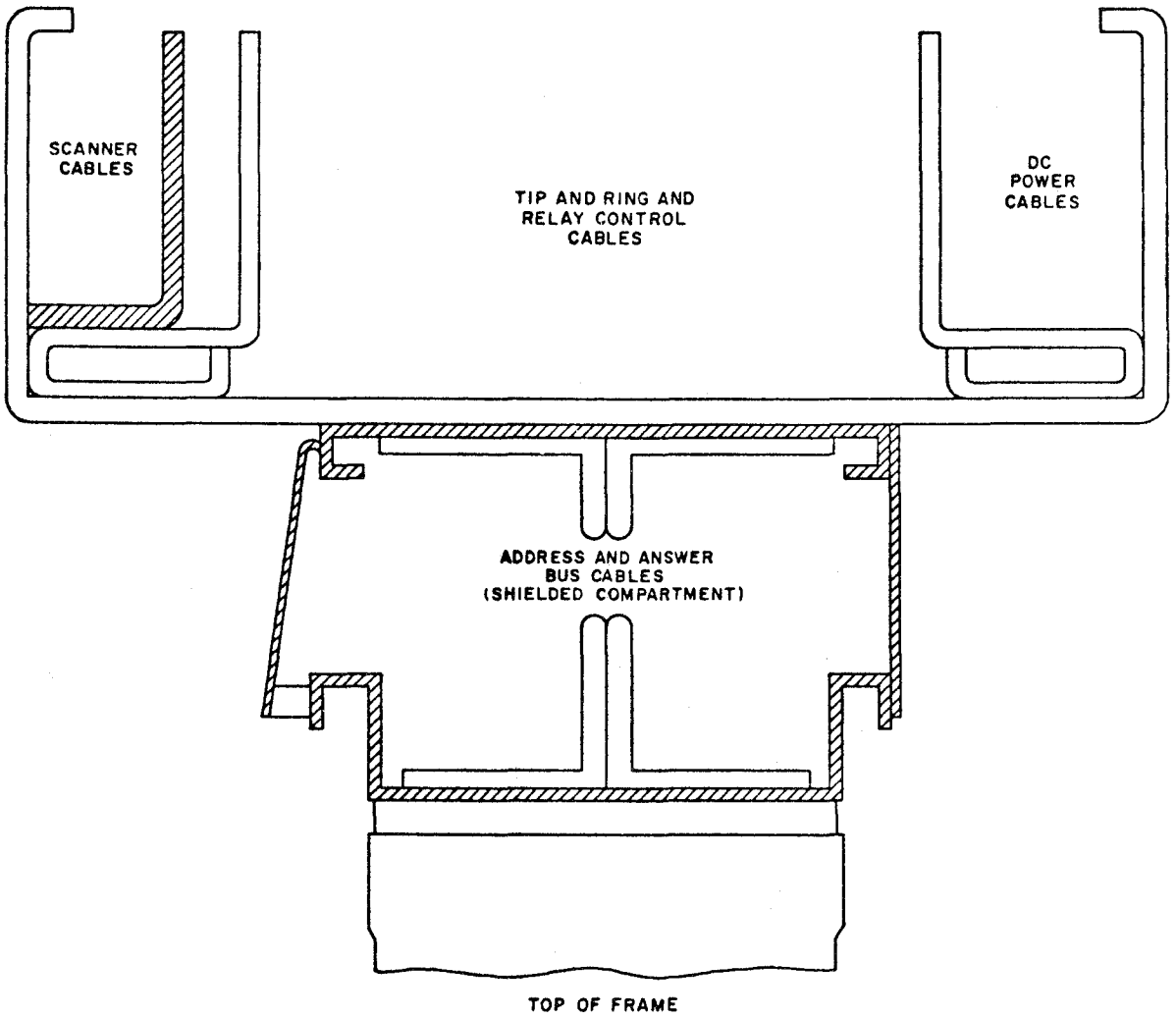


Fig. 4—Cable Rack, Sectional View Showing Four Components

winding and the out lead connects to the other end (Fig. 6). For leads that are not used, both the in and out leads are connected to the same terminal.

ELECTRICAL FEATURES

4.04 Buses for the No. 1 ESS may be compared to transmission lines requiring considerations of transmission loss and speed, immunity to noise and reflections, and crosstalk. The twisted pair of 26-gauge wires is used in the bus system because of the low cost when compared to the cost of coaxial cable. Also the twisted pair, carefully balanced and properly terminated in 100 ohms, has characteristics which are satisfactory for information interchange. The effective delay of the twisted pair is 2 microseconds per 1000 feet. The loss varies with frequency and length (6 db per 1000 feet at 1 megacycle). Tolerable delay limits the length of the twisted pair to less than 450 feet where the loss and distortion are relatively small. For example, the bus length between CC and the last PS is limited to 175 cable feet while CC or SP to peripheral units, via the CPD, have a maximum length of 450 cable feet. For other conductor limiting conditions reference should be made to Section 820-009-150.

OPERATION

4.05 Signals from the CC are transmitted over the buses by means of 12-volt pulses approximately 0.5-microsecond wide. These pulses may be applied as often as once every 5.5 microseconds; thus, the buses must be able to transmit high-frequency signals and be relatively insensitive to ambient electrical noise.

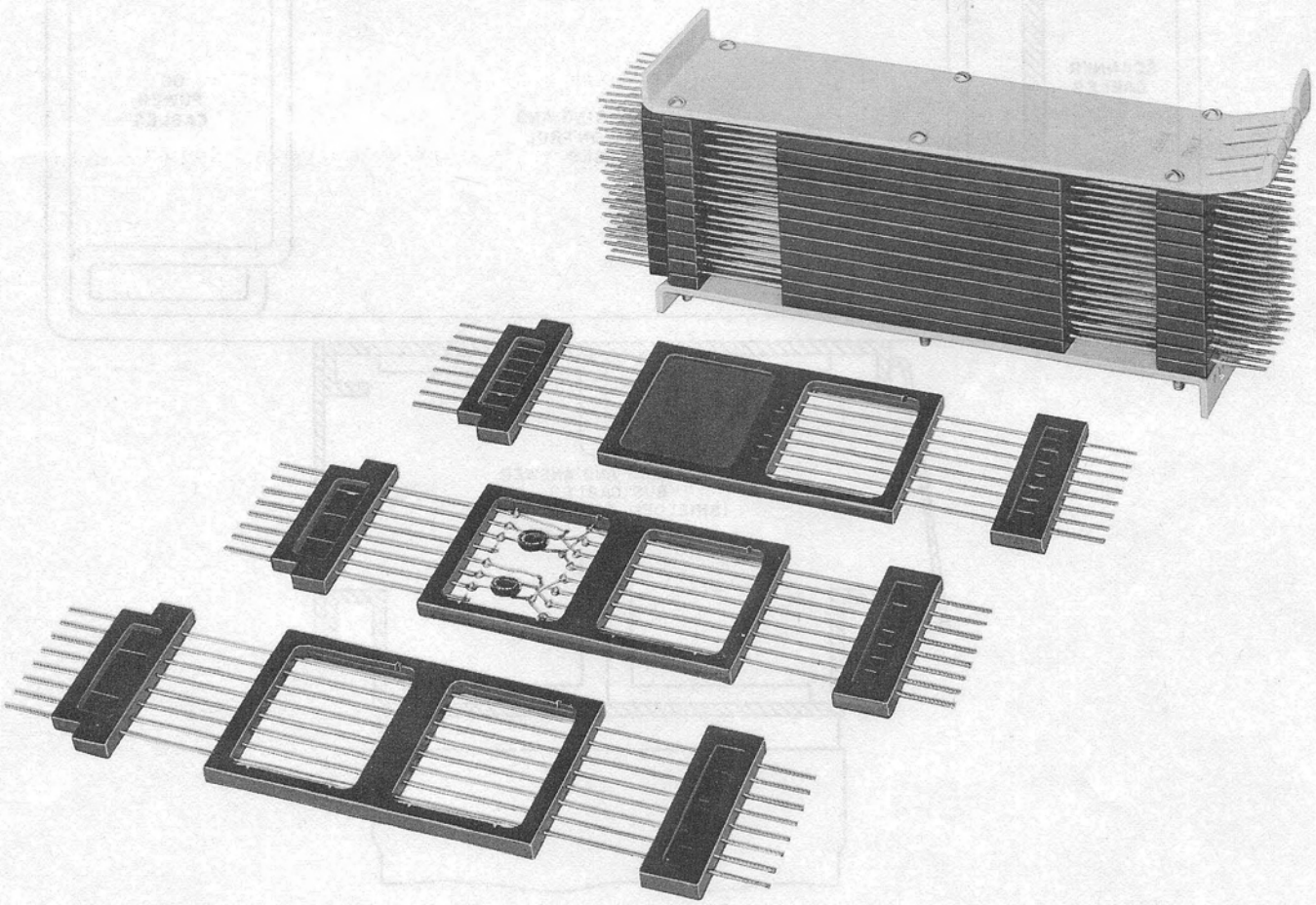


Fig. 5—Bus Transformer and Terminal Block Assembly

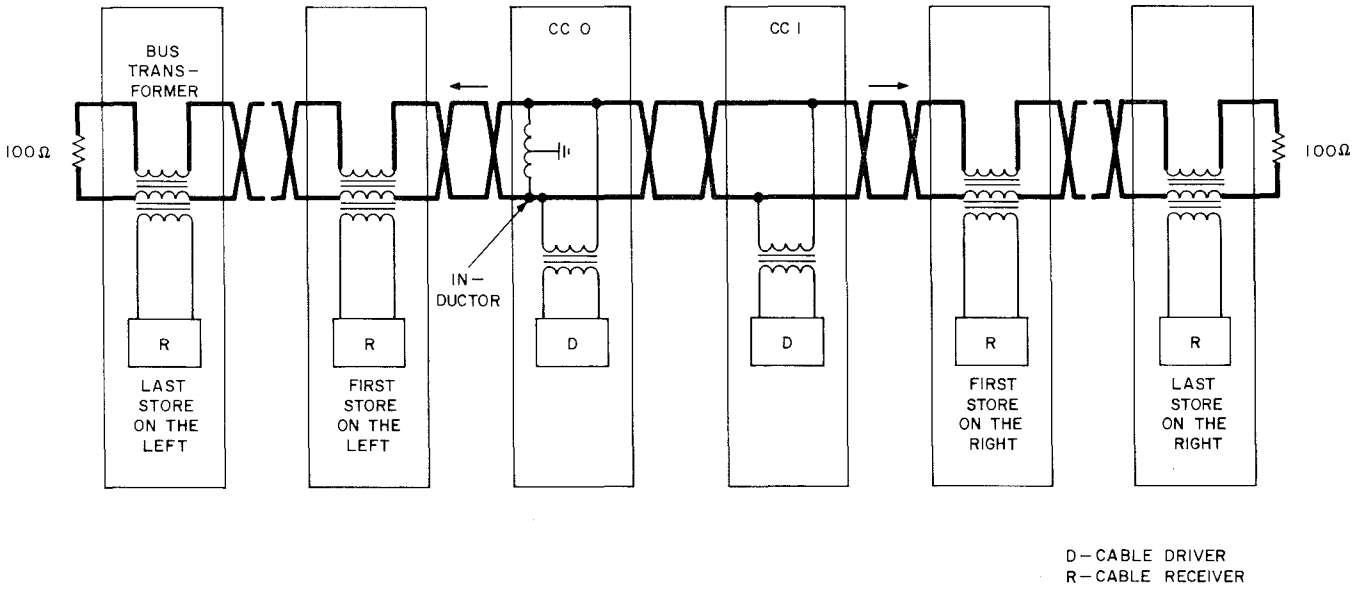


Fig. 6—Typical Bus Pair Showing Balance to Ground

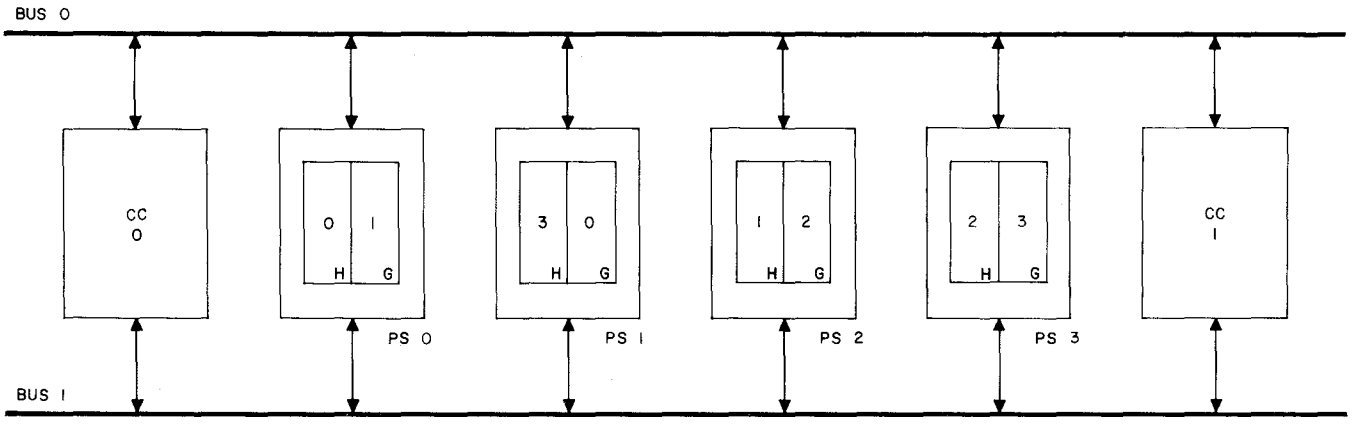
4.06 A bus pair for transmitting an address bit from the CC to the stores (program or call) is shown in Fig. 6. To minimize reflections that would cause undesired multiple operations, the bus pair is terminated at both ends with a 100-ohm noninductive resistor. A center-tapped inductor is bridged across the pair to provide a path to ground for unwanted longitudinal signals. Each pair is transformer coupled to a number of cable drivers and cable receivers. The driving transformers are bridged across the bus pair, whereas the receiving transformers are connected in series.

4.07 Two methods are used to select or enable the unit that must respond to information transmitted over a bus having access to several other units. The first method is used to enable CSs, PSs, and SPs. These units are assigned names in the form of unique binary combinations. For example, the CS is enabled by six binary coded digits. A code is transmitted over a number of bus leads to all the units on the bus shortly before the information to be acted upon. A unit can receive the rest of the information only if it has a name that matches the enabling code. The second method of enabling used for CPDs and peripheral units is covered in paragraph 4.14.

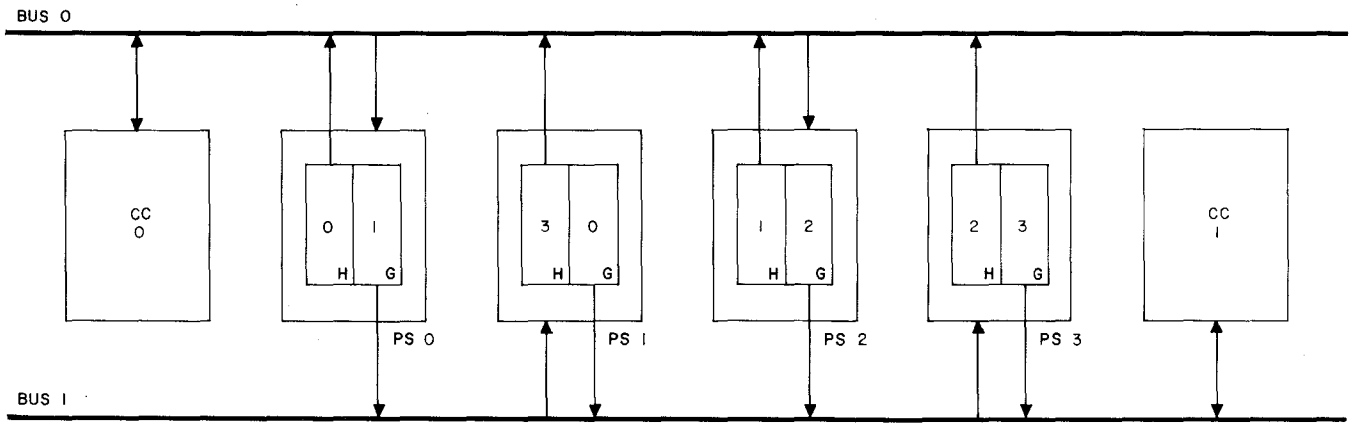
BUSES FOR PROGRAM OR CALL STORES

4.08 The duplicate buses linking CCs and PSs are shown in Fig. 7A. The various units have switching facilities that can associate CCs and PSs with the buses in different ways. For example, PS 1 can be addressed by and can send readout to either CC 0 or CC 1 over bus 0 or bus 1. In the configuration shown in Fig. 7B, CC 0 receives from and transmits to bus 0. The PS 0 receives the address from bus 0. The readout is transmitted from the H half on bus 0 and from the G half on bus 1.

4.09 The PSs are enabled by a code transmitted over the buses. Both the G half of PS 0 and the H half of PS 2 have 1 as a name, and both halves are enabled when a code equal to 1 is put on the buses. The G half of PS 0 transmits its readout to CC 1 over bus 1, and the H half of PS 2 transmits its readout to CC 0 over bus 0. The H half of PS 0 and the G half of PS 1 work in a similar manner. Thus each CC has access to a complete set of stored information. In Fig. 7C, it is assumed that PS 1 is out of service. The PS 0 still transmits the readout from the G half on bus 1; however, the readout from the H half is transmitted on both buses to compensate



(A)



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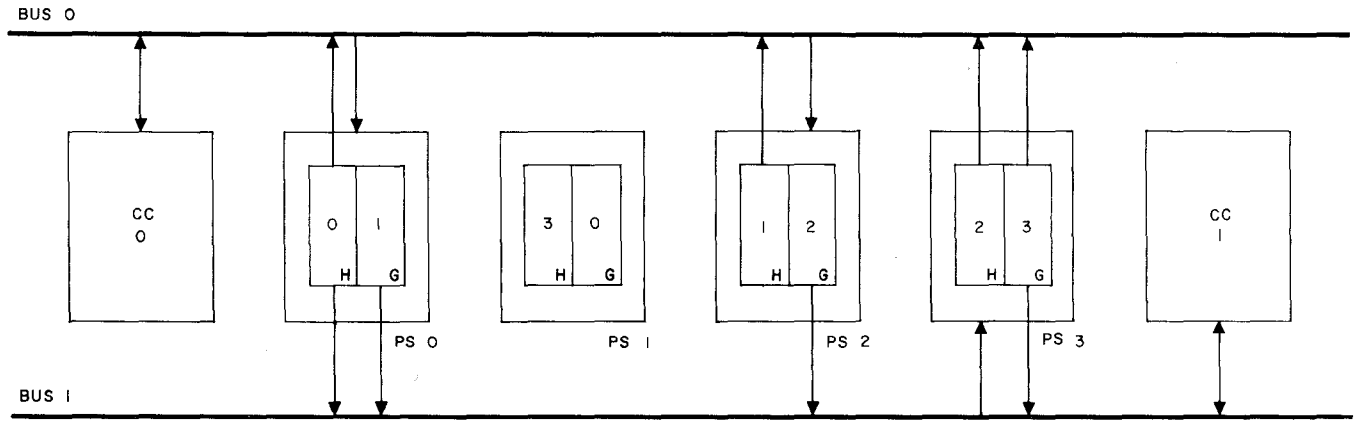

(C)

Fig. 7—Typical Bus Configurations

for the loss of the duplicate information block in PS 1. Similar considerations apply to PS 3. Either CC still has access to a complete set of stored information. Table A lists the pairs that make up each bus.

4.10 The PS is a read-only type of memory unit. As a result, there is no data bus for writing into the PS; however, there are other bits of information sent to the PSs.

4.11 The buses between CSs and CCs or SPs are basically similar to those described for the PSs. Table B lists the bus pairs between CC and 8K CSs. Table C lists the bus pairs between CC and 32K CSs.

BUSES FOR CENTRAL PULSE DISTRIBUTORS AND PERIPHERAL UNITS

4.12 All bus operations are initiated by the CC or SP. The CC requests input information or transmits instructions to units on the peripheral unit bus or the interconnecting leads. The typical bus system used in No. 1 ESS is shown in Fig. 3, and the buses (0 and 1) are shown duplicated. Each bus consists of two one-way groups of twisted wire pairs which are called address and answer. The actual operation allows only one unit to transmit at a time on any one bus.

4.13 The first signal in the operation of buses for CPDs is an enable address. The enable address is sent to all CPDs via the CPD enable address leads (Fig. 8). Then, over a private pair of wires, an execute signal is sent to the particular CPD that must respond to the CPD enable address. This signal goes to the primary windings of a bus-takeoff transformer. The output of the transformer is returned over a private pair of wires to CC. The return signal on this pair of wires is called the execute echo signal and allows CC to verify that the desired CPD has been reached.

TABLE A

BUS PAIRS BETWEEN CENTRAL CONTROL AND PROGRAM STORES

NUMBER OF BUS PAIRS		FUNCTION
TO PS	FROM PS	
1	—	Synchronizing signal for coded enable and mode
6	—	Name code (for enabling)
3	—	Mode of operation
1	—	Control write command
16	—	Address
—	1	Synchronizing signal for readout word
—	44	Readout word
—	1	All-seems-well signal
27	46	TOTAL

TABLE B

BUS PAIRS BETWEEN CENTRAL CONTROL AND 8K CALL STORES

NUMBER OF BUS PAIRS		FUNCTION
TO CS	FROM CS	
1	—	Synchronizing signal for coded enable and mode
6	—	Name code (for enabling)
3	—	Mode of operation
1	—	Synchronizing signal for address
12	—	Address
1	—	Synchronizing signal for read, write, and parity
1	—	Read command
1	—	Write command
1	—	Parity check over code and address
—	1	Synchronizing signal for readout word
—	24	Readout word
—	1	All-seems-well signal
1	—	Synchronizing signal for first 12 bits of write-in word
1	—	Synchronizing signal for other bits
24	—	Word to be written
53	26	TOTAL

4.14 The operation of address buses for peripheral units and the enabling of the peripheral units are shown in Fig. 8. Because peripheral units use a common bus (CC-PU), the time during which any one peripheral unit can use the bus is critical. To prevent a unit from possibly receiving an address designated for another unit, it must first be enabled by a CPD. Unless a unit receives an enable pulse, it cannot accept an address from the CC.

4.15 When a peripheral unit is enabled by a CPD, recognition of the enable pulse generates a window pulse. This window pulse is approximately

TABLE C

BUS PAIRS BETWEEN CENTRAL CONTROL AND 32K CALL STORES

NUMBER OF BUS PAIRS		FUNCTION
TO CS	FROM CS	
1	—	Synchronizing signal for address, code, and mode enable (AS1A)
4	—	Name code for enabling (A17-A14)
3	—	Mode of operation (AHM, AGM, and ACM)
14	—	Address (13-A00)
1	—	Synchronizing signal for read, write, and parity (AS2)
1	—	Read command (AR)
1	—	Write command (AW)
1	—	Parity check over code and address (AP or PKA)
—	1	Synchronizing signal for readout word (CSSYM)
—	24	Readout word (CS23-CS00)
—	1	All-seems-well signal (CSASW or ASWC)
1	—	Synchronizing signal for all 24 data bits of write-in word (DSA)
24	—	Word to be written (D23-D00)
51	26	TOTAL

2.5 microseconds in time. The address from the CC must arrive on the peripheral unit address bus during the time that this window is open; thus, the time factor is critical.

4.16 The following factors control the coincidence of the enable pulse and the address:

(a) Time of transmission from the CC

(b) Cabling of the address bus and enable leads.

The time of the transmission from the CC is strictly controlled, but special arrangements using the CPD frame are made to control the delay due to the cable lengths. The CPD frame is used as a distribution center for the peripheral unit address bus. By routing the address and the enable pulses through the CPD, the physical distance and electrical delay in the wiring of the bus are the same for the address and the enable signals. The CPD frame is also a center through which the answer bus passes. The answers are fanned into the CPD and then made available to the CC.

4.17 The CPD applies a pulse to the particular output specified by the address received. In some instances, the selected output is used to control, over an interconnecting path, a particular relay, flip-flop, or other circuit located in some system unit. In other instances as shown in Fig. 8, the selected CPD output is connected over an interconnecting path to a particular peripheral unit. The pulse from the CPD enables this peripheral unit to respond to an address that is broadcast to all peripheral units within a short time after the enable pulse. An enable verify signal is sent back to the CPD at a later time over the same path

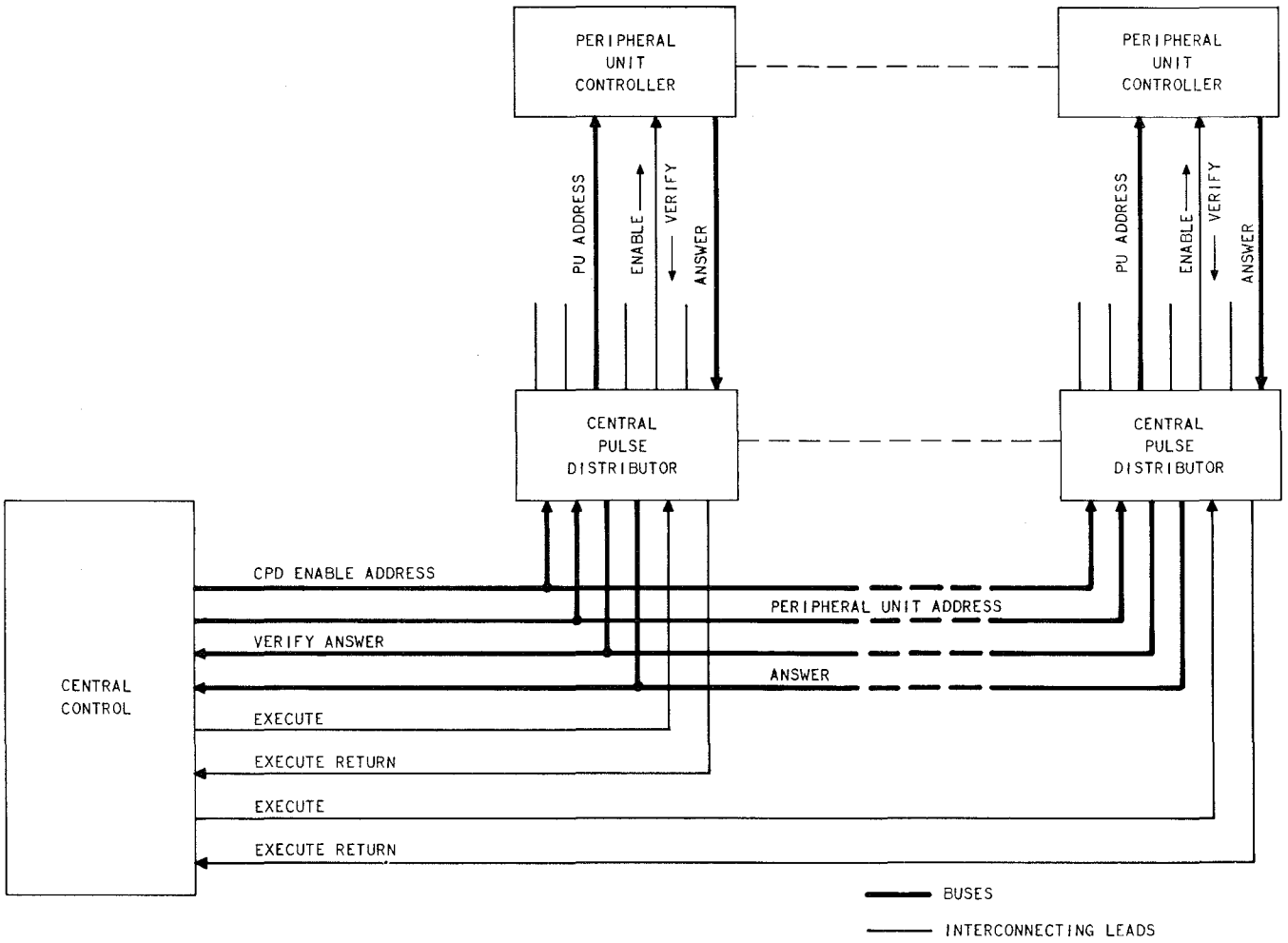

Fig. 8—Simplified Peripheral Unit Bus System

that has carried the enable pulse. The CPD translates the verify signal into three-coded 1 out of 8 combinations that are transmitted to CC over the verify answer leads (24 bits). The CC then matches this signal with the original enable address and decides whether the intended peripheral unit, and only that unit, has been enabled.

FAN-OUT AND FAN-IN

4.18 The method used to amplify and distribute the peripheral unit address pulses is shown in Fig. 9. This arrangement is called the address bus fan-out and is shown for one address bit only. The bus pair runs to all CPD frames and is coupled to the input of a bus fan-out amplifier at each CPD frame. The amplifier outputs branch out to four arms (north, east, south, and west), each of which feeds a group of peripheral units. This provides an adequate level so the pulses can drive all the cable receivers at a peripheral unit connected to a bus pair. It also allows the difference in length of enable leads and address leads to be held within a specified limit.

4.19 A similar scheme, but in reverse, is used for the scanner answer bus. At each CPD four branch buses are fanned-in to the main scanner answer bus going to the CC.

4.20 Table D lists all the bus pairs which provide communication between CC and CPD. Table E lists the bus pairs connecting CC and peripheral units. These leads are distributed by means of fan-out and fan-in circuits provided at the CPD frames. Table F lists the interconnections between

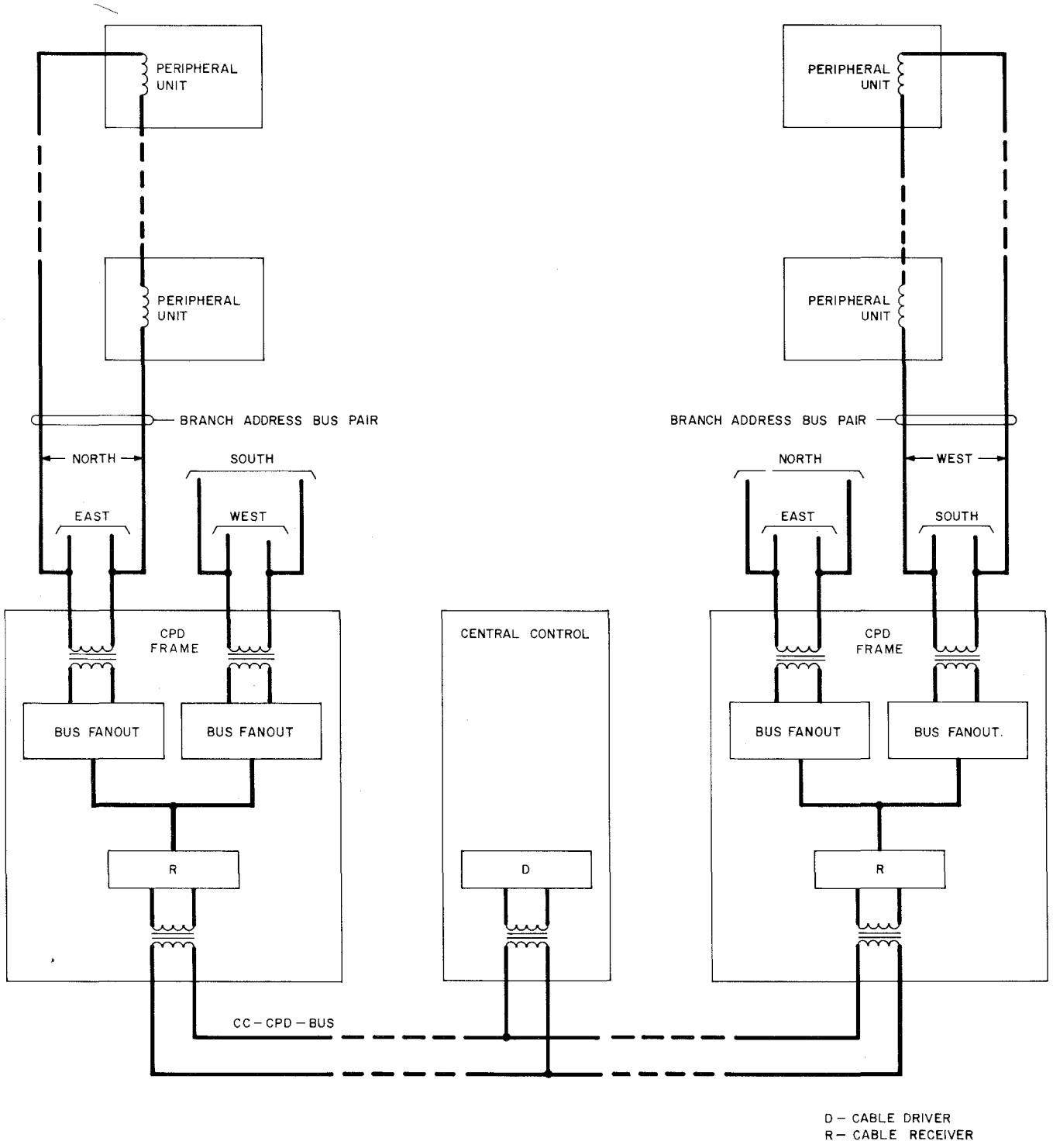

Fig. 9—Basic Fan-Out Scheme

units. All leads listed in Tables A through F are duplicated unless otherwise indicated.

BUS SYSTEM FLEXIBILITY

4.21 The No. 1 ESS bus system is sufficiently flexible to serve offices of various sizes and to permit office growth in an orderly fashion.

4.22 Greater call handling capability in a 2-wire No. 1 ESS office is accomplished by the addition of SPs which are needed to handle the additional switching demand by larger offices. The pair of SPs is connected by the CC-CS buses in parallel to the existing CSs. A separate additional bus (SP to SPCS) is added. The SPs are also connected to the CC-PU buses.

5. ABBREVIATIONS

AMA	Automatic Message Accounting
CC	Central Control
CCIS	Common Channel Interoffice Signalling
CPD	Central Pulse Distributor
CS	Call Store
DCT	Digital Carrier Trunk
ESS	Electronic Switching System
JSF	Junctor Switch Frame
MCC	Master Control Center
PIF	Processor Interface Frame
PS	Program Store
PU	Peripheral Unit
PUC	Peripheral Unit Controller
PUP	Peripheral Unit Parity
RSS	Remote Switching System
SC	Scanner
SD	Signal Distributor
SP	Signal Processor
SPCS	Signal Processor Call Store
TSF	Trunk Switch Frame
TTY	Teletypewriter

→ TABLE D ←

BUS PAIRS BETWEEN CENTRAL CONTROL AND CENTRAL PULSE DISTRIBUTOR

NUMBER OF BUS PAIRS		FUNCTION
TO CPD	FROM CPD	
32	—	CPD enable address
1	—	Bus choice
1	—	Reset lead
1	—	Test lead
1	—	We-really-mean-it enable signal
—	3	*Parity check
—	1	*Maintenance
—	24	Verify answer
—	1	All-seems-well signal
36	29	TOTAL

* Not duplicated

→ TABLE E ←

BUS PAIRS BETWEEN CENTRAL CONTROL AND PERIPHERAL UNITS VIA CENTRAL PULSE DISTRIBUTOR

NUMBER OF BUS PAIRS		FUNCTION
TO PERIPHERAL UNIT	FROM PERIPHERAL UNIT	
36	—	Peripheral unit address
2	—	Control leads
—	16	Scanner answer
—	2	Peripheral Unit Parity
—	1	All-seems-well signal
1	—	We-really-mean-it enable signal
39	19	TOTAL

TABLE F

INTERCONNECTIONS

FROM	TO	FUNCTION	QUANTITY
CC	CPD	Execute signal to controller	One per CPD
CPD	CC	Execute echo signal to CC	One per CPD
CPD	PERIPH UNIT	Enable signal to controller	Two per controller
	PS		
	CS, CC, SP, MCC		
CPD	MASTER SCANNER	We-really-mean-it signal	One per unit listed
	MCC		
	CC, CS, PS, SP		