32K CALL STORE
DESCRIPTION
NO. 1 ELECTRONIC SWITCHING SYSTEM

CONTENTS PAGE

CONTENTS PAGE

1. GENERAL

1.01 This section describes the 32K call stores (CSs) used in the No. 1 Electronic Switching System (ESS).

1.02 This section is reissued to include information on the tenth 32K call store.

1.03 The CSs are memory units that store information related mainly to the handling of calls as they are processed (Fig. 1). The CS is used for short-term scratch pad storage of events that occur in the No. 1 ESS. Certain long-term information is also stored temporarily in the CSs until enough of such information accumulates to make it worthwhile to write it into the program store memory cards.

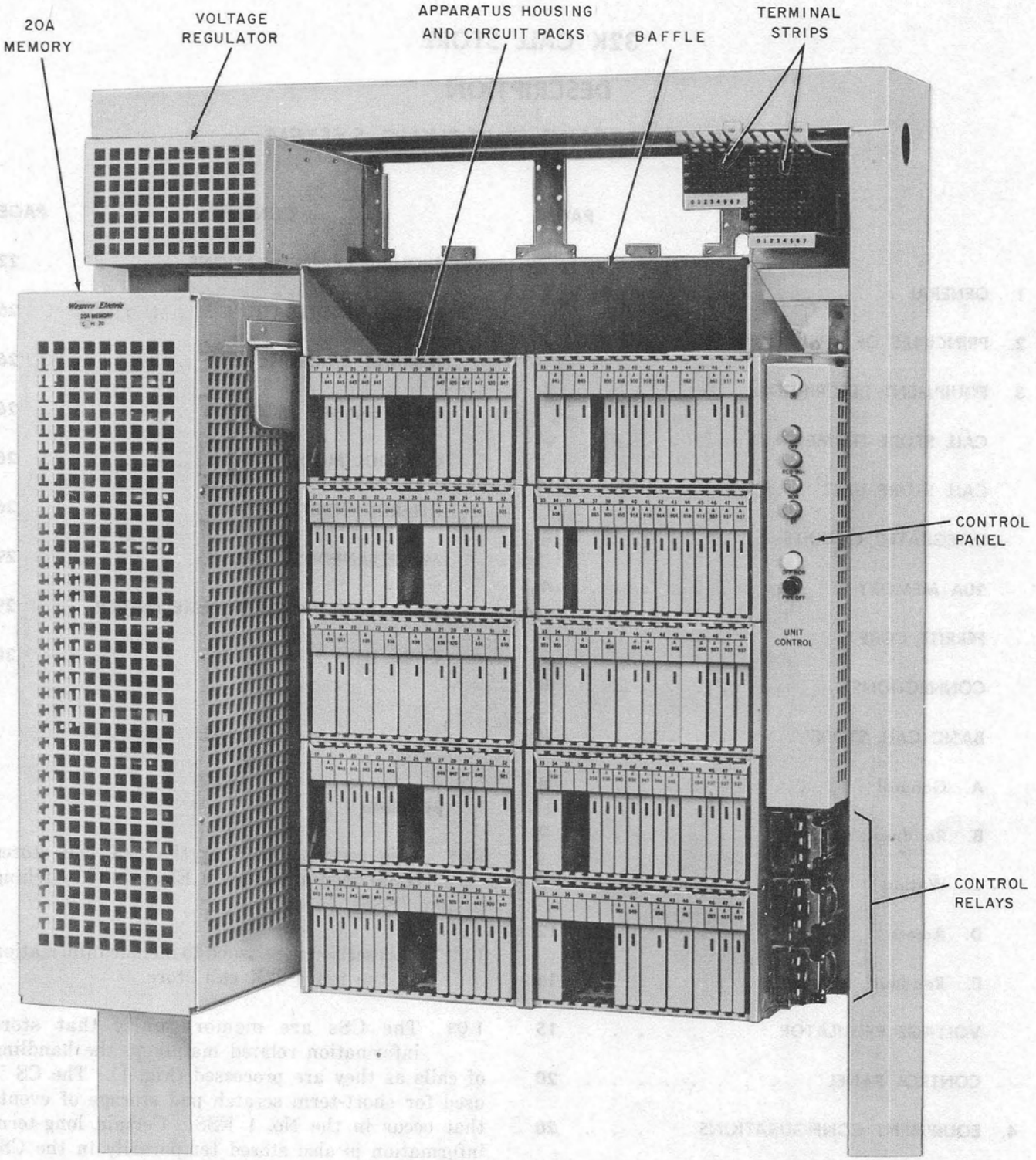


Fig. 1—32K Call Store Unit

2. PRINCIPLES OF OPERATION

2.01 The CSs are erasable read-write temporary memories used by the central control (CC) and signal processor (SP). The information stored in the CSs includes the following:

- Busy-idle status of customer lines, junctors, trunks, and network links
- Records of network terminations being used for each call in progress
- Digits received
- Digits to be outpulsed
- Data received
- Customer billing information prior to recording on the automatic message accounting (AMA) tape
- Recent change information related to customer lines and trunks prior to updating the translation information in the program store
- Administrative information
- Maintenance information related to program-controlled diagnostic tests.

2.02 The memory contained in each 32K CS is organized in words of 26 bits (24 bits for information and 2 spare bits that may be used as temporary patches for internal single bit failures). Each word occupies a location uniquely identified by an address. Inputs from a CC or an SP specify the operation (reading or writing), the CS address and, in the case of writing, the word to be written. The 32K CS carries out the order and, in the case of reading, sends the word read to the CC or SP.

2.03 The memory of each 32K CS unit consists of a ***fixed (F)*** half and a ***variable (V)*** half. Each half contains 16,384 words for a total of 32,768 words. In order to achieve maximum reliability, all information stored in the F half of one 32K CS is duplicated in the V half of another 32K CS.

2.04 The number of 32K CS units needed in each No. 1 ESS depends on the office size. In a 2-wire No. 1 ESS office, a minimum of two 32K CS units are required: central control call store (CCCS) 0 and CCCS1. ▶A maximum of ten [beginning with 1E(B5, B6)6] CCCSs and two signal processor call stores (SPCSs) can be used.◀

3. EQUIPMENT DESCRIPTION

CALL STORE FRAME

3.01 A 2-bay frame (bay 0 and bay 1), 4 feet 4 inches wide and 7 feet high, has been designed for the No. 1 ESS offices to accommodate the 32K CSs (Fig. 2). This 2-bay frame can be equipped with up to five 32K CS units associated with the CC and one 32K CS unit associated with the SP. ▶Two CS frames are required for each No. 1 ESS office: up to ten 32K CS units are associated with the CC and two 32K CS units are associated with the SP.◀ These two frames along with their 32K CS units meet the CS requirements for all No. 1 ESS offices.

3.02 The CS frame is prewired during initial installation. The bus cables (CC and SP address, answer, and data) enter the frame through connectors at the top rear of the frame and go into the cable ducts attached to the frame. The cable ducts are located on the rear side of the right upright of each bay (bays 0 and 1). The bus cables are multipled through all of the appropriate CS unit positions and go back to the top rear of the frame where the bus cables are terminated to other connectors. The bus cables are enclosed within a steel channel to shield the cable electrically and to protect the cables from accidental mechanical damage.

3.03 The control lead [central pulse distributor (CPD), scan point, we-really-mean it (WRMI), power alarm, and signal distributor applique] cables enter and leave the CS frame via terminal strips located at the top front of bays 0 and 1 of CS frame 0 and bays 0 and 1 of CS frame 1.

CALL STORE UNIT

3.04 Each 32K CS unit consists of one mounting plate which supports the apparatus housing, one voltage regulator, one control panel, and one 20A memory (Fig. 1). The mounting plate is supported by the frame upright on the left side and the frame cable duct assembly on the right side. The control panel and control relays are mounted between the apparatus housings and the

frame upright on the right side. The CS unit is completely connectorized to facilitate field installation.

3.05 The 32K CS uses for the most part standard No. 1 ESS hardware, such as 905 connectors and 36A apparatus mountings. Packaging of the supporting circuitry follows essentially the present No. 1 ESS A-type circuit pack requirements. A reasonably high degree of packaging density is achieved by use of beam leaded integrated circuits.

Circuit Packs

3.06 The circuit pack assemblies are contained in the apparatus housing of the 32K CS unit. These are a total of 113 A-coded circuit pack assemblies composed of 40 different A codes as shown in Fig. 1. The circuit packs consist of the double assemblies and single assemblies (Fig. 3 shows a double assembly). The double assemblies are composed of two boards which are mechanically and electrically connected so that they form a 56-pin circuit pack with high component capacity. All interconnections between the two boards are confined to one side of the double-board package so that it can be opened for maintenance and test purposes.

INTEGRATED CIRCUITS

3.07 There are two types of integrrated circuits (ICs) used in the 32K CS:

- HICS (hybrid integrated circuits) including thin film resistors and beam leaded multiple diode chips mounted on ceramic substrates. These are used extensively in the 20A memory access circuits of the CS unit.
- SICS (silicone integrated circuits) which are used extensively in the supporting circuitry (that is, circuit packs, etc), of the CS unit.

3.08 Table A and Table B contain information on the two types of integrated circuits. Substrate codes 26B and 48A (Fig. 4) are used in the memory access circuits. The substrate codes 10X and 11X (X being an alpha letter), used in the supporting circuitry of the CS, are shown in Fig. 5.

20A MEMORY

3.09 Each 32K CS unit contains a 20A memory 6 inches wide, 16 inches deep, and 21-3/4 inches high (Fig. 6). The 20A memory is located in the space provided in Fig. 1. Also, the 20A memory extends 4-1/2 inches into the equipment aisle.

3.10 The 20A memory (shown in Fig. 6) basically includes:

- Two identical core mat assemblies
- Bit and word diode transformer access circuitry
- Flexible tape wiring interconnections
- Temperature sense board.

3.11 The 20A memory includes two identical core assemblies (X and Y plane). Figure 7 shows one core mat assembly. Each core mat assembly contains 425,984 ferrite cores in a 512 by 832 matrix. The two assemblies are mounted back to back on a structual framework. The structural framework also supports 19 printed wiring boards (Table C) for the bit and word access circuits. Soldered flexible tape wiring (Fig. 6) interconnects the access circuit boards and the core mat terminal strips that the core wires are terminated on. All required external connections are routed through the 24 connectors located on the rear of the 20A memory. These 24 connectors provide access to the associated logic and driving circuits which are associated with the CS unit.

FERRITE CORE

3.12 Each core mat assembly is further separated into two symmetrical configurations containing four 208 by 256 core patches. Each patch contains an array of 53,248 miniature magnetic cores such as the core shown in Fig. 8. The A access (green color) and B access (red color) select wires are associated, via their intersections, with each memory core.

3.13 The ferrite cores used in the 20A memory have an outside diameter of 0.023 inches, an inside diameter of 0.014 inches, and a thickness of 0.006 inches (Table D). The cores are oriented at an angle of 45 degrees with respect to the horizontal and vertical axis of the core plane.

3.14 The ferrite core material has a square-loop magnetic characteristic (Fig. 9). The

TABLE A

32K CALL STORE SUBSTRATE CODE

SUBSTRATE CODE	CHIPS PER SUBSTRATE	INTEGRATED CIRCUIT CODE*
10A	1	17A
10B	1	15A
10F	2	15B
10G	1	15B
	1	73A
10H	4	73A
11A	2	17A
11B	2	15A
11C	3	15A
11E	2	17A
11G	2	15A
	1	17A
11K	2	17B
11L	2	15B
26B†	2	510A
	2	510B
48A†	2	510A
	2	510B

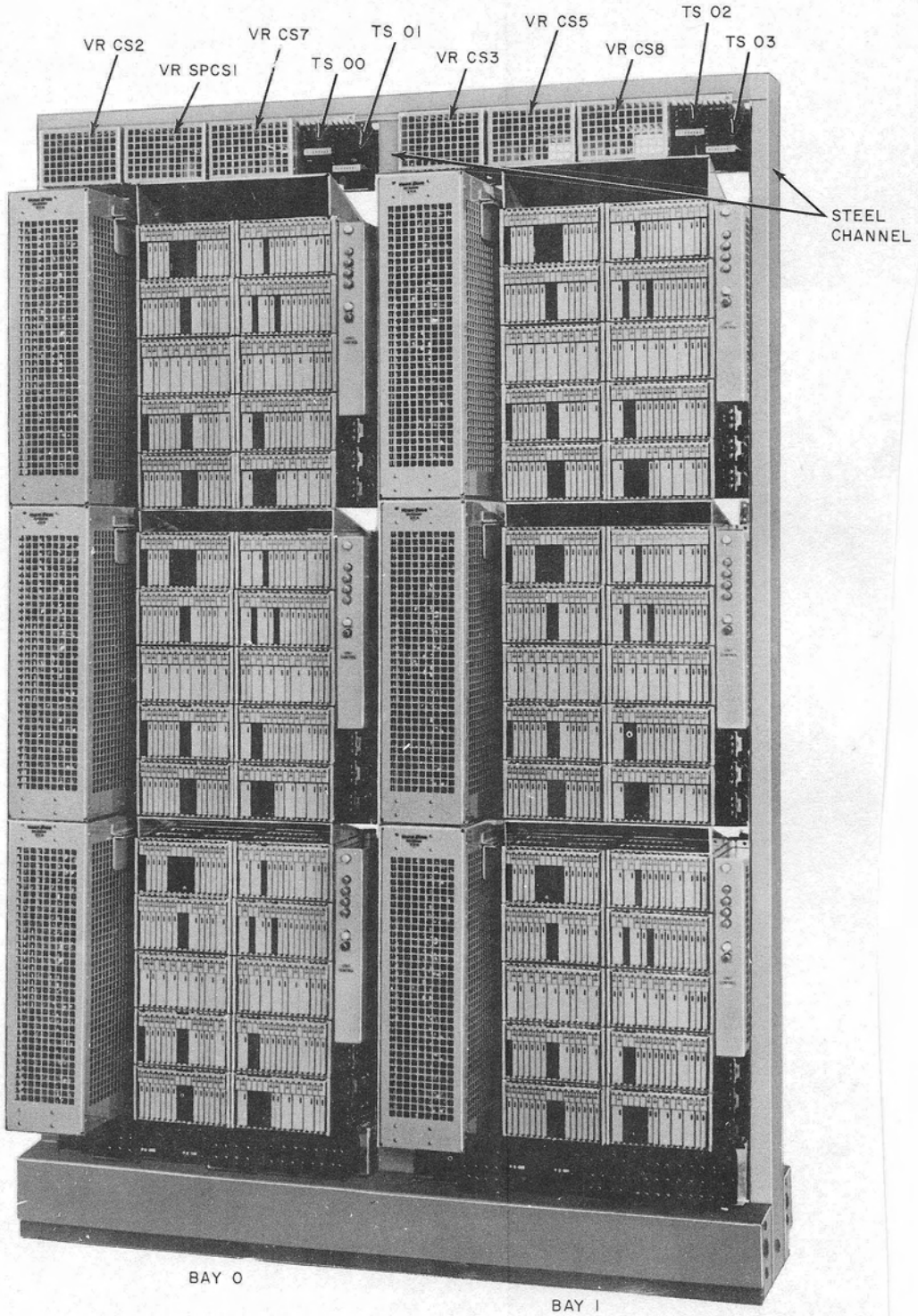
*See Table B.
†Used only on the 20A memory.

TABLE B

32K CALL STORE INTEGRATED CIRCUIT CODE

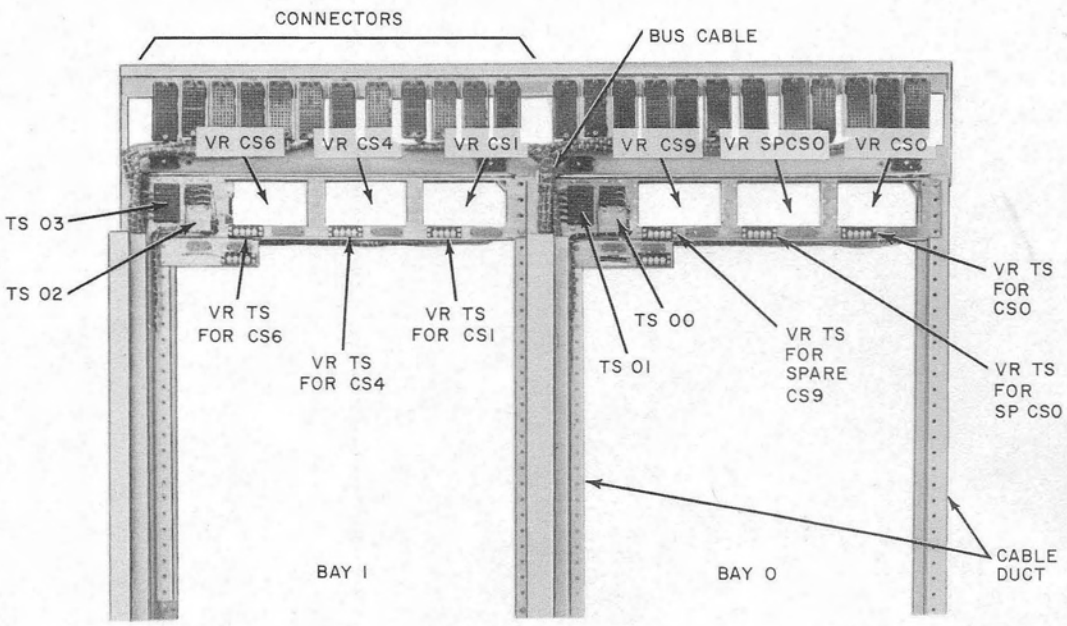
INTEGRATED CIRCUIT CODE*	DESCRIPTION
15A	Dual-Five Input Gate
15B	Differential Comparator
17A	High Power Quad
17B	JK Flip-Flop
73A	Matched Pair Transistors
510A	Common Anode Diode Matrix
510B	Common Cathode Diode Matrix

CALL STORE FRAME I



A. FRONT OF CALL STORE FRAME

CALL STORE FRAME O



LEGEND

S — SPARE
TS — TERMINATING STRIP
VR — VOLTAGE REGULATOR

NOTE:
CALL STORE FRAME I IS SIMILAR TO CALL STORE FRAME O.
FIG. 23 SHOWS THE FIXED LOCATION OF EACH CALL STORE UNIT ON THE CALL STORE FRAME.

B. REAR OF CALL STORE FRAME

Fig. 2—2-Bay Call Store Frame

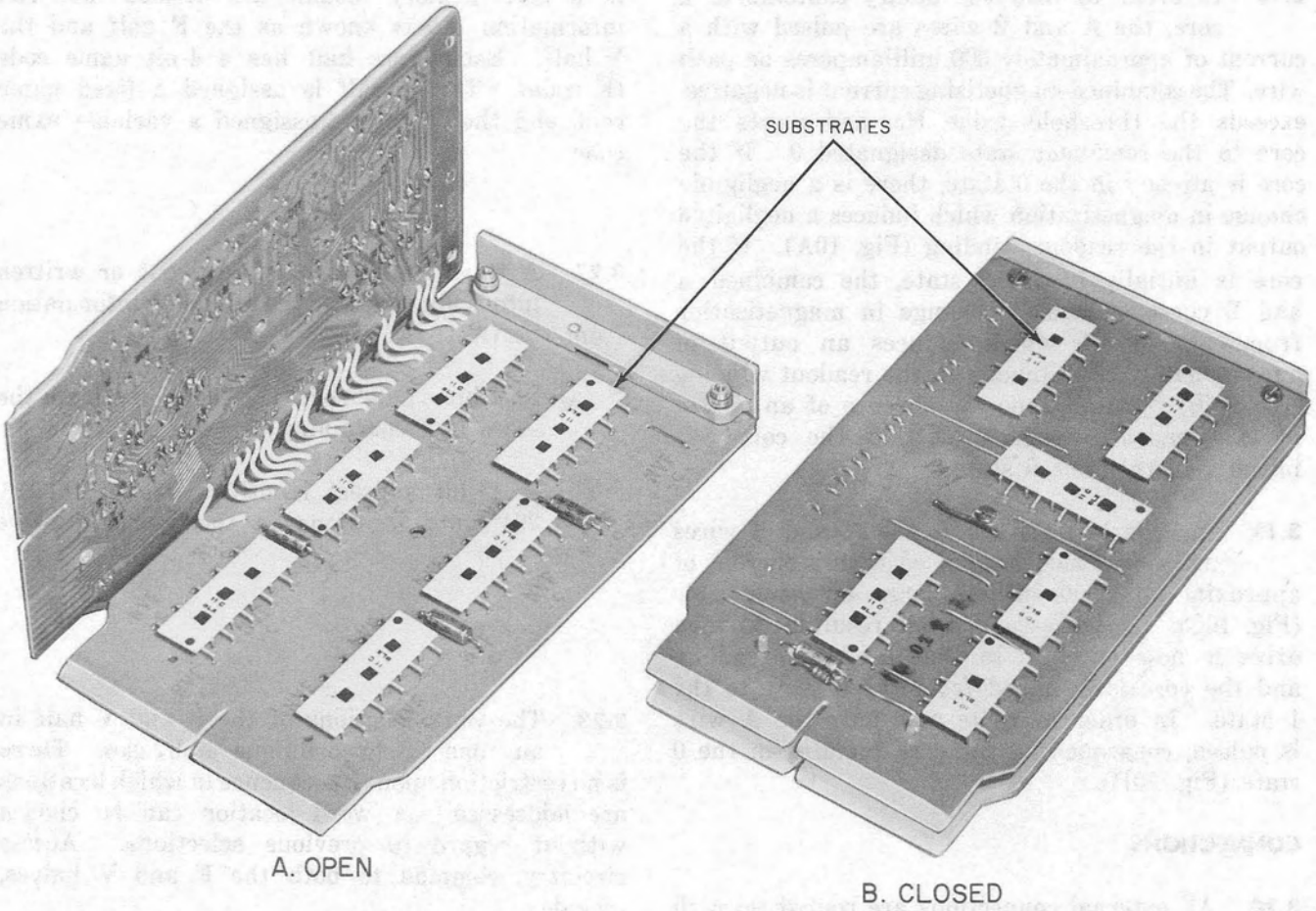


Fig. 3—Double Assembly Circuit Pack

ferromagnetic material around each hole can be magnetized in either the clockwise or counterclockwise direction to store a binary information bit. The magnetizing drive is established by current in conductors that act on the magnetic core material. After removal of the magnetizing drive, the ferrite material retains a remanent magnetization $+B_R$ or $-B_R$. In order to switch (reverse) the magnetization from $-B_R$ to $+B_R$, it is necessary to apply a positive magnetizing drive that exceeds the threshold value of $+H_C$. Similarly, in order to switch from $+B_R$ to $-B_R$, it is necessary to apply a negative magnetizing drive that exceeds the threshold value of $-H_C$.

3.15 If the state of the ferrite material is +BR, a negligible change in magnetization results from a positive drive or from a negative drive that does not exceed HC. The change in magnetization is also negligible when the ferrite material is -BR and the applied drive is negative or is positive but less than HC.

3.16 Since the ferromagnetic core material can be magnetized in either the clockwise or counterclockwise direction, the cores can be used for storage of binary data. One state of remanent magnetization is assigned the binary value 0, and the opposite state is assigned the binary value 1.

3.17 Reading and writing operations each have a read cycle followed by a write cycle. The read cycle is destructive because the core, regardless of its initial condition, is forced into the 0 state. During reading operations, the write cycle is used to restore the information just read. During writing operations, the read cycle is used to clear the core and the write cycle is used to store a 1 or a 0.

3.18 In order to read the binary contents of a core, the A and B wires are pulsed with a current of approximately 300 milliamperes on each wire. The combined magnetizing current is negative, exceeds the threshold value Hc, and resets the core to the remanent state designated 0. If the core is already in the 0 state, there is a negligible change in magnetization which induces a negligible output in the readout winding (Fig. 10A). If the core is initially in the 1 state, the combined A and B currents cause a change in magnetization from $+B_R$ to $-B_R$ which induces an output of approximately 30 millivolts in the readout winding (Fig. 10B). The presence or absence of an output in the readout indicates whether the core was initially in the 1 or 0 state.

3.19 In order to write a 1, the A and B wires are simultaneously pulsed with a current of approximately 300 milliamperes on each wire (Fig. 10C). The direction of the resultant applied drive is now opposite to that used for reading, and the core is switched from the 0 state to the 1 state. In order to write a 0, only the A wire is pulsed; consequently, the core remains in the 0 state (Fig. 10D).

CONNECTIONS

3.20 All external connections are routed through 24 connectors located on the rear of the module (Fig. 6). If failure occurs in the field, the defective memory unit can be unplugged, removed from the CS unit, and replaced with a spare memory unit. ***Field maintenance is not practical, and all repair work must be performed at the repair stations or the manufacturing plant.***

BASIC CALL STORE

A. General

3.21 A block diagram of the 32K CS is shown in Fig. 11. The 32,768 word locations contained in a 20A memory module are divided into two information blocks known as the F half and the V half. Each store half has a 4-bit name code (K code). The F half is assigned a fixed name code and the V half is assigned a variable name code.

3.22 A word location to be read out or written into is identified by the following information from the CC.

(a) A 4-bit name code (K code) specifies the store half containing the word location.

(b) A 14-bit address identifies one of the 16, 384 word locations in the specified store half.

3.23 The word locations of the F and V half in any one CS have unique addresses. There is no restriction upon the sequence in which locations are addressed. A word location can be chosen without regard to previous selections. Access circuitry, common to both the F and V halves, include

- Address register
- Readout detector circuits
- Current drivers
- Data registers
- Address detector.

B. Reading

3.24 During the first stage of a reading operation, access is gained to the desired word location by pulsing 1 of the 1024 A leads and 26 of 832 (1

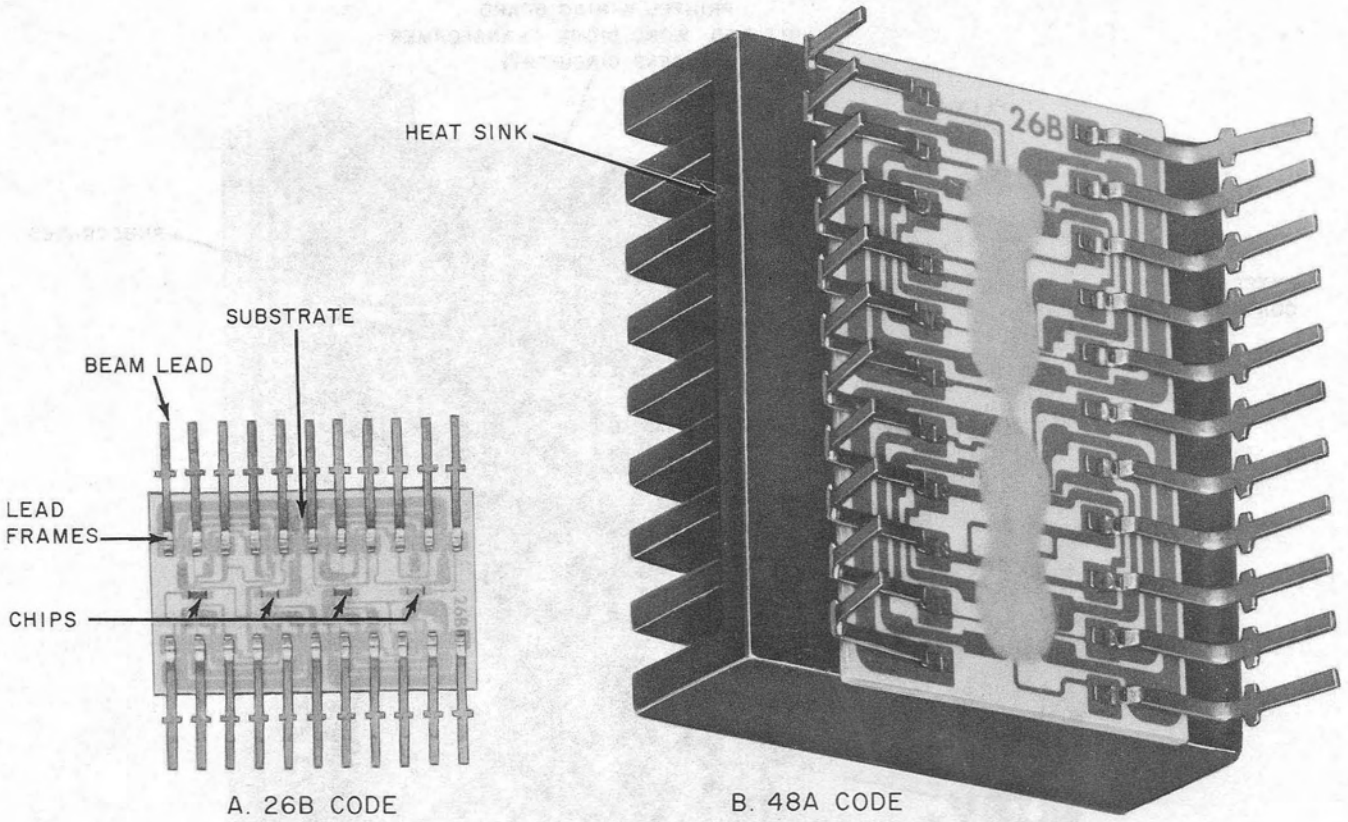


Fig. 4—Integrated Diode Substrates

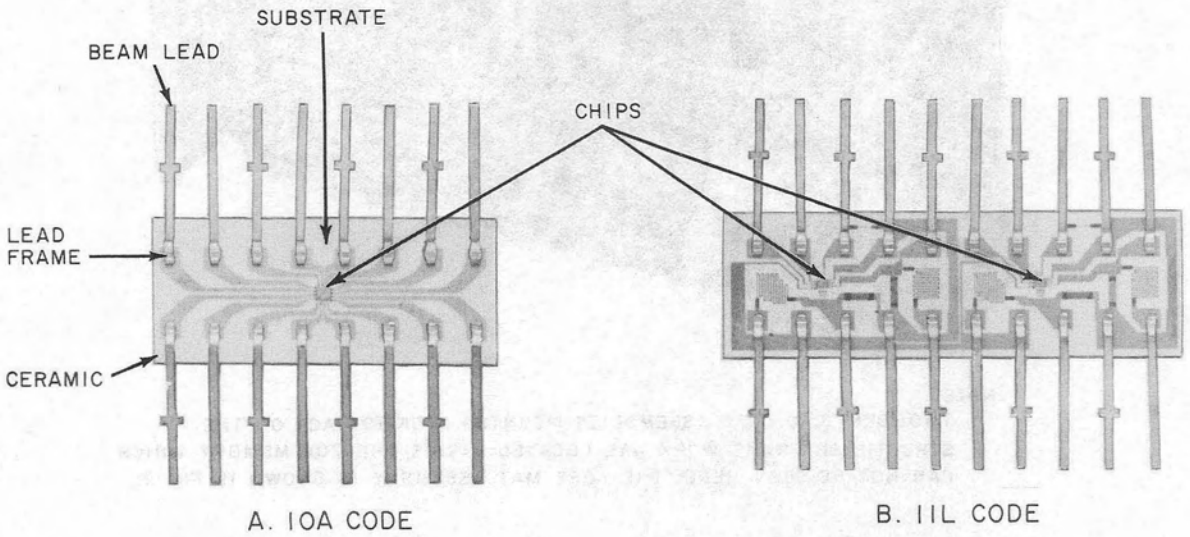
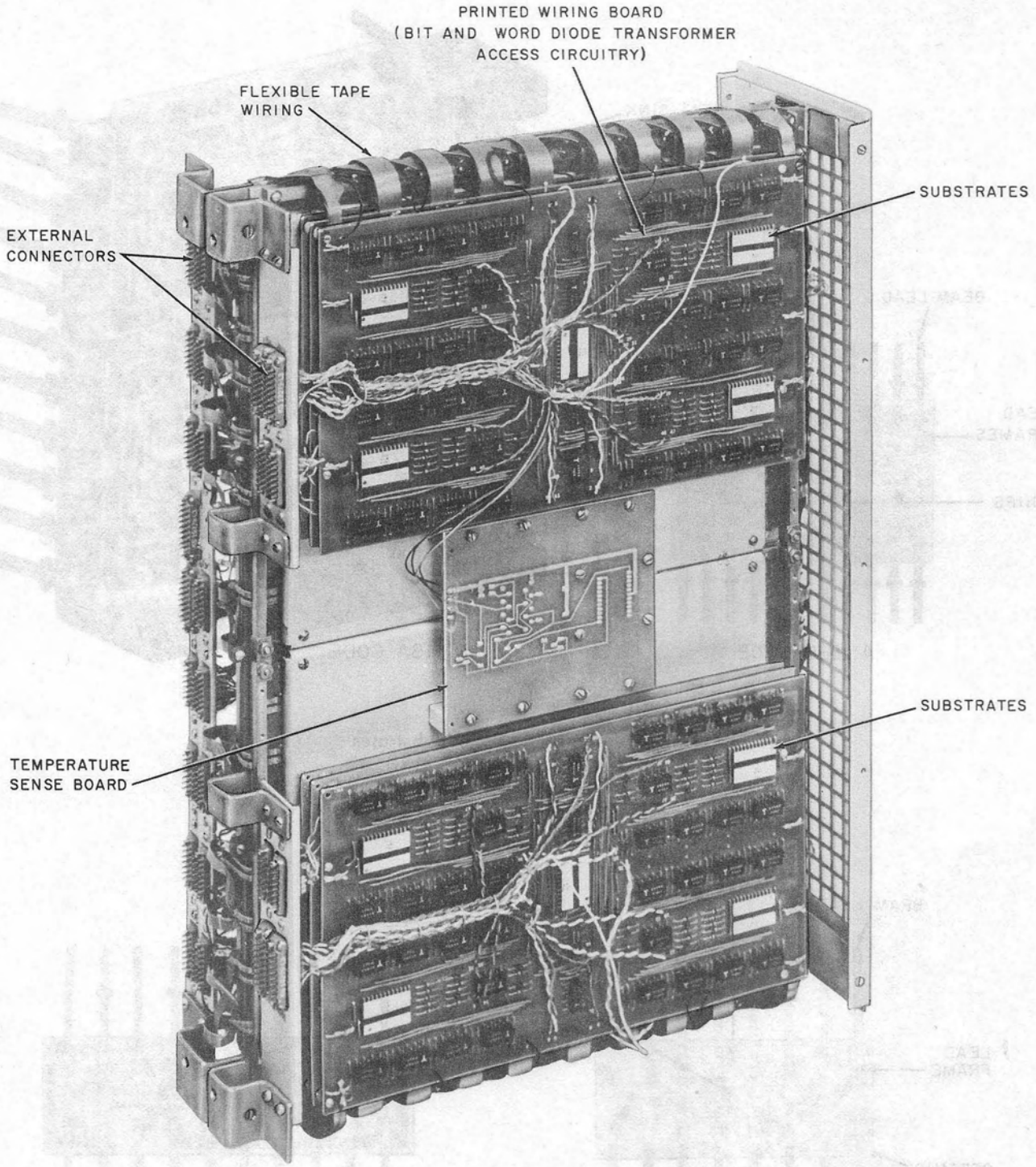


Fig. 5—Integrated Ceramic Substrates



NOTE:
TWO IDENTICAL CORE ASSEMBLIES MOUNTED BACK TO BACK ON THE STRUCTURAL FRAME WORK ARE LOCATED INSIDE THE 20A MEMORY WHICH CAN NOT BE SEEN HERE. THE CORE MAT ASSEMBLY IS SHOWN IN FIG. 7.

Fig. 6—20A Memory

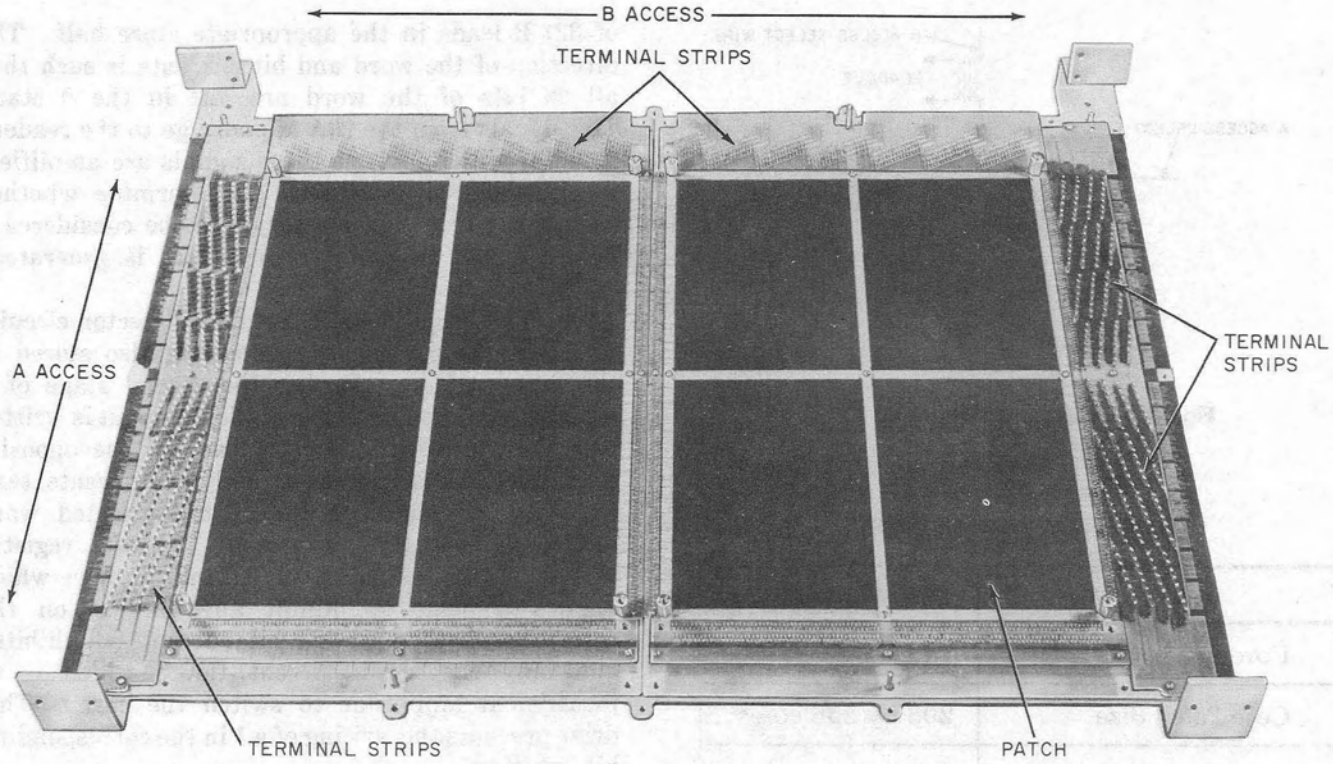


Fig. 7—Core Mat Assembly

TABLE C

PRINTED WIRING BOARDS ON 20A MEMORY

PRINTED WIRING BOARDS	NUMBER	DESCRIPTION
A Access	6	The bridge drive matrix and associated diode rails are equally divided on both sides of the core assembly.
B Access Rail	8	Current driver transformers located at the top of the module drive current through the cores to the bottom of the module where the access bridge rail diodes are located. The aluminum base plate to which the cores are secured serves as a ground return point to complete the current. The current driver transformers and associated circuitry are evenly divided on both sides of the core assembly.
B Access Current Driver	4	
Temperature Sensor	1	Consists of a temperature sensing regulator which automatically adjusts the drive currents to compensate for temperature variations.

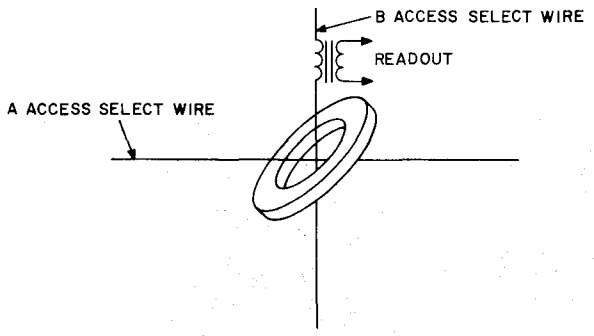


Fig. 8—Equivalent Magnetic Core

TABLE D

CORE MAT DIMENSIONS

CORE MAT	DIMENSIONS
Core Spacing	18 by 20 mils
Core Patch Size	208 by 256 cores
Core Patch Dimensions	3.726 inches by 5.10 inches
Total Cores Per Patch	53,248
Core Patches Per Mat	4
Overall Mat Dimensions	10 inches by 13.5 inches
Core Mats Per Memory	4

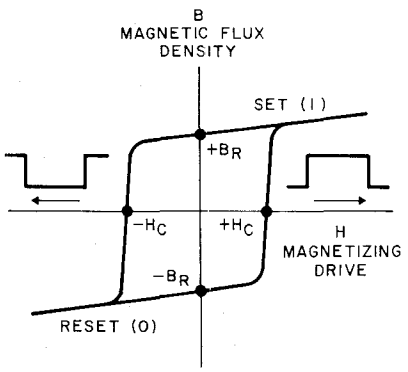


Fig. 9—Square-Loop Characteristics

of 32) B leads in the appropriate store half. The direction of the word and bit currents is such that all 26 bits of the word are left in the 0 state. The signals from the 20A memory go to the readout detector circuits where these signals are amplified. A threshold is referenced to determine whether each input from the memory is to be considered a 1 or a 0 and an appropriate output is generated.

3.25 The outputs of the readout detector circuits in the reading operation are also stored in the data register. During the second stage of a reading operation, the information readout is written back by the same A and B leads in the opposite direction. Thus, the word and bit currents tend to write a 1 in each bit of the selected word location. However, any bit of the data register that is 0 activates an associated inhibit drive which applies a pulse to inhibit any current on the associated B lead. (The bit current is inhibited and only the word current flows, which is of insufficient amplitude to switch the core.) This drive prevents the writing of a 1 in the corresponding bit position.

C. Writing

3.26 During the first stage of a writing operation, the specified word location is read out. The outputs of the readout detector circuits are not gated into the data register, and the net effect is to clear the word location. The data register is set by the 24-bit data word received via the bus from CC. During the second stage of a writing operation, these bits are written into the cleared word location in the same way as in the reading operation.

D. Access

3.27 Inputs from the CC specify the operation to be performed (reading or writing), the address of the word involved and, in the case of writing, the word to be written. The CS carries out the request and, in the case of reading, transmits to the CC the word it read. Within the 20A memory, a coincident current selection system consisting of a ***word*** or an ***A access*** and a ***bit*** or a ***B access*** is used to read and write information (Fig. 12 and Table E). The word access performs a 1 out of 1024 selection while the bit access performs a 1 out of 32 selection which is repeated 26 times. The word access is organized into two identical halves with each driving

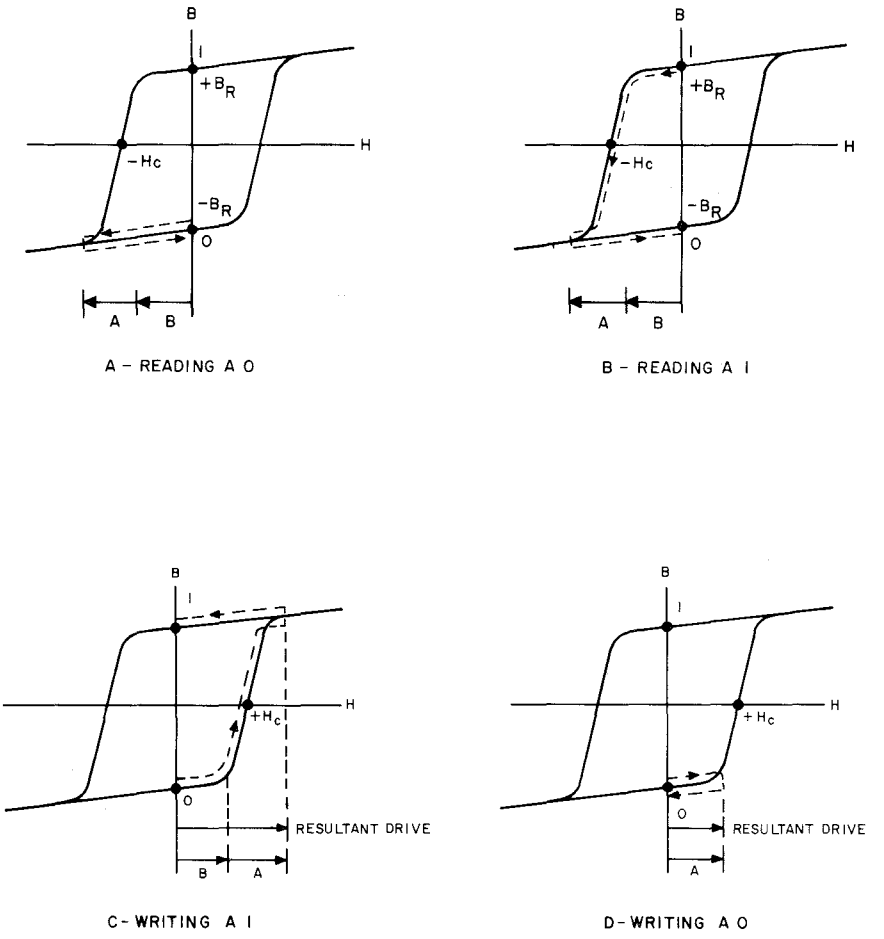


Fig. 10—Memory Core Read/Write Operations

12 bits per word (the 25th and 26th bits are shared between the left and right halves).

3.28 The core array is made of an X plane and a Y plane (Fig. 13) corresponding to the variable and fixed half. Each plane contains 425,984 bits. The B access selects two wires per bit: one wire in the X plane and one wire in the Y plane, driving current in each wire. Multipoled bidirectional switches, called rails, are required at the end of the B-memory wires. The rails are composed of ICs which form gang switches (analogous to "fast" multicontact relays). A specified set of switches must be closed at or before the time the B-memory current is driven down the B-wire. The 1 out of 8 B-rails (A2-A0) along with 1 out of 4 current drivers (A4-A3) provides the 1 out of 32 selection required of the B access.

3.29 Each word access selects only one A-wire on either the X plane or the Y plane. Two sets of A-access circuits are provided: one set of A-access circuits for the left half of each plane and one set of A-access circuits for the right half of each plane. Each half consists of 512 A-memory wires. Z equals the A-memory wire loop for bits 0 through 11; Z1 equals the A-memory wire loop for bits 12 through 23. (The 20A memory has the capacity to handle 26 bit words; however, the No. 1 ESS uses only the first 24 bits). Rails are required at the end of the A-memory wire loops (Fig. 14). The 1 out of 8 A-rails (A14-A12) along with 1 out of 8 A-horizontal (A11-A9), 1 out of 8 A-vertical (A8-A6), and two polarities of the A-current (A5) provide the 1 out of 1024 selection required of the A access. Polarity is important not only for read-write operations but also for proper core selection, since two cores are common to an A-access

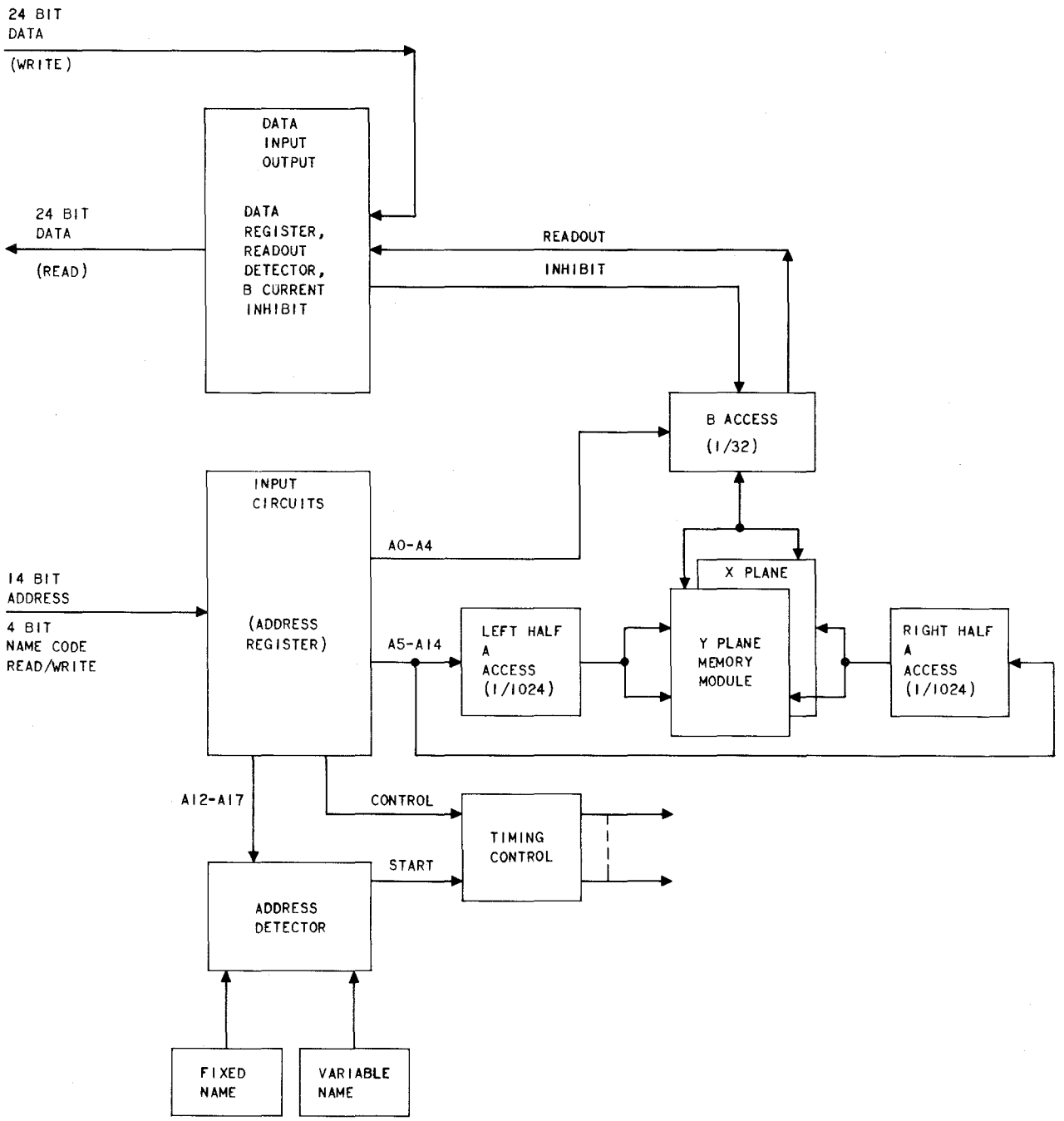


Fig. 11—32K Call Store Block Diagram

select wire. Figures 15A and 15B show polarity relationships for reading each of the core couplets. Please note that while the resultant drive of the A and B select wires is series-aiding to the core actually read, to the other core of the couplet it is series-opposing.

E. Readout

3.30 Figure 16A shows an example of 26 readouts.

A 1 out of 32 selection is necessary to extract the readout signals from the driven B wires. Since only one 26-bit word location at one time can be

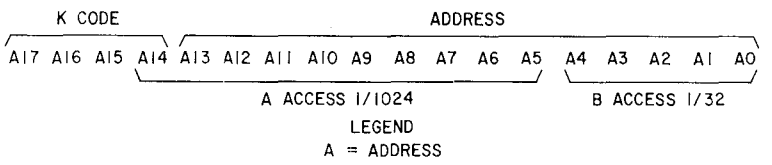


Fig. 12—Access Functions

TABLE E

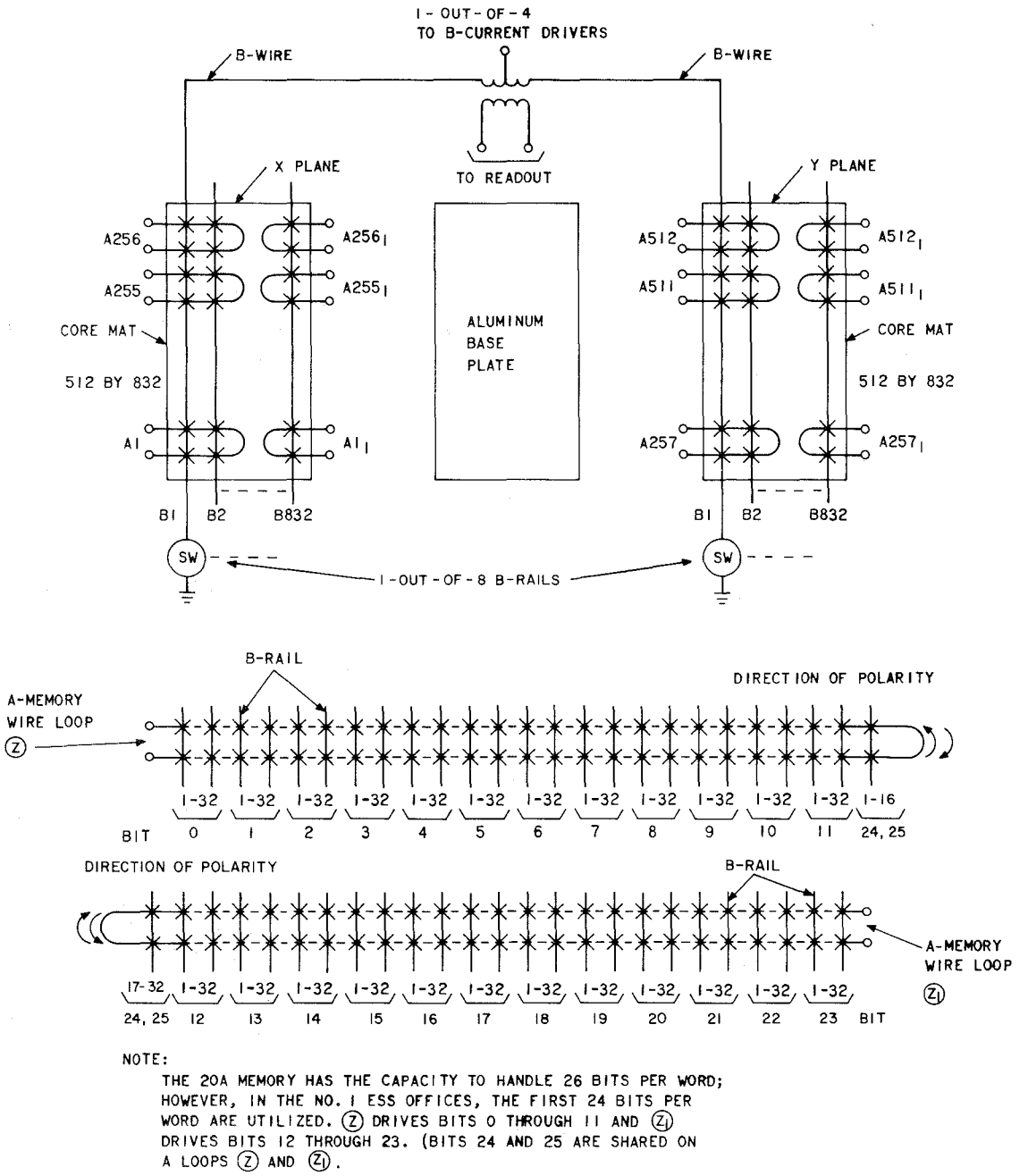
A AND B ACCESS FUNCTIONS

	BITS	FUNCTION
B ACCESS	A2-A0	B rail drivers perform 1 out of 8 selections of B diode rails and generate B rail bias.
	A4-A3	B current drivers perform 1 out of 4 selection of bit drivers and perform read-write switching.
A ACCESS	A5	Direction of polarity (A5 = 1, the read current is negative and the write current is positive; A5 = 0, the read current is positive and the write current is negative.)
	A8-A6	A current drivers perform 1 out of 8 selection of A verticals and sample current to generate strobe.
	A11-A9	A horizontal driver matrix performs 1 out of 8 selections of A horizontal rails and generates A horizontal bias.
	A14-A12	A rail driver matrix performs 1 out of 8 A rails and generates A rail bias.

read out differentially, only one set of 26 readouts can be active. Figure 16B is another view of the readout path. It shows the dual-core A-access select wires and the B-access select tape transformer coupled to the readout wires.

VOLTAGE REGULATOR

3.31 A voltage regulator provides the -3, +5, -12, and +12 voltages required for each CS unit (Fig. 1). Voltage regulators will be equipped as required and will be secured to a mounting plate located at the topmost mounting position in each bay. Each mounting plate can be equipped with up to three regulators (one voltage regulator per CS unit) which serve the CS unit located in the associated equipment bays. ▶The J1A072AC-1 voltage regulator unit is connectorized with the exception of four pairs of power leads that connect to a terminal block and four pairs of ground leads that connect to mounting screws of the voltage regulator. The J1A072AC-2 voltage regulator unit is connected with the exception of the output wires that connect to screw terminals on the rear of the voltage regulator.◀



NOTE:
THE 20A MEMORY HAS THE CAPACITY TO HANDLE 26 BITS PER WORD; HOWEVER, IN THE NO. 1 ESS OFFICES, THE FIRST 24 BITS PER WORD ARE UTILIZED. (Z) DRIVES BITS 0 THROUGH 11 AND (Z1) DRIVES BITS 12 THROUGH 23. (BITS 24 AND 25 ARE SHARED ON A LOOPS (Z) AND (Z1).

Fig. 13—Breakdown of X and Y Plane of Memory

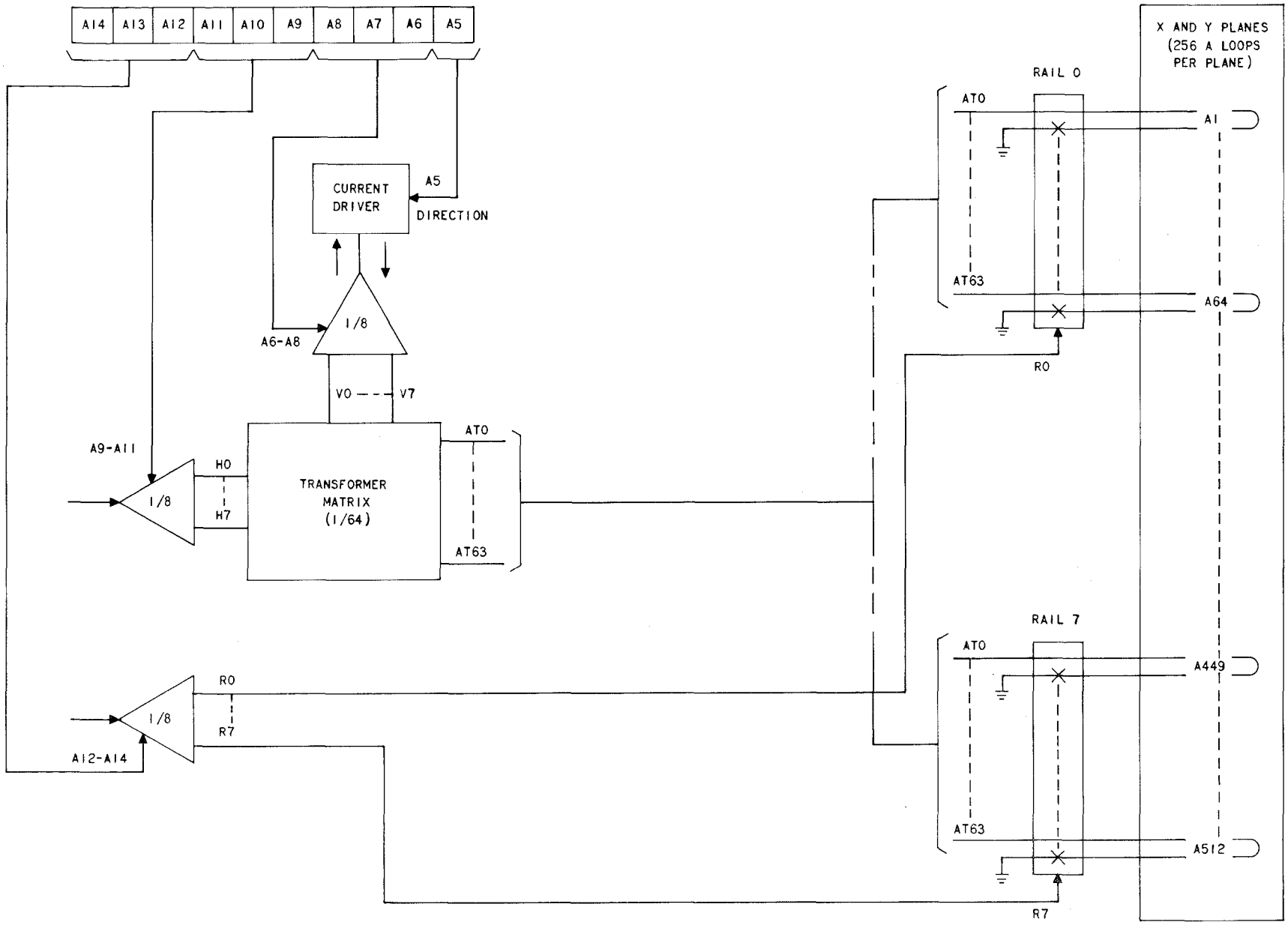


Fig. 14—A Loop Selection

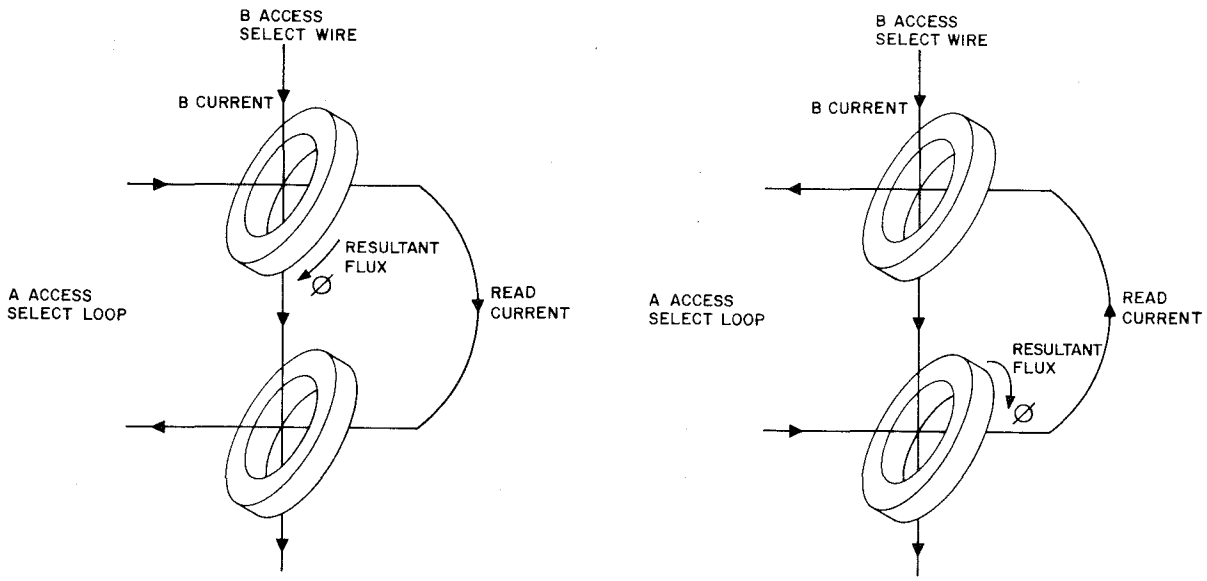
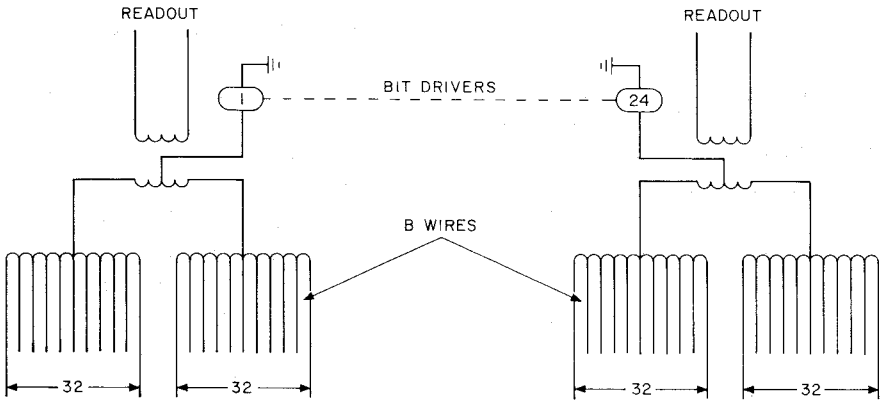
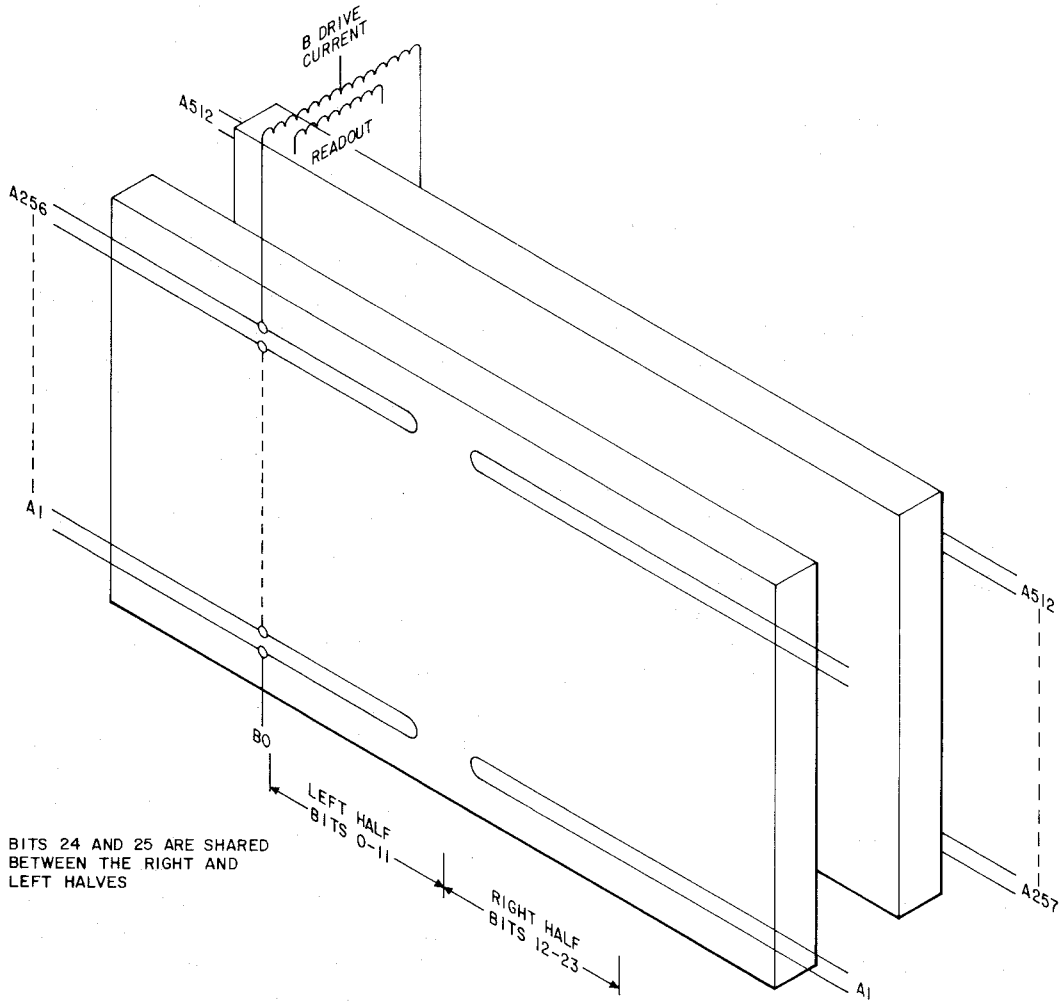


Fig. 15—Reading A Core Couplet



A - SYMBOLIC REPRESENTATION



B - PICTORIAL REPRESENTATION

Fig. 16—Example of Readout Selection

CONTROL PANEL

3.32 Each 32K CS unit is equipped with a control unit 1-3/4 inches wide and 21 inches long. This unit is mounted vertically as shown in Fig. 1. The control unit is composed of associated relays and a control panel containing lamps and switches so that the CS can be manually removed from service for maintenance or repairs. Three interlocked pushbuttons on the control panel are provided as follows:

DESIGNATION	FUNCTION
OFF	Power is manually disconnected and the system has no control of the CS.
REQ INH (request-inhibit)	System is requested to release the CS by placing it in an out-of-service state.
NOR (normal)	System has control of the CS.

A pushbutton type start (ST) key is used to restore power. Lamps on the control panel indicate whether the CS is normal, is out of service, or has a power alarm.

3.33 Spare jacks, telephone jacks, and test points for -48, +24, and ground ***are not*** provided on the CS frame. This facility will, however, normally be available on the adjacent and/or facing frames and may be used when necessary to service the CS frame. The facilities located on the adjacent and/or facing frames will be within approximately 9 feet of all points on the CS frame.

4. EQUIPMENT CONFIGURATIONS

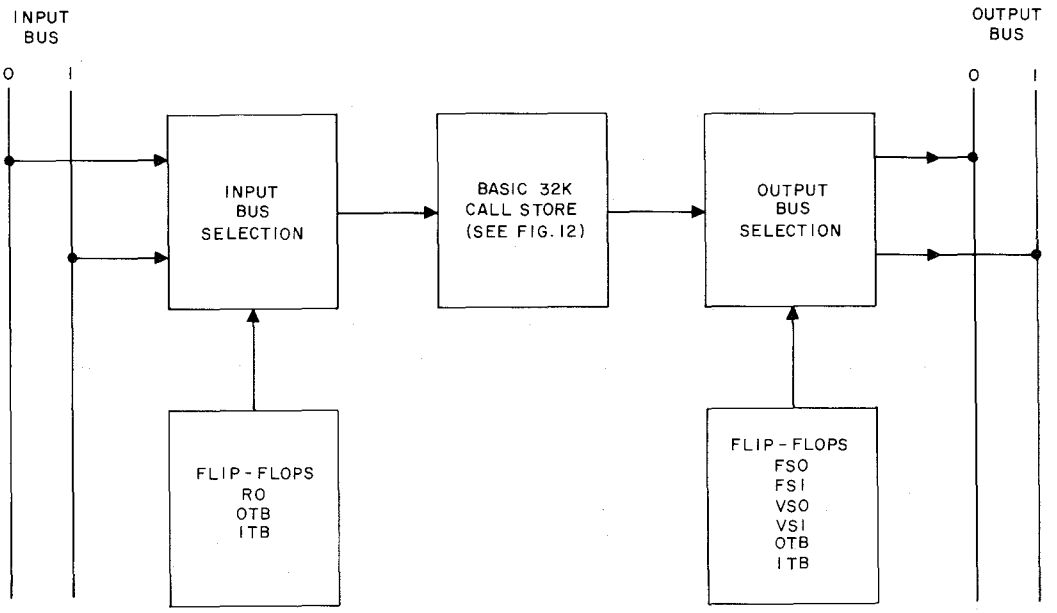
SYSTEM CONFIGURATIONS

4.01 Connection of the CS to the duplicate CC or SP buses is shown in Fig. 17A and Fig. 17B. Each bus consists of 51 pairs of wires to the CSs and 26 pairs of wires from the CSs. Each CS can communicate on either or both duplicate buses whether associated with a CC or an SP. Figure 17A shows a functional diagram of bus connections and their relation to route flip-flops. Figure 17B shows how a full compliment of 32K CSs would look in an SP office.

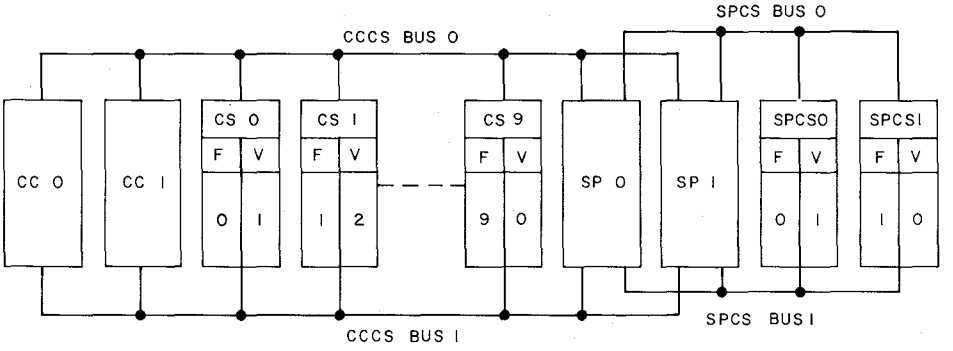
NORMAL CONFIGURATIONS

4.02 Each store half memory block is assigned a name code (K code) consisting of four bits (2 K codes of 4 bits per half). The purpose of this coding is to permit selective communication with a number of CSs using a common bus system. Each CS in a store community contains two memory blocks and is connected by a duplicated bus system to its processor (CC or SP). Answer flip-flops in the CS for each of its memory blocks determine the bus or buses over which data is to be sent back to the processor. A receive-on (RO) flip-flop in the CS selects the bus over which the store receives information and instructions from the processor. In this duplication scheme, commonly known as split duplication, one of the memory blocks in each CS has a permanently wired name while the name of the other memory block can be changed under program control. The memory block with the permanently wired name (fixed) is called the F half. The memory block whose name can be altered (variable) is known as the V half. An answer flip-flop in the CS determines the bus on which a given memory block will respond. The name of the answer flip-flop identifies the memory block and bus with which it is associated (FS0, VS1, etc). As an example, Fig. 18 shows four CSs connected to duplicate buses 0 and 1. Normally, identical names are assigned to the duplicate information blocks in the F half of one store and the V half of another store.

4.03 Normal nonmaintenance programs are written without taking into consideration that the information is duplicated. In the example, there are four pairs of duplicate information: blocks 0F and 0V, 1F, and 1V, 2F and 2V, and 3F and 3V. However, the program sees only the four unduplicated information blocks as shown in Fig. 18A. Assume that a program specifies word a in information block 1. There are two copies of word a available: one copy (aF) in CS 1 and the other copy (aV) in CS 0. The CC identifies word a by means of an 18-bit address which consists of a 4-bit name code (K code) to specify informaton block 1 and 14-bit address (A) to specify word a within information block 1. The name code and the address A (14 bits) are transmitted by CC on both buses to all the CSs. However, only two CSs (CS 0 and CS 1) will detect a match between the name code transmitted and a name internally assigned. As a result, only these two CSs will use address A. Within the two CSs, the 14-bit address A received



A. FUNCTIONAL DIAGRAM OF BUS CONNECTIONS



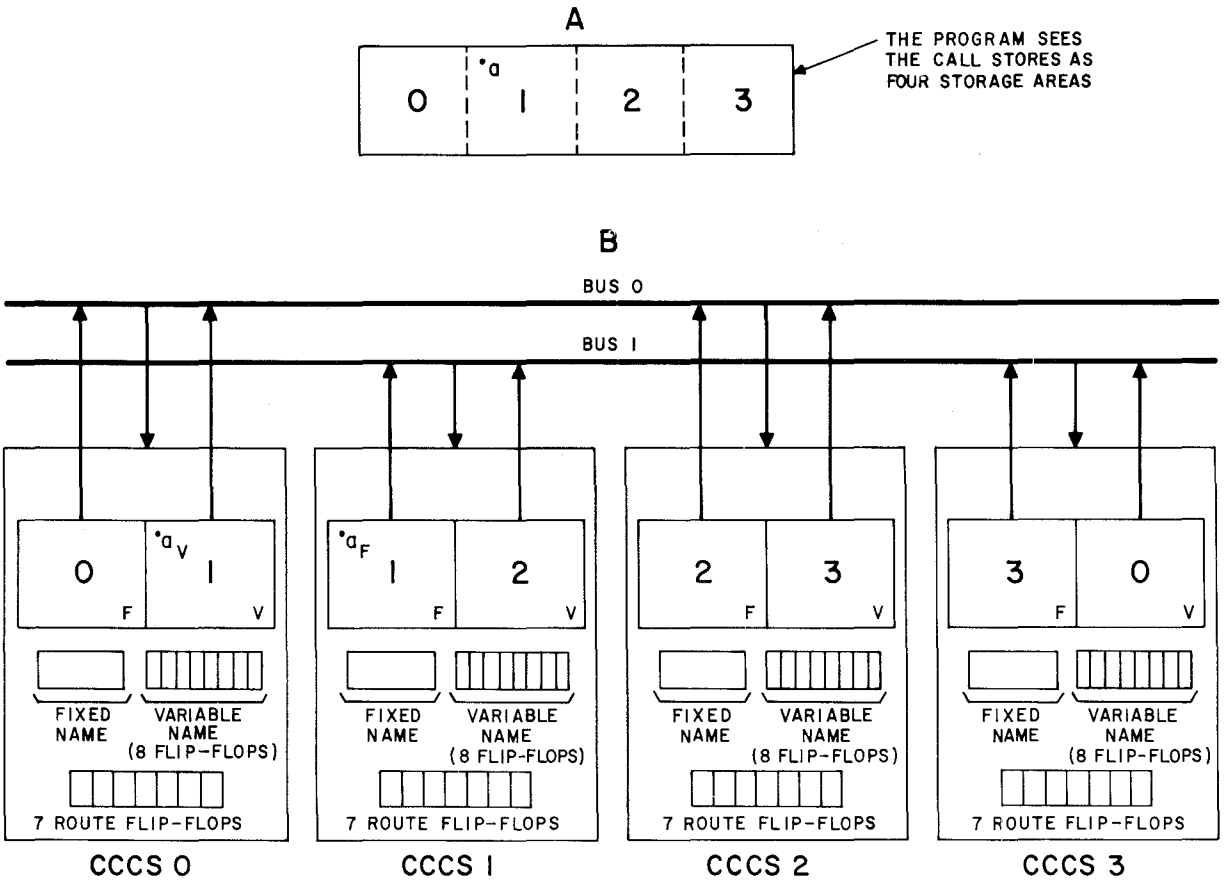
B. BUS CONNECTIONS IN AN SP OFFICE

Fig. 17—Connection to Duplicate Buses

from the buses is supplemented by a 15th bit (V half or F half select) generated within the store depending upon the store half being addressed. For example, CS 0 would generate F = 0 and V = 1 in order to locate the word aV; CS 1 would generate F = 1 and V = 0 in order to locate the word aF. In the CS 0, the access circuit activated is that of the V half since its variable name matches the name code received. Similarly, in CS 1, the access circuit activated is that of the F half since its fixed name matches the name code received.

4.04 Seven route flip-flops within each CS are preset by the ESS to control the inputs and outputs to and from the buses as specified in Table F and Fig. 17. The two trouble flip-flops (0TB and 1TB) are controlled by the system or by conditions within the CS.

4.05 The selection of input and output buses under normal conditions with an even number of CSs is shown in Fig. 18. Bus 0 supplies the address and receives the readout for a word such as av in



NOTE: THE F HALF NAME OF EACH STORE IS FIXED.
THE V HALF NAME IS SET ON 8 FLIP-FLOPS AND IS VARIABLE.

Fig. 18—Call Store Name and Route Flip-Flops

CCCS 0. Bus 1 supplies the address and receives the readout for the duplicate copy a_F in CCCS 1. The same configuration applies to all the other information blocks. This is also true with an odd number of CSs except for information blocks 0F and 0V; both of these blocks receive the address from bus 0 (Fig. 19).

TROUBLE CONFIGURATIONS

4.06 Malfunctions in CSs and buses cause changes in the system configuration until the trouble is corrected. Assume that CS 0 has been recognized to be operating improperly (Fig. 20A). Under these conditions the 0TB and 1TB flip-flops of CCCS 0 will have been set by a program, and CCCS 0 will be unable to satisfy any requests for either information block 0 or 1. Since only the F half of CS 1 can satisfy any requests for information block 1, the F readouts of CCCS 1 must be sent on both buses. This is accomplished by having a program set both the FS0 and the FS1 flip-flops of CCCS 1. Similarly, since only the V half of CCCS 3 can satisfy any requests for information block 0, the V readouts of CCCS 3 must be sent on both buses. Consequently, the VS0 and the VS1 flip-flops must be set in CCCS 3. If it is assumed that CC 0 is the active CC and that it transmits and receives via bus 0, then CCCS 1 and CCCS 3 must receive from active bus 0. Any request for information blocks 2 and 3 is handled normally as covered in 4.02.

4.07 When a bus malfunction occurs, the outputs of one half of each CS are connected to the operational bus. Assume that bus 0 is inoperative (Fig. 20B). Under these circumstances, the outputs of the V half of each CS are disconnected; the outputs of the F half of each CS are connected to bus 1. Inputs to both halves of each CS are applied

TABLE F

CALL STORE CONTROL FLIP-FLOPS

FLIP-FLOP	SET	RESET
RO	Receive all requests from bus 0. Send maintenance and control readouts on bus 0	Receive all requests from bus 1. Send maintenance and control readouts on bus 1
FS0	Send normal readouts from F on bus 0	———
FS1	Send normal readouts from F on bus 1	———
VS0	Send normal readouts from V on bus 0	———
VS1	Send normal readouts from V on bus 1	———
OTB	Inhibit inputs and outputs on bus 0 in all modes	———
ITB	Inhibit inputs and outputs on bus 1 in all modes	———

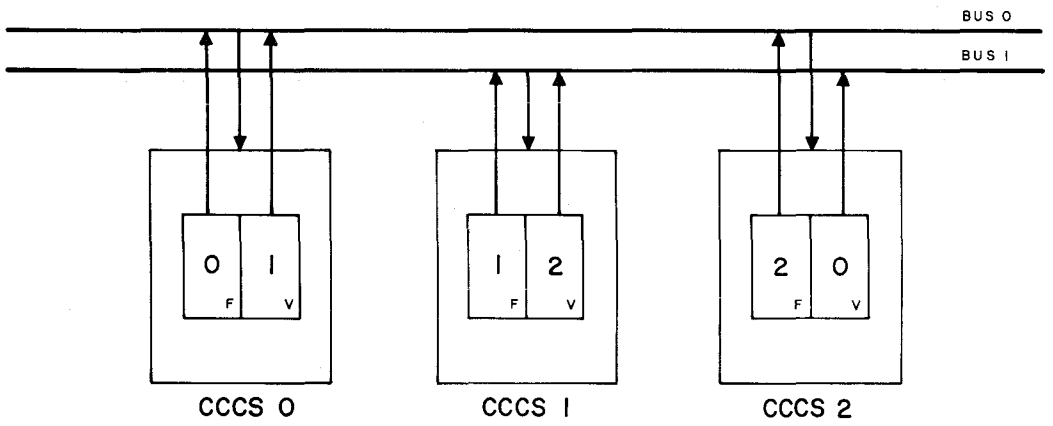
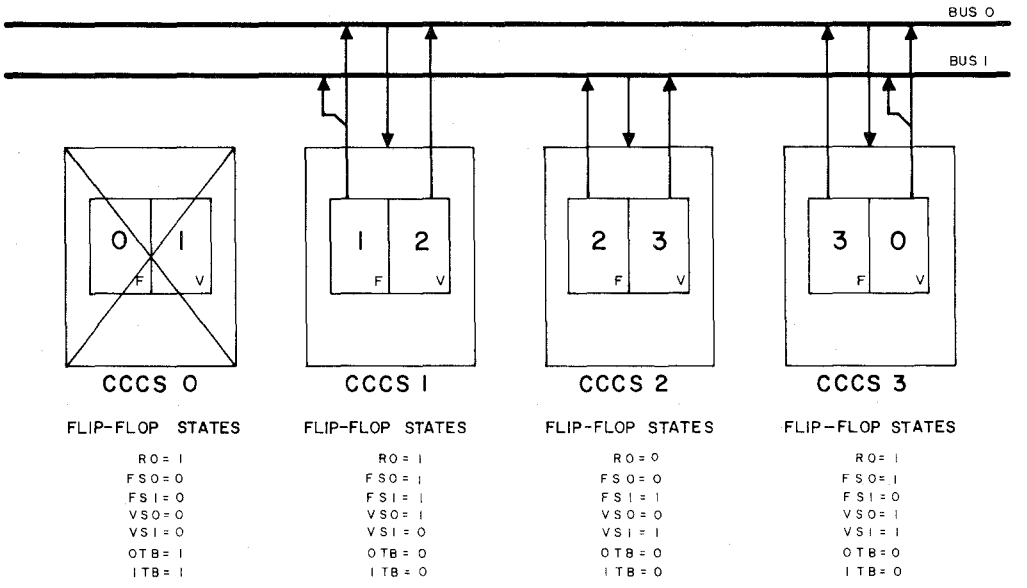


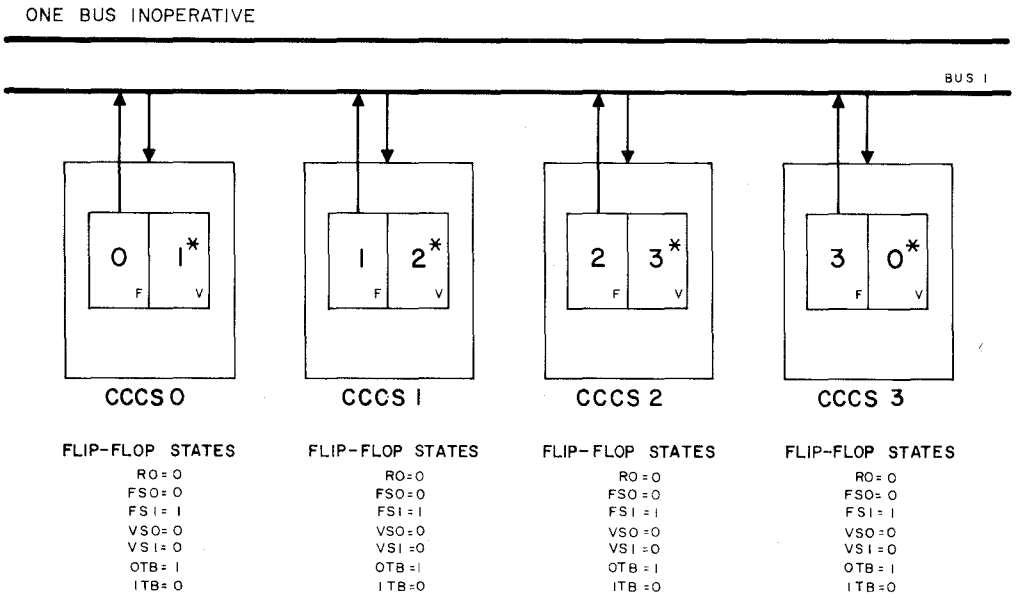
Fig. 19—Selection of Buses With an Odd Number of Call Stores

on bus 1 in order to keep the duplicate copies of all information blocks updated.

4.08 Figure 21 gives examples of trouble configurations that change the name flip-flops of variable memory block. Figure 21A shows CS 0 and CS 1 in trouble, which destroys both copies of memory block 1. By changing the name flip-flops for the V half of CS 2, block 1 can be temporarily reinstated. Figure 21B shows a case where special information, such as the network map, is assigned to a new V half before the losing of both copies forces such an action with its attendant catastrophic reinitialization. Again, CS 2 is used to provide the duplicate copy of block 1.



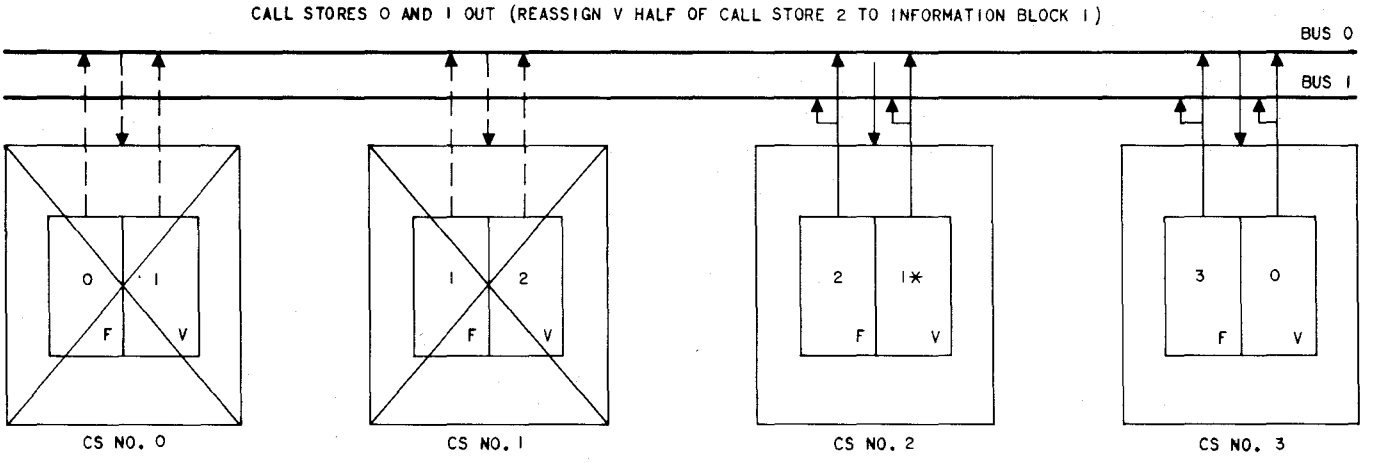
A-CALL STORE 0 OUT OF SERVICE



B-BUS 0 OUT OF SERVICE

Fig. 20—Trouble Configurations That Retain Normal Variable Memory Block Assignments

CALL STORES 0 AND 1 OUT (REASSIGN V HALF OF CALL STORE 2 TO INFORMATION BLOCK 1)

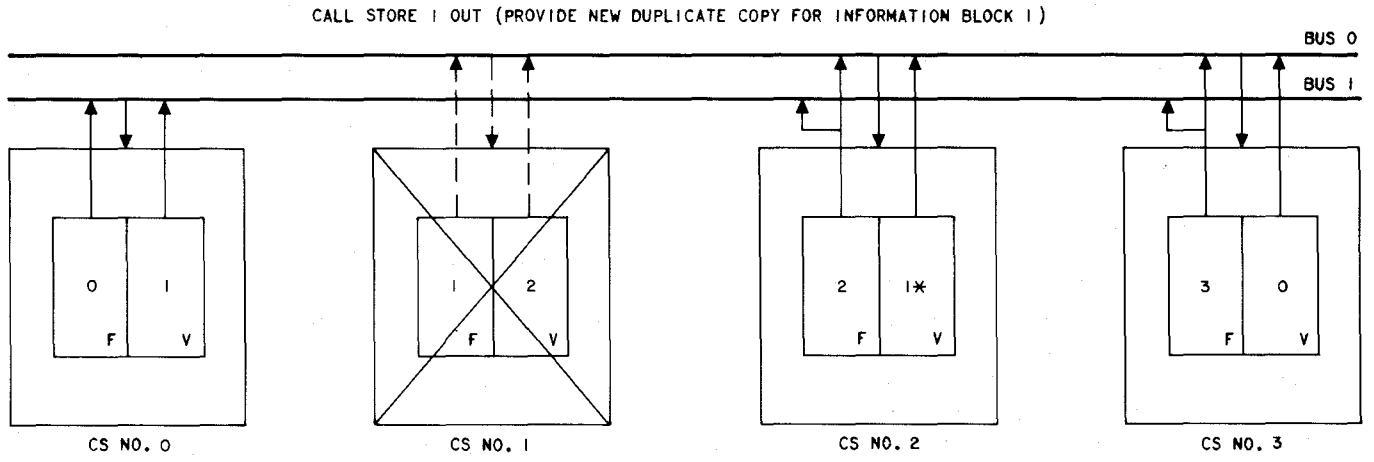


	CS NO. 0	CS NO. 1	CS NO. 2	CS NO. 3
RO - 1	1	1	1	1
FSO - 0	0	1	1	1
FSI - 0	0	1	1	1
VSO - 0	0	1	1	1
VSI - 0	0	1	1	1
OTB - 0	1	0	0	0
ITB - 1	1	0	0	0

* NORMALLY ASSIGNED TO INFORMATION BLOCK 3

A - CALL STORE 0 AND 1 OUT OF SERVICE

CALL STORE 1 OUT (PROVIDE NEW DUPLICATE COPY FOR INFORMATION BLOCK 1)



	CS NO. 0	CS NO. 1	CS NO. 2	CS NO. 3
RO - 0	1	1	1	1
FSO - 0	0	1	1	1
FSI - 1	0	1	1	1
VSO - 0	0	1	1	1
VSI - 1	0	0	0	0
OTB - 1	1	0	0	0
ITB - 0	1	0	0	0

* NORMALLY ASSIGNED TO INFORMATION BLOCK 3

B - DEFENSIVE DUPLICATION OF CRITICAL MEMORY

Fig. 21—Trouble Configurations That Alter Variable Memory Block Assignments

5. MODES OF OPERATION

5.01 The CS can carry out orders to read and write (specified by AR and AW leads) in any one of four modes of operation. The binary coded leads (ACM, AGM, and AHM) specify the modes as follows:

	ACM	AGM	AHM
Normal Mode	0	0	0
F Maintenance Mode	1	1	0
V Maintenance Mode	1	0	1
Control Mode	0	1	1

NORMAL MODE

5.02 In the ***normal mode*** of CS operation, a request to read or write can be satisfied by a store in which the name of either the F half or the V half matches the name code received from the buses. Thus, under normal conditions, such a request is carried out simultaneously by two stores. One CS reads from or writes into its F half, and the other CS reads from or writes into its V half. Readouts from the F and V halves are transmitted on separate buses. If one of the two CSs should be out of service, the readout from the other CS is sent on both buses.

MAINTENANCE MODE

5.03 During the execution of a nonmaintenance program, a request in the normal mode for a particular item of information can be satisfied by either or both of the two CSs containing a copy of that information. For maintenance purposes, however, it is necessary to specify the particular F or V half of the store from which the information is to be read or into which it is to be written.

5.04 A request to read or write in the E maintenance mode can be satisfied only by a store in which the name of the F half matches the name code from the CC or SP. A word is read from or written into the F half at the location specified by the 14-bit address. Provided that the trouble flip-flops are not set, the RO flip-flop selects the bus from which the inputs are received and on which the outputs are sent. This selection is independent of the states of the FS0, FS1, VS0, and VS1 answer flip-flops. Similar considerations apply to a request to read or write in the *V* maintenance mode. Such a request can be satisfied by only a store in which the name of the V half matches the name code from CC. A word is read from or written into the V half at the location specified by the 14-bit address.

CONTROL MODE

5.05 An instruction to read or to write in a control mode can be carried out only by a CS in which the name of the F half matches the name code from CC. Provided that the trouble flip-flops are not set, the RO flip-flop selects the bus from which the inputs are received and on which the outputs, if any, are sent. This selection is independent of the states of the FS0, FS1, VS0, and VS1 answer flip-flops.

5.06 Instructions to read or to write in a control mode do not involve any address location in the ferrite core memory. As the result of a control read order, a CS senses the output of a selected group of flip-flops (internal logic states including answer flip-flops, variable flip-flops, and test points) and transmits this information to the CC. As the result of a control write order, a CS controls the inputs of a selected group of flip-flops (set answer flip-flops, variable name flip-flops, and test the data register) in accordance with information received from CC.

6. INTERCONNECTIONS

6.01 The leads contained in the buses (0 or 1) that connect the CSs with a CC or an SP are listed in Table G.

6.02 The 51 inputs to the CS can be divided into three groups because information is sent in three separate intervals of time (T_1, T_2, and T_3) as shown in Fig. 22. Each group contains a synchronizing signal which defines a time interval during which signals can be gated into the CS from the bus. The use of synchronizing signals reduces the time interval in which a store is exposed to noise signals on a bus.

6.03 During interval T_1, the following information is sent to all CSs:

- A 14-bit address (A13-A00)
- A 4-bit name code (A17-A14)

TABLE G

CALL STORE BUS LEADS

NUMBER OF LEADS		FUNCTION
TO CS	FROM CS	
1	—	Synchronizing signal for address, code, and mode enable (AS1A)
4	—	Name code for enabling (A17-A14)
3	—	Mode of operation (AHM, AGM, and ACM)
14	—	Address (A13-A00)
1	—	Synchronizing signal for read, write, and parity (AS2)
1	—	Read command (AR)
1	—	Write command (AW)
1	—	Parity check over code and address (AP)
—	1	Synchronizing signal for readout word (ACSSYN)
—	24	Readout word (ACS23-ACS00)
—	1	All-seems-well signal (ACSASW:)
1	—	Synchronizing signal for all 24 data bits of write-in word (DSA)
23	—	Word to be written (D22-D00)
1	—	Data Parity on word to be written (DP)
51	26	TOTAL

- Three mode bits (ACM, AHM, and AGM)
- A synchronizing signal for the address, code, and mode (AS1A).

6.04 The address, code, mode, and synchronizing pulse are received by all the CSs. However, the mode and address signals are used only by the CSs in which the appropriate conditions are satisfied as explained in 5.02, 5.04, and 5.05.

6.05 During interval T_2, the following information is received by all CSs:

- Parity check bit (AP).
- Read order signal (AR)
- Write order signal (AW)
- Synchronizing signal (AS2).

6.06 The parity check bit (AP) is computed by the CC or SP over the 4-bit name code and 14-bit address. This parity bit is checked at each enabled CS. If the check passes, the specified read or write order is executed by the CS. If the check fails, a reading operation is performed regardless of the signals received on the read and write order leads. This reading operation serves as a lockout to safeguard against writing information at the wrong address. The synchronizing signal starts the timing of a lockout interval. The lockout interval can last up to 2.7 microseconds.

6.07 During interval T_3, the following information is sent to the CSs:

- A 23-bit write-in word (D22-D00)
- A 1-bit parity input (DP)
- A synchronizing signal for all 24 bits of the write-in word (DSA).

The synchronizing signal gates the respective write-in bits into one or two enabled CSs as explained in 4.03 through 4.06.

6.08 The write-in data includes a parity bit computed by the CC or SP over the address, name code, and write-in data. This parity bit is not checked at the CS but is stored as bit 23 of the write-in word. When this word is read out at some later time, the parity bit will be checked at the CC or SP.

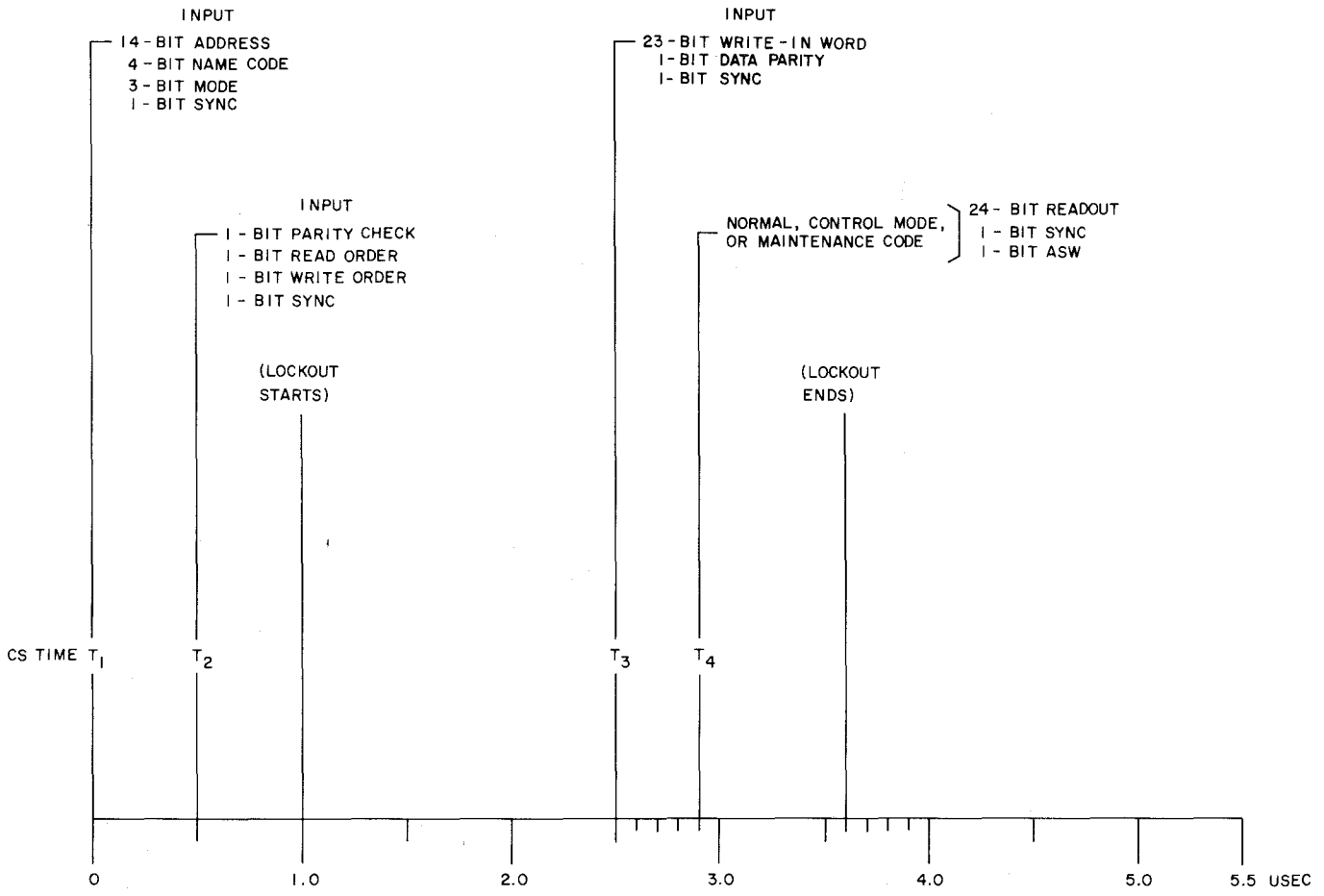


Fig. 22—Timing of Input-Output Signals

6.09 The CS outputs occur during time interval T_4 if the CS is operating in a normal, control, or maintenance mode. The CS produces the following outputs:

- A 24-bit readout word (ACS23-ACS00)
- A synchronizing signal (CCSYN)
- An all-seems-well signal (CSASW).

6.10 An ASW signal is generated if certain conditions have been properly satisfied during the execution of an operation. Some of these conditions are as follows.

- A valid order to read (R = 1, W = 0) or to write (R = 0, W = 1) has been received.
- A valid combination of mode signals has been received.
- A parity check on the address and name code has been successfully performed.
- The store has not detected a simultaneous multiple mode of operation.
- The store has not selected its F and V halves simultaneously.

6.11 The CSs are also connected to the master scanner, miscellaneous trunk, and central pulse distributor frames. The cables are completely wired to the CS frame, regardless of how many CS units are provided during the initial installation. If the leads are not all terminated on the master scanner, miscellaneous trunk, and central pulse distributor frames, then the unused leads are

identified and dressed to the frame uprights. When additional CS units are added, the corresponding leads can be identified and connected. For example, a signal distributor applique point is assigned to each CS unit. The signal distributor applique circuits are run to the CS frame in four separate switchboard cables. The cables are installer wired to the terminal strips which are located at the top right of bays 0 and 1 of CS frame 0 and bays 0 and 1 of CS frame 1 (Fig. 2). At the miscellaneous trunk frame if these leads are not terminated, the unused leads are identified and dressed to the miscellaneous trunk frame upright for future use.

6.12 Each CS unit requires ten scan points for monitoring and for detection purposes. These points are directly wired to the master scanner frame. Specific assignments are shown in Table H.

6.13 Each CS unit is connected to four bipolar central pulse distributor outputs shown in Table I. A positive pulse sets a flip-flop; a negative pulse resets it. Pulses on any of the central pulse distributor connections must be accompanied by a we-really-mean-it (WRMI) signal.

7. MISCELLANEOUS

FIXED AND VARIABLE NAME MATCH

7.01 The fixed and variable CS names for both the SP and CC are decoded as shown in Table J and Fig. 23. ⏵The CCCS name field (Table J) allows the use of ten 16K blocks fully duplicated. (See note.)⏴ There are two fully duplicated SPCS blocks available. Bits A11-A0 are used strictly for word selection. Bits A13 and A12 are used for both word selection and name decoding. Bits A17-A14 are used for name decoding and in conjunction with mode information. (Reference should be made to Part 5.) As shown in Table J, the all zeros condition in A17-A12 is an invalid CS address. Hence, the CS will not respond to this input set. The NAME 1 and NAME 2 address inputs are defined under NAME. Selection of NAME 1 and NAME 2 is under control of address bits A12 and A13. Internal CS circuitry defines NAME 2 as bits A13 and A12 equal to 0, and NAME 1 as the other three combinations. (This explains why the order of NAME 1 and NAME 2 is reversed in the SPCSs.)

TABLE H

SCAN POINT ASSIGNMENT

SCAN POINT (SC)	FUNCTION
0	Monitors power control relays.
1	Monitors the control panel NORMAL and OFF key.
2	Monitors the out-of-service lamp fuse.
3	Detects the completion of CS cycle.
4	When ITB is set, it inhibits CS communication via bus 1.
5	When OTB is set, it inhibits CS communication via bus 0.
6	CS receives from bus 1 when RO is reset (R).
7	CS receives from bus 0 when RO is set (S).
8	Monitors output of low level voltage monitoring circuit associated with the voltage regulator.
9	Detects a valid CS start.

TABLE I

CENTRAL PULSE DISTRIBUTOR OUTPUTS

OUTPUT	FUNCTION
TBL1P TBL1N	Used to set or reset bus 0 trouble flip-flop (0TB)
TBL0P TBL0N	Used to set or reset bus 1 trouble flip-flop (1TB)
ROP RON	Used to set or reset CS RO flip-flop which is used to select bus 0 and bus 1 in CS operation.
FLTP FLTN	Used to set or reset various internal CS control flip-flops as required. (For example, operate a relay used to test the crowbar switches located on the voltage regulators.)

▮***Note:*** The tenth 32KCS is available with 1E (B5, B6)6 and later generics.▮

7.02 The F141 lead, which is the most significant bit of the word select address, specifies the fixed (F141 high) or variable (F141 low) 16K word half of the memory. The fixed half of the memory may be obtained in the normal (N1) and maintenance fixed (MTFM1) modes. The variable half of memory may be obtained in the normal (N1) and maintenance variable (MTVM1) modes. The control mode is available only on fixed name matches and does not disturb the contents of the core memory.

GROWTH

7.03 Complete CS units are added to the frame as required to satisfy office requirements. A minimum of two units are required for initial installation. Additional units are added according to the fixed growth plan as shown in Fig. 23 and 24. The fixed growth plan is mandatory since the fixed name assignments are wired into the frame connector at each CS location. All CS units are, therefore, exactly identical. CS units associated with the SP must be equipped in the positions as shown in Fig. 24. Advantages of this fixed growth configuration are as follows.

(a) The two CS units containing copies of the same memory area are located in different equipment bays. This separation minimizes the susceptibility of the system to a failure which could occur as a result of mechanical damage.

(b) Power for each equipment bay is fused separately at the power distributor frame. Thus, this separation also would preserve the duplicated information in the event of a power failure to a bay.

(c) The CS units are equipped from the top of the frame down. Normally, additional units are not installed over active CS units.

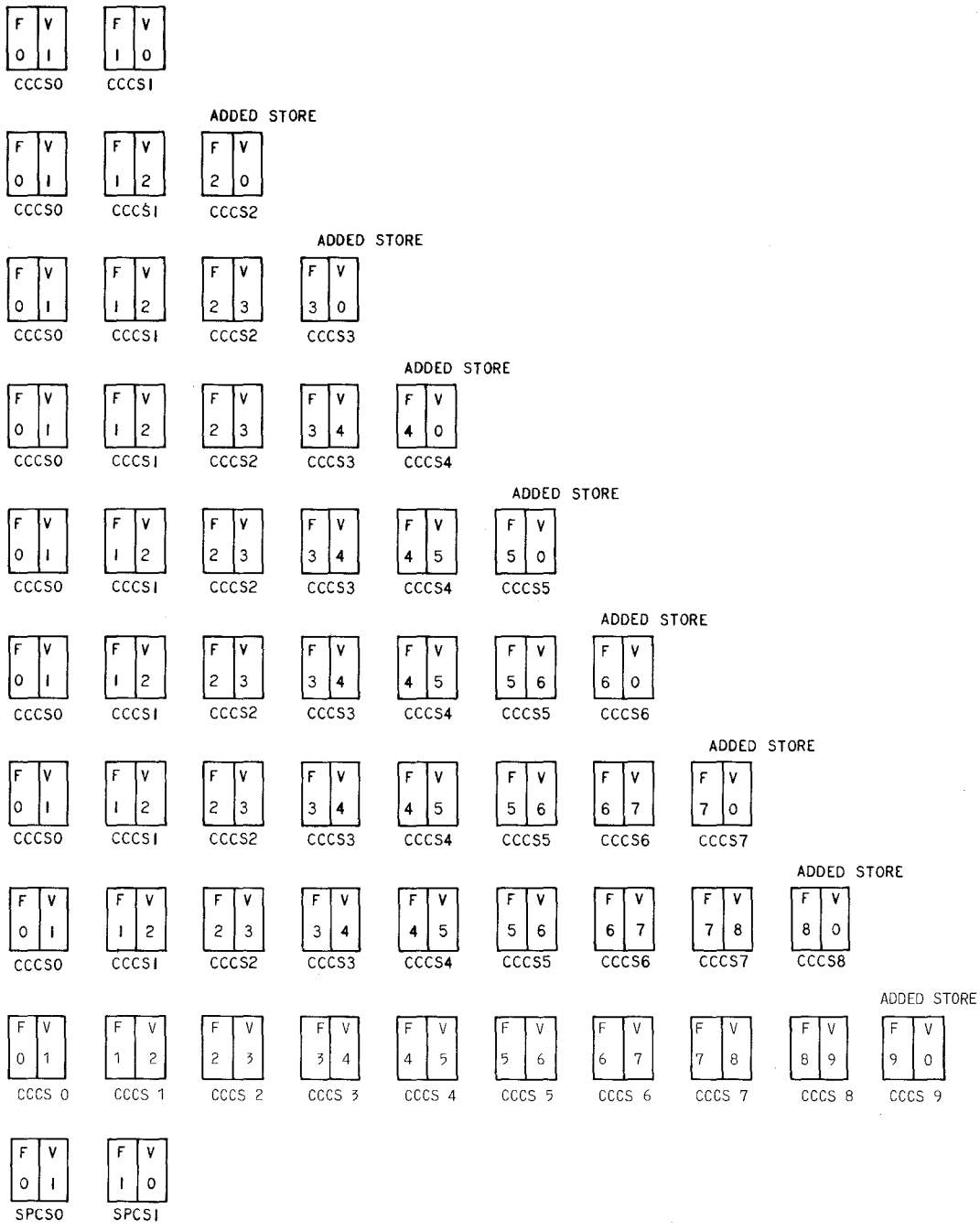
→TABLE J←

CALL STORE ADDRESS FIELD

	16K CS BLOCK	NAME	CS NAME (K CODE) A17	A16	A15	A14	ADDRESS A13	A12	A11-A0	ADDRESS RANGE IN OCTAL (A17-A0)
CCCS	NOT USED		0	0	0	0	0	0		----------
	0	1	0	0	0	0	0	1		10000-17777
		1	0	0	0	0	1	0		20000-27777
		1	0	0	0	0	1	1		30000-37777
		2	0	0	0	1	0	0		40000-47777
	1	1	0	0	0	1	0	1		50000-57777
		1	0	0	0	1	1	0		60000-67777
		1	0	0	0	1	1	1		70000-77777
		2	0	0	1	0	0	0		100000-107777
	2	1	0	0	1	0	0	1		110000-117777
		1	0	0	1	0	1	0		120000-127777
		1	0	0	1	0	1	1		130000-137777
		2	0	0	1	1	0	0		140000-147777
	3	1	0	0	1	1	0	1		150000-157777
		1	0	0	1	1	1	0		160000-167777
		1	0	0	1	1	1	1		170000-177777
		2	0	1	0	0	0	0		200000-207777
	4	1	0	1	0	0	0	1		210000-217777
		1	0	1	0	0	1	0	ADDRESS	220000-227777
		1	0	1	0	0	1	1		230000-237777
		2	0	1	0	1	0	0		240000-247777
	5	1	0	1	0	1	0	1		250000-257777
		1	0	1	0	1	1	0		260000-267777
		1	0	1	0	1	1	1		270000-277777
		2	0	1	1	0	0	0		300000-307777
	6	1	0	1	1	0	0	1		310000-317777
		1	0	1	1	0	1	0		320000-327777
		1	0	1	1	0	1	1		330000-337777
		2	0	1	1	1	0	0		340000-347777
	7	1	0	1	1	1	0	1		350000-357777
		1	0	1	1	1	1	0		360000-367777
		1	0	1	1	1	1	1		370000-377777
		2	1	0	0	0	0	0		400000-407777
	8	1	1	0	0	0	0	1		410000-417777
		1	1	0	0	0	1	0		420000-427777
		1	1	0	0	0	1	1		430000-437777
		2	1	0	0	1	0	0		440000-447777
	9	1	1	0	0	1	0	1		450000-457777
		1	1	0	0	1	1	0		460000-467777
		1	1	0	0	1	1	1		470000-477777
		2	1	1	0	0	0	0		600000-607777
SPCS	0	2	1	0	1	0	0	0		500000-507777
		1	1	0	1	0	0	1		510000-517777
		1	1	0	1	0	1	0		520000-527777
		1	1	0	1	0	1	1		530000-537777
	1	2	1	0	1	1	0	0	ADDRESS	540000-547777
		1	1	0	1	1	0	1		550000-557777
		1	1	0	1	1	1	0		560000-567777
		1	1	0	1	1	1	1		570000-577777

Note 1: Fig. 23 shows the duplicated information of each 16K CS block.

Note 2: CCCS 9 is available with 1E (B5, B6) 6 and later generic programs.



NOTE:
EACH NUMBERED BLOCK REPRESENTS A HALF STORE MEMORY BLOCK OF 16,384 (16K) 24-BIT WORDS. WHEN AN ADDITIONAL CALL STORE IS ADDED TO THE SYSTEM, ONLY THE INFORMATION IN THE V HALF OF THE LAST CALL STORE NEED BE CHANGED.

Fig. 23—Duplication of Information Contained in 32K Call Stores

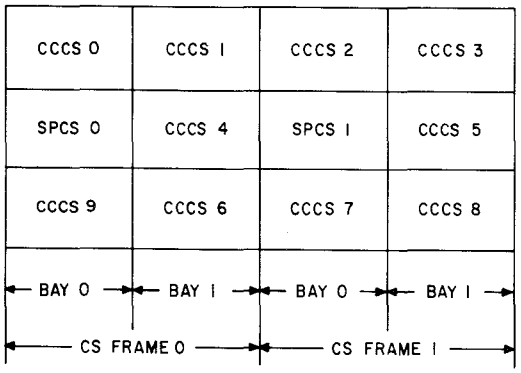


Fig. 24—32K Call Store Growth