ANALYZING AND LOCATING TROUBLE IN THE 32K CALL STORE NO. 1 ELECTRONIC SWITCHING SYSTEM

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1. GENERAL

1.01 The purpose of this section is to provide the maintenance personnel with trouble locating techniques available for the 32K call store (CS) used in 2 Wire No. 1 ESS. Most malfunctions in the 32K CS can be resolved by tactics suggested by this section.

1.02 This section is reissued for the following reasons

(a) To remove coverage for out of service generics

(b) To add coverage for the tenth 32K call store.

This reissue does not affect the Equipment Test List.

1.03 The CSs are erasable read-write temporary memories used by the central control (CC) and signal processor (SP). A block diagram of the 32K CS is shown in Fig. 1. The 32,768 word locations contained in a 20A memory module are divided into two information blocks known as the F-half and the V-half. Each store half has a 4-bit name code (K code). The F-half is assigned a fixed name code and the V-half is assigned a variable name code. The duplication of call store information is shown in Fig. 2.

1.04 A word location to be read out or written into is identified by the following information from the CC.

(a) A 4-bit name code (K code) specifies the store half containing the word location.

(b) A 14-bit address identifies one of the 16,384 word locations in the specified store half.

1.05 The word locations of the F- and V-half in any one CS have unique addresses. There is no restriction upon the sequence in which locations are addressed. A word location can be chosen without regard to previous selections. Access circuitry common to both F- and V-half includes

- Address register
- Readout detector circuits
- Current drivers
- Data registers
- Address detector.

1.06 Common abbreviations used in this section are as follows:

ASW	All seems well
CC	Central control
CR	Control read
CS	Call store
CW	Control write
OOS	Out of service
SP	Signal processor

2. REFERENCE DOCUMENTS

CD-1A290	32K Call Store Circuit Description
CD-4C002	20A Memory Module Circuit Description
CD-4C004	20B Memory Module Circuit Description
IM-1A001	Input Message Manual
OM-1A001	Output Message Manual
PD-1A018	Call Store Deferred Fault Recognition Program Description
PD-1A019-26	Diagnostic Program Description
PF-1A019	Program Flowchart
PK-1A019	32K Call Store Raw Data Analysis
PR-1A019-26	Call Store Diagnostics and Exercise
SD-1A290	32K Call Store Schematic Drawing
SD-4C002	20A Memory Schematic Drawing
SD-4C004	20B Memory Schematic Drawing
TLM-1A290	32K Call Store Trouble Locating Manual
231-025-101	32K Call Store Description
231-025-801	32K Call Store Replacement Procedures
231-105-302	Taking Equipment Out of Service—Procedures
231-109-301	Analyzing Maintenance Interrupts
231-117-301	OFF-LINE Operations

3. CALL STORE TROUBLESHOOTING OVERVIEW

3.01 The flowchart in Fig. 3 gives an overall indication of the types of CS troubles that can be encountered. It gives a logical approach to locating a fault and references a paragraph that

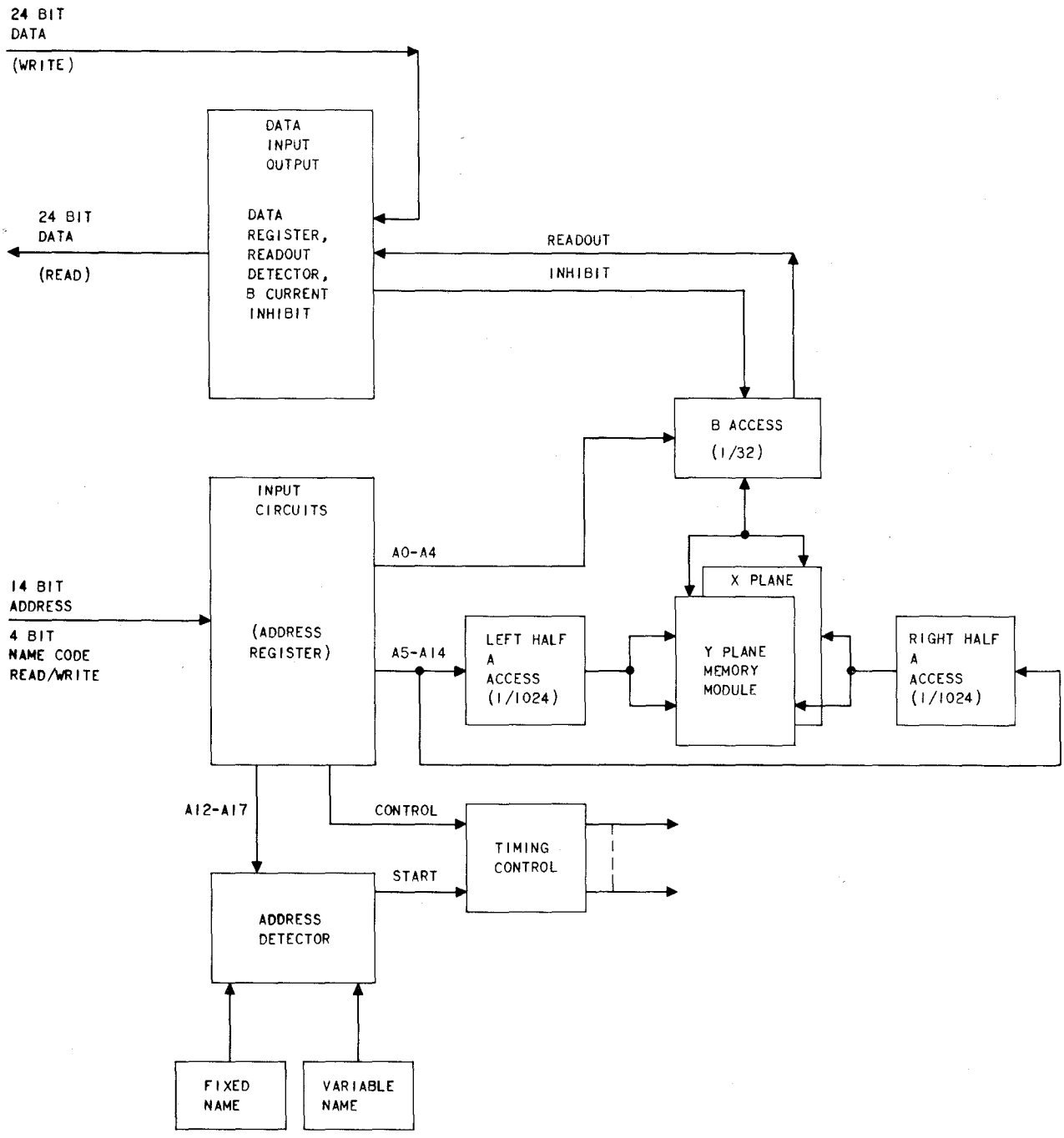


Fig. 1—32K Call Store Block Diagram

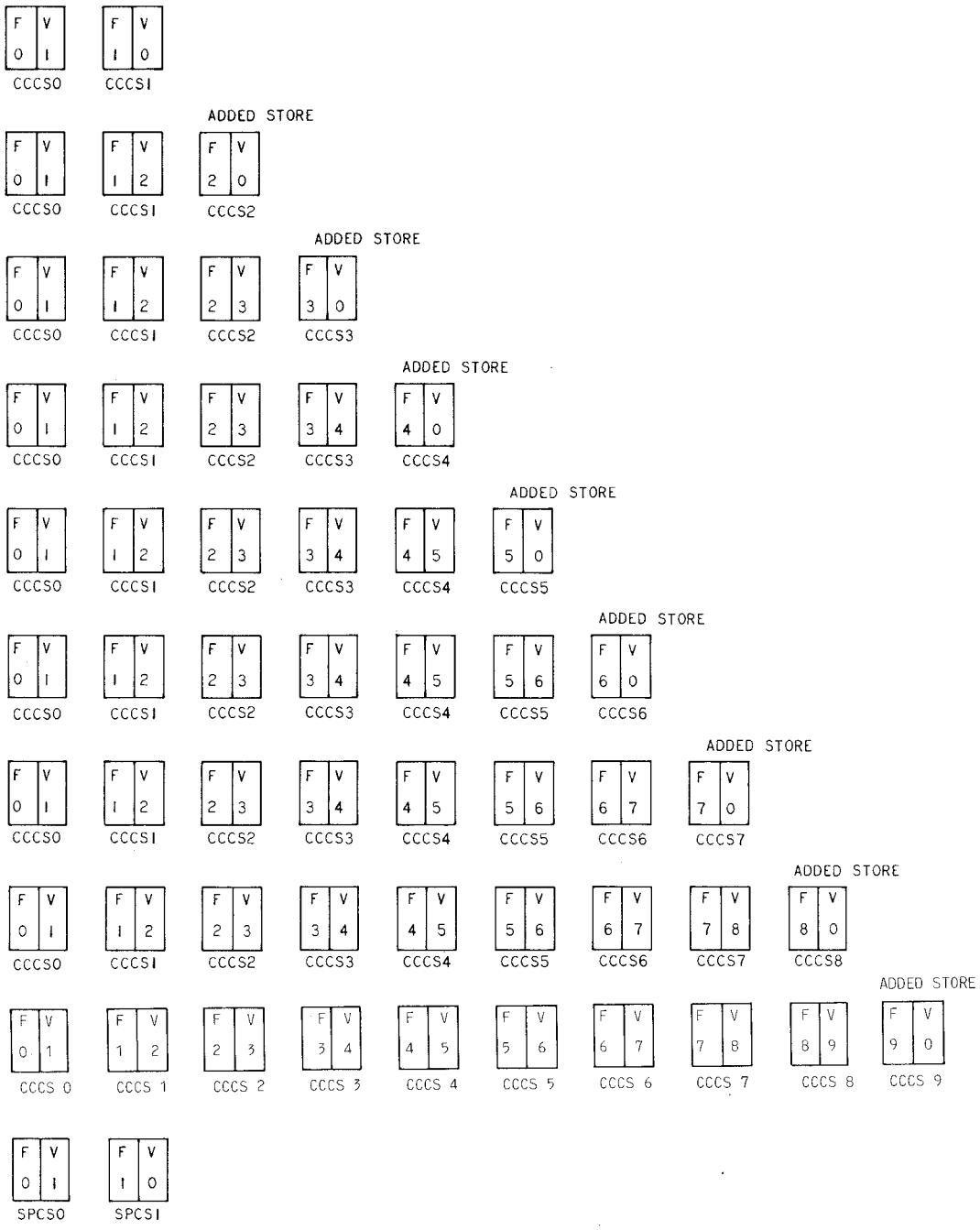
has a detailed procedure for locating that type of fault.

3.02 The flowchart is laid out on the basis of dealing with one type of trouble at a time.

4. DIAGNOSTIC FAILURES

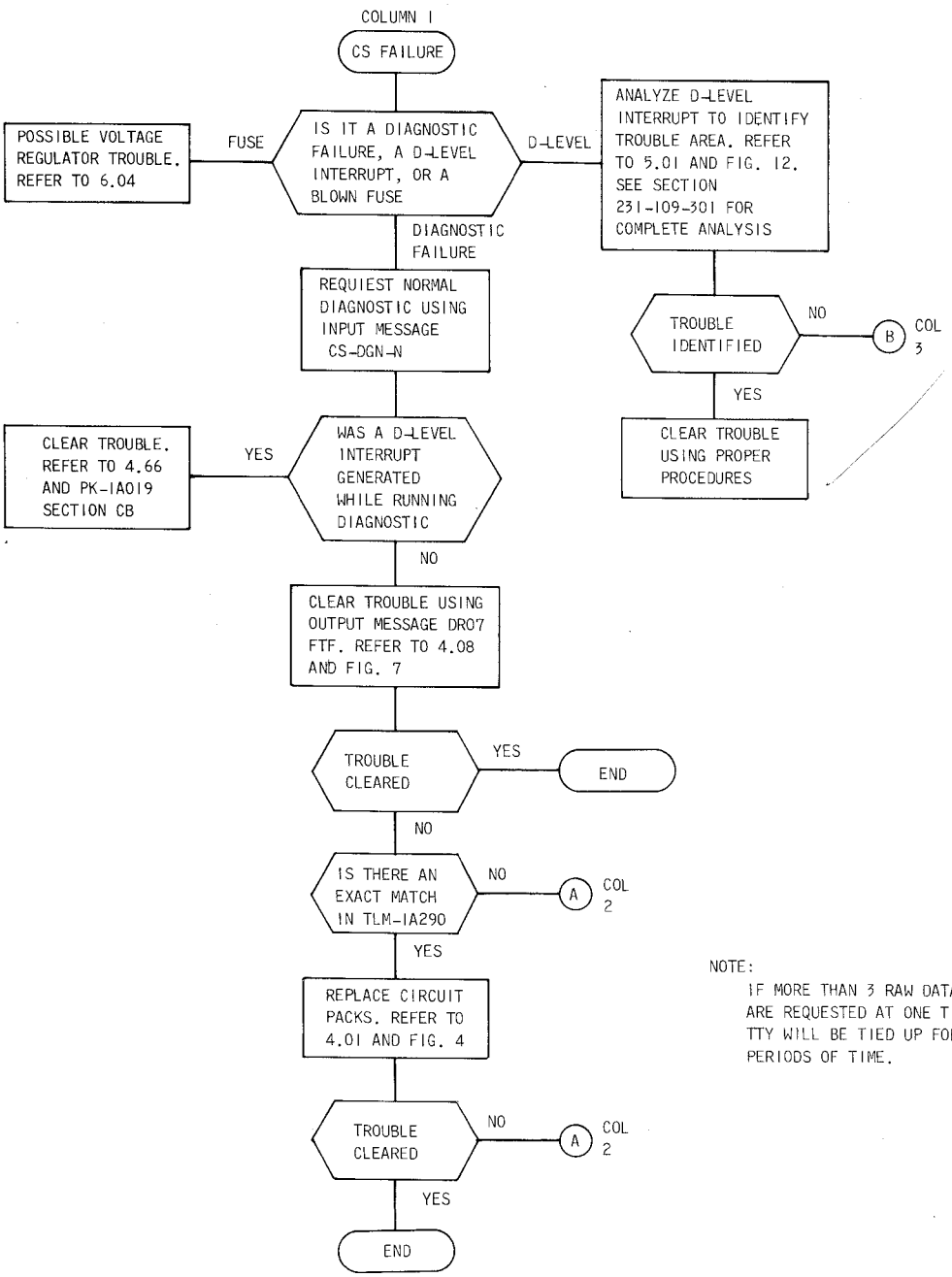
NORMAL DIAGNOSTIC FAILURE

4.01 When a fault arises, the system automatically performs a series of diagnostic tests on the



NOTE:
EACH NUMBERED BLOCK REPRESENTS A HALF STORE MEMORY BLOCK OF 16,384 (16K) 24-BIT WORDS. WHEN AN ADDITIONAL CALL STORE IS ADDED TO THE SYSTEM, ONLY THE INFORMATION IN THE V HALF OF THE LAST CALL STORE NEED BE CHANGED.

Fig. 2—Duplication of Information in 32K Call Stores



NOTE:
IF MORE THAN 3 RAW DATA FAILURES ARE REQUESTED AT ONE TIME, THE TTY WILL BE TIED UP FOR LONG PERIODS OF TIME.

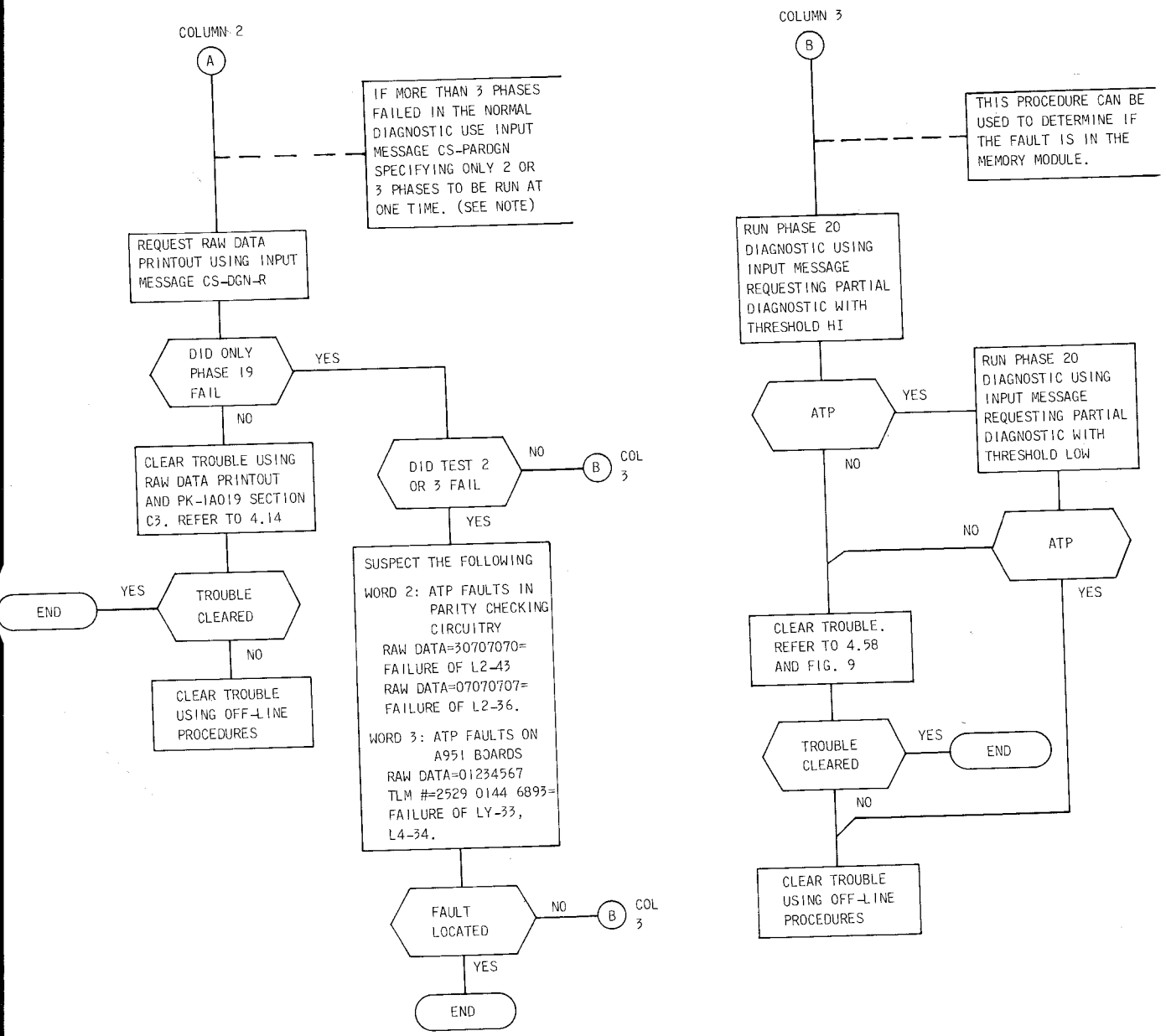
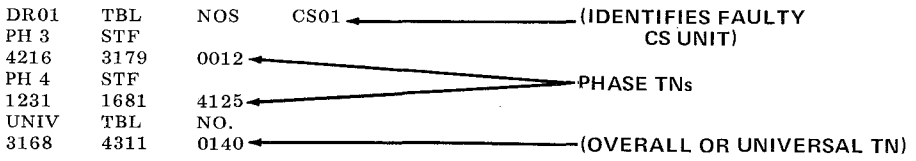


Fig. 3—General Trouble Locating Flowchart

call store. The results of the test are reported via a TTY DR01 output message. The DR01 message contains a 12-digit universal trouble number (TN) and one or more 12-digit phase TNs. A complete DR01 message is shown in the following example:



4.02 Request a second normal diagnostic by the TTY input message CS-DGN—(refer to IM-1A001 for complete input message) to insure that the trouble is a solid fault. Figure 4 gives a flowchart approach to locating faults in a CS.

4.03 Using TLM-1A290 Section D, locate the exact match of the universal TN. The corresponding specific circuit pack, if faulty, could yield the universal TN. The circuit packs are listed in order of the most likely to cause the fault. Always replace circuit packs from the top of the list first, one at a time.

4.04 Should the universal TN fail to pinpoint the fault, locate as many of the phase TNs as possible in Section G of TLM-1A290. Prepare a list containing all circuit packs associated with phase numbers in such a way that the packs appearing more frequently are on top of the list and those occurring less frequently are at the bottom of the list. Replace circuit packs one at a time, starting at the top of the list. The phase TNs are supplied as a secondary means of diagnosing faults and should only be used in the case where the universal TN cannot be located in the TLM, or where the universal TN does not locate the fault.

4.05 Two universal TNs will be produced by the system if the fault is bus dependent or if one of the duplicate buses is out of service. Usually, but not necessarily, only one of the TNs will yield an exact TLM match. Use the matching TN to locate the fault.

4.06 The TLM will show the circuit packs associated with a TN and the circuit pack location in the CS. Figure 5 shows the circuit pack location in the CS.

4.07 Equipment locations associated with TNs of relays and frame control pushbuttons are approximate equipment locations of the hardware within the frame. The unique identity of the particular hardware is given in Table A.

TABLE A

TLM NON-CIRCUIT PACK LOCATIONS

TLM EQUIPMENT CODE	HARDWARE IDENTITY
R00001	Relay R1
R00002	Relay R2
R00003	Relay PA
R00004	Relay MON2
R00005	Relay MON1
R00006	Relay PON2
S00011	Switch ST
S00012	Switch NOR
S00013	Switch REQ INH
S00014	Switch OFF

FIRST TEST FAILURE (FTF)

4.08 The first test failure (FTF) pattern or the first failing word in the raw data is an alternative to using the regular phase and exact match trouble numbers (TNs) in TLM-1A290. The FTF interpretation process is similar to regular raw data analysis approach except that, in this case, only the first failing raw data word is examined. The basic theory behind the use of the FTF pattern is as follows.

While a large number of faults may cause a particular single word failure pattern, only a smaller subset of these faults will cause this particular single word failure to be the first failing word. Moreover, an even smaller subset of these same faults will fail a specific number of times within the first failing phase.

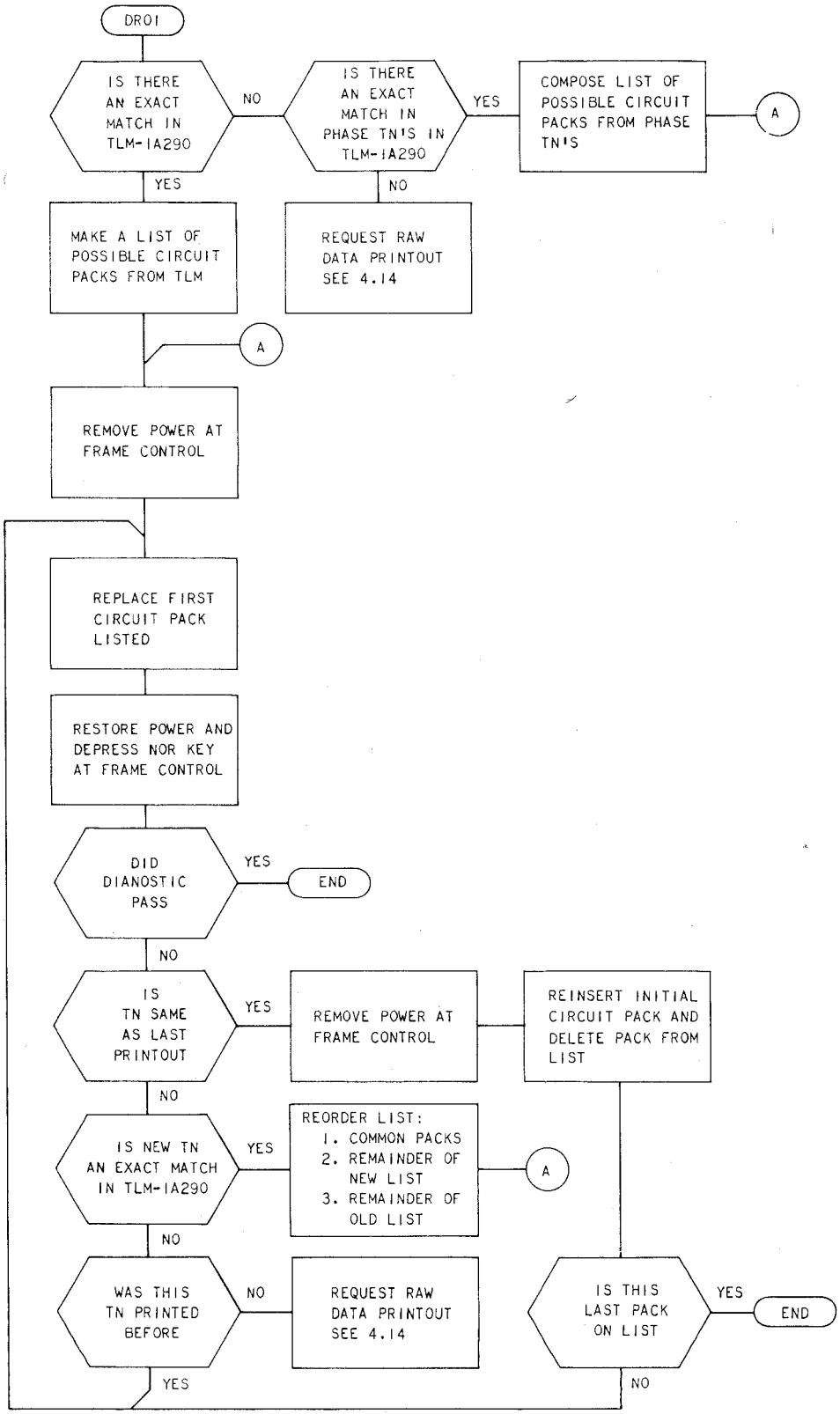


Fig. 4—Normal Diagnostic Trouble Locating Flowchart

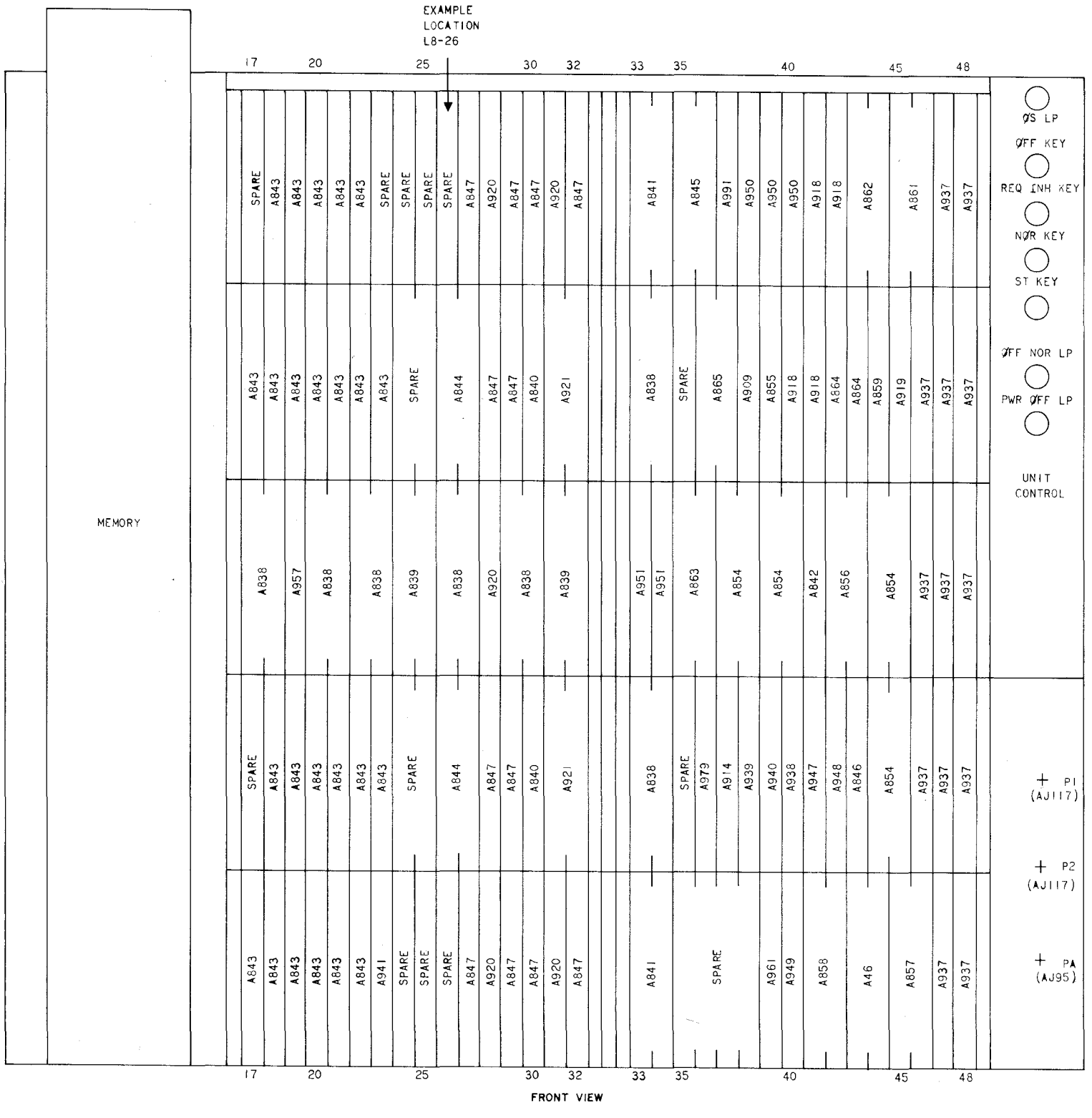


Fig. 5—Call Store Circuit Pack Location

4.09 The FTF pattern will be printed by the TTY immediately following a failing CS diagnosis. This applies to all forms of CS diagnostic request, whether system requested or manually requested. A typical FTF printout is given in Fig. 6.

4.10 The first step in interpreting the FTF pattern is to locate the proper first failing phase and first failing test word in the FTF TLM located in PK-1A019, Section C2. The test word number is referenced to the first raw data word (word No. 1) in the phase.

4.11 The maintenance personnel then find the failure pattern listed for the given phase and word number which matches that printed by the TTY. If more than one circuit pack is listed for the failure patterns, subdivide the circuit pack by using the number of failing raw data words (detections) for the phase. The circuit packs are listed (in descending order) according to the number of faults within each pack which may cause the failure pattern. Replace the packs that contain the highest number of faults first; these will be the packs which most likely contain the fault. A flowchart approach for FTF trouble shooting is given in Fig. 7.

4.12 In some cases, a near match in the number of failing words within the first failing phase or the first failing test word number will also locate the faulty circuit pack. However, one should not dwell too long in this area before proceeding to the raw data analysis given in PK-1A019 Section 3. If an excessive number of circuit packs are implicated by using the FTF pattern in the FTF TLM, proceed to the regular raw data analysis in Section 3 of PK-1A019.

4.13 If two FTF TLMs are listed, the first is to be consulted if CS bus 0 is the active bus (bus 1 can be standby or out of service). The second is to be consulted if CS bus 0 is out of service. If one universal trouble number is printed, both buses are in service and the first TLM is always used. If two universal TNs are printed (indicating that a bus is out of service), one can determine which bus is active from the FTF printout.

RAW DIAGNOSTIC FAILURE

4.14 There are 22 test phases in the CS diagnostic. The first 19 are run automatically (if there are no failures) whenever a diagnosis is requested. The special test phases, 20 through 22, can be run only by manually requesting a partial diagnostic, specifying the phase to be run (refer to IM-1A001 for complete input message). Do not request more than one of these phases (20 through 22) at a time.

4.15 Bus associated phases will automatically be skipped for all diagnostic requests if a bus is out of service (OOS). The bus configuration requirement for each phase is given in Table B.

4.16 There are three possible termination points during a CS diagnosis; after phase 1 if phase 1 fails, after phase 16 (or 15 if bus 1 is

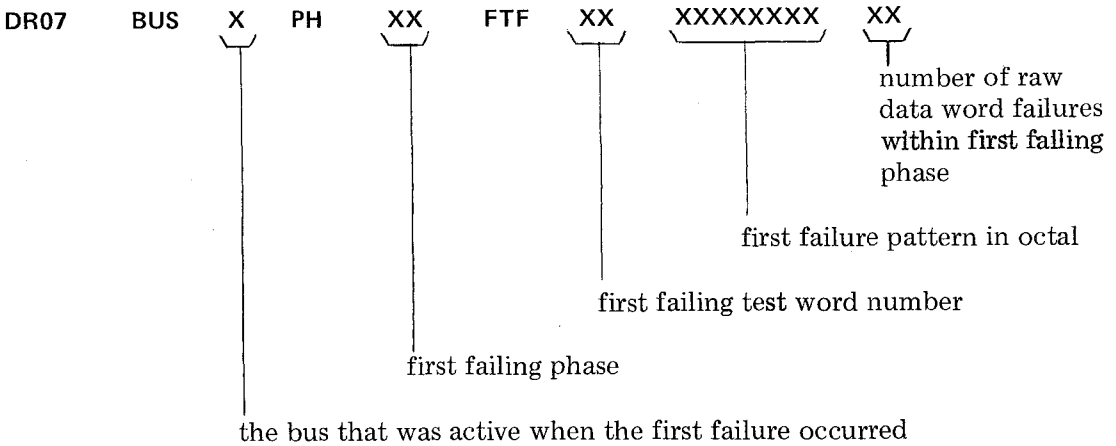


Fig. 6—First Test Failure (FTF) Printout

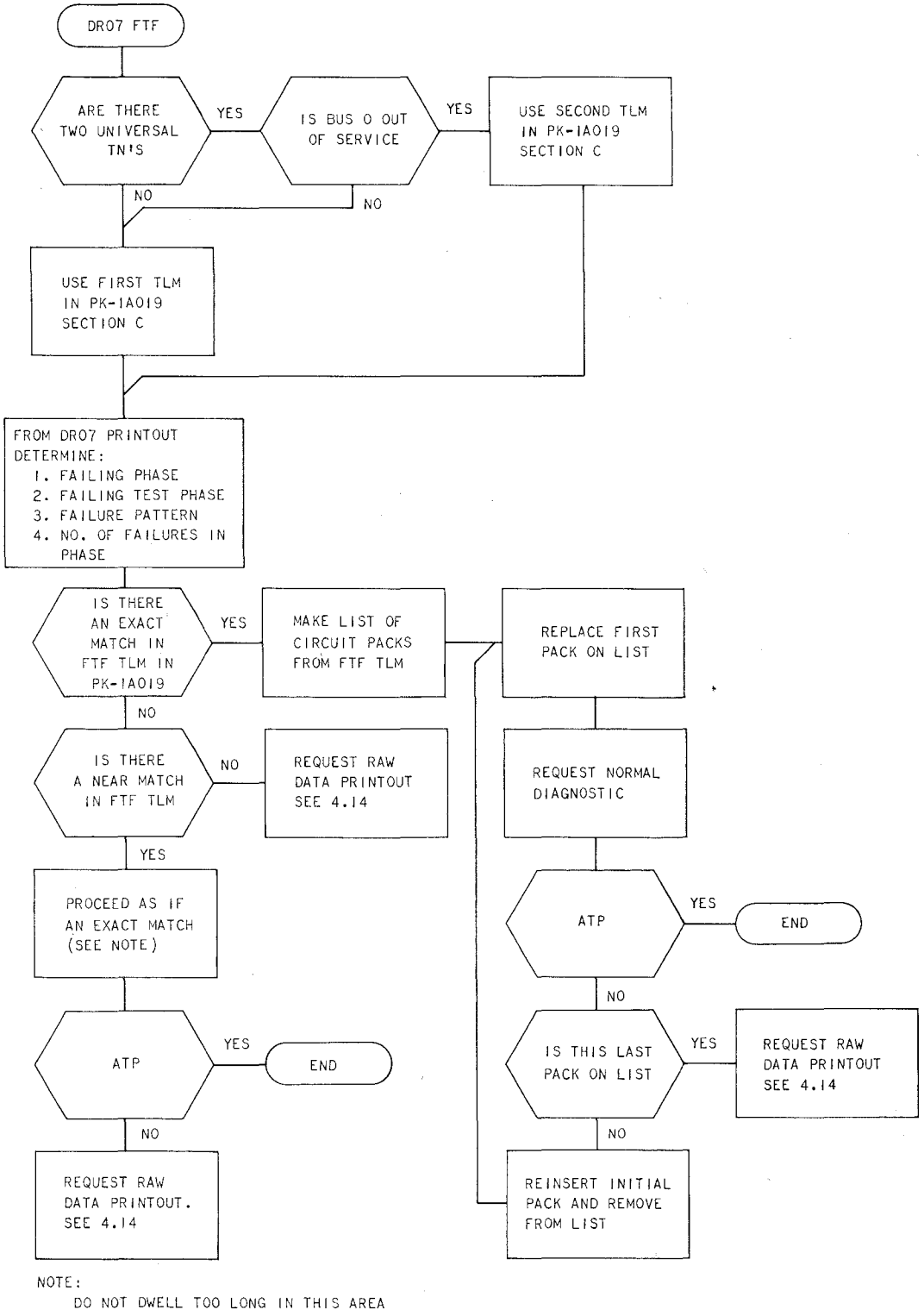


Fig. 7—FTF Trouble Locating Flowchart

TABLE B

BUS CONFIGURATION FOR PHASES 1 THROUGH 18

PHASE NO.	BUS REQUIREMENT
1	Active Bus
2	Bus 0 active, bus 1 standby or out of service (OOS)
3	Bus 1 active, bus 0 standby or OOS
4—10	Active bus
11	Bus 0 active, bus 1 standby or OOS
12	Bus active, bus 0 standby or OOS
13—14	Active bus
15	Bus 0 active, bus 1 standby or OOS
16	Bus 1 active, bus 0 standby or OOS
17	Bus 0 active, bus 1 standby (both available)
18	Bus 1 active, bus 0 standby (both available)

OOS) if one or more failures occur in phases 2 through 16, and after phase 19 if all tests pass (ATP) in phases 1 through 16. Early termination is not employed for a partial diagnosis request. All requested phases are run except for cases where a bus is OOS.

4.17 A special note of caution should be added in regard to the input message requesting raw data. Before rquesting a raw data printout, request a normal diagnostic. From the DR01 printout, determine which, and how many, test phases are failing. If more than three phases have failed, only three phases should be requested at a time. Use the input message to request a partial diagnostic, specifying the phases to be run. If data for more than three phases is printed at one time, the TTY will be tied up for an undesirable length of time. If for some reason a long raw data printout is initiated, the diagnostic can be terminated with the following input message:

ZIP-CLIENT-9.

PHASE 1

4.18 This phase is used to test the power scan ferrods to verify that the ferrods are saturated. Then the lamp fuse and low limit voltage monitor scan ferrods are checked to see if they are saturated. Finally, the TBL0, TBL1, and RO flip-flops are exercised through the use of CPD operations and the ferrods are scanned.

4.19 This phase is run on the active bus. Table C gives the test run in phase 1. If phase 1 fails, the diagnosis will be terminated.

PHASE 2

4.20 This phase contains tests that detect faults which are sensitive to Bus 0. All tests in this phase are run using CS Bus 0. Bus sensitive faults in the following CS circuits are detected:

- Address register (FS1)
- Sync input circuits (FS2)
- Data input circuits (FS6)
- Data output circuits (FS6)
- Data output control circuits (FS2).

4.21 If CS Bus 0 is out of service, this phase will be skipped. The FTF DR07 message

TABLE C

TEST RUN IN PHASE 1

TEST NO.	TEST RUN
1	Scan the power ferrods (SC0 and SC1) and check for saturation.
2	Test lamp fuse and low limit voltage monitor ferrods (SC2 and SC8) both ferrods should be saturated.
3 and 4	Exercise TBL0, TBL1, and RO FFs (SC4, SC5, SC6, and SC7). FFs are set/reset via CPD pulses and FF states are determined by scanning the associated ferrods.

will be printed twice. Use the second DR07 message for locating a fault.

PHASE 3

4.22 This phase contains 12 tests that detect faults which are sensitive to CS Bus 1. All tests in this phase are run using CS Bus 1. This phase is the same as phase 2 except that Bus 1 is the active bus. Bus-sensitive faults in the following CS circuits are detected:

- Address register (FS1)
- Sync input circuits (FS2)
- Data input circuits (FS6)
- Data output circuits (FS6)
- Data output control circuits (FS2).

4.23 If CS Bus 1 is out of service, this phase will be skipped. The FTF DR07 message will be printed twice. Use the first DR07 message for locating fault.

PHASE 4

4.24 This phase contains 7 tests that detect faults in the following circuits:

- CPD WRMI circuits (FS2)
- Address register (FS1)
- Fixed name address detector (FS4)
- Parity circuit (FS3)
- Data register (FS6).

4.25 The test in this phase is run on the active bus.

PHASE 5

4.26 In this phase, various points in the timing circuit (FS2) are monitored during the CS cycle. These points are monitored by performing a series of snap-shot operations. The snap-shot function is performed via the CRWMODE (NBTA) macro call and is performed once for each state of the odd and even binary counters. The circuit points monitored by the NBTA(10)B functions are examined in this phase. Refer to SD-1A290 D sheets for the NBTA data layout.

4.27 The 31 tests in this phase are run on the active bus. For tests 1 through 15, the sequence of CS orders, the NBTA(10)B monitor points are examined for each state of the even binary counters (0000 through 1110). Bit 5 in the address is equal to zero. This affects the monitor points ANG1 and APG1. For tests 16 through 31, the monitor points are examined for each state of the odd binary counters (0000 through 1111). Bit 5 in the address is equal to zero. This affects the monitor points ANG1 and APG1.

PHASE 6

4.28 In this phase, various points in the timing circuits (FS2) are monitored during the CS cycle. These points are monitored by performing a series of snap-shot operations. The snap-shot function is performed via the CRWMODE (NBTA) macro call and is performed for eleven states of the even binary counters. The circuit points monitored by the NBTA(10)B function are examined in this phase. Refer to SD-1A290 D sheets for the NBTA data layout.

4.29 This phase uses the presently active bus for testing. During this sequence (tests 1 through 10) of CS orders, the NBTA(10)B monitor points are examined for eleven states of the even binary counter (0010 through 1011). Bit 5 in the address is equal to one. This affects the monitor points ANG1 and APG1.

PHASE 7

4.30 In this phase, various points in the timing circuit (FS2) are monitored during the call store cycle. These points are monitored by performing a series of snap-shot operations. The snap-shot function is performed via the CRWMODE (NBTA) macro call and is performed once for each state of the even and odd binary counters. The circuit points monitored by the NBTA(10)D function are examined in this phase. Refer to SD-1A290 D sheets for the NBTA data layout.

4.31 These tests are run on the presently active bus. During tests 1 through 15 the NBTA(10)D monitor points are examined for each state of the even binary counter (0000 through 1110). During tests 16 through 31 the NBTA(10)D monitor points are examined for each state of the odd binary counter (0000 through 1111).

PHASE 8

4.32 This phase contains tests that detect faults in the variable name detector (FS4). The first four tests check the variable name registers to show that they can be set and reset properly. The next four tests verify the acceptance by the variable name detector of legal variable names. The remaining tests check for the rejection of various variable names.

4.33 The 34 tests of this phase are run on the presently active bus. A list of tests run in this phase is given in Table D.

TABLE D

TEST RUN IN PHASE 8

TEST NO.	TEST RUN
1 to 4	Exercise both variable name registers.
5 to 8	Check the variable name detector for acceptance of various legal variable names. Verify by scanning ferrod associated with VGO FF.
9 to 24	Check variable name detector for rejection of illegal variable names.
25 and 26	Check rejection of maintenance mode orders. The VGO ferrod should be saturated.
27 to 32	Check the all zero K code inhibit circuit (AZ0 and 0 1231 leads) in the name detector.
33 and 34	Check the inhibit start (I start) detector by causing a simultaneous fixed and variable name match.

PHASE 9

4.34 The first 8 tests in this phase test the call store parity check circuit (FS3). Variable names are used in these tests. These tests check the parity circuit by alternately performing a normal mode write with inverted parity (even) and a normal mode read with normal parity (odd). The response from the parity check circuit is determined by control reading the contents of the PF1 FF. Each test consists of 4 steps.

- Set the variable name registers A and B to specified names
- Clear the PF1 FF with NBTB(10) order
- Perform the test order (even or odd parity) using a test address
- Control reads the contents of the PF1 FF.

4.35 The next 16 tests check the store access circuitry (FS7 through FS16) through the eight access error flipflops (FS5). These tests check the store access circuits via the eight access error FFs (WATV, ARL, ARB, ATH, RATV, BRL, BRB, RBD and WBO). Each test consists of a normal mode read at a specific address, followed by an NBTB order to read the contents of the error flipflops. The access error FFs are automatically cleared by each preceeding test. The NBTB instruction clears the error FFs after reading these contents.

4.36 The next two tests check the eight access error FFs and the operational amplifiers in the access comparison circuit.

4.37 The next two tests check the sending FFs (VS1, VS0, FS1, and FS0) by setting and resetting the FFs.

4.38 If phase 9 fails, a checkerboard test can be used to help locate the fault.

PHASE 10

4.39 The tests in this phase are directed at the following points in the CS:

- Voltage monitor and crowbar circuits (FS17)
- Maintenance and control mode decoder circuits (FS2)
- ASW suppression circuits for CR(11) and CW(11) (FS2)
- Circuits that automatically reset FFs when power is removed (FS2 and FS5)
- Access window test circuit (FS16)
- MTC and FRH FFs (FS5).

4.40 The 27 tests in this phase are run on the active bus. A list of tests run in this phase is given in Table E.

PHASE 11

4.41 The tests in this phase are designed to detect faults that are sensitive to CS Bus 0, in the CS input-output circuits. The first 5 tests check the input sync control logic (sync 1, sync 2, and data sync in FS2). The next 12 tests check the CS output control logic (ODZ1) in FS2. The last 9 tests check the sync enable inputs (1AZ1 and 1AZ2) in the address register (FS1).

4.42 The 26 tests in this phase are run on CC-CS Bus 0 or SP-CS Bus 0.

PHASE 12

4.43 The tests in this phase are designed to detect faults that are sensitive to Bus 1 in the CS input-output circuits. The first 5 tests check the input sync control logic (sync 1, sync 2, the data sync in FS2). The next 12 tests check the CS output control logic (OD01) in FS2. The last 9 tests check the sync enable input (IA01 and IA02) in the address register (FS1).

4.44 The 26 tests in this phase are run on CC-CS Bus 1 or SP-CS Bus 1.

PHASE 13

4.45 The tests in this phase are designed to locate faults in the following circuitry:

- Circuits which automatically reset FFs when power is removed (FS2 and FS5)

TABLE E

TEST RUN IN PHASE 10

TEST NO.	TEST RUN
1 to 4	Check the voltage level monitor and crowbar circuit. The four voltage monitor points (3NLO, 12PLO, and 12NLO) are checked.
5 to 8	Check response of CS to various illegal control mode orders.
9 to 13	Check ASW inhibit circuits for the CR(11) and CW(11) control mode orders (FS3).
14 to 17	Check the automatic reset functions that are activated when power is removed from CS via the frame control keys.
18	Test that sending FFs can be reset by the RESOC line.
19	Verify that a NBTB order resets the 8 access error FFs.
20 to 23	Check access window test circuits (FS16).
24 to 27	Check the following FFs: F, R, H, and MTC (FS5).

- Points in timing circuit (FS2) monitored by NBTA(10)C (The layout of NBTA is located in SD-1A290 D sheets.)
- Access strobes STBBP and STBAP (FS16)
- END FF (FS5)
- Access via the eight access error FFs.

4.46 The 32 tests in this phase are run on the active bus.

PHASE 14

4.47 This phase is a collection of miscellaneous tests aimed at faults within the maintenance circuits (FS5). Various off-normal operations are executed (ie, FRH FF set in undefined states). While these tests are aimed at maintenance circuitry a small sampling of faults in other FSs will be detected. The 23 tests of this phase are run on the active CS bus.

PHASE 15

4.48 This phase contains tests that detect faults sensitive to bus 0. All tests in this phase are run on call store communication bus 0. Bus-sensitive faults in the following call store circuits are detected:

- Sync 1 input to bits 13-0 in the address registers (FS1)
- All-seems-well cable driver (FS2)
- Data output control circuit (FS2)
- BTF flip-flop (FS2)
- Timing circuit (FS2).

4.49 The 10 tests of this phase are run on CS Bus 0. A list of tests run in this phase is given in Table F.

PHASE 16

4.50 This phase contains tests which detect faults sensitive to Bus 1. All tests in this phase are run on call store communication Bus 1. Bus sensitive faults in the following call store circuits are detected:

- Sync 1 input to bits 13-0 in the address register (FS1)

TABLE F

TEST RUN IN PHASE 15

TEST NO.	TEST RUN
1	Verify that the lower portion of the address (bits 13 through 0) cannot enter the address register in CS(1) with SYNC 1 suppressed.
2 and 3	Check the All-Seems-Well circuits in the CS(1).
4 and 5	Check the data output control circuit.
6 and 8	Check the BTF FF in FS2.
9 and 10	Test for faults in the Sync input circuits (FS2).

- All-seems-well cable driver (FS2)
- Data output control, control circuit (FS2)
- BTF flip-flop (FS2)
- Timing circuit (FS2).

4.51 The 10 tests in this phase are the same as phase 15 except the tests are run on CS Bus 1. A list of tests run in this phase is given in Table F.

PHASE 17

4.52 This phase contains tests which detect faults sensitive to Bus 0. All tests in this phase are run with call store Bus 0 active. Both buses, however, are needed for these tests. If one bus is out of service this phase will be skipped. Bus sensitive faults in the data output decoder (FS2) are detected in this phase.

4.53 The 11 tests of this phase are run on CS Bus 0. A list of tests run is given in Table G.

PHASE 18

4.54 This phase contains tests which detect faults sensitive to Bus 1. All tests in this phase are run with call store bus 1 active. Both buses, however, are needed for these tests. If one bus is out of service this phase will be skipped. Bus sensitive faults in the data output decoder (FS2) are detected in this phase.

4.55 The 11 tests of this phase are the same as phase 17 except that Bus 1 is the active bus. A list of tests run is given in Table G.

PHASE 19

4.56 Phase 19 is a memory access test of 512 test addresses using a checkerboard. This phase serves only to keep the call store out of service if a memory failure is present that is not detected in an earlier phase. The all ones row data word —O.37777777 is only used as a failure indicator. At this point, the pack listed in TLM-1A290 ***should not be changed.*** Checkerboard tests should be performed and the results analyzed to determine the cause of the failure.

4.57 A new test three in phase 19 has been included to detect ALL-TEST-PASS faults on the A951 circuit boards L4-33 and L4-34 (SD-1A290 FS-1). These faults generally consist of one or more stuck bits on the A951 board. These circuits are connected beyond the address parity checking circuit. Therefore, the stuck bits will cause the store to access memory improperly, but will not cause any maintenance circuitry checks to fail. A failure of test three of phase 19 will output a constant raw data word 01234567 and the trouble number of 2529-0144-6893. The A951 circuit boards at location L4-33 and L4-34 should be suspected.

TABLE G

TEST RUN IN PHASE 17

TEST NO.	TEST RUN
1 to 3	Verify that the RO FF properly determines the bus over which data is outputted.
4	Verify that TBL0 (or TBL1 with Bus 1 active) can inhibit the CS under test from outputting over the active bus.
5	Test the data register reset RDRO.
6 to 8	Test the response from the CS for maintenance and normal mode orders with senders set.
9 to 11	Test the response from the CS for maintenance and normal mode orders with senders set.

CHECKERBOARD TEST

4.58 When phases 20 and 21 tests are requested, only one test should be requested at a time. If both checkerboard tests are requested at the same time, only phase 20 will be run.

PHASE 20

4.59 The checkerboard test is required via the following TTY input message:

CS-PARDGN-02000000RCSII

where: R = Raw data printout

A = SP community

C = CC community

S = CS

II = CS member number (See IM-1A001).

4.60 A typical printout for a checkerboard test failure is as follows:

	58 CS03	CHKBD CC 1	
	20000000	00001000	
CS FAILING	20100001	00004000	FAILING DATA
ADDRESS	20000001	00004200	
	20000002	00000040	
BIT 15 = 1	20100003	00001040	
F-HALF OF	20000003	00001000	
STORE	20100005	10000040	
	20000005	00001000	
	20100006	00000040	

4.61 The left column contains the failing CS addresses. It should be noted that if address bit 15 is set, the failure occurred in the F-half of the store; otherwise, the failure is in the V-half. The right column contains the octal representation of the failing data word. This octal number should be converted to binary. Any bit containing a binary 1 is a failing bit. An all 1-data word failure (—O.37777777) indicates a data parity failure (bit 23). The checkerboard failure printout will provide up to 18 failing addresses.

4.62 To determine if the memory module is defective, the spare bit can be used. If it is determined that a single bit failure is not due to a data channel circuit pack (A843), the following test should be performed to determine if the fault

is in the module. Swap the BD connector containing the failing data bit on the back of the module with the adjacent BD connector (to the immediate right or left). Figure 8 shows the BD connector locations. The data bits and their respective connectors are given below:

DATA BITS	CONNECTOR
Parity, 22	BD14
21, 20	BD13
19, 18	BD12
17, 16	BD11
15, 14	BD10
13, 12	BD09
11, 10	BD05
9, 8	BD04
7, 6	BD03
5, 4	BD02
3, 2	BD01
1, 0	BD00

4.63 If the data failure pattern changes to a new bit location, the module is defective. The trouble can be cleared by returning the BD connectors to their proper locations. Then connect the BD connector containing the original data bit failure to the spare position, BD08 on the module (if it is not defective or already being used). If the connector will not reach the spare position, it can be moved by moving the intervening connectors toward the spare position. For example, if connector BD00 must be moved to the spare position, move the connector at position BD05 to position BD08, BD02 to BD05 and BD00 to BD02 (Fig. 8).

Note: This is a temporary fix. The module should be replaced as soon as possible.

4.64 A flowchart procedure for locating faults with the checkerboard test is given in Fig. 9. Other troubleshooting aids are Table H and Fig. 10 and 11.

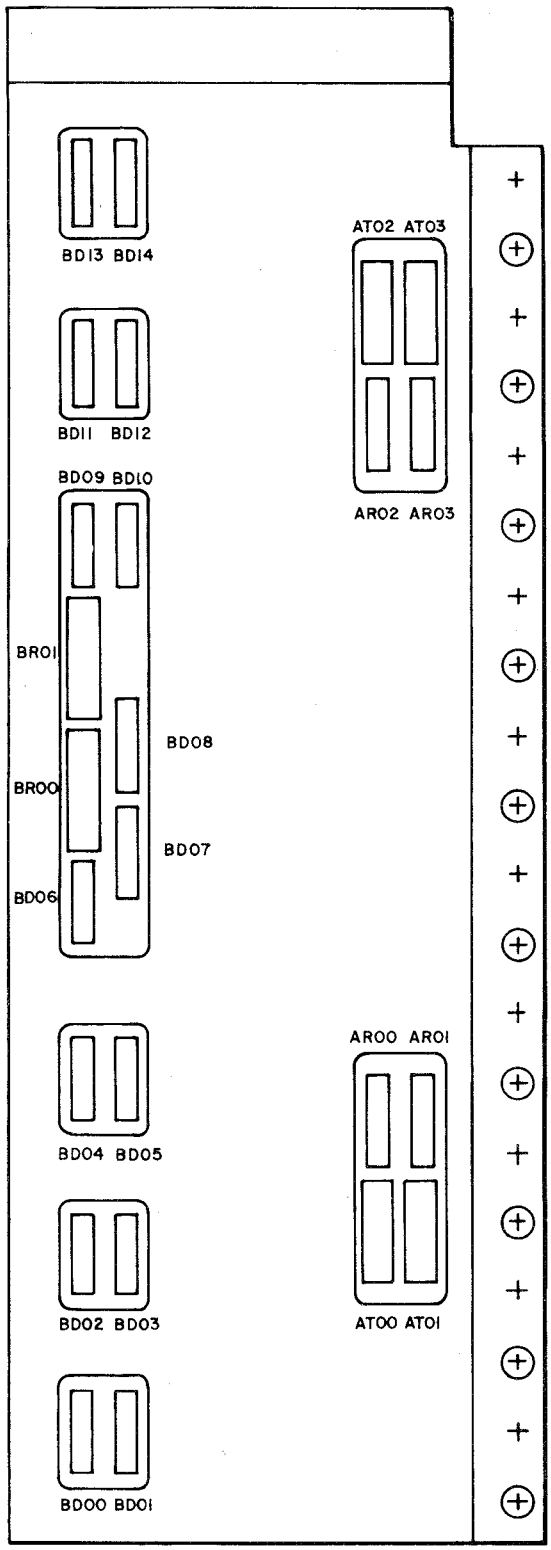
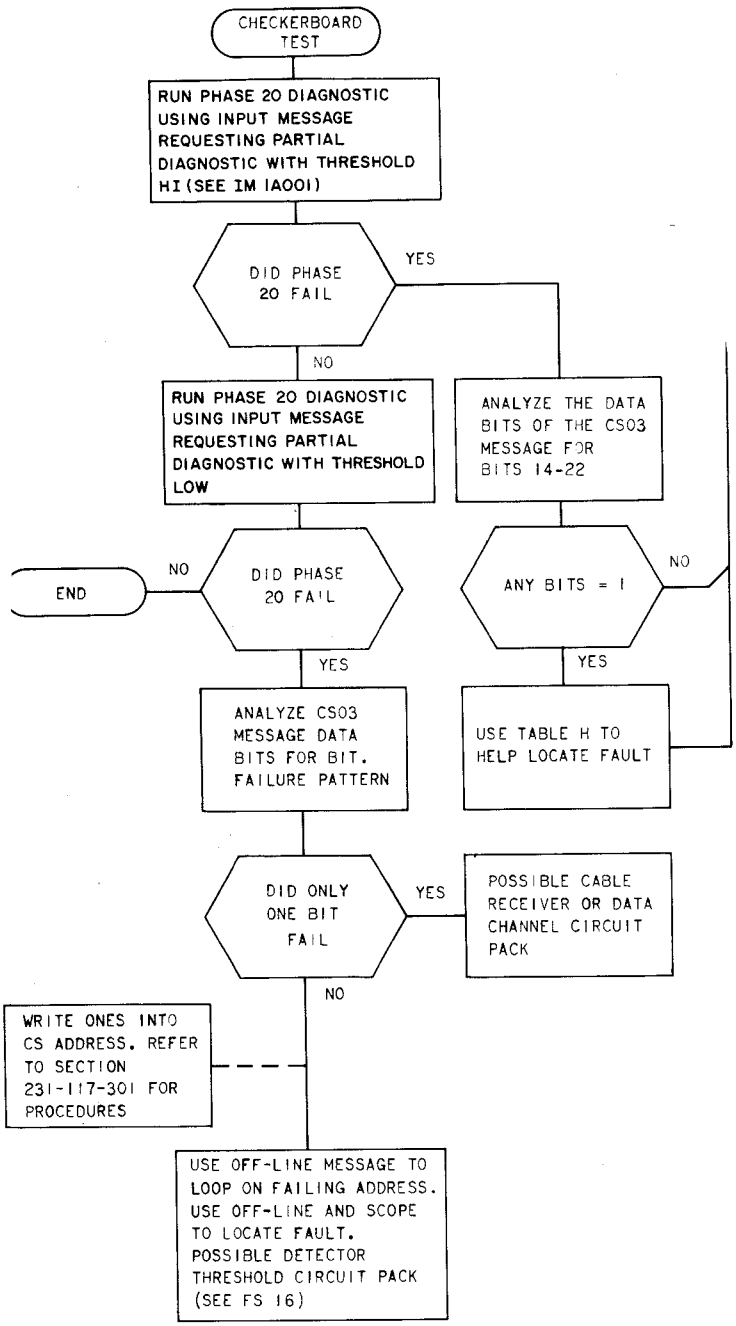


Fig. 8—BD Connector Location


CHECKERBOARD TEST
RUN PHASE 20 DIAGNOSTIC USING INPUT MESSAGE REQUESTING PARTIAL DIAGNOSTIC WITH THRESHOLD HI (SEE IM IA001)
DID PHASE 20 FAIL
YES
NO
RUN PHASE 20 DIAGNOSTIC USING INPUT MESSAGE REQUESTING PARTIAL DIAGNOSTIC WITH THRESHOLD LOW
ANALYZE THE DATA BITS OF THE CS03 MESSAGE FOR BITS 14-22
END
NO
DID PHASE 20 FAIL
ANY BITS = 1
NO
YES
YES
ANALYZE CS03 MESSAGE DATA BITS FOR BIT. FAILURE PATTERN
USE TABLE H TO HELP LOCATE FAULT
DID ONLY ONE BIT FAIL
YES
POSSIBLE CABLE RECEIVER OR DATA CHANNEL CIRCUIT PACK
NO
WRITE ONES INTO CS ADDRESS. REFER TO SECTION 231-117-301 FOR PROCEDURES
USE OFF-LINE MESSAGE TO LOOP ON FAILING ADDRESS. USE OFF-LINE AND SCOPE TO LOCATE FAULT. POSSIBLE DETECTOR THRESHOLD CIRCUIT PACK (SEE FS 16)

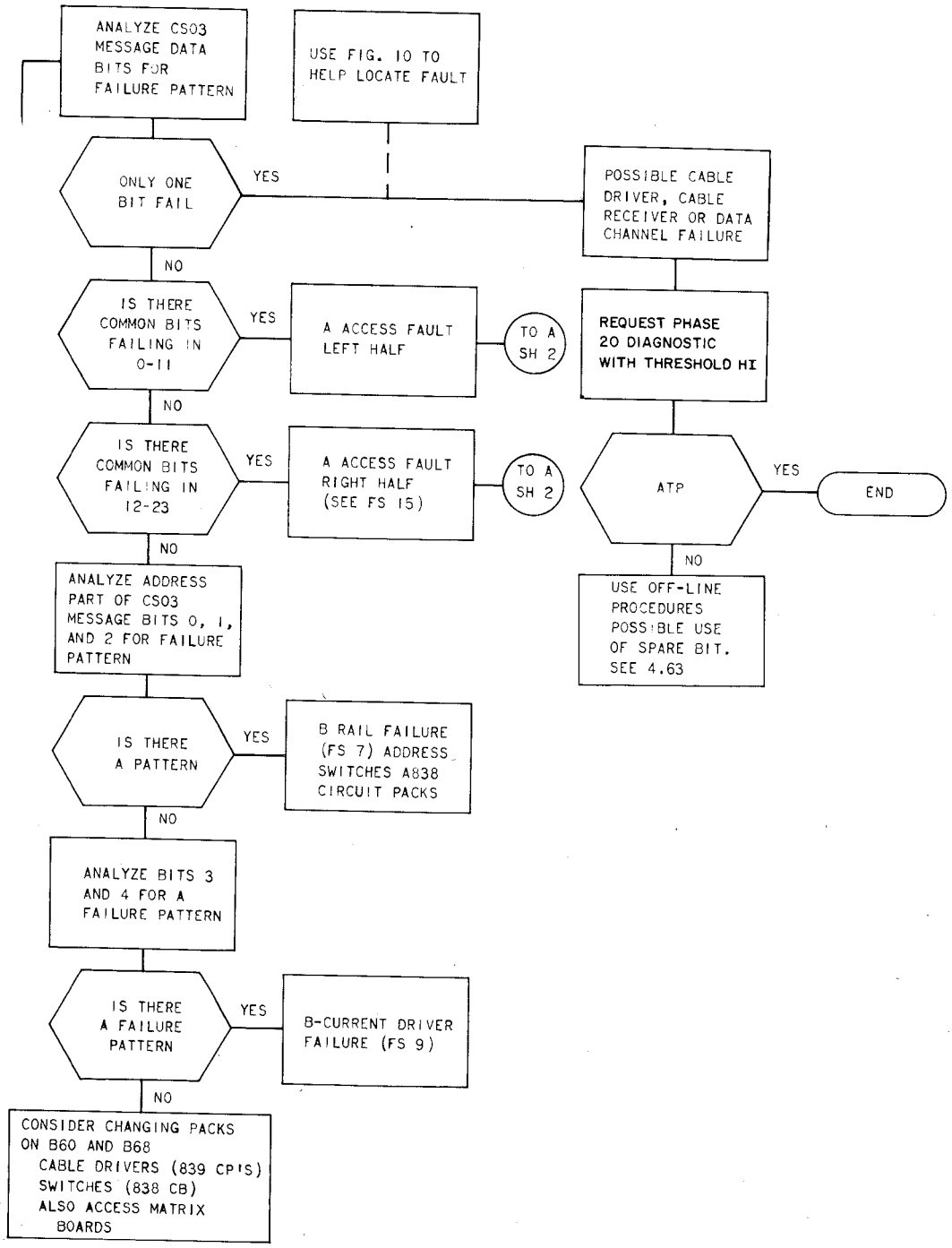


Fig. 9—Checkerboard Test Flowchart (Sheet 1 of 2)

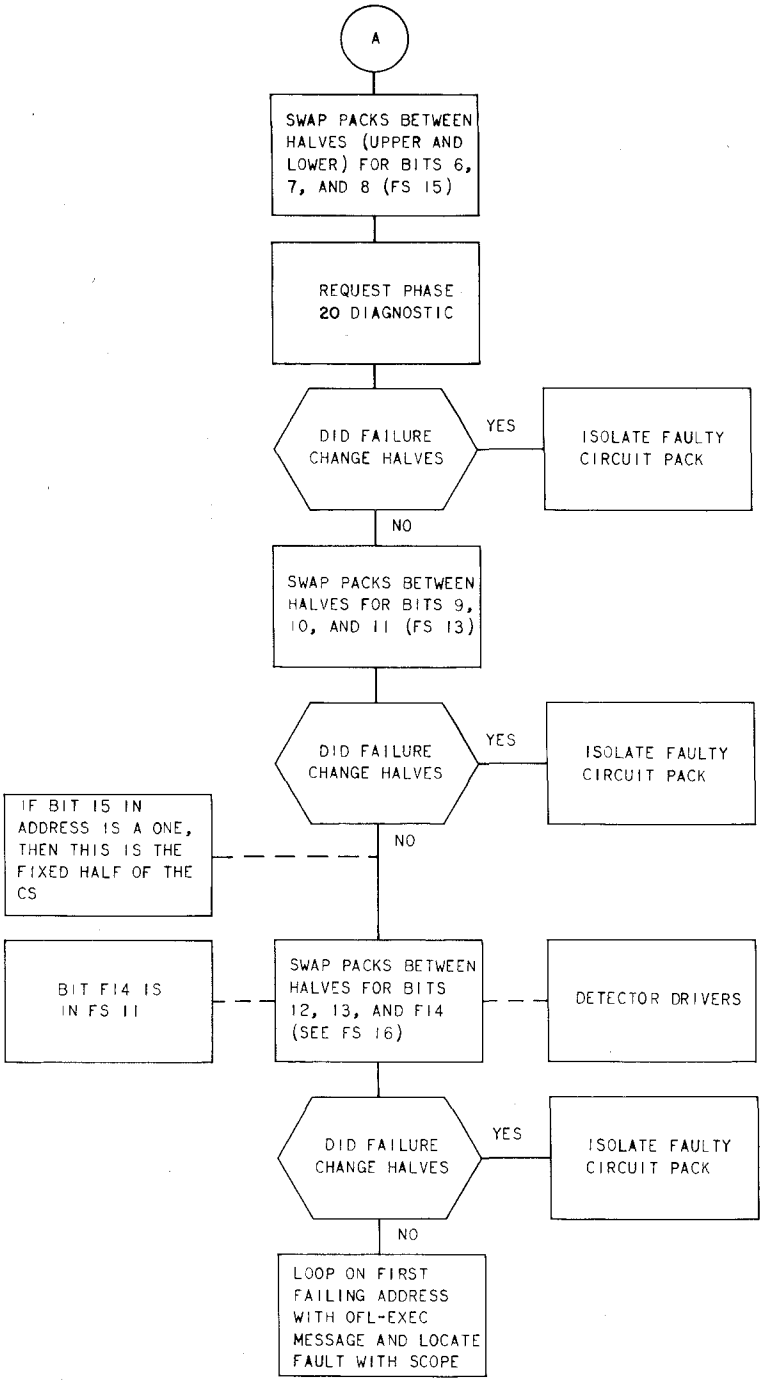


Fig. 9—Checkerboard Test Flowchart (Sheet 2 of 2)

PHASE 21

4.65 Phase 21 is the DATA=ADDRESS test. This is an access test that is run to verify that every address of the call store under test can store different data. This is done by initializing and then verifying every word in the call store under test with the data=address and data=address complemented test patterns. The test results can be used along with the checkerboard results to

TABLE H

NBTB ORDER DATA BITS

NBTB BIT	BIT NAME	CIRCUIT CHECKED	FS
14	WBD	B currect driver on write cycle	7
15	RBD	B current driver on ready cycle	7
16	BRB	B rail bias — set if no current is present	9
17	BRL	B rail — set if more than one rail is selected or no rail is selected	
18	RATV	A current — on read cycle, set if no current is present	15
19	ATH	A transformer select access	13
20	ARB	A rail bias — set if no current is present	11
21	ARL	A rail — set if more than one rail is selected or no rail is selected	11
22	WATV	A rail current on write cycle through vertical	15

DATA BITS — 32K CALL STORE CIRCUIT PACK CHART

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	PACK	DESCRIPTION	FS
L8	L8	L8	L8	L8	L6	L6	L6	L6	L6	L6	L6	L2	L2	L2	L2	L2	L2	L0	L0	L0	L0	L0	L0	A843	DATA CHANNEL	6
18	19	20	21	22	23	22	21	20	19	18	17	18	19	20	21	22	23	22	21	20	19	18	17			
L8-48		L8-47		L6-48		L6-47		L4-48		L4-47		L4-46		L2-48		L2-47		L2-46		L0-48		L0-47		A937	BUS RECEIVER/DRIVER	6
L6-32												L2-32												A921	WAVEFORM CONTROL	15
L8-34												L0-34												A841	CURRENT DRIVER	15
L6-27												L2-27												A844	DETECTOR DRIVER	16
L8-28												L0-28												A920	ACCESS MATRIX	13
L8-31												L0-31												A920	ACCESS MATRIX	11
L4-25																								A839	CURRENT DRIVER	7
L4-23																								A838	SWITCH	7
L4-19																								A957	READ ACCESS MATRIX	7
L4-32																								A839	CURRENT DRIVER	7
L4-34																								A838	SWITCH	9
L4-28																								A920	ACCESS MATRIX	9

CIRCUIT PACK LOCATIONS

Fig. 10—Data Bit Sensitive Troubleshooting Aid

CIRCUIT PACK LOCATIONS

ADDRESS BITS 17-14	ADDRESS BITS 13-5	ADDRESS BITS 4-0	PACK	DESCRIPTION	FS
	L2-29		A847	ADDRESS DECODER	15,6,7,8
	L2-28		A847	ADDRESS DECODER	15,6,7,8
	L2-30		A840	DIODE BRIDGE RECT	15,6,7,8
	L0-27		A847	ADDRESS DECODER	13,9,10,11
	L0-29		A847	ADDRESS DECODER	13,9,10,11
	L0-28		A920	ACCESS MATRIX	13,9,10,11
	L0-30		A847	ADDRESS DECODER	11,12,13,14
	L0-32		A847	ADDRESS DECODER	11,12,13,14
	L0-31		A920	ACCESS MATRIX	11,12,13,14
	L2-34		A838	SWITCH	15,5
	L2-32		A921	WAVEFORM CONTROL	15,5
	L6-29		A847	ADDRESS DECODER	15,6,7,8
	L6-28		A847	ADDRESS DECODER	15,6,7,8
	L6-30		A840	DIODE BRIDGE RECT	15,6,7,8
	L8-27		A847	ADDRESS DECODER	13,9,10,11
	L8-29		A847	ADDRESS DECODER	13,9,10,11
	L8-28		A920	ACCESS MATRIX	13,9,10,11
	L8-30		A847	ADDRESS DECODER	11,12,13,14
	L8-32		A847	ADDRESS DECODER	11,12,13,14
	L8-31		A920	ACCESS MATRIX	11,12,13,14
	L6-34		A838	SWITCH	15,5
	L6-32		A921	WAVEFORM CONTROL	15,5
	L4-32		A839	CURRENT DRIVER	9,0,1,2
	L2-34		A838	SWITCH	9,0,1,2
	L4-28		A920	ACCESS MATRIX	9,0,1,2
	L4-25		A839	CURRENT DRIVER	7,3,4
	L4-23		A838	SWITCH	7,3,4
	L4-19		A957	READ ACCESS MATRIX	7,3,4
		L4-30	A838	SWITCH	9,0,1,2
		L4-27	A838	SWITCH	9,0,1,2
		L4-21	A838	SWITCH	7,3,4
		L4-18	A838	SWITCH	7,3,4

Fig. 11—Address Bit Sensitive Troubleshooting Aid

locate a problem that may be sensitive to a certain address configuration.

FAULTS THAT CANNOT BE DIAGNOSED

4.66 There are certain faults that occur in the CS which will interfere with normal system operation if a diagnostic is attempted. These faults can permit spurious outputs from an out-of-service CS (senders are reset so CS cannot transmit for normal mode orders) and the CS is still able to receive from either bus. If the out-of-service CS were not able to receive from either bus (both trouble FFs set), the spurious outputs would cease.

4.67 There are certain segments in the CS diagnostic which necessarily allow the store to listen to the active bus while the senders are

reset. When a diagnostic is attempted on the CS, an interrupt may occur which will abort the diagnostic, leaving the CS out of service. Another symptom of these faults is that the CS diagnostic may appear erratic (ie, terminating early within a phase, repeating the same phase, etc.). Spurious output from the CS can affect the CS diagnostic control sanity.

4.68 When faults such as these occur, other means to locate the faults are available. These faults are located in a well defined portion of the CS circuitry as follows:

- Data channel cable drivers circuits (FS6)
- Data output enables (FS2).

4.69 All these faults are common in that they allow a permanent output enable to be applied to the data output cable drivers (A937 CPs). The actual data output pulse is then produced by strobing data from memory into the data register FF.

4.70 The circuit shown in Table I are suspect when a diagnostic is interrupted (due to a fault in the CS being tested) before it is completed. The interrupt message should be examined to determine the failing bits (5.01). If the interrupt messages point to the same data bits, replace those CPs listed in Table I that affect these bits.

5. D-LEVEL INTERRUPTS

5.01 A D-level maintenance interrupt occurs when a reread or rewrite failure of a CS word is encountered, or when an invalid transfer to a CS address rather than a PS address is encountered. When one of these failures is detected and the interrupt request is made by the system, the address at which the failure occurred is saved in the CC match registers.

5.02 To analyze D-level interrupts, use Fig. 12 flowchart. Fig. 13 and Fig. 14 and Table J through Table P are troubleshooting aids to be used with the flowchart.

TABLE I

POSSIBLE SEVERE FAULTS ON DIAGNOSTIC

LOCATION	BIT AFFECTED	
L0-42-A858	all data bits affected	
L8-44-A862	all data bits affected	
L2-45-A854	all data bits affected	
L2-43-A846	all data bits affected	
L8-46-A861	all data bits affected	
L2-42-A948	all data bits affected	
L8-48-A937	data bits, parity and 22	
L8-47-A937	data bits, 21 and 20	
L6-48-A937	data bits, 19 and 18	
L6-46-A937	data bits, 17 and 16	
L4-48-A937	data bits, 15 and 14	
L4-47-A937	data bits, 13 and 12	
L4-46-A937	data bits, 11 and 10	
L2-48-A937	data bits, 9 and 8	
L2-47-A937	data bits, 7 and 6	
L2-46-A937	data bits, 5 and 4	
L0-48-A937	data bits, 3 and 2	
L0-47-A937	data bits, 1 and 0	
0D01A lead open	data bits, 0—3	Bus 1
0D01B lead open	data bits, 4—7	Bus 1
0D01C lead open	data bits, 8—11	Bus 1
0D01D lead open	data bits, 12—15	Bus 1
0D01E lead open	data bits, 16—19	Bus 1
0D01F lead open	data bits, 20-P	Bus 1
0DZ1A lead open	data bits, 0—3	Bus 0
0DZ1B lead open	data bits, 4—7	Bus 0
0DZ1C lead open	data bits, 8—11	Bus 0
0DZ1D lead open	data bits, 12—15	Bus 0
0DZ1E lead open	data bits, 16—19	Bus 0
0DZ1F lead open	data bits, 20-P	Bus 0

6. FUSE AND POWER FAULT LOCATING

CABLE DRIVERS

6.01 When a fuse fails indicating a problem in the cable driver circuitry, consult the power and fusing data table on the associated B sheet listed in Table Q. To isolate the faulty pack, remove power from the CS, remove one or more of the associated A937 CPs, restore power by operating the REQ-INH and ST keys at the frame control but not the NOR key, and continue until fault circuit is isolated.

ACCESS CIRCUITRY

6.02 When a fuse common to the access circuitry fails, consult the power and fusing data table on the associated B sheets listed in Table Q to isolate the circuit packs that are fed by the fuse.

6.03 If the blown fuse is the -48G or -48H, more than one circuit pack could be defective. Figure 15 gives a flowchart procedure for locating these faults. Table R gives a list of access circuit packs. The 20L transistors on the isolation switch and the address switches (A838 CPs) must be checked for collector to emitter shorts. The collector to emitter pins are 24 to 25, 13 to 14, 11 to 12, and 1 to 2, respectively. Also, the associated access matrix board (A920 or A957) must be checked for burnt resistors. If there is any doubt, use an ohmmeter. The reading across each pair of resistors should be 150 ohms.

VOLTAGE REGULATOR TROUBLESHOOTING

6.04 This part provides an approach for analyzing and locating the cause of a blown fuse associated with the voltage regulator.

6.05 The following apparatus is required to perform the tests given in this section:

- One KS-14510-L3 Volt-ohmmeter
- One 428B H-P Clip-on DC milliammeter.

6.06 The method for analyzing and locating trouble in the voltage regulator is divided into four major procedures. A fifth procedure is provided to bring the CS back to service with full diagnostics after the voltage regulator has been replaced. The procedures are presented in flowchart format to clarify the steps involved. Listed below are the procedures and the figures on which they are illustrated.

Fig. 16—Blown Fuse Procedure: This procedure is used to determine if the voltage regulator is the actual cause of the blown fuse. It should not be prematurely assumed that ***only*** the voltage regulator associated with the troubled CS is defective. If the blown fuse is ***not*** associated with a voltage regulator, normal procedures used for isolating the trouble should be followed.

Fig. 17—Voltage Regulator Continuity Check Procedure: This procedure is used to verify continuity in remote sense leads between voltage regulator ED boards and their respective voltage distribution 905-type connectors. Tables S and T are used in this part.

Fig. 18—+24 Volt and -48 Volt Control Check Procedure: This procedure is used to verify that the 32K CS unit control panel is operating properly.

Fig. 19—3 Volt, +5 Volt, +12 Volt, and -12 Volt Verification, Distribution, and Load Check Procedure: This procedure is used to verify the voltage regulator unit and the four converters within the voltage regulator. The four voltage regulator output voltages and fuse currents are first measured to verify that they are within tolerance. The -12 volt supply is measured while inserting groups of circuit packs (in different steps) to determine if the load, created by the circuit packs, is irregular. Any abnormal load will be indicated as an abnormal voltage or as current measurement. By using this procedure, a faulty circuit pack that may have contributed to the blown fuse can be isolated.

Fig. 20—Returning 32K Call Store to Service: This procedure is used to restore the 32K CS unit to service. Included in this procedure is a checkerboard test.

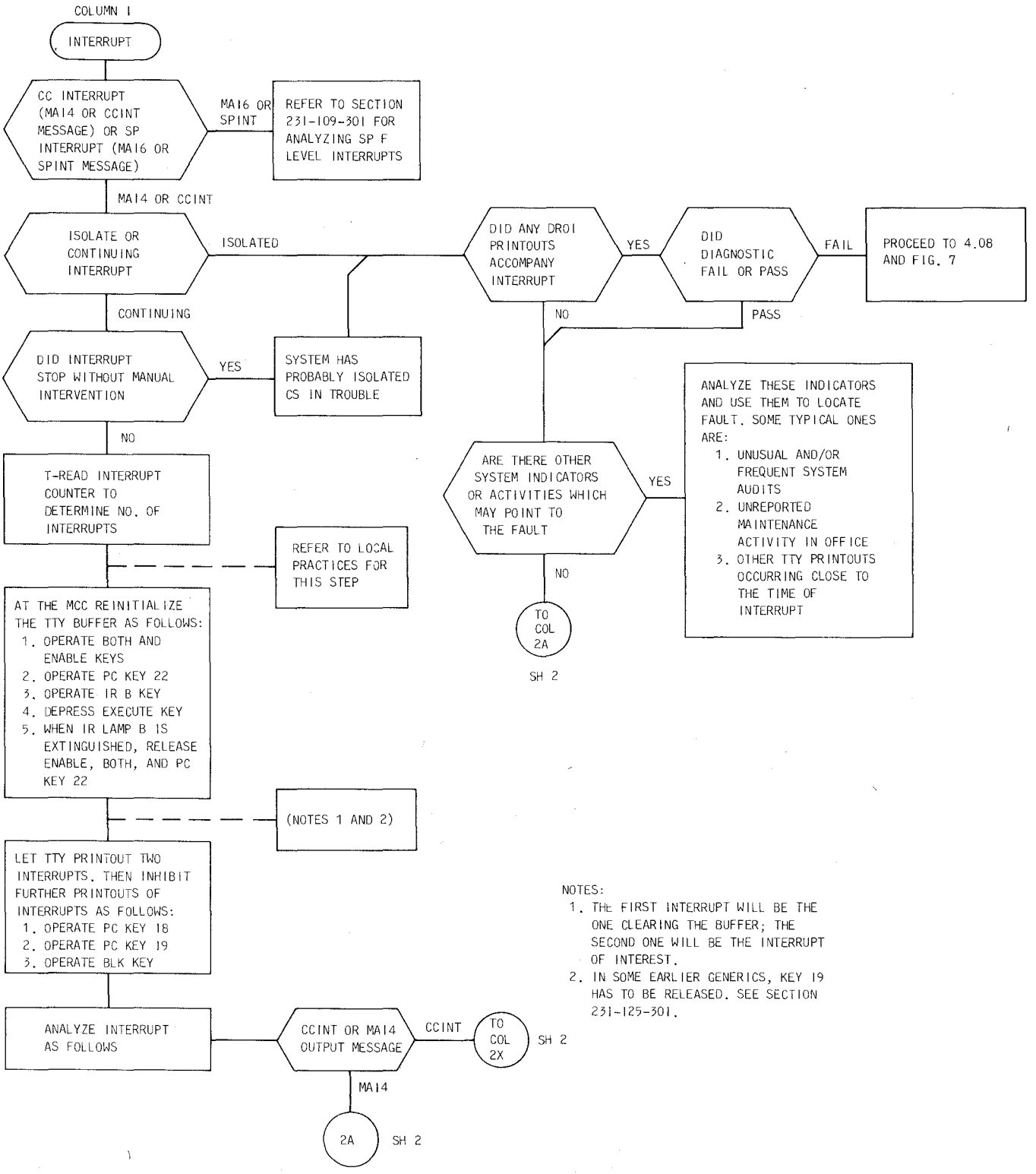


Fig. 12—Analyzing D-Level Interrupt Flowchart (Page 1 of 7)

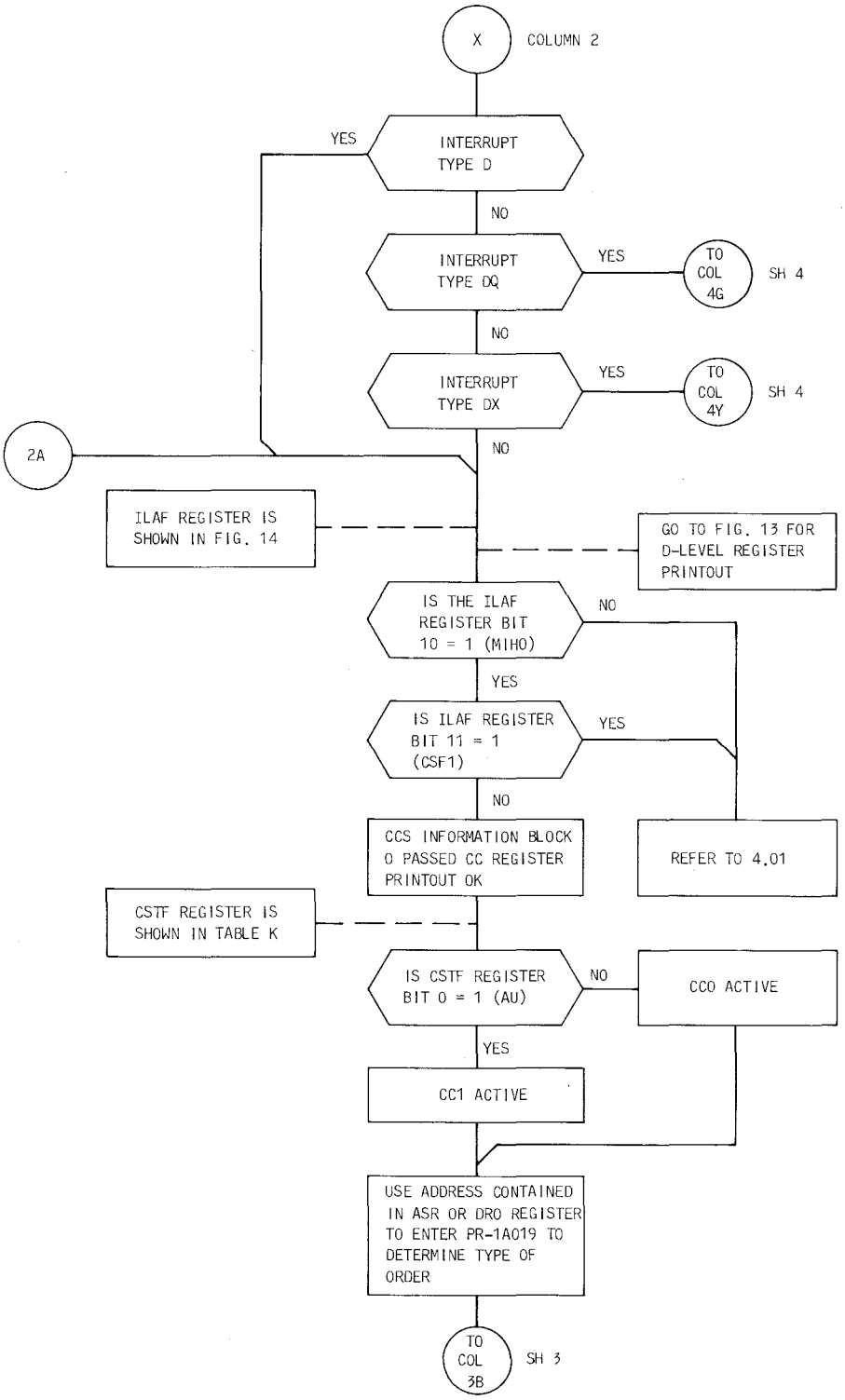


Fig. 12—Analyzing D-Level Interrupt Flowchart (Sheet 2 of 7)

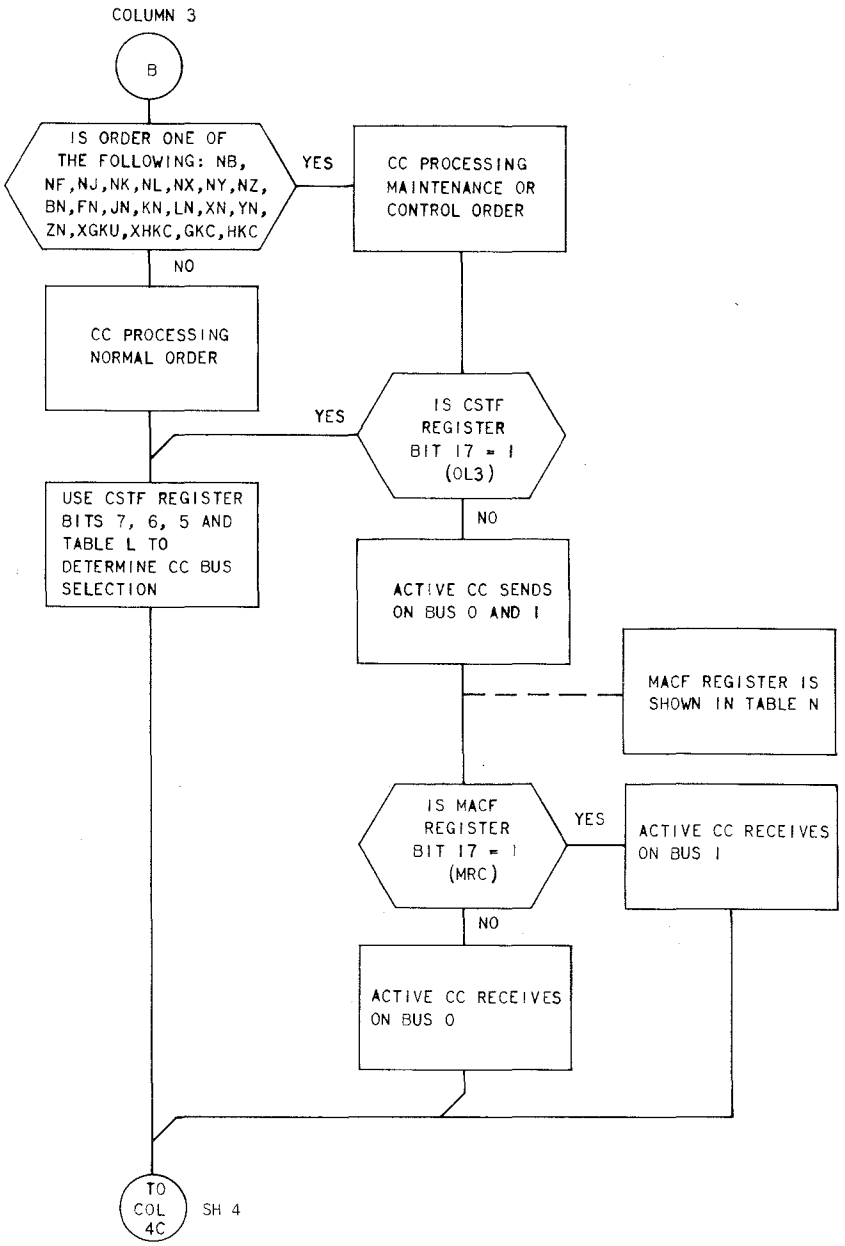


Fig. 12—Analyzing D-Level Interrupt Flowchart (Sheet 3 of 7)

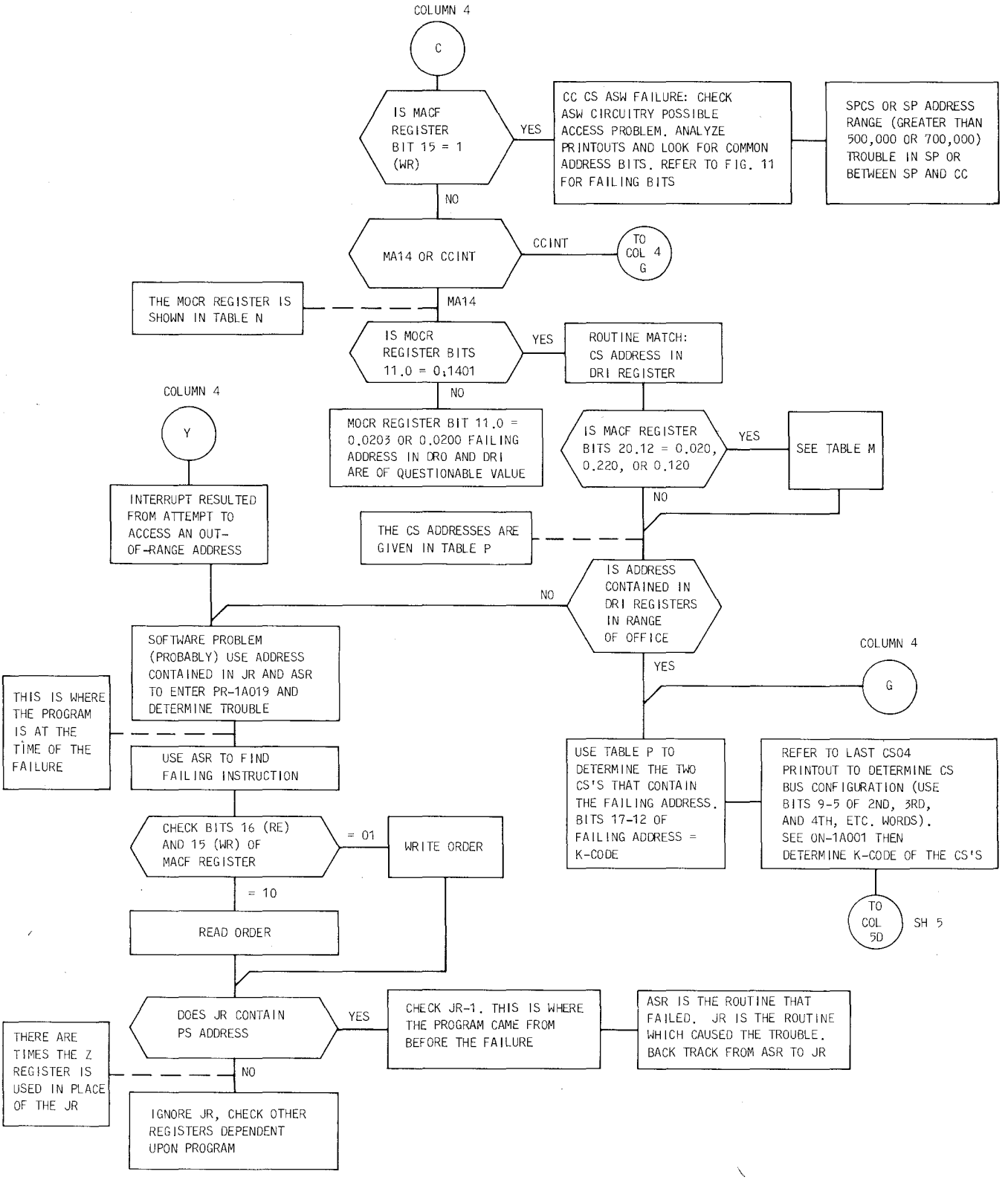


Fig. 12—Analyzing D-Level Interrupt Flowchart (Sheet 4 of 7)

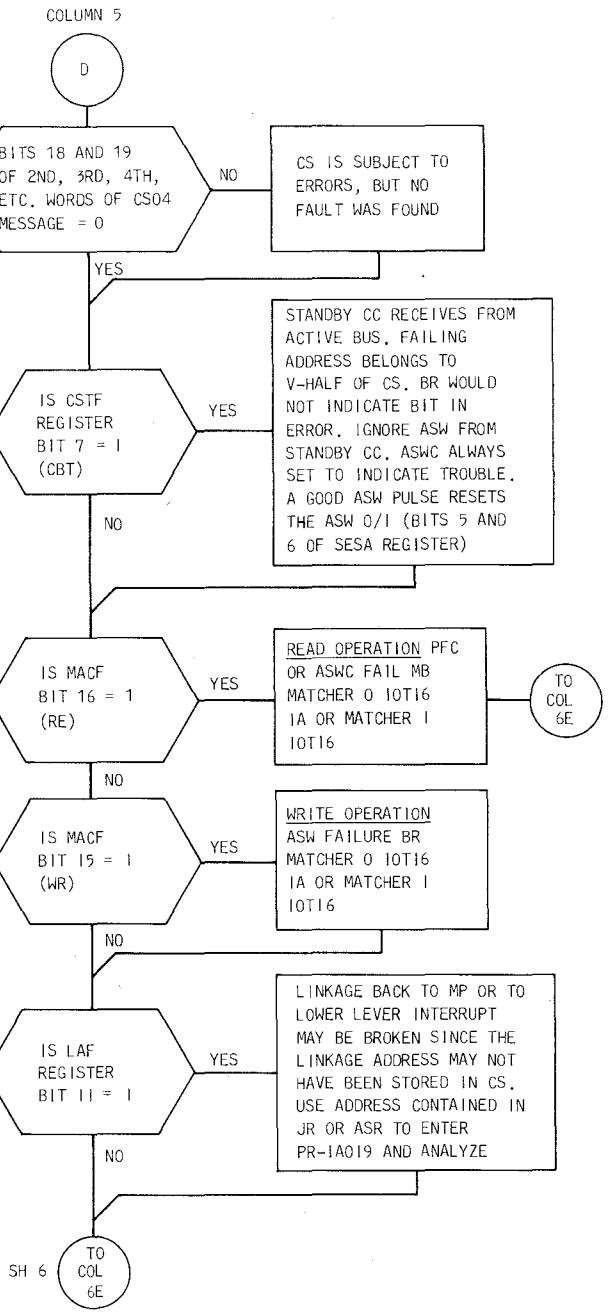
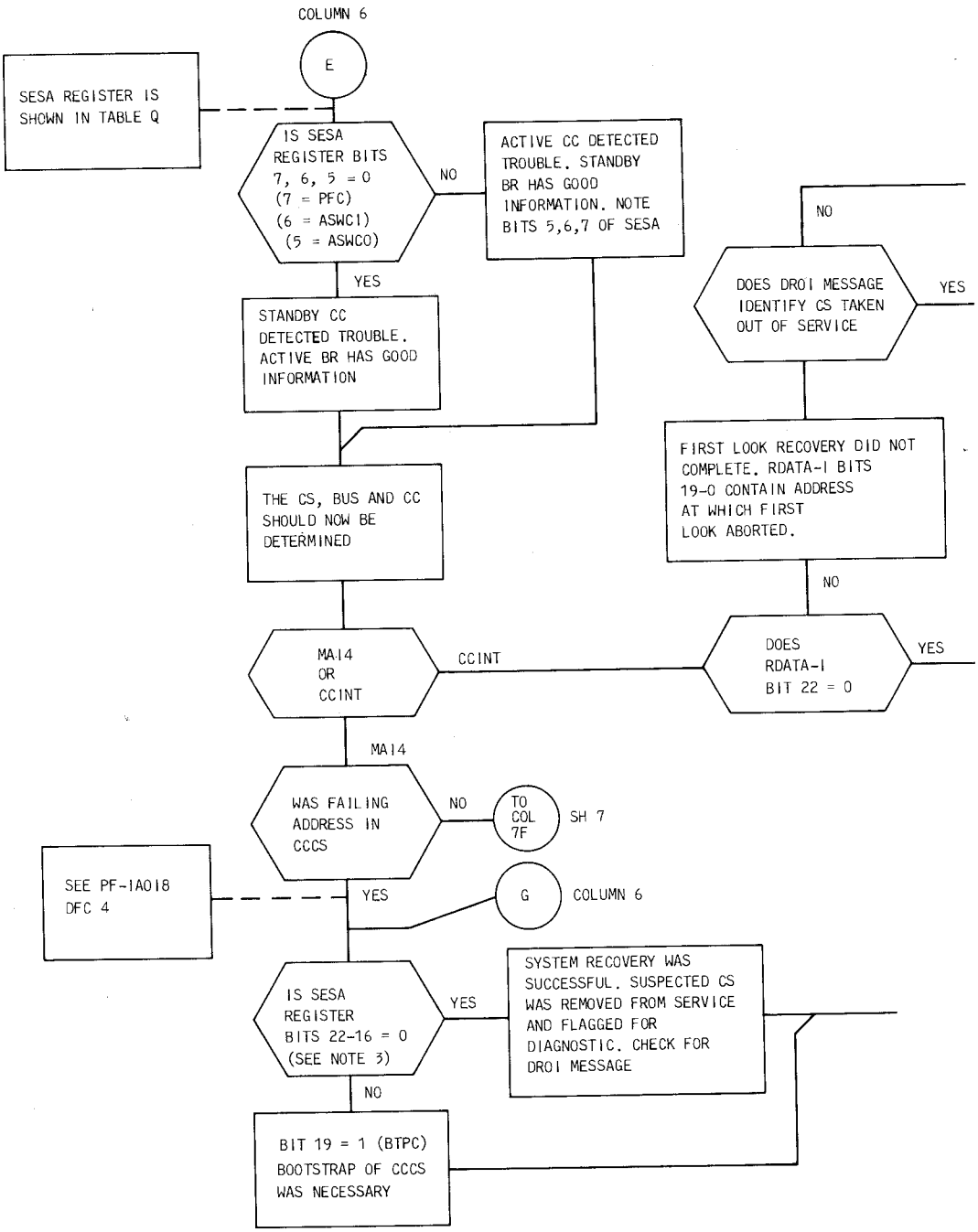
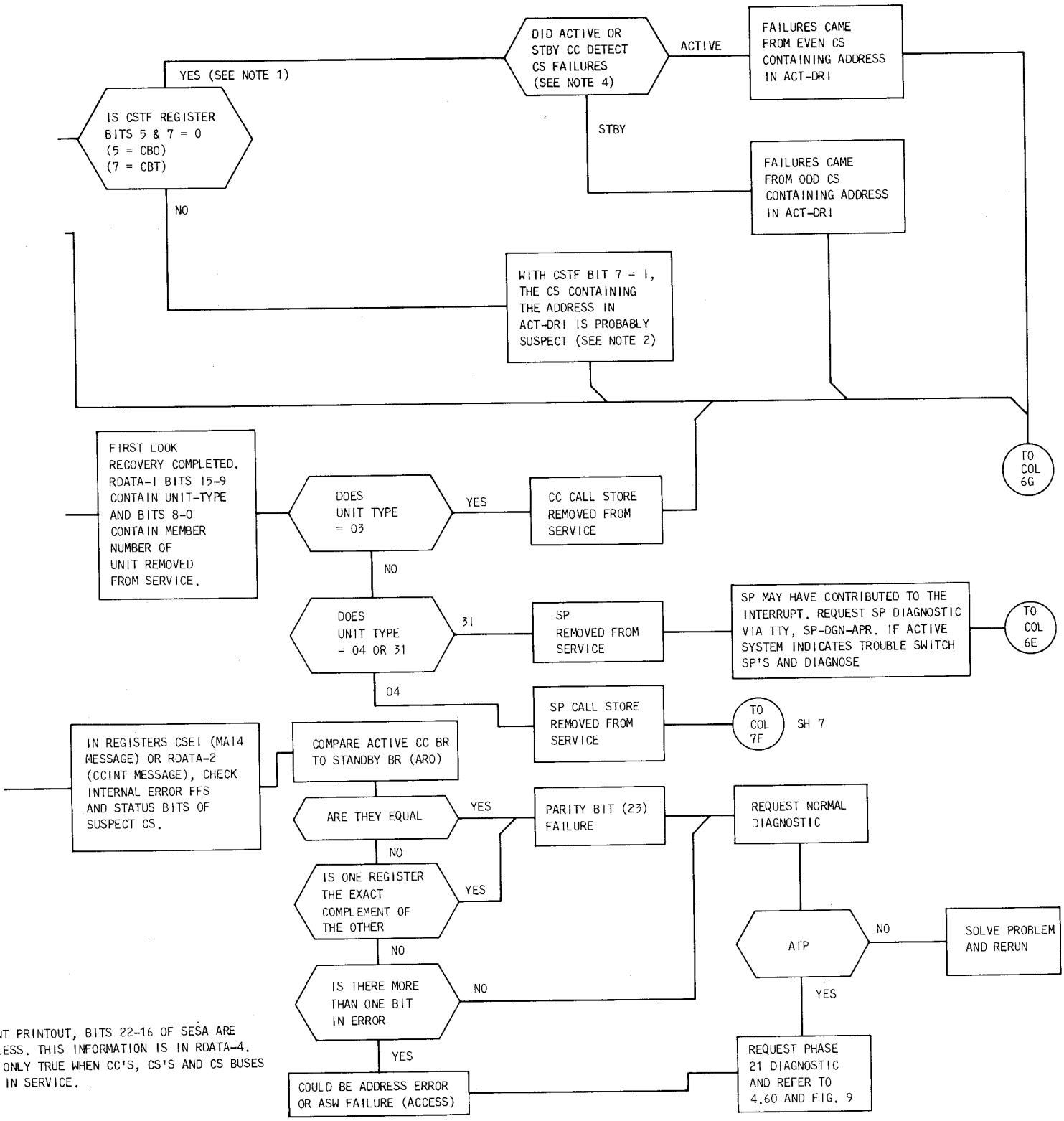


Fig. 12—Analyzing D-Level Interrupt Flowchart (Sheet 5 of 7)



NOTES:

1. IN A NORMALIZED CS CONFIGURATION, CBO AND CBT IN CSTF ARE RESET; THE EVEN-NUMBERED CSS TRANSMIT AND RECEIVE ON THE ACTIVE CS BUS AND THE ODD-NUMBERED CSS TRANSMIT AND RECEIVE ON THE STANDBY CS BUS.
2. WITH CBT IN CSTF SET, THE STANDBY CS BUS IS OUT OF SERVICE. IN THIS STATE, THE SYSTEM IS GENERALLY CONFIGURED WITH THE FIXED NAME MEMORY BLOCKS TRANSMITTING ON THE ACTIVE BUS AND THE VARIABLE NAME BLOCKS OFF-LINE.



3. FOR CCINT PRINTOUT, BITS 22-16 OF SESA ARE MEANINGLESS. THIS INFORMATION IS IN RDATA-4.
4. THIS IS ONLY TRUE WHEN CC'S, CS'S AND CS BUSES ARE ALL IN SERVICE.

Fig. 12—Analyzing D-Level Interrupt Flowchart (Sheet 6 of 7)

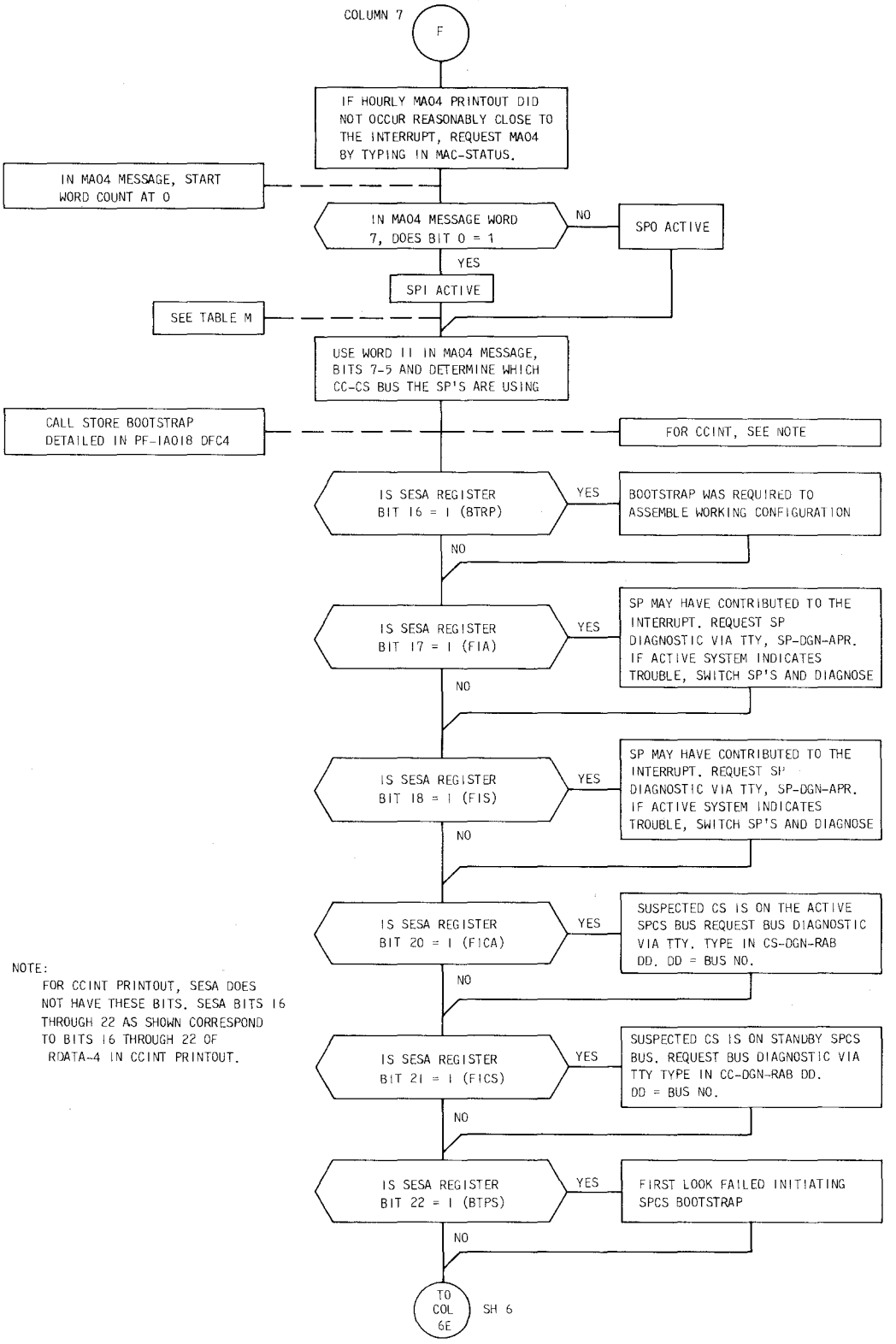


Fig. 12—Analyzing D-Level Interrupt Flowchart (Sheet 7 of 7)

MA14 CC INT

B	ASR	F	J	K	X
Y	Z	L	ADK	ARO	DRO
CSEI	DRI	SESA	MOCR & MACF	CSTF	ILAF

ARO = B REG OF STANDBY CC
DRO = PA ADDRESS AT TIME OF INTERRUPT
DRI = FAILING CALL STORE ADDRESS
CSEI = ERROR INDICATORS

A. MA14 -D-LEVEL REGISTER LOCATIONS

CCINT LL P ASR TT:TT:TT.T

BREG	FREG	JREG	KREG	AKREG
LREG	XREG	YREG	ZREG	
SHEM-ILAF	PEST-NOIS	MAIS	MACF-MOCR	CSTF

U ADDRESS C JI AAAA

VVVVVVVV VVVVVVVV VVVVVVVV VVVVVVVV VVVVVVVV VVVVVVVV

. . . .
. . . .
. . . .

VVVVVVVV VVVVVVVV VVVVVVVV VVVVVVVV VVVVVVVV VVVVVVVV

VARIABLE DATA VVVVVVVV:

(SUBTYPE ... D,DU)

ACT-ARO	ACT-DRO	ACT-AR1	ACT-DR1	B23/SESA	ACT-SECF
SBY-ARO	SBY-DRO	SBY-AR1	SBY-DR1	B23/SESA	SBY-SECF
ACT-MACR	SBY-BREG	RDATA-I	RDATA-2	RDATA-3	RDATA-4

(SUBTYPE ... DX)

ACT-ARO	ACT-DRO	ACT-AR1	ACT-DR1	B23/SESA	ACT-SECF

B. CCINT D-LEVEL REGISTER LOCATIONS

Fig. 13—D-Level Interrupt Register Locations

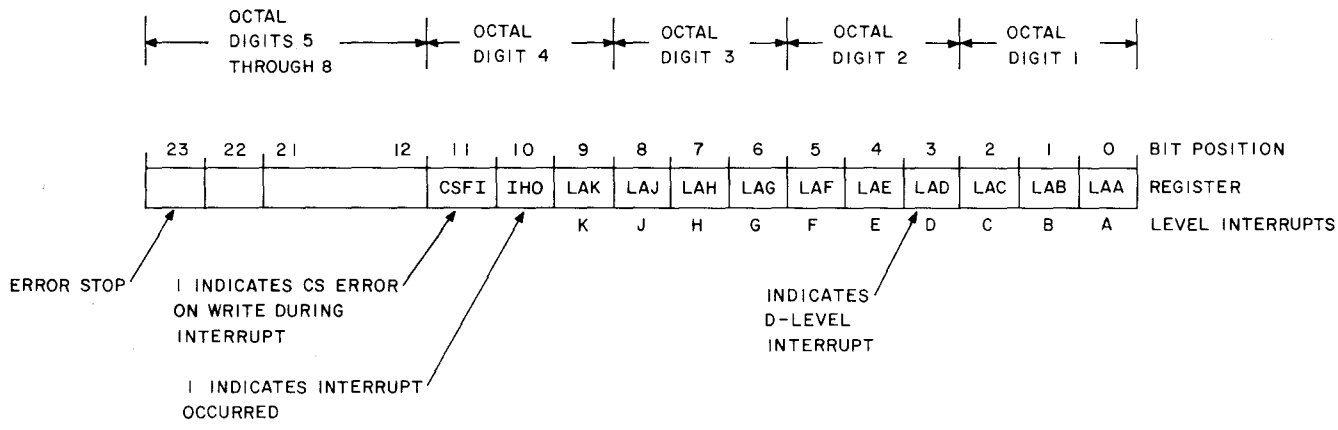


Fig. 14—LAF Register Layout

TABLE J

CSTF REGISTER LAYOUT

BIT	NAME OF BIT	COMMENTS
0	AU	Defines active CC
1	TCC	Marks standby CC in trouble
2	PBO	PS bus control
3	PBA	
4	PBT	
5	CBO	CS bus control
6	CBA	
7	CBT	
8	CW	Control word bus selection
9	CWC	Enables standby to receive control words

TABLE K

CC-CS BUS SELECTION

CBT CSTF7	CBA CSTF6	CBO CBTF5	ACT CC		STBY CC	
			SEND	REC	SEND	REC
0	0	0	0	0	1	1
0	1	0	1	1	0	0
1	0	0	0	0	X	0
1	1	0	1	1	X	1
0	0	1	0 AND 1	0	X	1
0	1	1	0 AND 1	1	X	0
1	0	1	0 AND 1	1	X	0
1	1	1	0 AND 1	1	X	1

0 = FF RESET
1 = FF SET

0 = BUS 0
1 = BUS 1
X = NEITHER BUS

TABLE L

SP-CS BUS SELECTION

BIT 7 CCBT	BIT 6 CCBA	BIT 5 CCBO	ACTIVE SP		STBY SP	
			SEND	REC	SEND	REC
0	0	0	0	0	1	1
0	1	0	1	1	0	0
1	0	0	0	0	X	0
1	1	0	1	1	X	1
0	0	1	0 AND 1	0	X	1
0	1	1	0 AND 1	1	X	0
1	0	1	0 AND 1	0	X	0
1	1	1	0 AND 1	1	X	1

0 = FF RESET
1 = FF SET

0 = BUS 0
1 = BUS 1
X = NEITHER BUS

TABLE M

MACF REGISTER LAYOUT

BUFFER REGISTER BIT POSITION	NAME OF BIT	ACCESS SEE NOTE			COMMENTS
		R	W	C	
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
10					
11					
12	M0	√			Flip-flop outputs of matchers
13	M1	√			
14	PU	√	√	√	This flip-flop is set on peripheral orders
15	WR	√	√	√	This flip-flop is set on write orders
16	RE	√	√	√	This flip-flop is set on read orders
17	EC	√	√	√	This flip-flop is set on error correction
18	MC13	√	√	√	Bits of match cycle counter
19	MC23	√	√	√	
20					

TABLE M (Contd)

MACF REGISTER LAYOUT

BUFFER REGISTER BIT POSITION	NAME OF BIT	ACCESS SEE NOTE			COMMENTS
		R	W	C	
21	MRC	√	√	√	Defines which CS bus is to be used for CS maintenance and control word reception
22	MRP				Defines which PS bus is to be used for PS maintenance and control word reception

Notes:

R — Bit position can be read with read-memory orders.

W — Bit position can be written into with write-memory orders.

C — Bit position can be written into with control-write orders.

B8MACF BITS 20-12	EXPLANATION
0.020	MISMATCH ON READ ORDER, DR1 CONTAINS FAILING ADDRESS, AR0 CONTAINS DATA BEING READ.
0.220	MISMATCH ON READ ORDER, DR1 CONTAINS FAILING ADDRESS, AR0 CONTAINS DATA (OR ITS COMPLIMENT) BEING READ.
0.120	MISMATCH ON READ ORDER, DR1 CONTAINS FAILING ADDRESS, AR0 CONTAINS COMPLIMENT OF DATA BEING READ.

TABLE N

MOCR REGISTER LAYOUT

BUFFER REGISTER BIT POSITION	NAME OF BIT	ACCESS SEE NOTE			COMMENTS
		R	W	C	
00	X	√	√	√	These bits establish matching mode
01	Y	√	√	√	
02	MS	√	√	√	
03	TD	√	√	√	
04	CB	√	√	√	
05	PB	√	√	√	
06	TR	√	√	√	
07	IC	√	√	√	
08	I	√	√	√	Interrupt on abnormality
09	HM	√	√	√	Stop match on abnormality
10	E	√	√	√	Stop standby with execute-stop on abnormality
11	F	√	√	√	Stop standby with fast-stop on abnormality

Notes:

R — Bit position can be read with real-memory orders.

W — Bit position can be written into with write-memory orders.

C — Bit position can be written into with control-write orders.

TABLE O

K-CODE AND ADDRESS FIELD

	16K CS BLOCK	NAME	CS NAME (K-CODE)				ADDRESS			ADDRESS RANGE IN OCTAL (A17–A0)
			A17	A16	A15	A14	A13	A12	A11–A0	
CC CS	NOT USED		0	0	0	0	0	0		
	0	1	0	0	0	0	0	1		10000—17777
		1	0	0	0	0	1	0		20000—27777
		1	0	0	0	0	1	1		30000—37777
		2	0	0	0	1	0	0		40000—47777
	1	1	0	0	0	1	0	1		50000—57777
		1	0	0	0	1	1	0		60000—67777
		1	0	0	0	1	1	1		70000—77777
		2	0	0	1	0	0	0		100000—107777
	2	1	0	0	1	0	0	1		110000—117777
		1	0	0	1	0	1	0		120000—127777
		1	0	0	1	0	1	1		130000—137777
		2	0	0	1	1	0	0		140000—147777
	3	1	0	0	1	1	0	1		150000—157777
		1	0	0	1	1	1	0		160000—167777
		1	0	0	1	1	1	1		170000—177777
		2	0	1	0	0	0	0		200000—207777
	4	1	0	1	0	0	0	1	ADDRESS	210000—217777
		1	0	1	0	0	1	0		220000—227777
		1	0	1	0	0	1	1		230000—237777
		2	0	1	0	1	0	0		240000—247777
	5	1	0	1	0	1	0	1		250000—257777
		1	0	1	0	1	1	0		260000—267777
		1	0	1	0	1	1	1		270000—277777
		2	0	1	1	0	0	0		300000—307777
	6	1	0	1	1	0	0	1		310000—317777
		1	0	1	1	0	1	0		320000—327777
		1	0	1	1	0	1	1		330000—337777
		2	0	1	1	1	0	0		340000—347777
	7	1	0	1	1	1	0	1		350000—357777
		1	0	1	1	1	1	0		360000—367777
		1	0	1	1	1	1	1		370000—377777
		2	1	0	0	0	0	0		400000—407777
	8	1	1	0	0	0	0	1		410000—417777
		1	1	0	0	0	1	0		420000—427777
		1	1	0	0	0	1	1		430000—437777
		2	1	0	0	1	0	0		440000—447777

TABLE O (Cont'd)

K-CODE AND ADDRESS FIELD

	16K CS BLOCK	NAME	CS NAME (K-CODE)				ADDRESS			ADDRESS RANGE IN OCTAL (A17-A0)
			A17	A16	A15	A14	A13	A12	A11-A0	
CC CS	9 (See Note)	1	1	0	0	1	0	1		450000—457777
		1	1	0	0	1	1	0		460000—467777
		1	1	0	0	1	1	1		470000—477777
		2	1	1	0	0	0	0		600000—607777
SP SC	0	2	1	0	1	0	0	0	ADDRESS	500000—507777
		1	1	0	1	0	0	1		510000—517777
		1	1	0	1	0	1	0		520000—527777
		1	1	0	1	0	1	1		530000—537777
	1	2	1	0	1	1	0	0		540000—547777
		1	1	0	1	1	0	1		550000—557777
		1	1	0	1	1	1	0		560000—567777
		1	1	0	1	1	1	1		570000—577777

Note: CS9 is available with 1E (B5, B6) 6 and later generics.

TABLE P

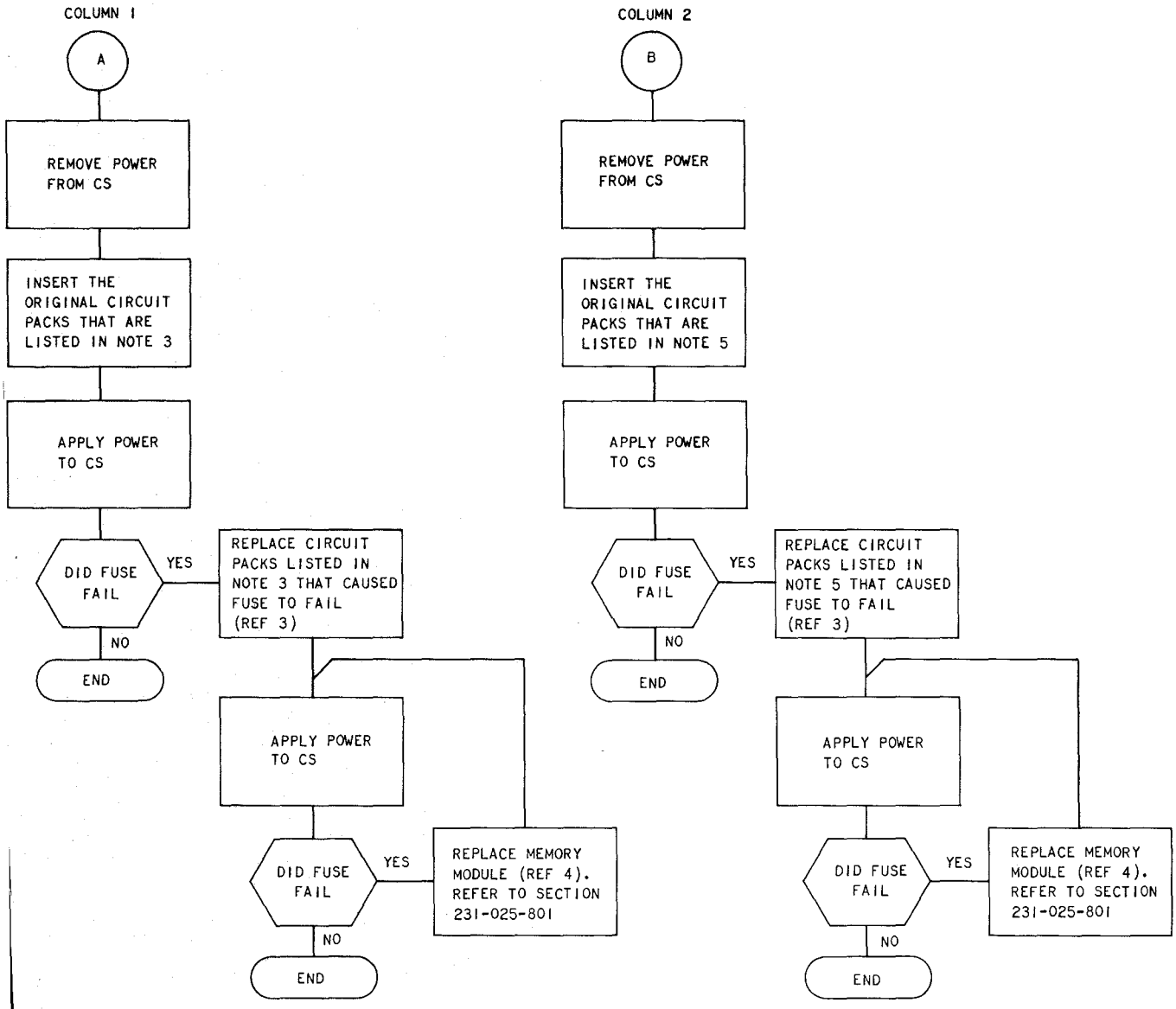
SESA REGISTER LAYOUT

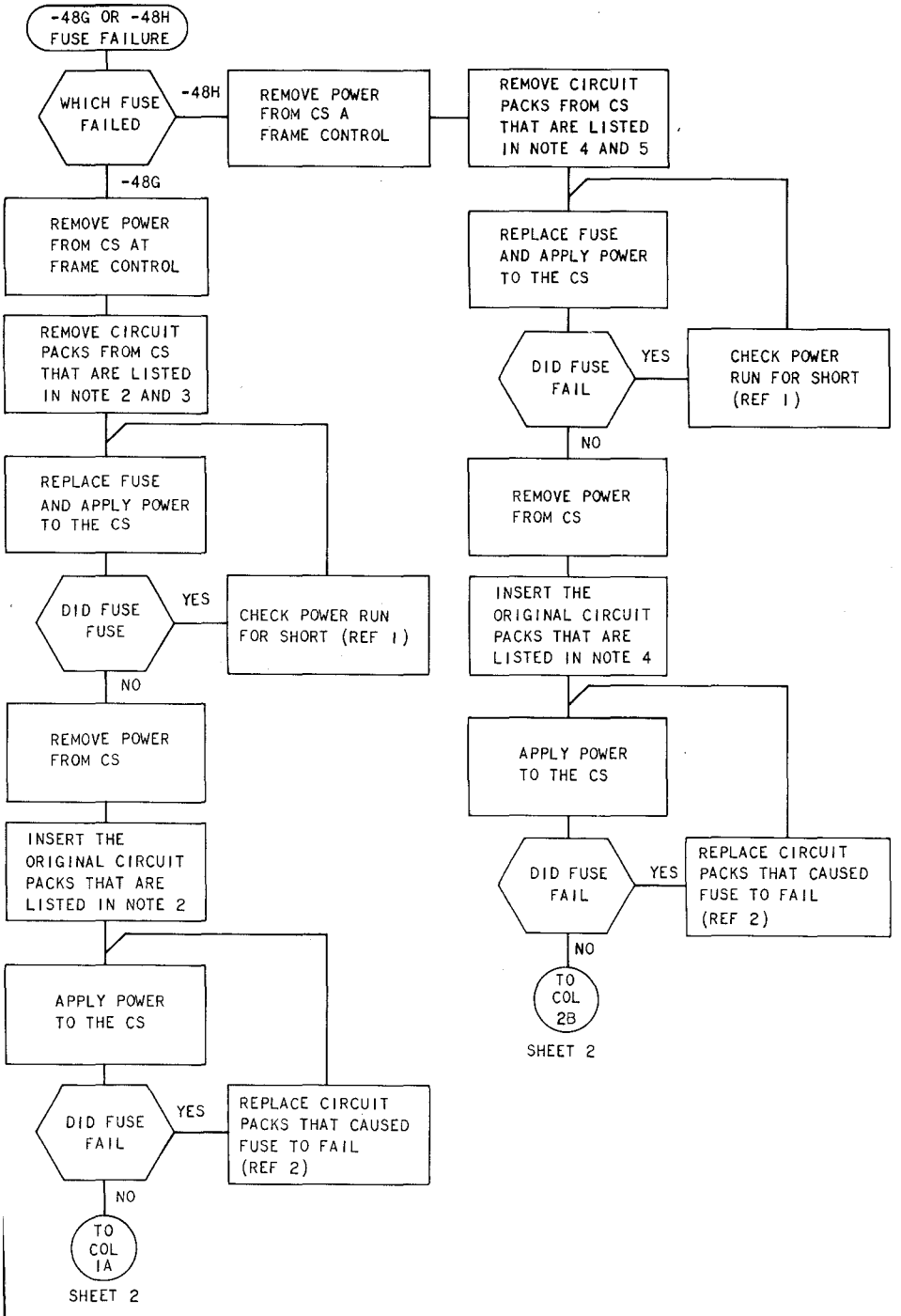
BIT	NAME OF BIT		COMMENTS
0	ASWPF-0	ASW Failure from PS Bus-0	P.S. error, summary FFs have inputs from error detection, and correction circuits are gated on interrupt request or on maintenance orders.
1	ASWPF-1	ASW Failure from PS Bus-1	
2	ADEF	Address Error	
3	DBEF	Double Error	
4	PF	Single Error	
5	ASWC-0	ASW Failure from CS Bus-0	Call Store Summary Group, inputs controlled similar to above.
6	ASWC-1	ASW Failure from CS Bus-1	
7	PFC	Parity Failure of CS word at buffer REG.	
8	X23-1	Bit 24 of Adden-K REG.	

TABLE Q

32K CS FUSES

FUSE	VALUE	CIRCUIT	B SHEET	DESCRIPTION
+24VB	1/2 amp	Cable Driver	B50 to B59	+24V supply for cable driver bits 0 to 9 A937CPs.
+24VC	3 amp	Volt. Reg.	B84A or B98	2.4 amp input current to +5V Reg. which powers almost all CPs.
+24VD	2 amp	Volt. Reg.	B84A or B98	1.25 amp input current to +12V Reg. which powers all A843CPs (data channels) and most of the access packs.
+24VE	1/2 amp	Volt. Reg.	B84 or B98	+24V supply for −12V Reg., 12V and +5V crow-bar circuit.
+24VF	1/2 amp	Volt. Reg.	B84A or B98	+24V supply for −3V Reg., −3V and +12V crow-bar circuit and relay interface board.
+24VG	1-1/3 amp	"A" Access	B71 to B82	+24V supply for "A" access CPs. Also powers A845CP and A991CP (B84A or B98).
+24VH	1/2 amp	Cable Driver	B36 to B39, 42, 43, 16	+24V supply for cable driver bits 20 to 23, 16, 17 A937CPs. Also cable driver for ASW and SYNC.
+24VJ	1/2 amp	Cable Driver	B44 to B49, 40, 41	+24V supply for cable driver bits 10 to 15, 18, 19 A937CPs.
+24VK	1-1/3 amp	"B" access	B60 and B68	+24V supply for "B" access circuit packs.
+24VL	.18 amp	A991CP	B84B or B98	Fuse blows when a low voltage is detected from the A845CP, possibly due to Volt. Reg. current limiting.
−48VB	1/2 amp	Volt. Reg.	B84A or B98	.3 amp input current to −3V Reg. which powers almost all CPs. Also is −48V supply for the relay interface board.
−48VC	2 amp	Volt. Reg.	B84A or B98	1.3 amp input current to −12V Reg. which powers the current drivers.
−48VF	1-1/3 amp	"A" access	B81 and B82	−48V supply for "A" access CPs, also powers A845CP (B84A).
−48VG	1/2 amp	"B" access	B60	−48V supply for "B" current driver matrix (FS7).
−48VH	1/2 amp	"B" access	B68	−48V supply for "B" access bridge drive matrix (FS9).


COLUMN 1
A
REMOVE POWER FROM CS
INSERT THE ORIGINAL CIRCUIT PACKS THAT ARE LISTED IN NOTE 3
APPLY POWER TO CS
DID FUSE FAIL
YES
NO
END
REPLACE CIRCUIT PACKS LISTED IN NOTE 3 THAT CAUSED FUSE TO FAIL (REF 3)
APPLY POWER TO CS
DID FUSE FAIL
YES
NO
END
REPLACE MEMORY MODULE (REF 4). REFER TO SECTION 231-025-801
COLUMN 2
B
REMOVE POWER FROM CS
INSERT THE ORIGINAL CIRCUIT PACKS THAT ARE LISTED IN NOTE 5
APPLY POWER TO CS
DID FUSE FAIL
YES
NO
END
REPLACE CIRCUIT PACKS LISTED IN NOTE 5 THAT CAUSED FUSE TO FAIL (REF 3)
APPLY POWER TO CS
DID FUSE FAIL
YES
NO
END
REPLACE MEMORY MODULE (REF 4). REFER TO SECTION 231-025-801



NOTES:

1. THE FOUR MOST COMMON FAILURE MODES FOR -48G OR -48H FUSE FAILURES ARE LISTED BELOW:

   REF 1: FUSE WIRING RUN SHORTED
   REF 2: SHORTED CAPACITOR ON CIRCUIT PACKS LISTED IN TABLE A AND C
   REF 3: SHORTED SWITCHES ON CIRCUIT PACKS LISTED IN TABLE B AND D (IN MANY CASES THESE SWITCHES WILL NOT FAIL UNTIL THE CS IS ACCESSED)
   REF 4: A SHORT IN THE MEMORY MODULE (TRANSFORMER OR INTERNAL LEAD) OR A SHORT ON ANY OF THE CONNECTING LEADS FROM THE STORE TO THE MEMORY MODULE.

2.

-48G	
PACK	LOCATION
A839	L4-23
A941	L0-23

3.

-48G	
PACK	LOCATION
A838	L4-23
A838	L4-21
A838	L4-18
A957	L4-19

4.

-48H	
PACK	LOCATION
A839	L4-32

5.

-48H	
PACK	LOCATION
A838	L2-34
A838	L4-30
A838	L4-27
A920	L4-28

Fig. 15—-48G or -48H Fuse Failure Flowchart

TABLE R

ACCESS CIRCUIT PACKS

CIRCUIT PACK	LOCATION		PURPOSE
	"B" Current Driver Matrix FS7 Sheet B60		
A839	L4-25		1.2 amp current driver
A838	L4-23		Isolation switch for current driver
A957	L4-19		Read access matrix board
A838	L4-21		Write address switches
A838	L4-18		Read address switches
	"B" Access Bridge Drive Matrix FS9 Sheet B68		
A839	L4-32		1.2 amp current driver
A838	L2-34		Isolation switch for current driver
A920	L4-28		Access matrix board
A838	L4-27		Address switches
A838	L4-30		Address switches
	LEFT B81	RIGHT B82	
	"A" Vertical Primary Matrix FS15		
A841	L0-34	L8-34	.6 amp current driver
A838	L2-34	L6-34	Isolation switch for current driver
A921	L2-32	L6-32	Waveform control board
A847	L2-28	L6-28	Address decoder
A847	L2-29	L6-29	Address decoder
A840	L2-30	L6-30	Diode bridge rectifier
	LEFT B75	RIGHT B76	
	"A" Horizontal Primary Matrix FS13		
A847	L0-27	L8-27	Address decoder
A847	L0-29	L8-29	Address decoder
A920	L0-28	L8-28	Access matrix board
	LEFT B71	RIGHT B72	
	"A" Access Bridge Drive Matrix FS11		
A847	L0-30	L8-30	Address decoder
A847	L0-32	L8-32	Address decoder
A920	L0-31	L8-31	Access matrix board

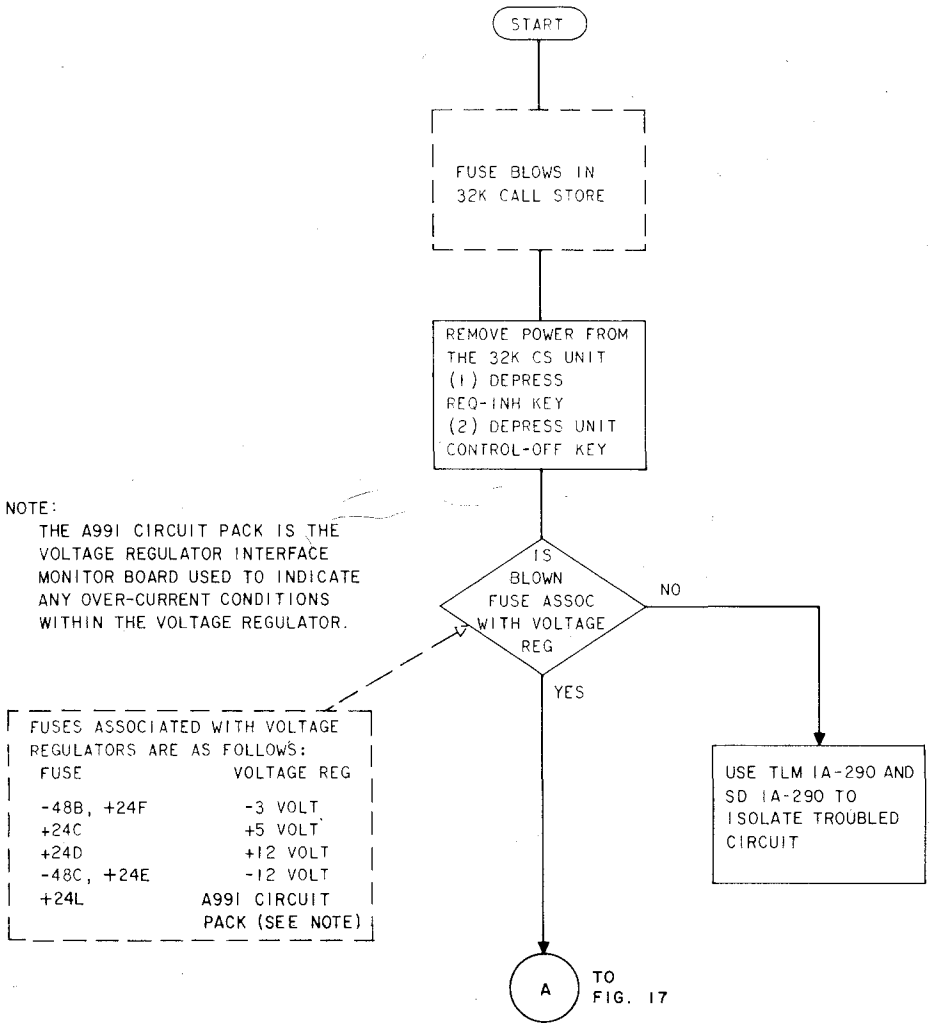


Fig. 16—Blown Fuse Procedure Flowchart

TABLE S

VOLTAGE REGULATOR CIRCUIT PACKS

CIRCUIT PACK DESIGNATION	CIRCUIT PACK LOCATION
A957	L4-19
A920	L4-28
A841	L8-34, L0-34
A839	L4-32, L4-25
A838	L6-34, L4-30, L4-27, L4-23, L4-21, L4-18, L2-34
A991	L8-37

TABLE T

REMOTE SENSE LEAP CONTINUITY

VOLTAGE REGULATOR CIRCUIT BOARDS		CONNECTOR VR-00	CONNECTOR PWR-00	VOLTAGE DISTRIBUTION 905 TYPE CONNECTORS	
ED NO.	TERM NO.	TERM NO.	TERM NO.	LOCATION	TERM NO.
−3V REG. ED-1A-268	3	A	A	L2-33	14
	4	B	B		GT
+5V REG. ED-1A-270	3	E	E	L8-33	0
	4	F	F		GB
+12V REG. ED-1A-272	3	K	K	L6-33	14
	4	L	L		GT
−12V REG. ED-1A-273	3	P	P	L6-33	0
	4	R	R		GB

Note: *GT* indicates Ground Top; *GB* indicates Ground Bottom.

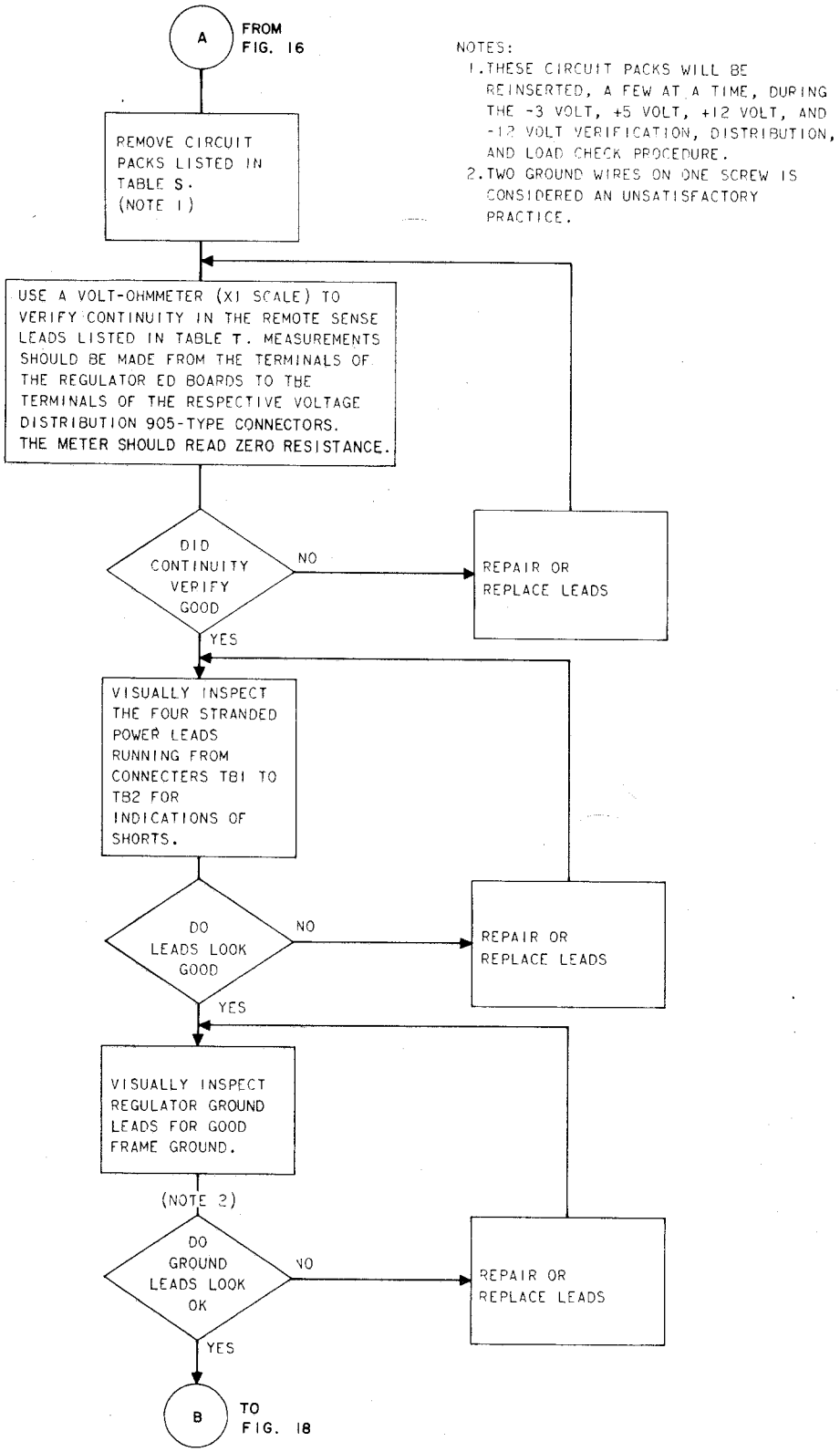


Fig. 17—Voltage Regulator Continuity Check Procedure Flowchart

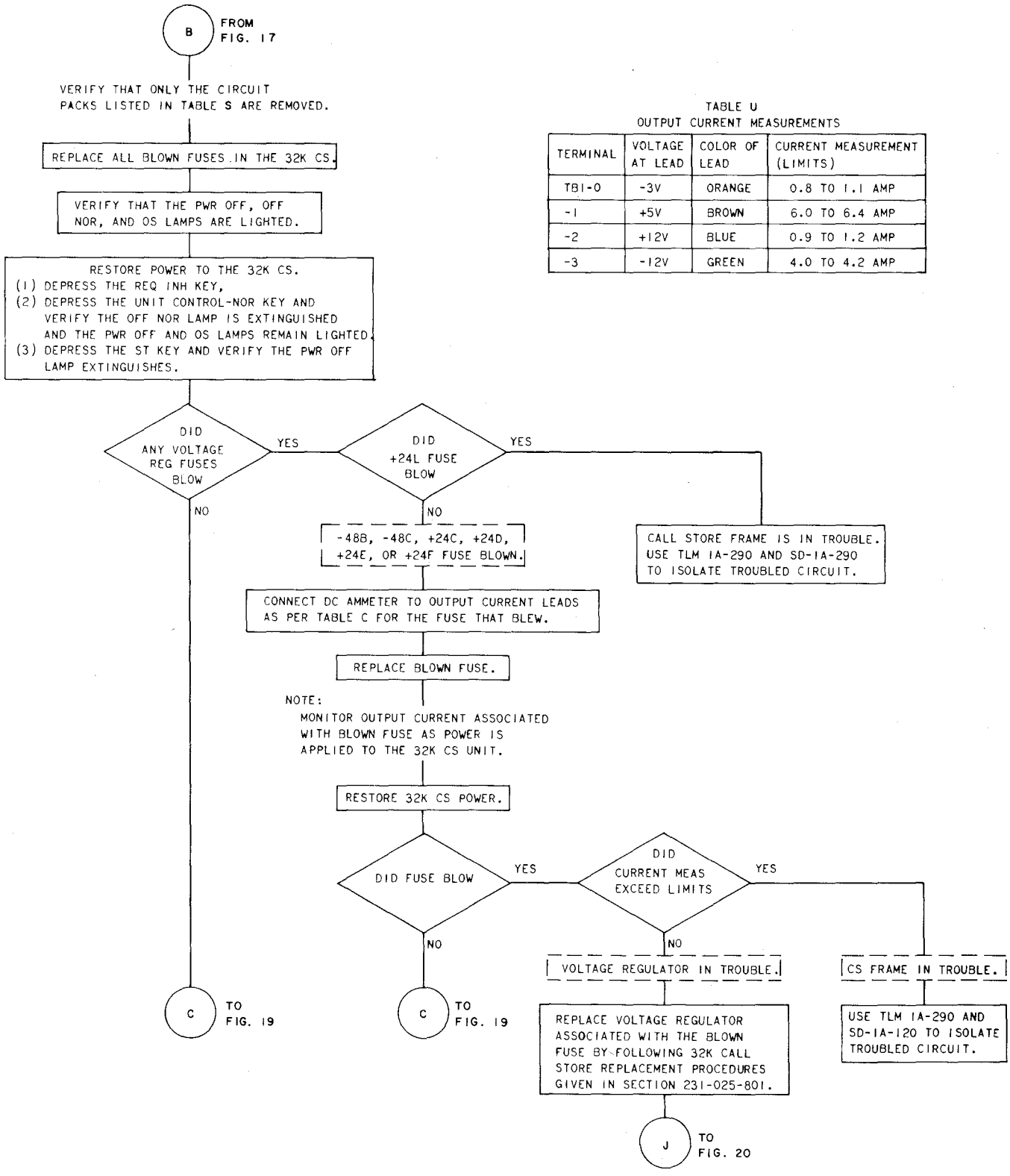


TABLE U
OUTPUT CURRENT MEASUREMENTS

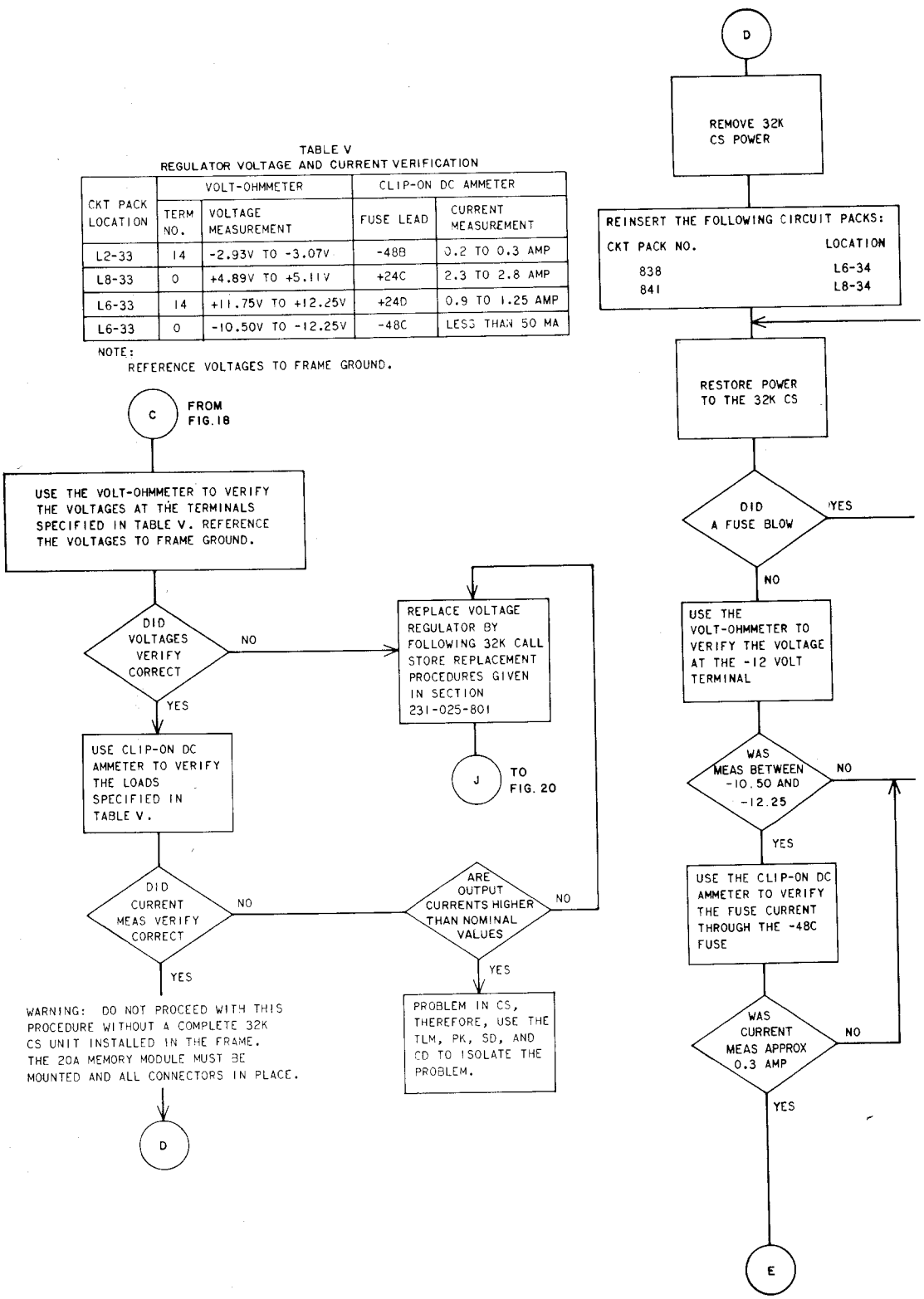
TERMINAL	VOLTAGE AT LEAD	COLOR OF LEAD	CURRENT MEASUREMENT (LIMITS)
TB1-0	-3V	ORANGE	0.8 TO 1.1 AMP
-1	+5V	BROWN	6.0 TO 6.4 AMP
-2	+12V	BLUE	0.9 TO 1.2 AMP
-3	-12V	GREEN	4.0 TO 4.2 AMP

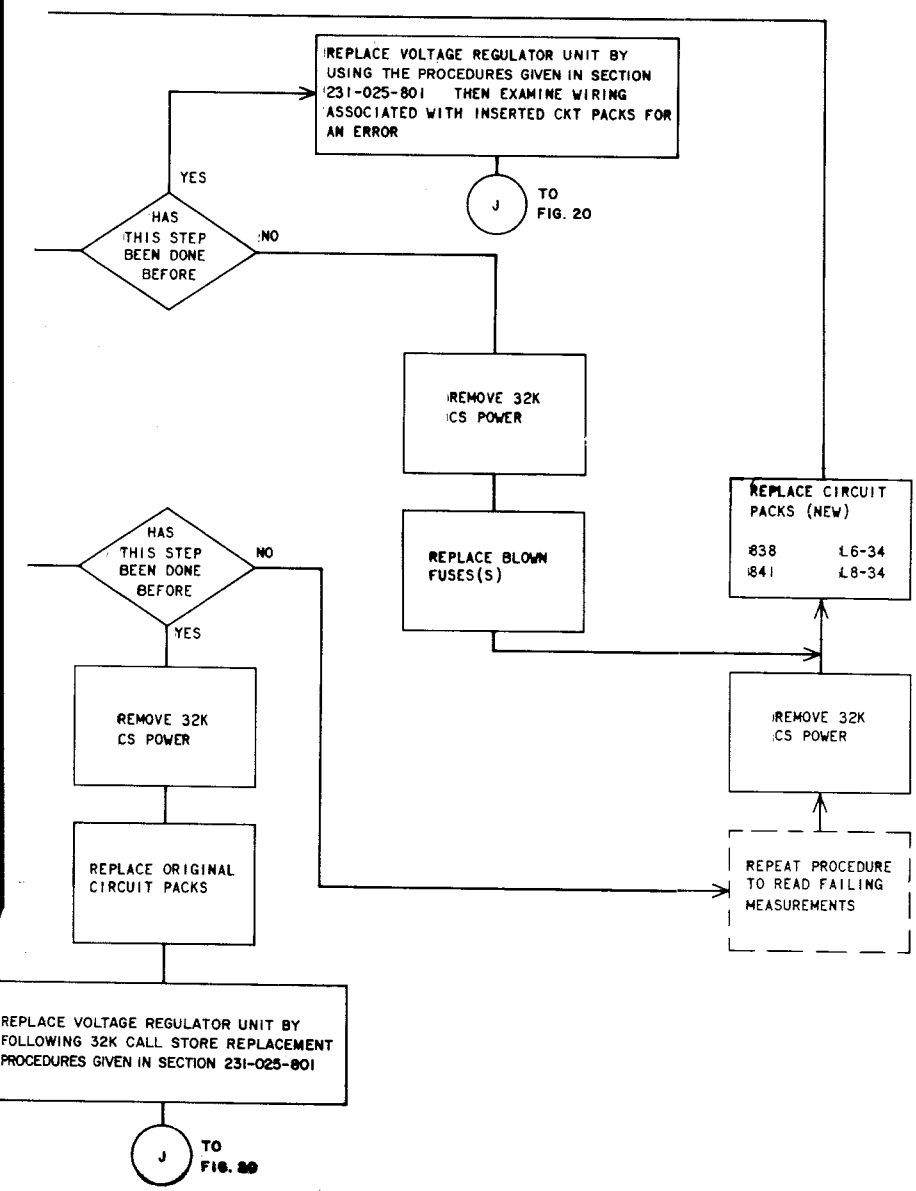
Fig. 18—+24 Volt and -48 Volt Control Check Procedure Flowchart (Table U Included)

TABLE V
REGULATOR VOLTAGE AND CURRENT VERIFICATION

CKT PACK LOCATION	VOLT-OHMMETER		CLIP-ON DC AMMETER	
	TERM NO.	VOLTAGE MEASUREMENT	FUSE LEAD	CURRENT MEASUREMENT
L2-33	14	-2.93V TO -3.07V	-48B	0.2 TO 0.3 AMP
L8-33	0	+4.89V TO +5.11V	+24C	2.3 TO 2.8 AMP
L6-33	14	+11.75V TO +12.25V	+24D	0.9 TO 1.25 AMP
L6-33	0	-10.50V TO -12.25V	-48C	LESS THAN 50 MA

NOTE:
REFERENCE VOLTAGES TO FRAME GROUND.




REPLACE VOLTAGE REGULATOR UNIT BY USING THE PROCEDURES GIVEN IN SECTION 231-025-801 THEN EXAMINE WIRING ASSOCIATED WITH INSERTED CKT PACKS FOR AN ERROR
J
TO FIG. 20
YES
HAS THIS STEP BEEN DONE BEFORE
NO
REMOVE 32K CS POWER
REPLACE BLOWN FUSES(S)
REPLACE CIRCUIT PACKS (NEW)
838 L6-34
841 L8-34
HAS THIS STEP BEEN DONE BEFORE
NO
YES
REMOVE 32K CS POWER
REPLACE ORIGINAL CIRCUIT PACKS
REMOVE 32K CS POWER
REPEAT PROCEDURE TO READ FAILING MEASUREMENTS
REPLACE VOLTAGE REGULATOR UNIT BY FOLLOWING 32K CALL STORE REPLACEMENT PROCEDURES GIVEN IN SECTION 231-025-801
J
TO FIG. 20

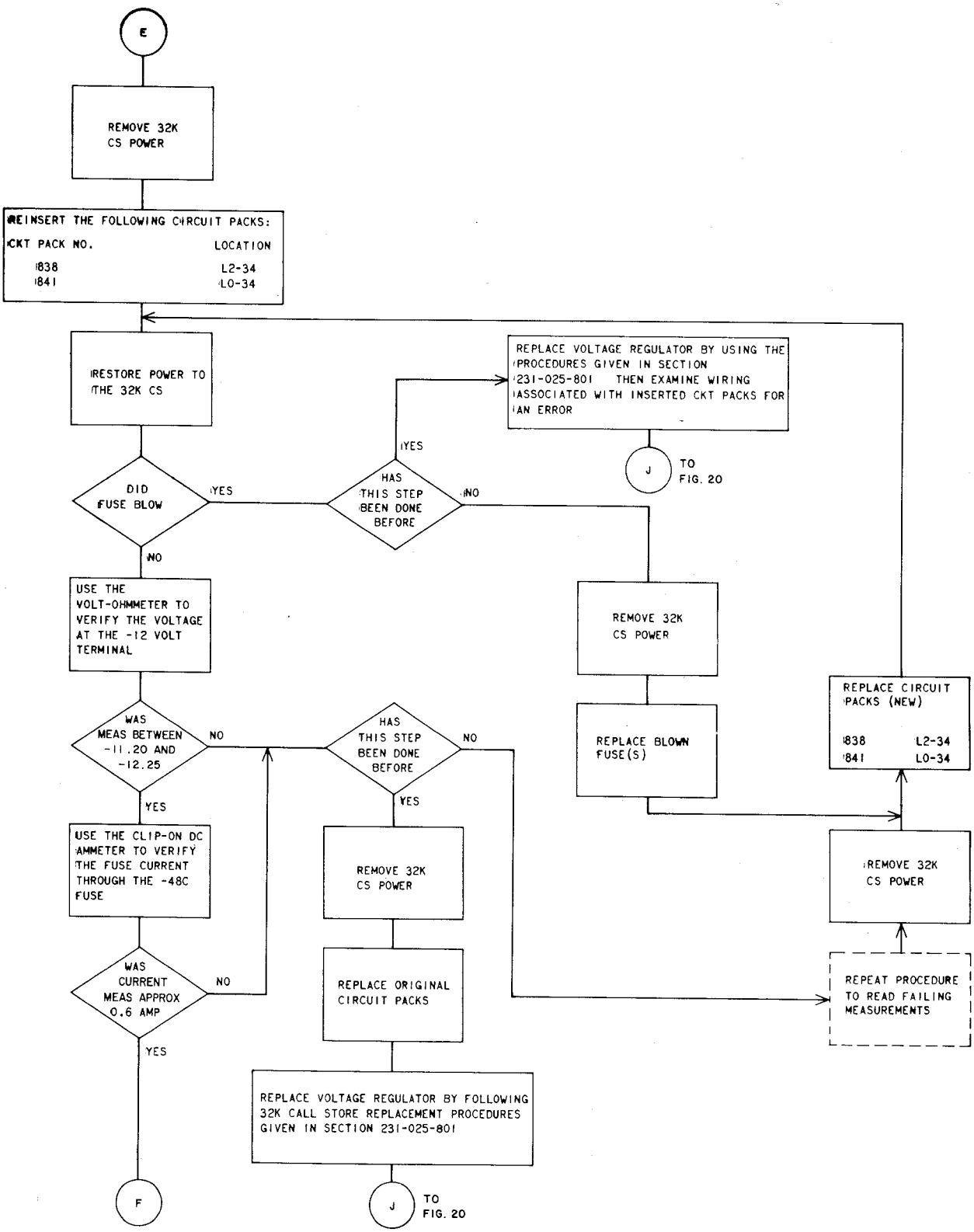
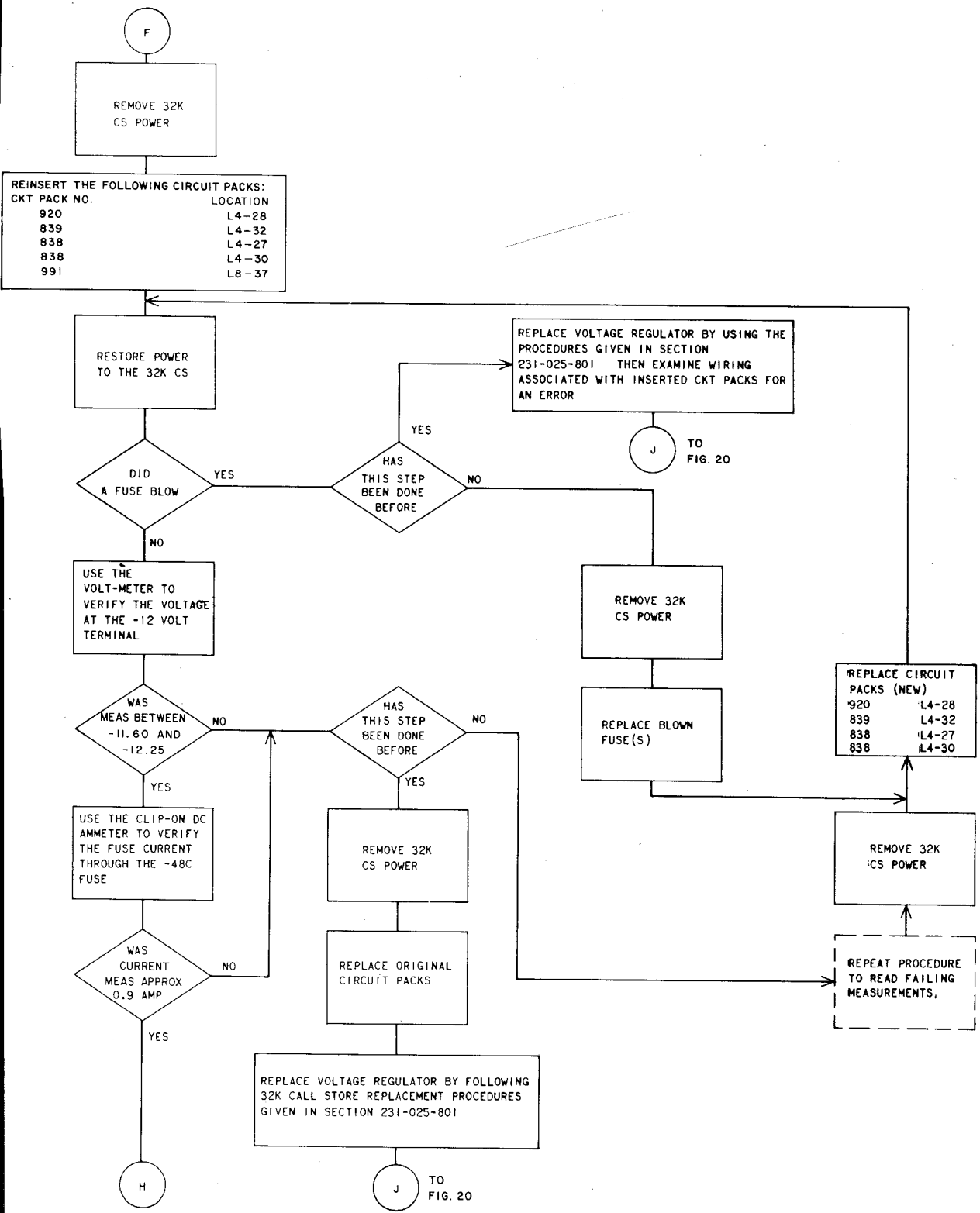


Fig. 19—3 Volt, +5 Volt, +12 Volt and -12 Volt Verification, Distribution and Load Check Procedure Flowchart (Table V Included) (Sheet 1 of 2)


F
REMOVE 32K CS POWER
REINSERT THE FOLLOWING CIRCUIT PACKS:
CKT PACK NO. LOCATION
920 L4-28
839 L4-32
838 L4-27
838 L4-30
991 L8-37
RESTORE POWER TO THE 32K CS
DID A FUSE BLOW
YES
NO
HAS THIS STEP BEEN DONE BEFORE
YES
NO
REPLACE VOLTAGE REGULATOR BY USING THE PROCEDURES GIVEN IN SECTION 231-025-801 THEN EXAMINE WIRING ASSOCIATED WITH INSERTED CKT PACKS FOR AN ERROR
J
TO FIG. 20
USE THE VOLT-METER TO VERIFY THE VOLTAGE AT THE -12 VOLT TERMINAL
WAS MEAS BETWEEN -11.60 AND -12.25
NO
YES
HAS THIS STEP BEEN DONE BEFORE
NO
YES
REMOVE 32K CS POWER
REPLACE BLOWN FUSE(S)
REPLACE CIRCUIT PACKS (NEW)
920 L4-28
839 L4-32
838 L4-27
838 L4-30
REMOVE 32K CS POWER
USE THE CLIP-ON DC AMMETER TO VERIFY THE FUSE CURRENT THROUGH THE -48C FUSE
WAS CURRENT MEAS APPROX 0.9 AMP
NO
YES
REMOVE 32K CS POWER
REPLACE ORIGINAL CIRCUIT PACKS
REPEAT PROCEDURE TO READ FAILING MEASUREMENTS,
REPLACE VOLTAGE REGULATOR BY FOLLOWING 32K CALL STORE REPLACEMENT PROCEDURES GIVEN IN SECTION 231-025-801
H
J
TO FIG. 20

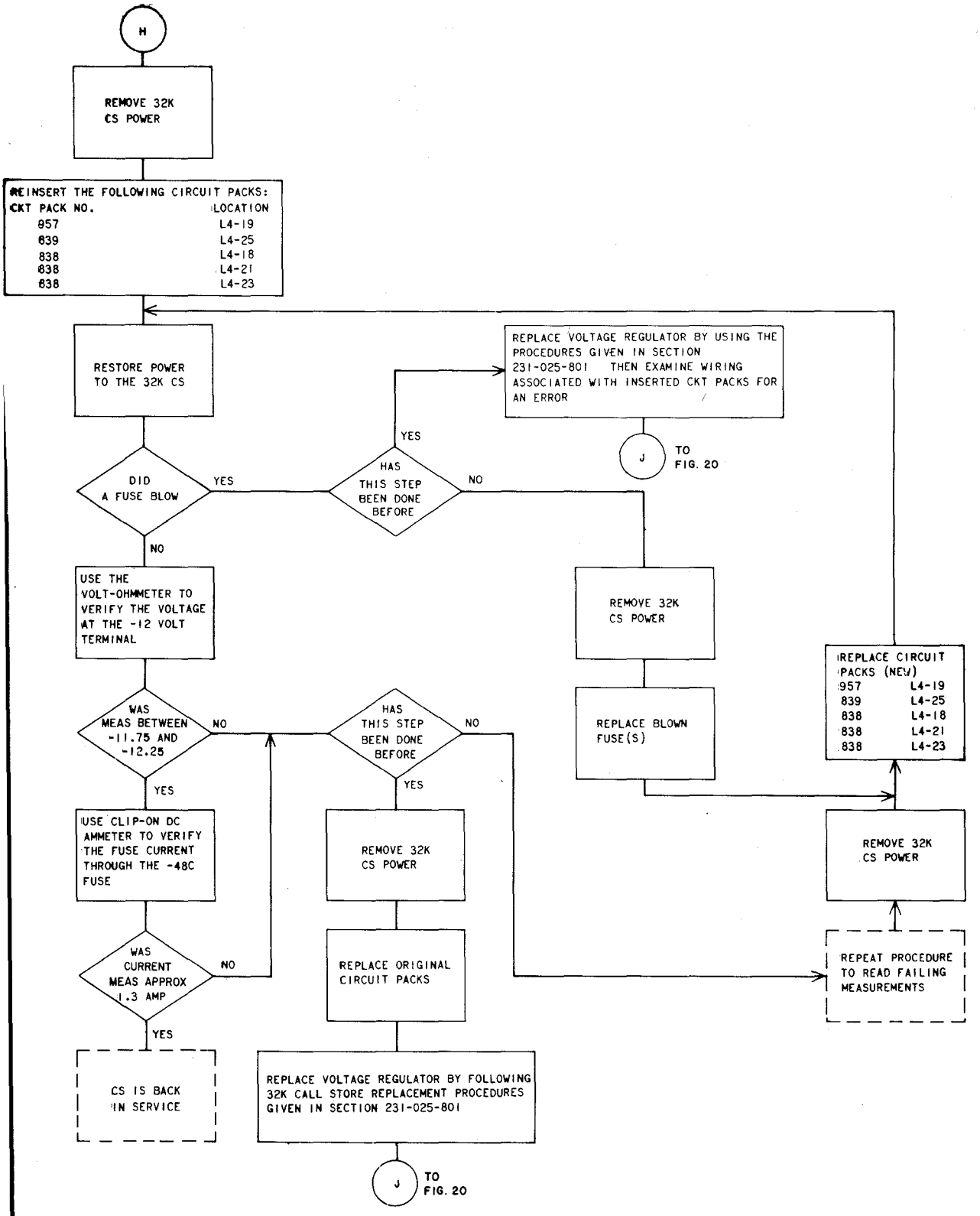


Fig. 19—-3 Volt, +5 Volt, +12 Volt and -12 Volt Verification, Distribution and Load Check Procedure Flowchart (Table J Included) (Sheet 2 of 2)

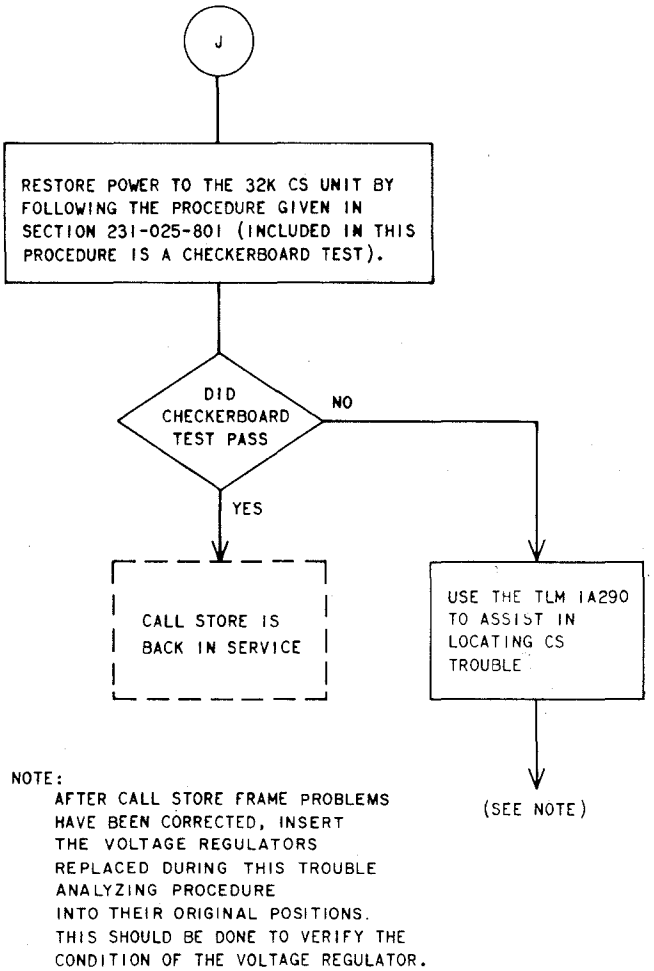


Fig. 20—Returning 32K Call Store To Service