

**CENTRAL PULSE DISTRIBUTOR  
DESCRIPTION**

**NO. 1 AND NO. 1A ELECTRONIC SWITCHING SYSTEMS**

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**NOTICE**

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**1. GENERAL**

**1.01** This section describes the Central Pulse Distributor (CPD) used in the 2-Wire No. 1 and No. 1A Electronic Switching System (ESS) and the 4-wire No. 1 ESS. The CPDs provide central control (CC) with a fast control of many points throughout the central office. CPDs are completely duplicated. This section replaces Section 231-008-101 and schematic diagram SD-1A109-01.

**1.02** When this section is reissued, the reasons for reissue will be listed in this paragraph.

**1.03** Upon receiving an order from CC or SP (No. 1 ESS), a CPD selects and pulses one of the outputs specified by the address from CC or SP (No. 1 ESS). Outputs from the CPD may be unipolar (pulses of only one polarity) or bipolar (pulses of either polarity).

**1.04** The interconnections between CC and CPDs are shown in Fig. 1. The CC determines whether bus 1 or bus 0 is to be used and transmits a signal to all CPDs over the bus choice lead of that bus. Then via the chosen bus, CC transmits an address which is received and stored by all CPDs. The address consists of three parts: a 1-out-of-8 X code, a 1-out-of-8 Y code, and a 1-out-of-16 Z code. The address information specifies one of the unipolar outputs or one of the bipolar outputs and the polarity of the pulse to be supplied

by it. Finally, CC transmits an execute signal over a private path to the CPD that is to execute the order.

**1.05** The basic organization of a CPD is shown in Fig. 2. The predecoder, decoder, and matrix are three consecutive stages of selection. In each stage, an output is activated when one of the horizontal inputs and one of the vertical inputs are activated in coincidence.

**1.06** When a peripheral unit controller receives an enable pulse from a unipolar CPD output, it returns a verify signal over the same path. The matrix steers this verify signal to the encoder which translates it into a verify answer in a 1-out-of-8 X code, a 1-out-of-8 Y code, and a 1-out-of-8 Z code. The verify answer is sent to CC where it is compared with the enable address initially transmitted.

**2. EQUIPMENT DESCRIPTION**

**MECHANICAL**

**2.01** A double-bay frame is used to mount CPDs. Each bay contains a complete CPD and also includes the bus input, bus distribution, and bus termination (communication bus apparatus) which occupy five 4-inch mounting areas at the top of the frame. Figure 3 shows one bay of the double-bay CPD frame.

**2.02** Bay 0 of the two-bay frame mounts the even-numbered CPD, and Bay 1 mounts the odd-numbered CPD. The two CPDs on a frame work as mates.

**ELECTRICAL**

**2.03** The CPDs are composed of transistorized circuit packs. These circuit packs provide the electronic gates and flip-flops. In the CPD circuit, these circuit packs operate as output gates, encoders, and decoders for interrogating and controlling peripheral units.

**2.04** There may be as many as 768 outputs from a CPD. Of these outputs, 512 are normally unipolar and 256 are bipolar. This capacity for bipolar and unipolar outputs from a single CPD is the same wherever used. The unipolar outputs may be converted to bipolar operation. In this case, the total number of outputs will be reduced

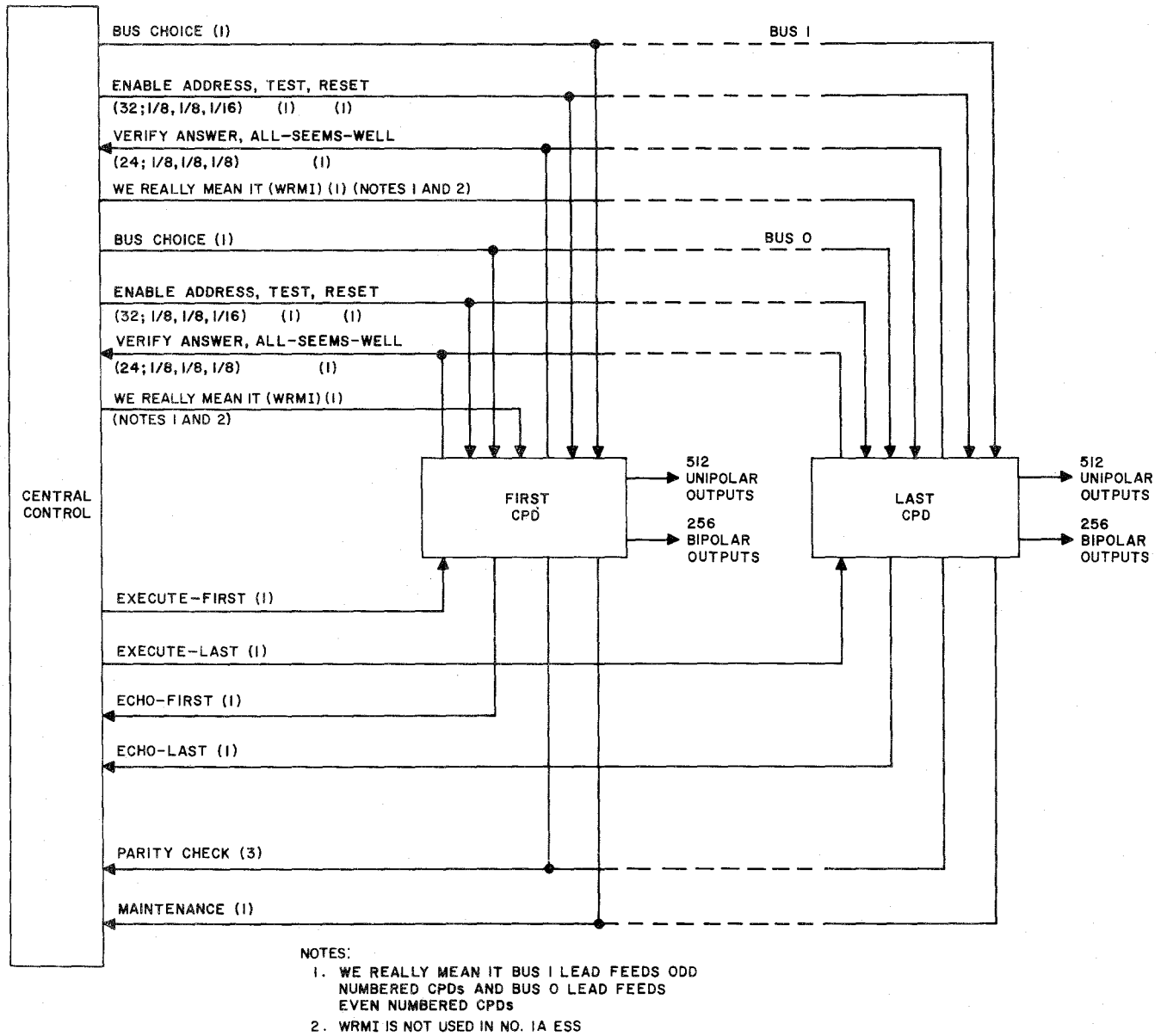


Fig. 1—Communication Between Central Control and Central Pulse Distributors

on a basis of one bipolar replacing two unipolar outputs. Unipolar outputs are used mainly to enable peripheral units, while bipolar outputs are used to control flip-flops and other logic circuits in various units. All the outputs are connected over private paths to the points controlled by the CPD. The minimum interval between consecutive requests

from CC to a CPD is 11 microseconds in No. 1 ESS and 7 microseconds in No. 1A ESS.

2.05 The CPDs are used in varying numbers with 2-wire or 4-wire systems as the traffic demands. As the traffic increases and more switching frames and other networks are required, more

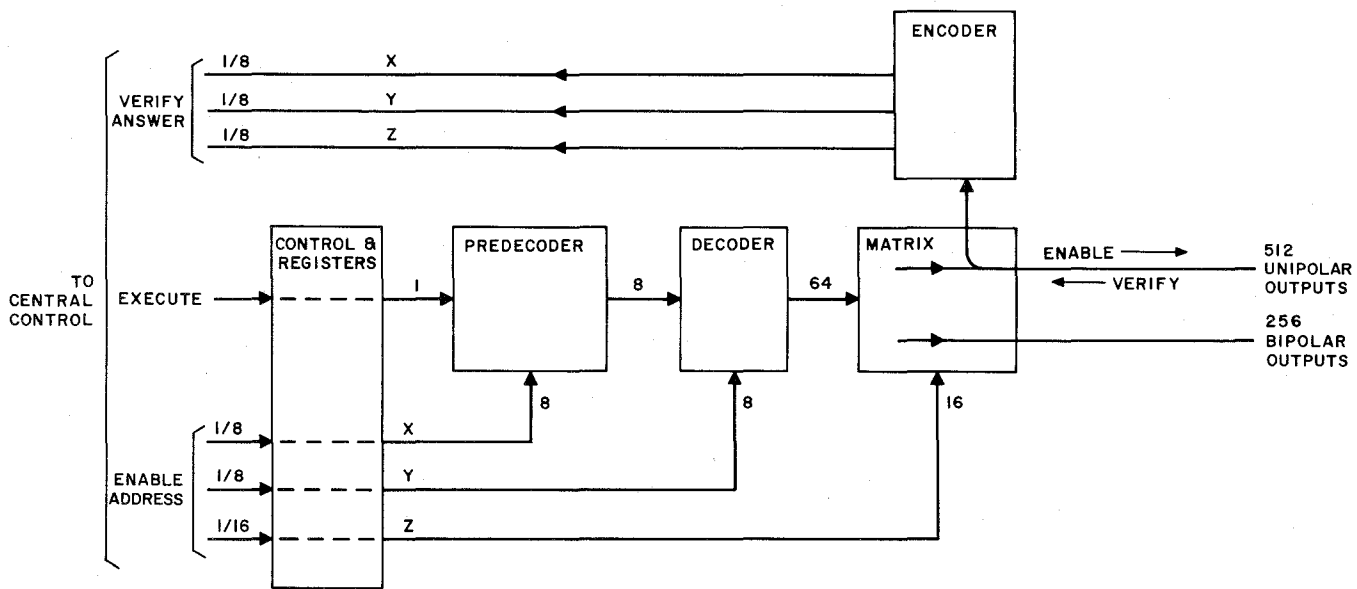


Fig. 2—Basic Central Pulse Distributor

CPDs can be added. The CPDs are provided two to a frame. Up to eight frames of CPDs may be used in a system, bringing the total of CPDs to 16. In the larger systems, CPDs will be grouped into peripheral unit communities to simplify the control function.

**2.06** In most 2-Wire No. 1 ESS systems, signal processors are provided to increase the traffic handling capacity of the central office. The signal processors operate in conjunction with the CC part of the No. 1 ESS. The CPDs operate with a signal processor in the same manner as with the CCs. The signal processor is not used in No. 1A ESS.

**2.07** Power for the CPD operation is derived from the No. 1 ESS via the power distribution circuit. Each pair of CPDs is supplied with +24 volts over the two power buses. The power for the even-numbered CPD is fed by the +24 volt 0 bus, while the odd-numbered CPD is fed by the +24 volt 1 bus. Fuses and filters for the +24 volts are located at the bottom of the CPD frame.

#### PERIPHERAL UNIT BUS CONTROL

**2.08** The peripheral unit address (PUA) bus is controlled from CPD frames. The circuit is covered in SD-1A119-01. The PUA-0 bus is controlled

from even-numbered CPD frames, and the PUA-1 bus is controlled from odd-numbered CPD frames. To remove power from the PUA-0 bus, the BUS 0 DISTRIBUTION-OFF key on all even-numbered CPD frame control panels must be operated. The PUA-1 bus is controlled by the BUS 1 DISTRIBUTION-OFF key on all odd-numbered CPD frame control panels. The control panel is shown in Fig. 16.

### 3. FUNCTIONAL DESCRIPTION

#### BASIC CENTRAL PULSE DISTRIBUTOR

**3.01** The basic CPD is a matrix of 1024 high-speed, low-level pulsing sources which can provide 256 bipolar and 512 unipolar output pulses. The bipolar output pulse is transmitted over a single twisted wire pair and requires two CPD matrix points to produce a pulse that can be either positive or negative. The unipolar output pulse is also transmitted over a single twisted wire pair. One point in the matrix is required for each unipolar output. The assignment of unipolar and bipolar points is covered in SD-1A270-01 for No. 1 ESS and SD-6A270-01 for No. 1A ESS.

**3.02** The bipolar matrix points are assigned in pairs: one point is in the even CPD and the other is in the odd CPD (of the CPD pair)

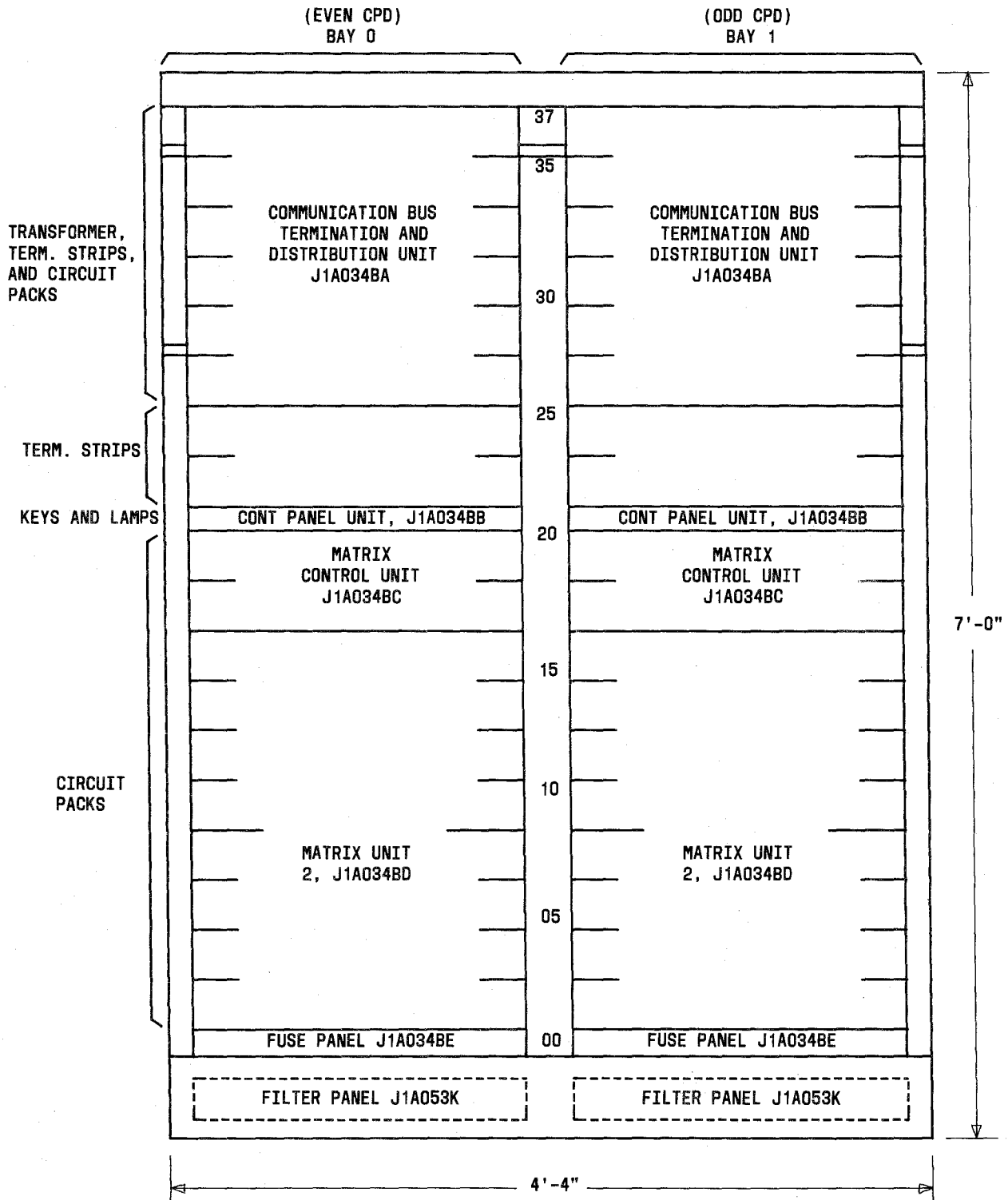


Fig. 3—Central Pulse Distributor Frame

and in the same position on the matrix. These two points are wired together. Bipolar outputs are always multiplied except for the inhibit point in the mate CPD.

**3.03** Bipolar points for any given circuit are to be assigned in groups and in consecutive locations within the same half. The zero point in the group is assigned to the lowest numbered address being assigned.

**3.04** Bipolar points connect the matrix output pulses being used to control flip-flops in the trunk, in service circuits, and in the various units via twisted pair switchboard cable. These signals are used to control some of the following circuits:

- (a) (No. 1 ESS only) Receive-only, trouble flip-flops in the program store and call store
- (b) (No. 1 ESS only) Lamps and relays in the master control center
- (c) Relays in trunk and service circuits, such as, dial pulse, transmitter, or digit receiver
- (d) Other points in the CPD for inhibit and test purposes.

**3.05** Unipolar point assignments start at the lowest numerical address, that is, in group 0, row 0, and column 0. A given group is arranged to accommodate either unipolar or bipolar points. The group cannot be shared by the two types of points.

**3.06** Unipolar points connect the matrix output pulses used to enable the circuits of frames served by the peripheral bus. The majority of units that use enable CPD points have duplicate controllers. For each controller two outputs are provided: one for enabling bus 0 and one for enabling bus 1. These enable pulses in a No. 1 ESS are used to activate controllers for the scanner, signal distributor, network, teletypewriters, and automatic message accounting (AMA) recorders (tape units in 1A Processor).

**3.07** The CPD also has special output points that are wired internally to permit test exercising of the CPD, inhibiting a faulty CPD, and testing the bus fanout circuitry in the communication bus circuit.

## Operation

**3.08** Time relationships are very important in the operation of the CPD. Timing diagrams for peripheral operation are shown in Fig. 4 and 5. When a peripheral unit is enabled by a unipolar output pulse, the mechanism which recognizes the enabling triggers a 2.2-microsecond pulse referred to as a peripheral unit address window pulse. The address for this peripheral unit is transmitted from CC on the peripheral unit address bus and must arrive during the time that this window is open. For this reason, the address and enable signals must arrive at the peripheral unit within this window pulse.

**3.09** Two factors control the time coincidence of address and enable pulses. One factor is the time of transmission from the CC which can be strictly controlled. The other factor is the time delay due to the length of the cabling of the peripheral unit address bus and the enable leads which pass through the office.

**3.10** To control the length of cable for the peripheral unit address bus and the enable leads in all sizes of offices, the CPD frame is used as a distribution center. In this way the distance and, therefore, the time delay between the point of transmission (the CC through the CPD frame) to the peripheral unit are the same for both the address and enable signals.

**3.11** The CPD requires three communications in rapid succession from CC: the bus choice, the enable address, and the execute signal (Fig. 6 and 7).

**3.12** The 0.5-microsecond bus choice pulse from the CC specifies which of the two buses will be used to transfer information. In addition to this, the bus choice pulse indicates to the system that an address will be sent within the next 1.25-microsecond time slot. The bus choice pulse is stretched from 0.5 microsecond to 1.8 microseconds by pulse shaping amplifiers. This stretched pulse is used as an enable pulse for the gating of the address into the registers.

**3.13** The bus choice pulse also sets or resets the bus choice flip-flop which is used to gate the answer-back signals to the same bus from which the address information is received. In addition to setting or resetting the bus choice

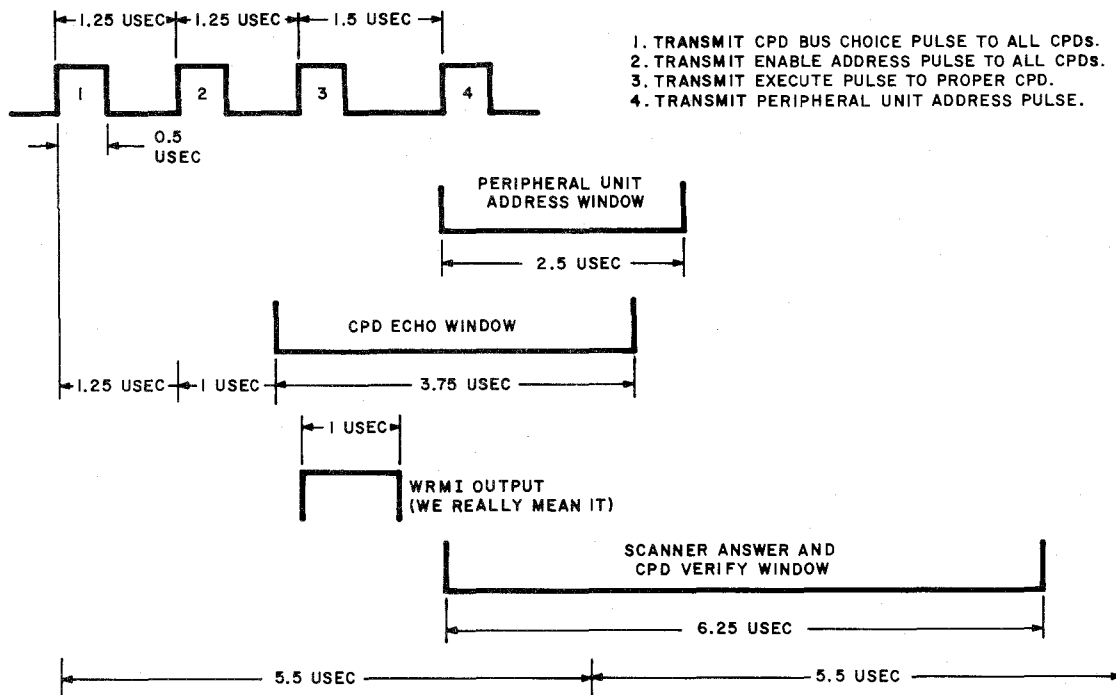


Fig. 4—No. 1 ESS Peripheral System Timing for Non Speeded Up Periphery

flip-flop, the bus choice pulse causes a strobing pulse which checks sampling for parity by the state of inputs to the X, Y, and Z circuitry.

**3.14** When the address pulses arrive from CC and are registered, the CPD control circuitry makes a parity check to determine whether a legitimate address has been received. The address is registered long enough to enable the execute pulse to activate the corresponding matrix output.

**3.15** When the execute pulse is received from CC, it is reshaped and applied to the predecoder input if the address parity check has been successful. The reshaped execute pulse is transmitted from the decoder input to the matrix output via three transformer-coupled stages. In

addition, the 0.5-microsecond execute pulse (see timing in Fig. 7) causes:

- (a) The three parity flip-flops, which were set during the strobing pulse,
- (b) Circuitry to enable the answer-back bus
- (c) An echo pulse to be returned to CC which verifies that the execute pulse has been received by the proper CPD
- (d) A we-really-mean-it (WRMI) pulse to be transmitted to peripheral and other units (WRMI is not used in No. 1A ESS)
- (e) The results of the X, Y, and Z parity checks to be transmitted to CC.

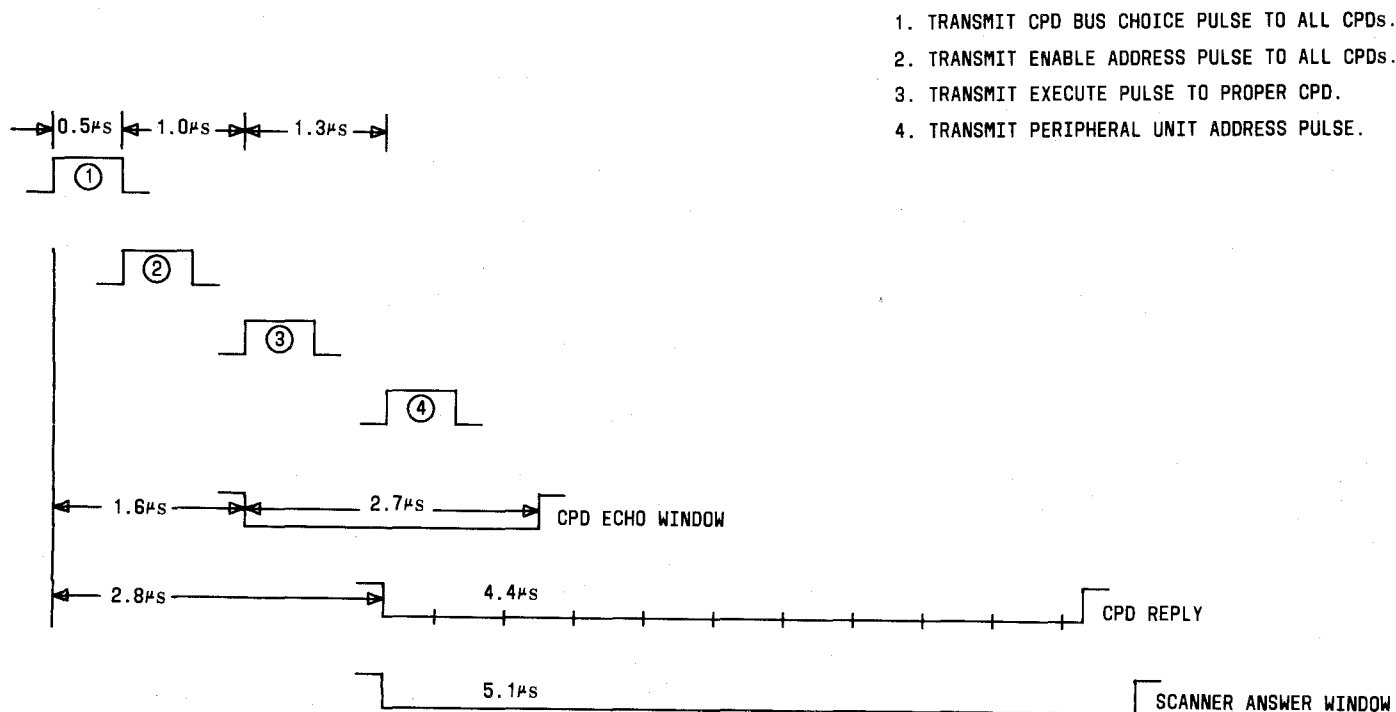


Fig. 5—Peripheral System Timing for No. 1 and No. 1A ESS

**COMMUNICATION****No. 1 ESS Central Control to Central Pulse Distributor to Peripheral Unit**

**3.16** Communications from the No. 1 ESS CC to the peripheral units via the CPD are shown in Fig. 8. The CPD bus choice is made in the CC by setting the appropriate flip-flop in the buffer bus register to make either bus 1 or bus 0 active. The active bus will transmit the address information to the CPD.

**3.17** The CPD enable address is generated in the enable address translator. This translator receives its inputs from bit positions  $F_{14}$  to  $F_{22}$  and  $F_9$  of the CC F register. (See notes in Fig. 9). The translator converts this binary address to 1/8,

1/8, and 1/16 codes which are sent to the CPD (Fig. 8).

**3.18** The CPD execute pulse comes from the execute translator. The execute translator receives its input from bit positions  $F_{10}$  to  $F_{13}$  in the F register. The execute translator converts this binary code to a 1/16 code which will select one of the possible 16 CPDs in the system. The echo signal from the CPD returns to the execute match circuit via the buffer bus register where it is matched with a signal from the execute translator. This execute match circuit will indicate whether the appropriate CPD returned the echo signal. If the appropriate CPD did not return the echo signal, the CC will take maintenance action.

**3.19** The peripheral unit address is generated in the peripheral address translators. The



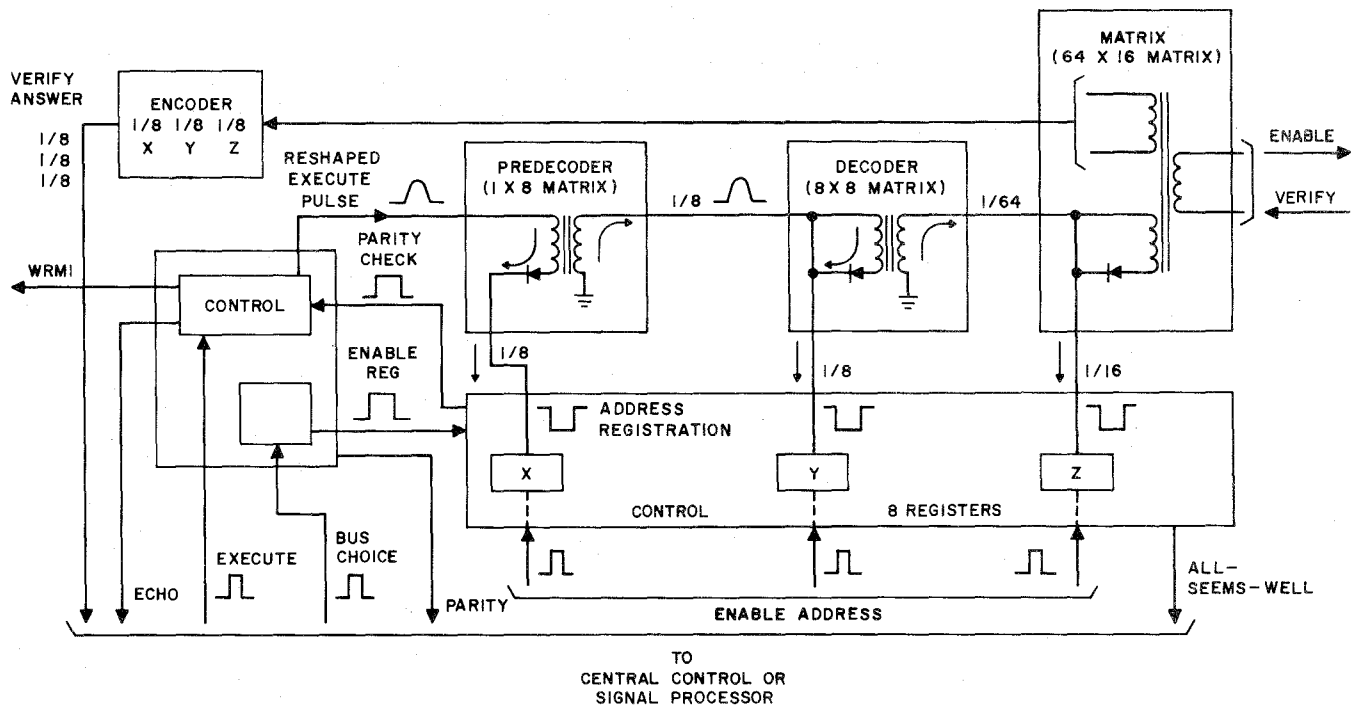


Fig. 6—Central Pulse Distributor Communications from Central Control

peripheral address translators receive inputs from the K register, the addend K register, and the translator selector. The peripheral address translators on orders from the translator selector will arrange the information from the addend K register and the K register into the proper code form before transmitting it on the peripheral unit address bus. This coding is necessary because the addressed peripheral units will not respond unless the information from the peripheral address translators is coded correctly.

**3.20** The inputs to the translator selector come from bit positions  $F_7$  to  $F_9$  in the F register as well as from the order word decoder. Bit positions  $F_7$  to  $F_9$  will tell the translator selector what type of peripheral unit is involved along with the decoded information from the order word decoder.

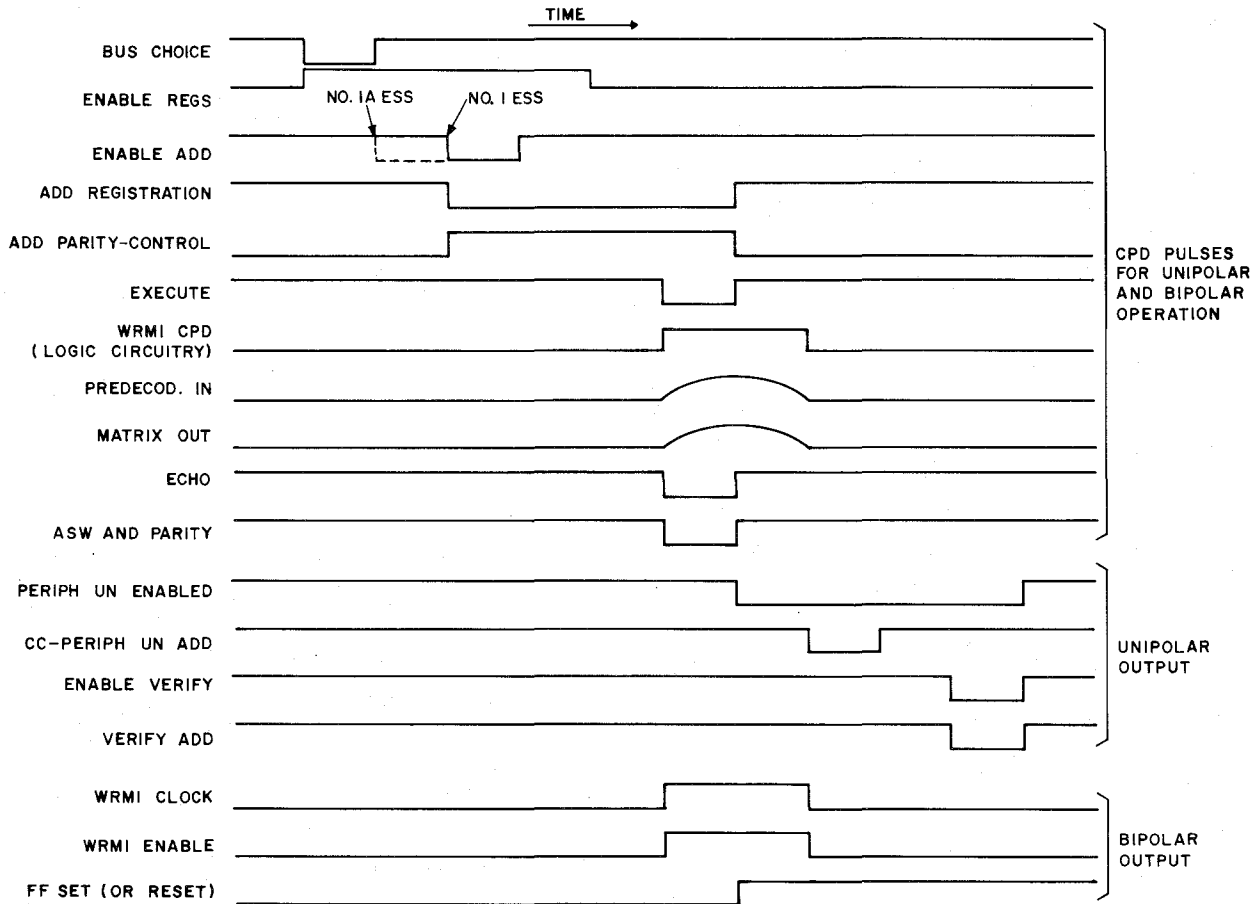
**3.21** The CPD verify answer comes back into the Y register from peripheral units. The Y register in turn has one input to the CPD reply match circuit. The other input to this match circuit comes from the CPD enable address which is

generated in the enable address translator. This CPD reply match circuit will decide if the proper peripheral unit was enabled to receive the peripheral unit address from the CC to the peripheral unit address bus. If the peripheral unit did not receive the proper address, the central processor will initiate maintenance action.

**3.22** The CPD test and reset leads come from the K register. These leads are used to place the CPD in the test mode as well as return the CPD to normal after testing has been completed.

**3.23** The CPD maintenance bus has inputs to the buffer bus register. These inputs include three parity check leads, one maintenance lead, and one all-seems-well (ASW) signal lead. The CC can check the status of these five leads at any time.

**3.24** The scanner answer from ferrod scan points is returned to the L register. The ASW signal from scanners is returned to the buffer bus register. These signal inputs are the result of



## NOTES:

1. THE ENABLE REGS PULSE IS INTERNAL TO THE CPD AND DOES NOT APPEAR ON THE BUS.
2. THE ECHO PULSE APPEARS ON THE BUS AND IS NOT INTERNAL TO CPD.
3. THE FF SET (OR RESET) IS A TIME EVENT AND DOES NOT APPEAR ON THE BUS.
4. WRMI IS NOT USED IN NO. 1A ESS.

Fig. 7—Central Pulse Distributor Timing Sequence Showing Differences in Output Pulses

enabled scanners which have received an address from the CC to the peripheral unit bus system.

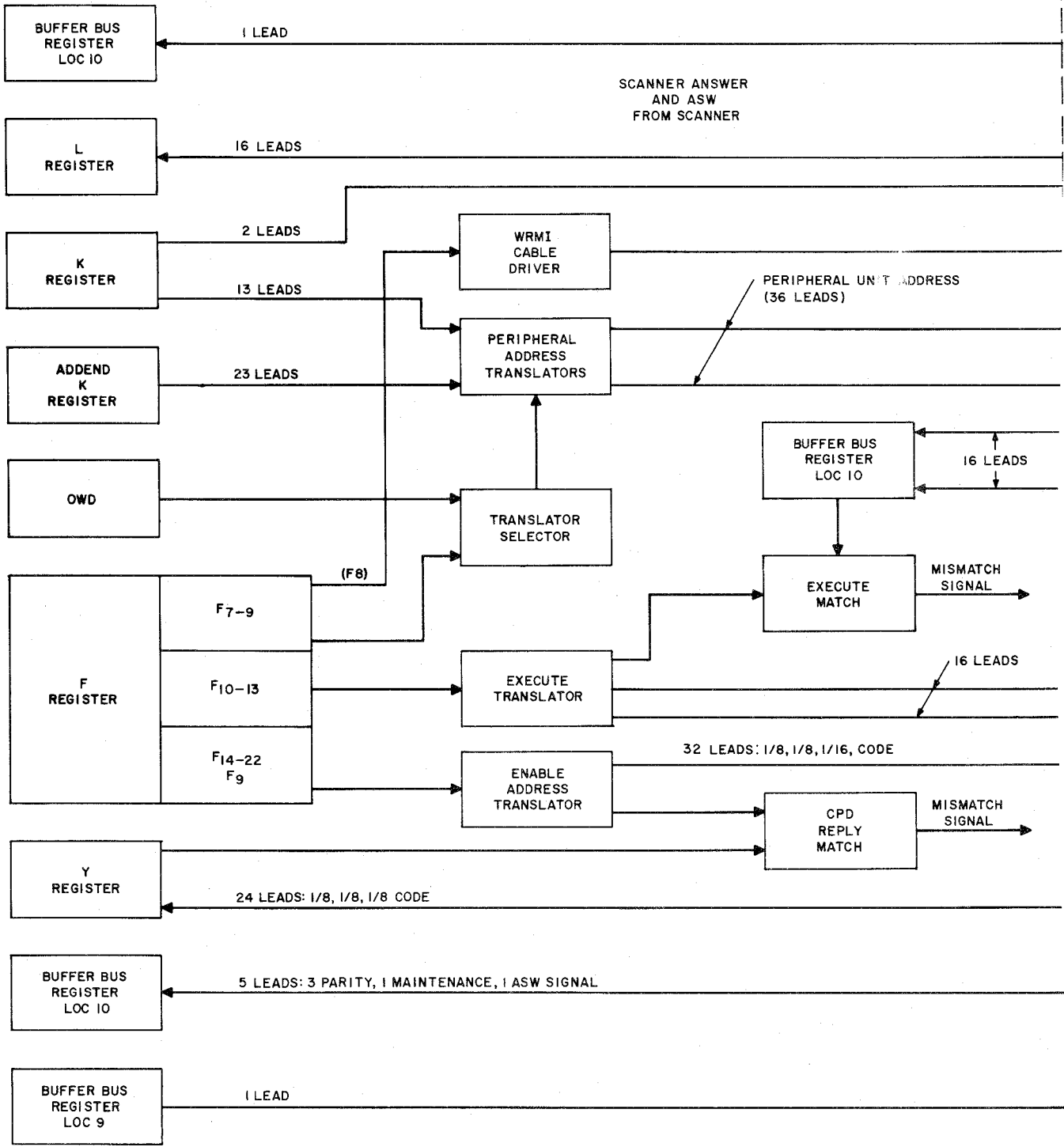
#### No. 1A ESS Central Control to Central Pulse Distributor to Peripheral Unit

3.25 Communications from the No. 1A ESS CC to the peripheral unit via the CPD are shown in Fig. 10. The bus choice signal arrives from the communications bus circuit either on bus 0 or bus 1 and sets or resets the appropriate bus control flip-flop. The active bus will transmit the address information to the CPD.

3.26 The CPD enable address is generated in the CPD address and execute translator except on CPD long binary translations. On CPD long binary translation, bits 0 through 31 of the P register are gated directly to the PU enable address bus. The address translator receives its inputs from bit 9 and bits 14 through 22 of the PU enable register (E register). See notes in Fig. 11. The translator converts this binary address to 1/8, 1/8, and 1/16 codes which are sent to the CPD.

3.27 The CPD execute pulse is also generated in the CPD address and execute translation.

PART OF CENTRAL CONTROL



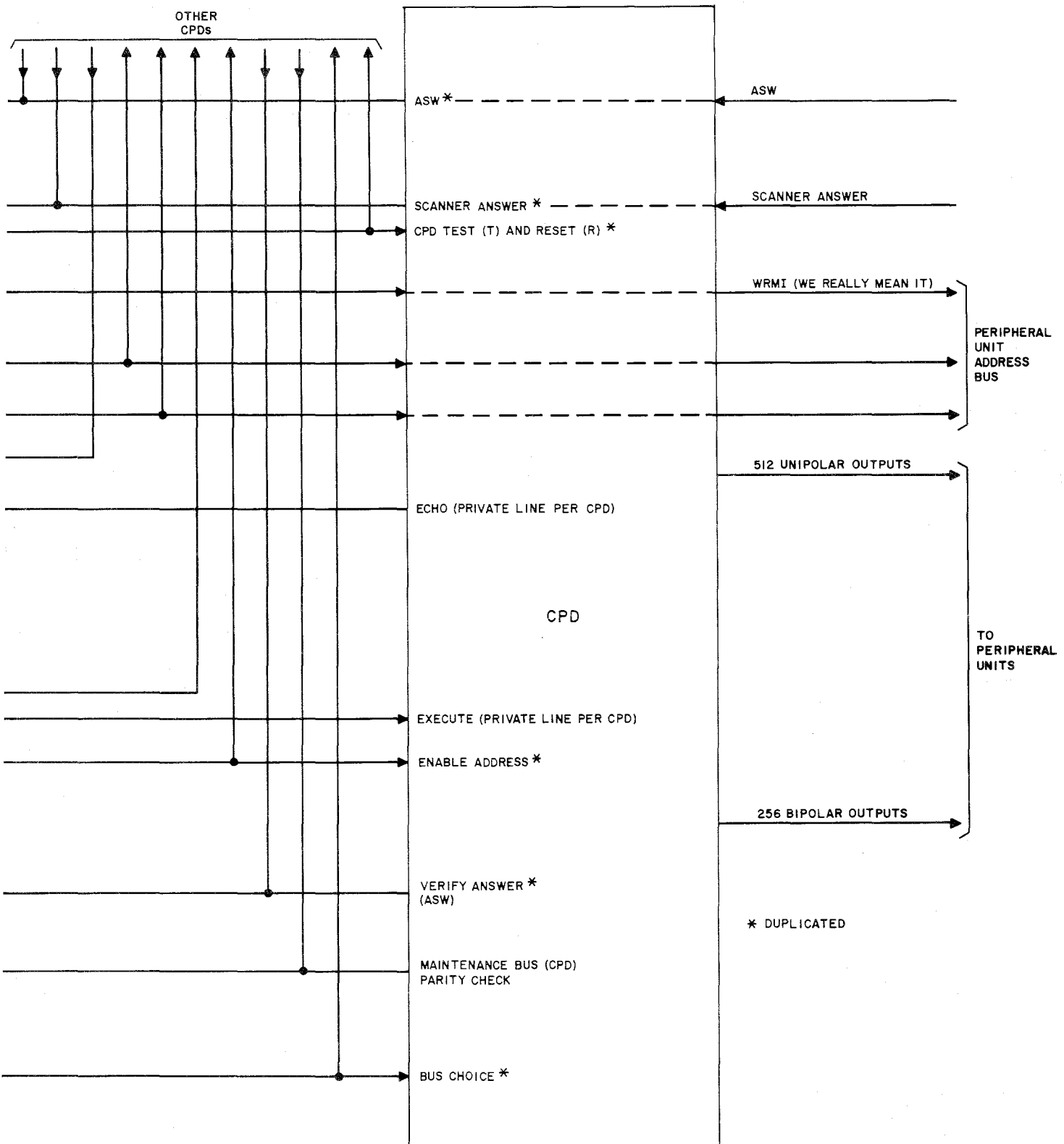
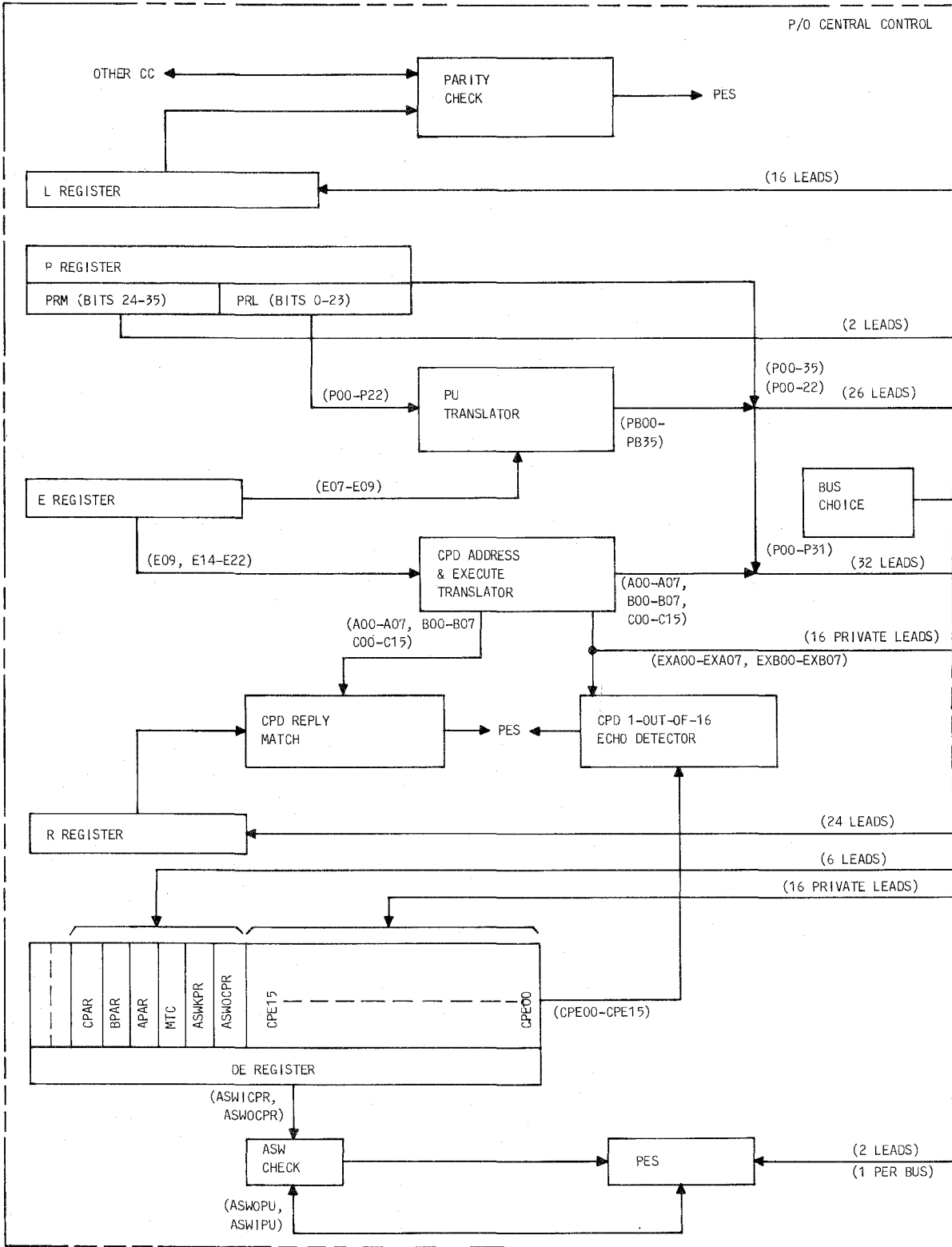
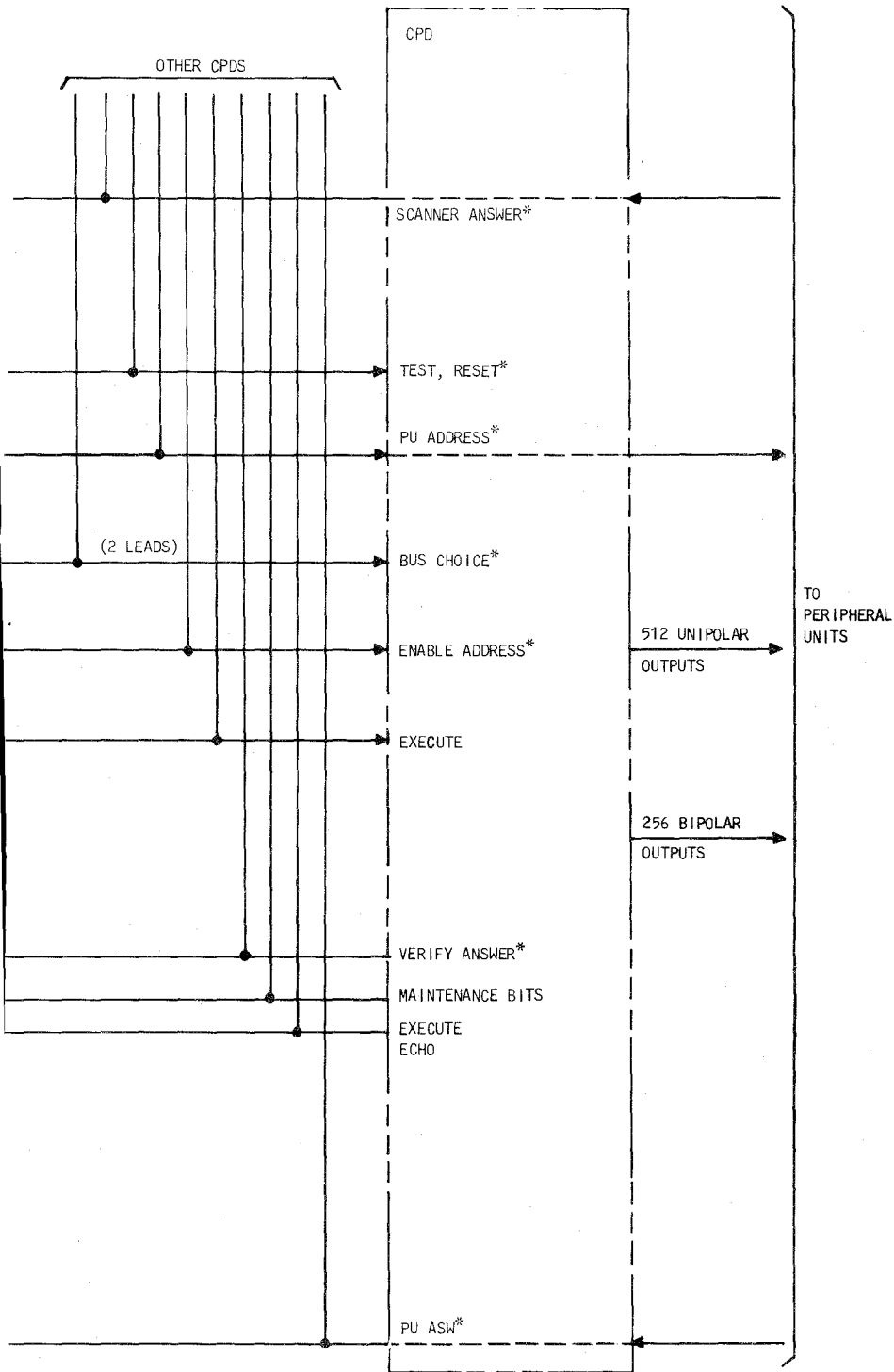


Fig. 8—Central Control and Central Pulse Distributor Communications with Peripheral Units in a No. 1 ESS





\* DUPLICATED

Fig. 9—Central Control and Central Pulse Distributor Communications with Peripheral Units in a No. 1A ESS

The execute translator receives its inputs from bits 10 through 13 of the E register. See notes in figure 11. The execute translator converts this binary code to a 1/16 code which will select one of the possible 16 CPDS in the system. The echo signal from the CPD returns to the CPD 1/16 echo detector circuit via the CPD diagnostic-echo (DE) register where it is matched with a signal from the execute translator. This echo detector circuit will indicate whether the appropriate CPD returned the echo signal. If the appropriate CPD did not return the echo signal, the execute return failure (ASWECP) error source in the peripheral error summary (PES) register will be set.

**3.28** The peripheral unit address is generated in the PU translators except on PU long and short binary translations. On the PU long and short binary translations, bits 0 through 35 and bits 0 through 22, respectively, are gated directly to the PU write data bus. On the PU, short binary bit 23 is transmitted as a parity bit. The PU translator receives its inputs from the P and E registers. The E register inputs, bit 7 through 9, are used to select which translation will be made. See Fig. 11. The P register bits 0 through 22 are used to generate the specific peripheral unit address based on the translation selected.

**3.29** The CPD verify answer comes back into the CPD reply register (R register) from the CPD units. The CPD reply register is one input to the CPD reply match circuit. The other is the CPD address translator. The CPD reply match circuit will decide if the proper peripheral unit was enabled to the peripheral unit address from the CC. If the proper peripheral unit was not enabled, the CPD reply match failure (RMFCP) error source in the PES will be set. This check is inhibited if bit 6 of the E register is set.

**3.30** The CPD has five maintenance reply bits. These consist of three parity check bits, one maintenance lead, and one all-seems-well (ASW) signal per bus. These bits are registered in the DE register, bits 16 through 21. If an ASW signal was not received from the CPD, the ASW error from CPD (ASWEL) error source on the PES will be set. The other bits are only checked by software.

**3.31** The scanner answer from the scan points is returned to the PU reply register (L register). The ASW signal from the scanner is registered in

the PES. These signals are the result of the enabled scanner which has received an address from the CC. If the CCs are duplexed, odd parity is calculated over the PU reply in the L register in each CC. The result is cross-coupled to the other CC where it is matched. If the parity check fails, the parity reply match error (RMEPU) error source in the PES will be set. If an ASW signal was not received from the peripheral unit, the ASW error from peripheral unit (ASWEPU) error source in the PES will be set. The check is inhibited if bit 5 of the E register is set.

**3.32** If any of the error sources in the PES are set, the peripheral unit F-level interrupt (PUFIS) source in the interrupt source (INS) register will be set. The CC will take maintenance action through an F-level interrupt if the PUFIS source is not pested (inhibited).

**3.33** The CPD test and reset leads come from the P register, bits 32 and 33, respectively. These leads are used to place the CPD in the test mode as well as return the CPD to normal after testing has been completed.

## FUNCTION OF EXECUTE AND ENABLE PULSES

### A. Execute Pulse

**3.34** The execute pulse is the horizontal input to the 1/8 matrix in the predecoder. The transmission of this pulse is shown in Fig. 12. The vertical input to the predecoder is bit positions 0 through 7 of the X register. A 1 stored in the X register will cause a ground to appear as a vertical input to one side of the gate associated with this bit position. The execute pulse will follow the line of least resistance to this ground and select the appropriate gate to generate an output to the decoder. The eight horizontal inputs (bit positions 00 through 07) to the decoder come from the eight outputs of the predecoder. The eight vertical inputs to the decoder come from the Y register (bit positions 0 through 7). The Y register like the X register will cause a ground to appear at one and only one vertical input to eight of the gates. The execute pulse on one of the eight leads from the predecoder will follow the line of least resistance through this gate and generate a signal on only one of the 64 outputs from the decoder (00 to 63).

**3.35** The transmission of the execute pulse through the register matrix is similar to the transmission of the execute pulse through the predecoder and decoder. A block diagram of this is shown in Fig. 13. The 64 inputs to the matrix come from the 64 outputs of the decoder. The Z register, which is made up of dynamic registers, stores the appropriate 1/16 code. This 1/16 code will apply a ground potential to only one of the 16 vertical inputs. The matrix is divided into 512 unipolar gates and 256 bipolar gates. The unipolar gates are used to enable peripheral unit controllers, while the 256 bipolar gates are used to activate logic circuitry throughout the system.

#### B. Enable Pulse

**3.36** The transmission of the enable pulse through the predecoder and decoder is similar to the transmission of the execute pulse shown in Fig. 12. The ac gates for transmission in both the predecoder and decoder are also illustrated in Fig. 12. As shown, the positive input pulse (enable pulse) will generate a positive output pulse only on that gate which has its vertical input grounded. Only one of the vertical inputs in the predecoder and the decoder are grounded at one time because the information stored in the X and Y registers is in the form of a 1/8 code. The 1/8 code is stored in the dynamic registers in the X and Y registers. These dynamic registers will function as monostable multivibrators and will apply the ground to the appropriate input position for approximately 2 microseconds on receiving a 1/8 code.

#### OUTPUT PULSE SELECTION

**3.37** The 16 vertical inputs from the Z register select the type of output pulses (Fig. 13). Bit positions 0 through 7 will select the 512 unipolar outputs, while bit positions 8 through 15 in the Z register will select the 256 bipolar outputs. Odd-numbered bit positions 9, 11, 13, or 15 will select a positive output from the bipolar gates while even-numbered bit positions 8, 10, 12, or 14 will select a negative output from the bipolar gates.

#### BIPOLAR OUTPUTS

**3.38** The polarity of the output pulse for each bipolar gate of the matrix depends on whether the Z register selection is even or odd. As shown in Fig. 14A, an odd Z selection will ground the lower section of the bipolar gate. A positive pulse

from the decoder will result in a positive output pulse as shown. For an even Z selection (Fig. 14B), the top part of the circuit is grounded. The positive pulse from the decoder now will result in an output pulse from the gate which is opposite in polarity to the one in the odd Z selection.

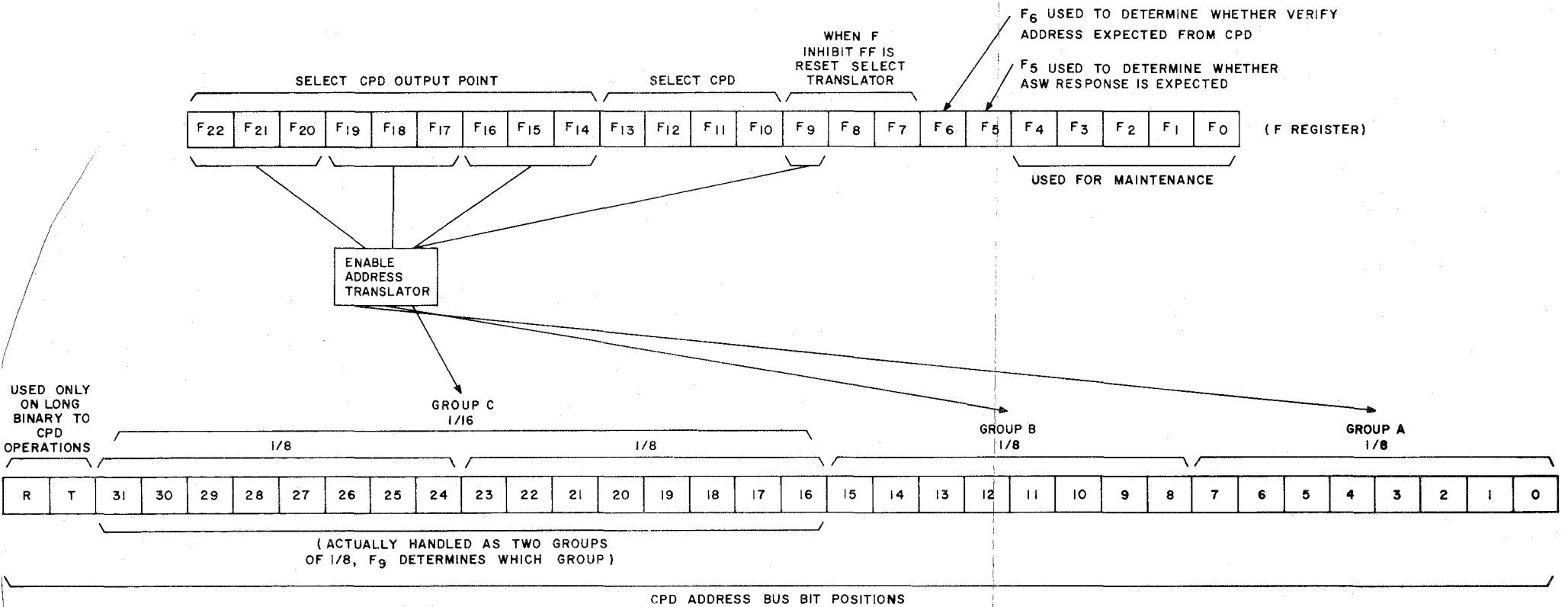
#### UNIPOLAR OUTPUTS

**3.39** The unipolar gate outputs are used to enable peripheral unit controllers on the peripheral unit bus and supply logic enable pulses to nonperipheral bus units (No. 1 ESS only) such as a signal processor or buffer control. As shown in Fig. 15A, the input from the decoder to the unipolar gate will cause an output to enable the peripheral unit controller and will cause a verify output to be generated from the gate. At this time, however, the verify answer to the CC is inhibited. In the No. 1A ESS, for all peripheral units except scanners, the peripheral unit controller will generate an enable verify pulse back to the CPD about 1.5 microseconds after being enabled by the CPD. The peripheral unit controller in the No. 1 ESS will generate an enable verify pulse back to the CPD about 2.5 microseconds after being enabled (No. 1 ESS only) by the CPD (Fig. 15B). This verify pulse will arrive at the unipolar gate at a time when the verify answer bus is enabled by the execute pulse. The encoder will receive the verify output, encode it into 1/8 X, 1/8 Y, and 1/8 Z codes, and transmit the verify answer to the CC. The CC will subsequently compare this verify address with the address previously transmitted to the CPD to verify that the appropriate peripheral unit controller was enabled.

**3.40** Upon receiving the enable verify pulse from the peripheral unit controllers, the unipolar gates will generate outputs to the encoder. The Z portion of the verify address is generated by sensing the vertical column of unipolar gates which are sending the verify answer pulse to the encoder (Fig. 16). This is the manner in which the unipolar gate was initially enabled.

**3.41** Generating the X and Y verify addresses is somewhat more complicated than generating the Z portion because the encoder must reverse the coding functions previously performed by the predecoder. The encoder generates the verify address with the appropriate 1/8 X, 1/8 Y, and 1/8 Z code gates, respectively; amplifies these signals; and then transmits these signals to the CC.





**NOTES:**

1. F<sub>9</sub> CONTROLS WHICH OF THE TWO 1/8 GROUPS IN GROUP C— IS ENABLED F<sub>9</sub> = 1 ENABLES 24-31 F<sub>9</sub> = 0 ENABLES 16-23
2. WHEN PERFORMING NONENABLE OPERATIONS, THE F<sub>14</sub> BIT IS STILL USED TO CONTROL THE SELECTION BETWEEN HALVES OF WHICHEVER PORTIONS OF THE CPD MATRIX THE F<sub>9</sub> BIT SELECTS. AS SUCH, THE F<sub>14</sub> BIT IS USED TO DETERMINE WHETHER OR NOT A BIPOLAR OUTPUT PULSE IS THE SET OR RESET POLARITY. IF A PAIR OF UNIPOLAR OUTPUTS IS USED FOR SUCH CONTROL, THE F<sub>14</sub> BIT IS USED TO CHOOSE BETWEEN THEM.
3. THE WRMI IS CONTROLLED BY F<sub>8</sub>

**Fig. 10—Central Pulse Distributor Address Bus Selection in the No. 1 ESS Central Control**

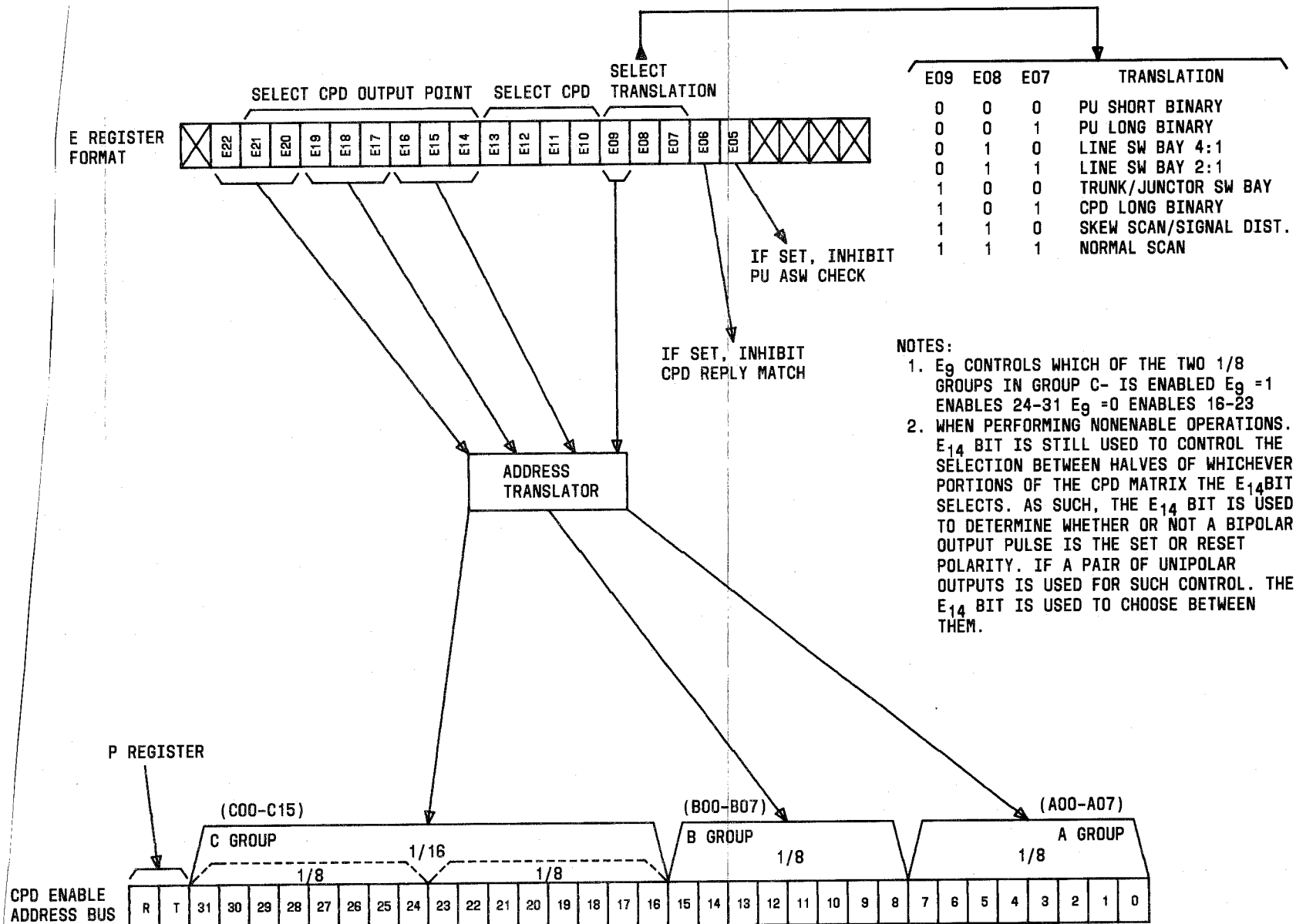


Fig. 11—Central Pulse Distributor Address Bus Selection in the No. 1A ESS Central Control

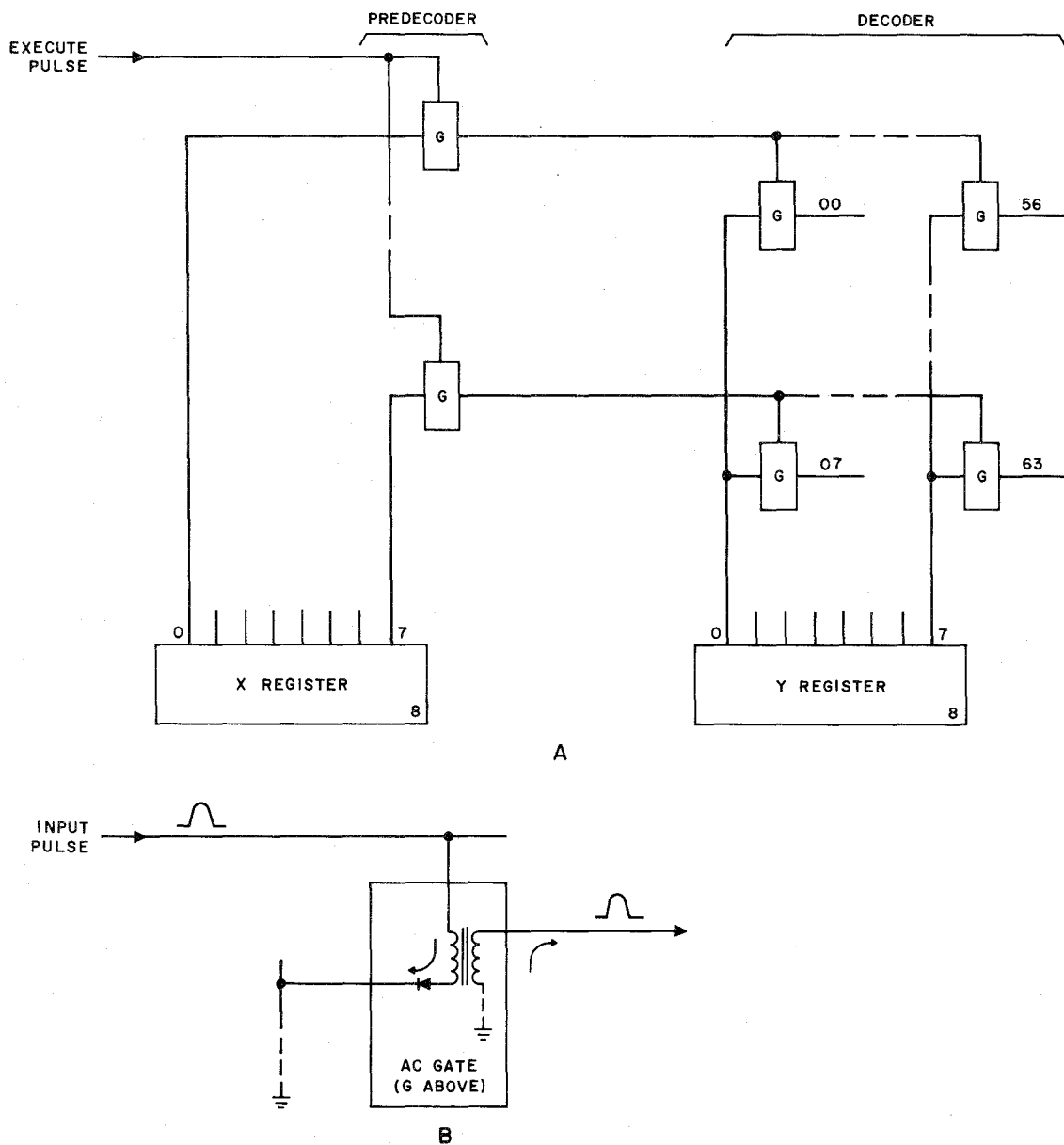


Fig. 12—Transmission of Execute Pulse through the Predecoder and Decoder

#### 4. DUPLICATION AND MAINTENANCE

##### DUPLICATION

**4.01** A maximum of eight frames can be used. The CPDs in each frame operate independently of one another. One CPD of each frame is even-numbered (bay 0) and the other CPD is odd-numbered (bay 1).

**4.02** Redundancy is provided for the CPD output signals which are used to enable peripheral units. As shown in Fig. 17, there are four paths through which the central processor is given access to each peripheral unit. The route information stored in the call store is used to determine which of the four possible paths is used.

**4.03** As shown in Fig. 18, full duplication is provided for the bipolar CPD outputs which

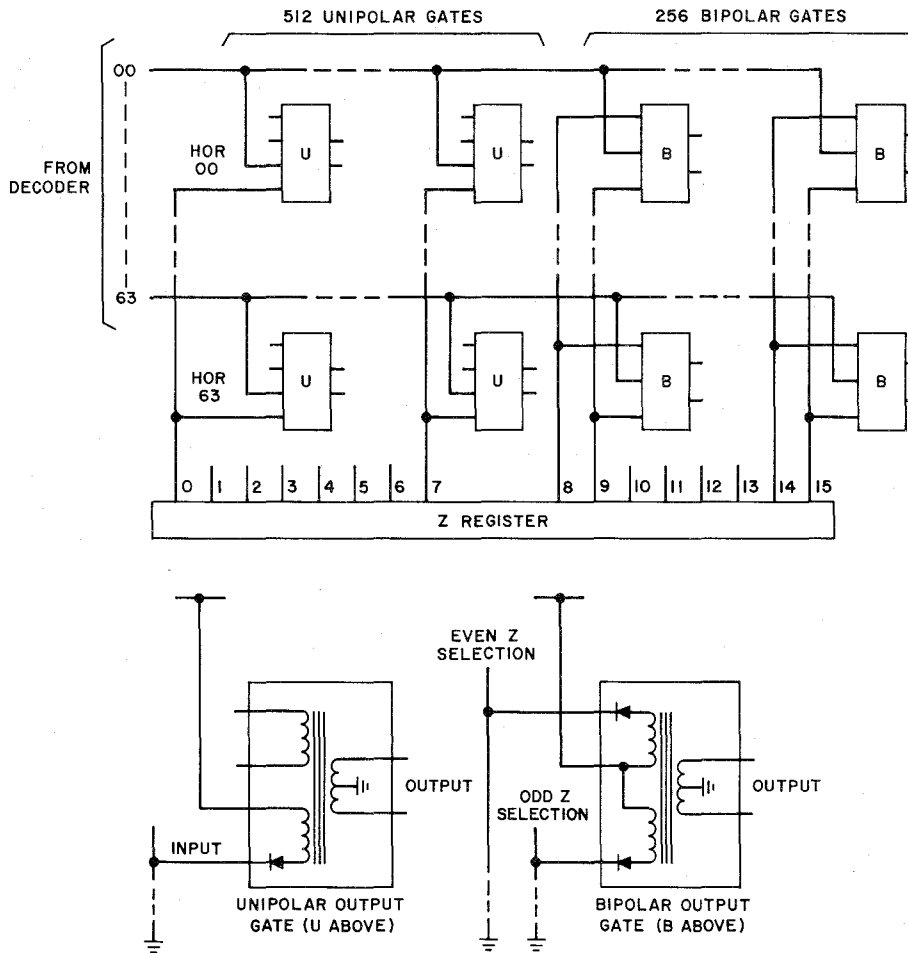


Fig. 13—Transmission of Execute Pulse through the Matrix

are used to control flip-flops and logic circuitry throughout the central office. The two outputs from a CPD have identical enable addresses. These addresses are identical for both of the CPDs in a given pair. As shown in Fig. 18, the two CPD outputs are multiplied and then wired to the termination circuit.

**4.04** In No. 1 ESS only, some bipolar outputs are used to control flip-flops that can critically affect the operation of the system. For these outputs, a safeguard is provided to prevent a noise signal on a CPD output from causing an undesired change of state in the associated flip-flop. A pulse on a protected CPD output is not effective unless a WRMI signal is simultaneously present on a common lead.

**4.05** In No. 1 ESS only, whenever a CPD receives an execute pulse, if the parity check of the address were successful, it generates a WRMI clock pulse. The CC generates an enable WRMI signal only when required by the nature of the flip-flop to be reached. At either CPD frame where both a WRMI clock pulse and an enable WRMI signal are present, a WRMI pulse is generated and fanned out to all the units that are served by that CPD and require the WRMI signal.

#### MAINTENANCE

**4.06** Many detected troubles are treated by denying to CC the use of a particular bus choice or CPD choice. This denying is done by altering a route record which is kept in a call store of the

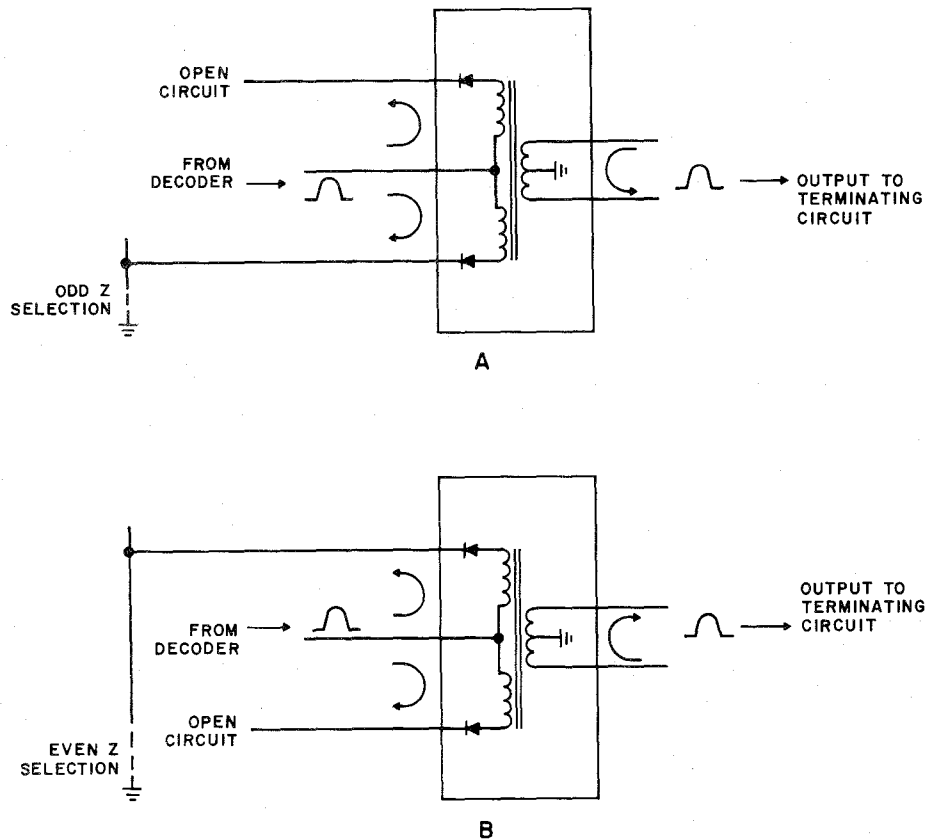


Fig. 14—Bipolar Output Gates

central processor. This mode of operation is called marked-in-trouble mode with the words in memory implied. When a CPD is in this mode, a diagnosis has been or will be made. When the fault is cleared, the route record is updated to permit CC to use the route previously denied.

**4.07** Certain matrix troubles produce parity check failures despite the fact that valid enable addresses have been received by the CPD. In this situation, the central processor orders the other CPD in the pair to pulse a bipolar output which activates circuitry within the faulty CPD. This circuitry then causes the CPD to ignore any parity check failures. This mode of operation is called parity-inhibited mode. When a CPD is in this mode, a diagnosis has been or will be made. The CC can still make use of the CPD. To return the CPD to the normal mode of operation, the central processor orders the other CPD in the pair

to produce a pulse that deactivates the circuitry formerly activated.

**4.08** If the output from a CPD is other than normal, the level of current in the output gate matrix will be incorrect. The level of the current in this matrix is tested by two detectors which will indicate whether the matrix current is below 55 milliamperes, between 65 and 170 milliamperes, or above 200 milliamperes. If the current is between 65 and 170 milliamperes, the matrix is operating normally. In this condition, the ASW signal will be transmitted to CC. If the current is below 55 milliamperes or above 200 milliamperes, the transmission of the ASW signal will be inhibited.

**4.09** During some tests, the CC transmits a pulse on the test lead instead of a Z address. This pulse activates a single-bit T register. While the activated X and Y address registers provide

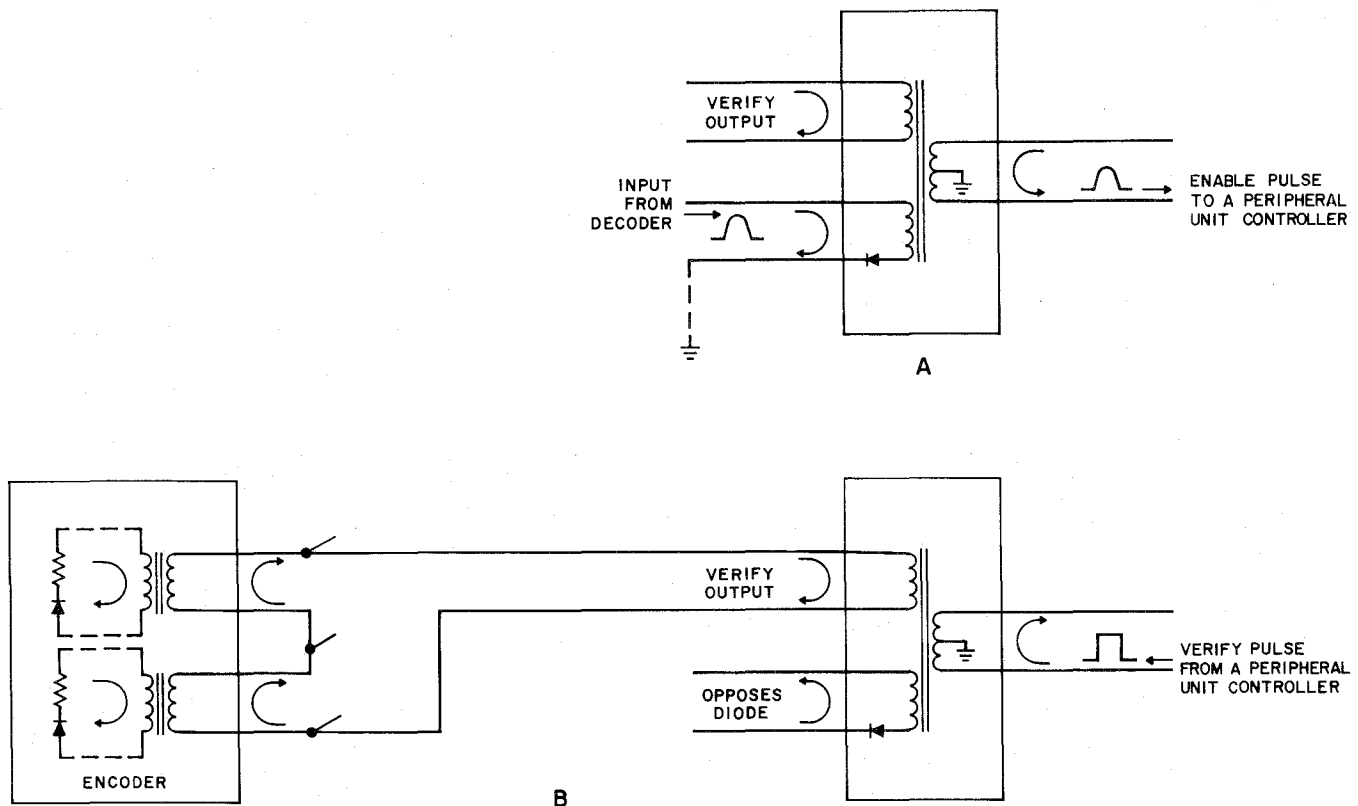


Fig. 15—Unipolar Gate Enable and Verify Signals

low-resistance paths for the execute pulse, the T register connects a dummy load to each of the 64 outputs from the decoder. By successively varying the combination of X and Y addresses and observing the resulting parity and ASW signals, the CC can determine which predecoder or decoder component is defective without having generated any outputs from the matrix.

**4.10** Whenever a printed wiring circuit pack has to be removed or inserted, power must be removed from the unit. The control panel is shown

in Fig. 19. In order to remove power, the PULSE DISTRIBUTION-REQ INH pushbutton key must be depressed. This key will release the PULSE DISTRIBUTION-NOR pushbutton key, light the OFF NOR lamp, and activate a scan point. The system will recognize the condition of the scan point. The power can now be removed by depressing the PULSE DISTRIBUTION-OFF pushbutton key. This key will remove power, light the PULSE DISTRIBUTION-OS lamp and the PWR OFF lamp. A blown fuse will also light the PWR OFF lamp.

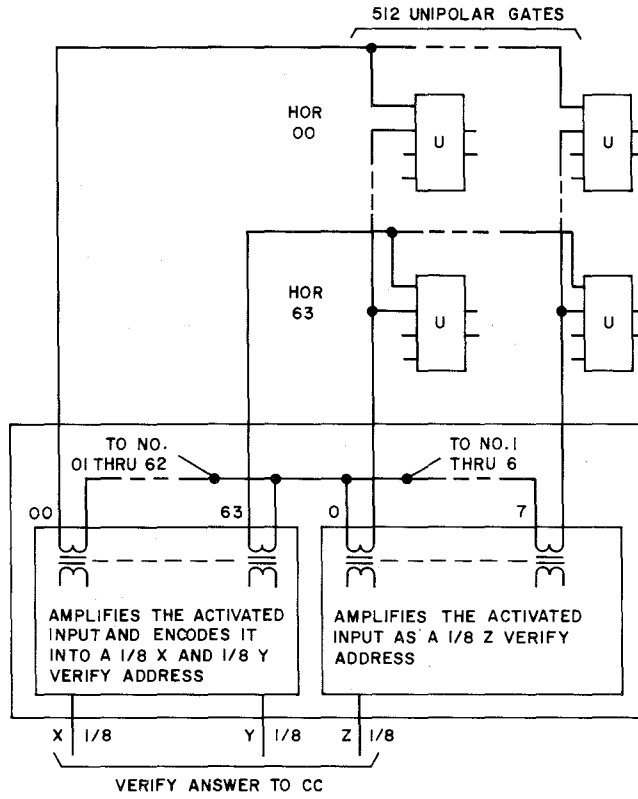
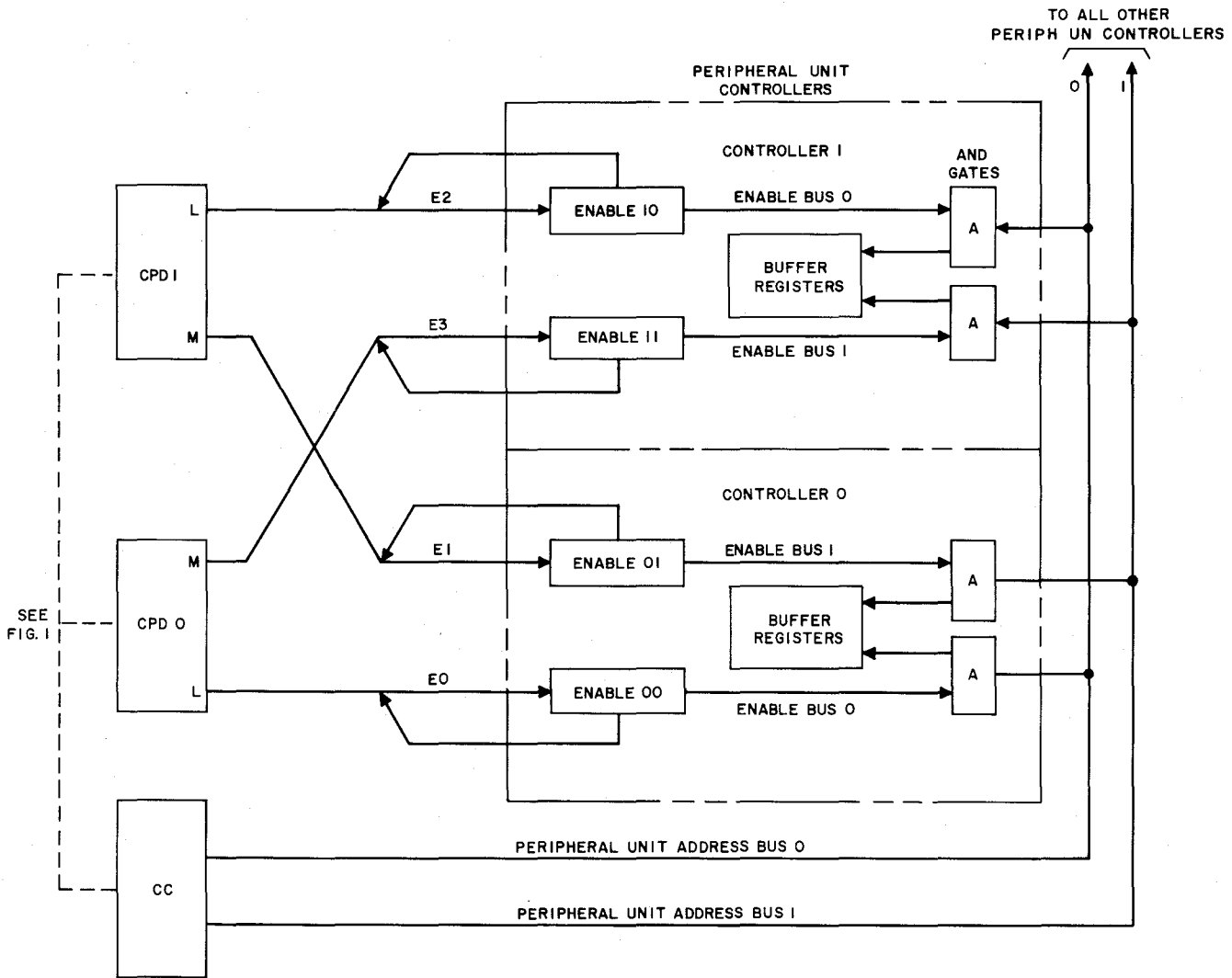


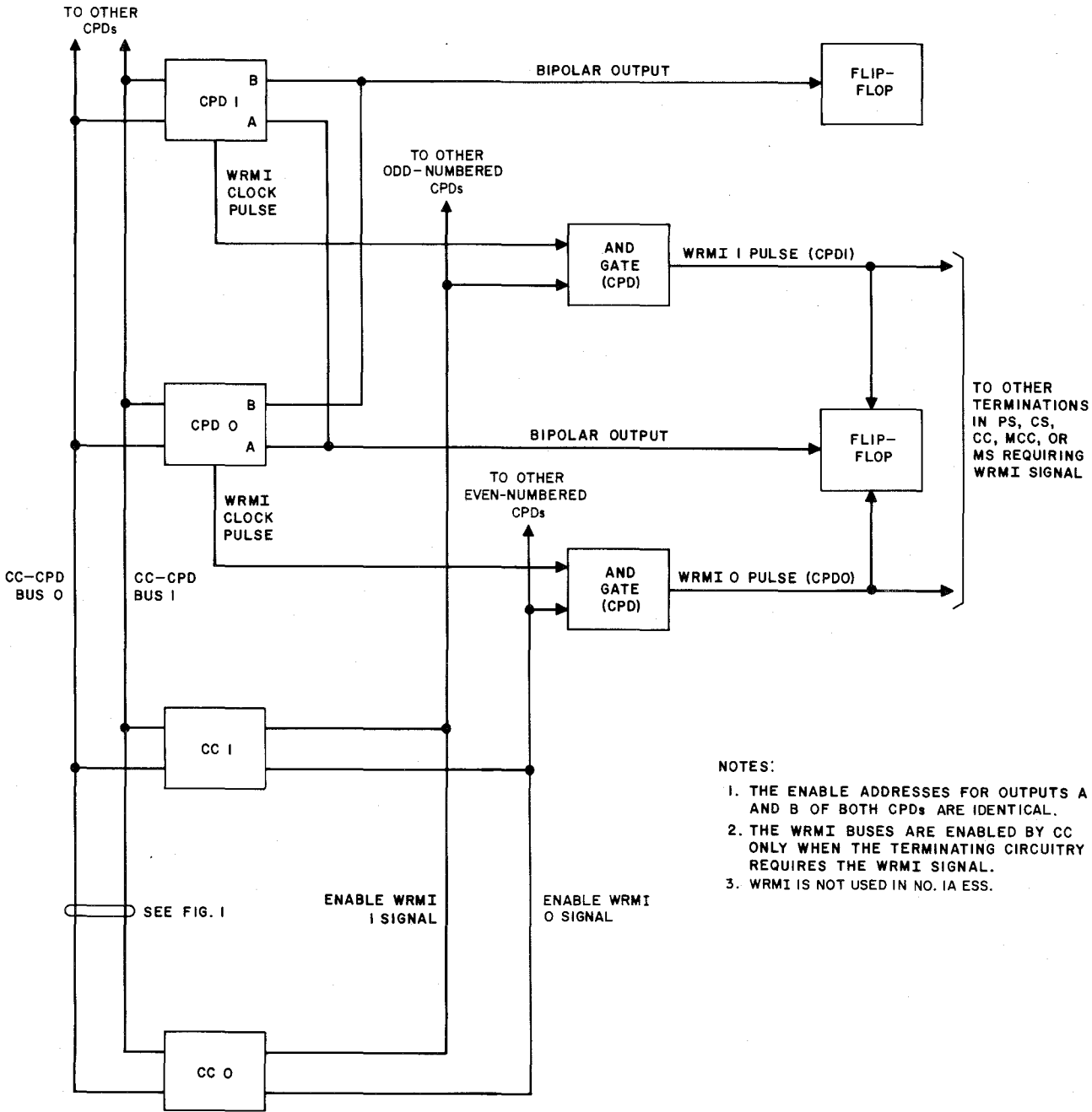
Fig. 16—Generating a Verify Address



- NOTES:
1. THE ENABLE ADDRESSES FOR OUTPUTS L AND M OF BOTH CPDs ARE IDENTICAL.
  2. THE VERIFY PULSE IS RETURNED ABOUT 2 MICROSECONDS AFTER THE ENABLE PULSE IS RECEIVED.

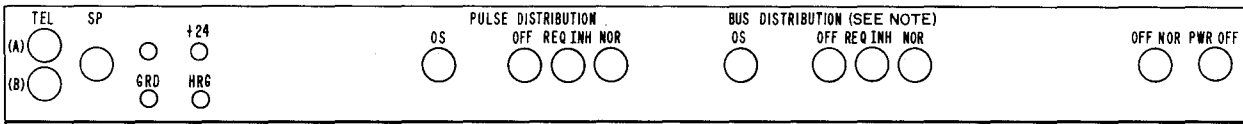
Fig. 17—Enable-Peripheral Unit Controller





- NOTES:
1. THE ENABLE ADDRESSES FOR OUTPUTS A AND B OF BOTH CPDs ARE IDENTICAL.
  2. THE WRMI BUSES ARE ENABLED BY CC ONLY WHEN THE TERMINATING CIRCUITRY REQUIRES THE WRMI SIGNAL.
  3. WRMI IS NOT USED IN NO. 1A ESS.

Fig. 18—Duplication of Bipolar Outputs



NOTE:  
ON NEWER PANELS NUMBERS (O) OR (I) DESIGNATE WHICH PUA BUS IS CONTROLLED

Fig. 19—Central Pulse Distributor Control Panel