

**COMBINED MISCELLANEOUS TRUNK FRAME
 DESCRIPTION AND THEORY
 2-WIRE NO. 1 AND NO. 1A "ESS*" SWITCHES**

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1. GENERAL

1.01 This section describes the combined miscellaneous trunk (CMT) frame used in No. 1 and No. 1A ESS switches.

1.02 This section is reissued to add a description of the improved minitrunk signal distributor diagnostic (IMD) feature. Change arrows are used to indicate significant changes.

1.03 All No. 1/1A ESS switch generics starting with Generic 1/1AE7 contain the IMD diagnostic program. The IMD hardware is compatible with all generic programs while the diagnostic benefits of that hardware are only available with Generic 1/1AE7 and later generics.

2. LIST OF ABBREVIATIONS

2.01 Abbreviations and acronyms used in this section are listed below.

ASW	All Seems Well
ASWS	All Seems Well Scanner
CC	Central Control
CMT	Combined Miscellaneous Trunk
CPD	Central Pulse Distributor
IMD	Improved Minitrunk Signal Distributor Diagnostic
LS	Least Significant
MS	Most Significant
MT	Maintenance Test
MUT	Miniaturized Universal Trunk
PIMT	Plug-In Miscellaneous Trunk
PU	Peripheral Unit
PUAB	Peripheral Unit Address Bus
SCAB	Scanner Answer Bus
SD	Signal Distributor
SSD	Supplementary Signal Distributor

TIC	Trunk Interconnection Circuit
TOP	Task Oriented Procedure
TS	Terminal Strip
TTY	Teletypewriter
UTF	Universal Trunk Frame.

cuit boards containing miniaturized ferrods for scanner functions and circuit boards containing triacs (solid-state switches) for SD functions. A total of 16 PIMTs can be provided in each TIC. A CMT frame can provide housing for 16 TICs. Each TIC can provide housing for 16 miscellaneous trunk circuits, plug-in triac matrix circuit boards, and plug-in scanner matrix circuit boards.

3. PHYSICAL DESCRIPTION

3.01 The CMT frame consists of a pair of 3-foot, 3-inch bays that contain one or two signal distributors (SD), a 1024 point scanner, and peripheral bus units (see Fig. 1). The optional SD is called a supplementary signal distributor (SSD). The bays are arranged in a home-mate configuration that provides plug-in housing for up to 256 plug-in miscellaneous trunk (PIMT) circuits (Fig. 2). The CMT frame also provides power, filters, and fusing for the trunk circuits.

3.02 The PIMTs are plugged into the trunk interconnection circuit (TIC). Figure 3 shows the TIC layout. The TIC provides interconnection between the plug-in miscellaneous trunk circuits and the scanner and SD points. The TIC is designed for a specific group or type of miscellaneous trunk and is mounted in the CMT frame. Each TIC houses cir-

3.03 The miscellaneous trunks are organized into nine groups of trunk circuits. Each group requires a TIC that accepts only trunk circuits from that particular group. A TIC can accept any trunk circuit in the group it is designed for, but cannot accept trunk circuits from any other group. Table A gives the TICs and the trunk circuits for each group.

3.04 The TICs are hardwired in the CMT frame using order information from the telephone company. The various TICs can be mixed on the frame to interface with the various trunks.

IMD Hardware Changes

3.05 The IMD hardware changes include changing 11 controller circuit packs in the CMT frame. In addition, the point selector second stage circuit packs are changed. The codes of the non-IMD and IMD circuit packs are shown in Table B.♦

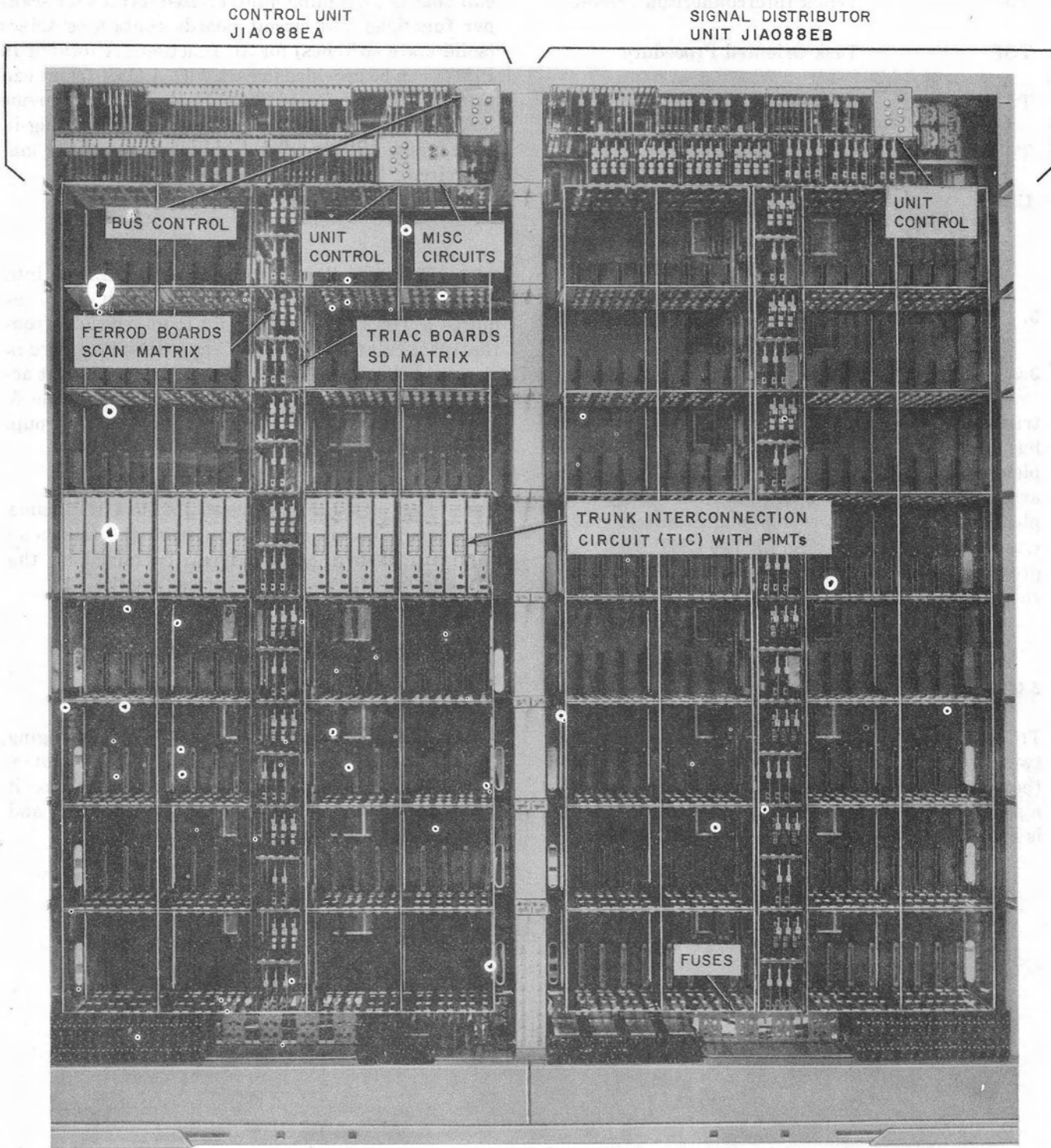


Fig. 1—Layout of CMT Frame with One SSD

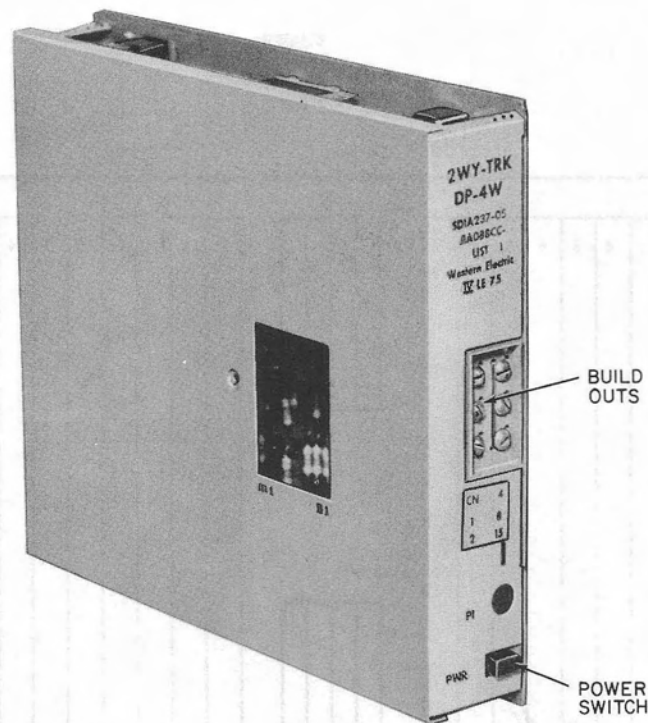


Fig. 2—Typical Plug-In Miscellaneous Trunk Circuit

4. OVERALL FUNCTIONAL DESCRIPTION

A. General

4.01 The CMT frame accommodates most of the trunks that cannot be mounted in the MUT or UTF frames. This includes most service circuits. Low runner trunks, including most test circuits, will remain mounted on miscellaneous trunk frames. The CMT frame contains a dedicated master scanner and a dedicated supplementary SD. A second nondedicated SD may be added as an option.

4.02 The PIMT circuits have little, if any, autonomy. With few exceptions, relays within these circuits operate only under the direction of central control (CC) via the central pulse distributor (CPD) and the SD. CC detects via a scanner any change in the trunk or loop conditions that results from relay operation.

B. Bus Circuits

4.03 The bus circuit provides the necessary interface circuitry between the SD controllers or scanner control circuits and the peripheral unit ad-

dress bus (PUAB) and scanner answer bus (SCAB). Since the circuit controllers, as well as the buses, are duplicated for reliability, the system needs to select either of the bus-to-controller paths via the enable-verify leads from the CPD. The bus circuit also includes the circuitry to generate enable-verify signals on the enable-verify leads.

4.04 The enable pairs have the letters EN in their lead designation, followed by two numbers signifying controller and bus, in that order. The enable-verify leads have EV in the lead designation, followed by two numbers showing controller and bus. The L and R prefix differentiates between the two SDs. The home frame is L and the mate frame is R. The absence of an L or R prefix identifies the enable and enable-verify leads as being associated with the scanner controllers.

4.05 The peripheral unit (PU) bus bits are called the address bits. The incoming address bits have the letters AD in their lead designation. A 0 or 1 prefix indicates the bus number, and a P or N suffix indicates the relative voltage polarity of the wire.

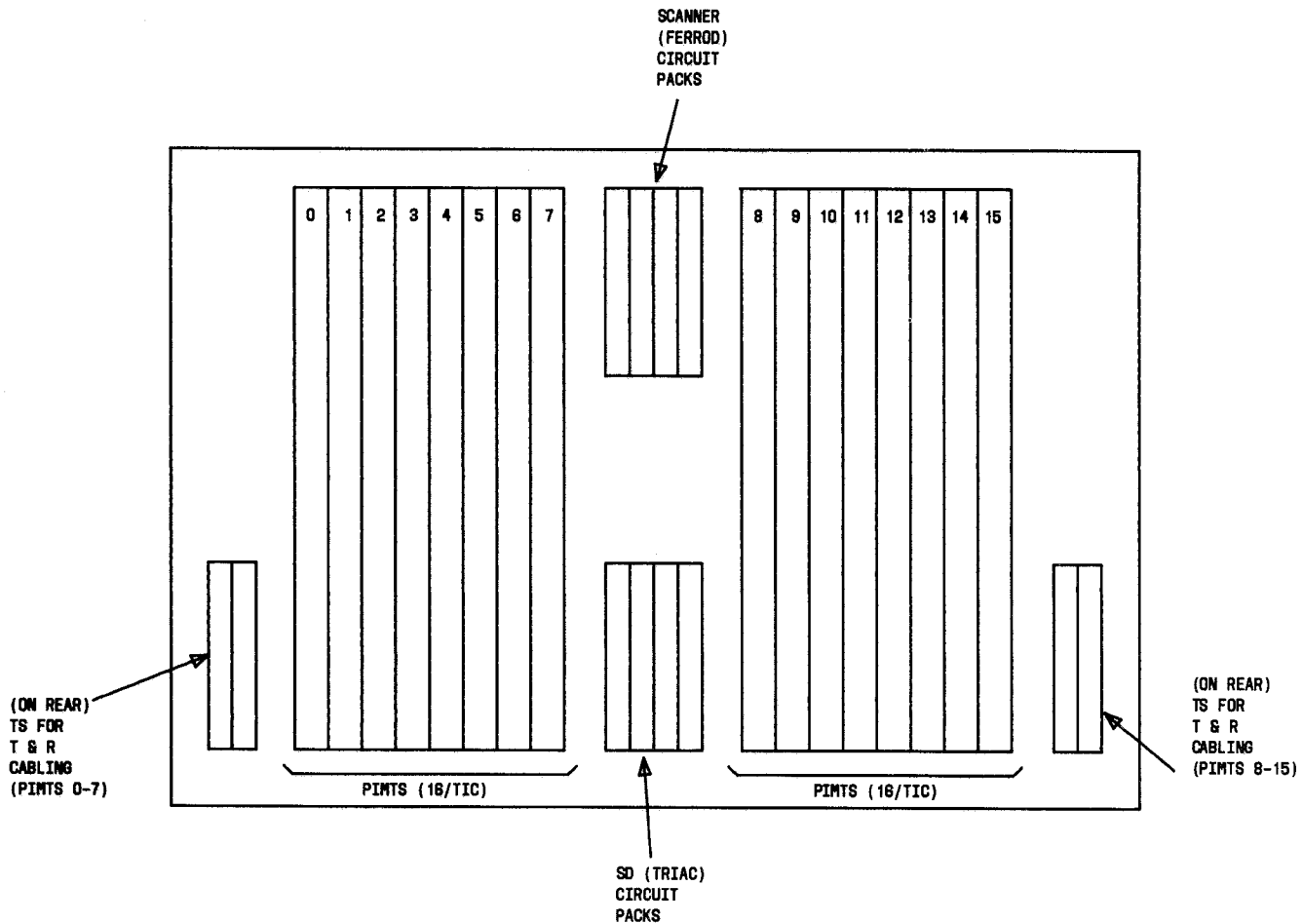


Fig. 3—Layout of CMT Trunk Interconnection Circuit

The remaining two digits indicate the bit number 00 through 36. An example of the PUAB is as follows:

bus 0 → 0 A D 08 P ← relative polarity

This is No. of bit
a PU
address

C. Signal Distributor Controller

4.06 There are one or two pairs of SD controllers in the CMT frame. The two controllers of a pair are designated by 0 and 1. The SD controller pair for the home frame (left) is designated by the letter

L. The SD controller pair for the mate frame (right) is designated by the letter R.

4.07 The SD controller used in No. 1 and No. 1A ESS switches is provided to give the central processor the ability to select magnetic latching relays in miscellaneous trunk circuits within the CMT frame. The SD controller acts as a buffer between the central processor (electronic speeds) and the peripheral relays (relay speeds).

4.08 The basic SD is composed of a controller and a 1-out-of-480 point selector. Two of these units make up a 960-point SD. Normally, they operate independently of each other as separate identities in what is known as *split mode* operation. In No. 1 and No. 1A ESS switches, they are always provided in pairs, as shown in Fig. 4. Each basic SD, when directed by information sent in the form of a 28-bit

TABLE A

**TRUNK INTERCONNECT UNITS AND
COMPATIBLE TRUNK CIRCUITS**

TRUNK INTERCONNECT CIRCUIT (TIC)	TYPE OF TRUNKS USED IN TIC	TRUNK USE
SD-1A404-01 (J-1A088EC)	SD-1A236-05 SD-1A237-05 SD-1A163-05 SD-1A415-05 SD-1A416-05	4-Wire 2-way E and M MF 4-Wire 2-way E and M DP 2-Wire E and M DP Long-haul FX TRK FX TRK
SD-1A407-01 (J-1A088EK)	SD-1A172-05	CDPR
SD-1C650-01 (J99388C)	SD-1C650-01	TOUCH-TONE® REC
SD-1A409-01 (J-1A088EM)	SD-1A168-05	1- and 2-Party Ringing
SD-1A413-01 (J-1A088EN)	SD-1A221-05 SD-1A222-05 SD-1A223-05 SD-1A224-05 SD-1A169-05	Recorded ANN. Permanent Signal OGT to 3CL ICT from 3CL OGT to Distant 3CL
SD-1A410-01 (J-1A088EP)	SD-1A245-05 SD-1A248-05 SD-1A283-05	Attendant Trunk 2-Wire Attendant Trunk 4-Wire Attendant Loop
SD-1A411-01 (J1A088ER)	SD-1A284-05	3-Port Conference
SD-1A412-01 (J-1A088ES)	SD-1A177-05 SD-1A239-05 SD-1A319-05	Verify Request and Intercept DP REPTR Line Access Trunk
SD-1A414-01 (J1A088ET)	SD-1A220-05 SD-1A321-05	ICT from SXS ICT from TSPS
SD-1A408-01 (J-1A088EL)	SD-1A311-05	CAMA ICT from SXS

address from the central processor, sets up a signal path to one of the 480 magnetic latching relays. The address also directs the controller to send a release or an operate signal to the relay. The controller detects the movement of the relay armature that initiates the reset of the controller enable and address register. Until this reset function has been accomplished, no new addresses can be registered or acted upon.

4.09 The CMT frame can have up to two SDs per frame depending upon the configuration. Each SD has two controllers for reliability which are designated 0 and 1. Each controller normally controls 480 SD points. If one controller fails, the mate controller will operate all 960 SD points.

D. Scanner Controller

4.10 The scanner controller circuit provides supervision of the miscellaneous trunk circuits in the CMT frame. The scanner consists of two basic parts: the control equipment and the scanner matrix.

The control equipment provides the circuits necessary for interrogating 1024 ferrod rods and converting these outputs into signals that can be used by other parts of the system. The scanner matrix consists of ferrod sensors mounted on plug-in printed circuit boards (Fig. 5) which are distributed throughout the frame. The control equipment contains the interrogate and readout circuitry which is duplicated for reliability, and these are referred to as controller 0 and controller 1. The ferrod sensors are assigned to trunks and are not duplicated. Groups of 16 ferrod sensors are scanned (interrogated) simultaneously.

Ferrod Sensor

4.11 The ferrod sensor is the basic unit of the scanner. The ferrod sensor can be considered a 2-winding transformer whose coupling (the ability to induce a signal from the primary winding to the secondary winding) is controlled by the current in its control winding. The primary and secondary windings of the transformer are associated with the access and readout equipment and are referred to as the interrogate and readout windings, respectively. The control windings are associated with either the network side or the trunk side of a plug-in type trunk circuit. When a transmission path is established

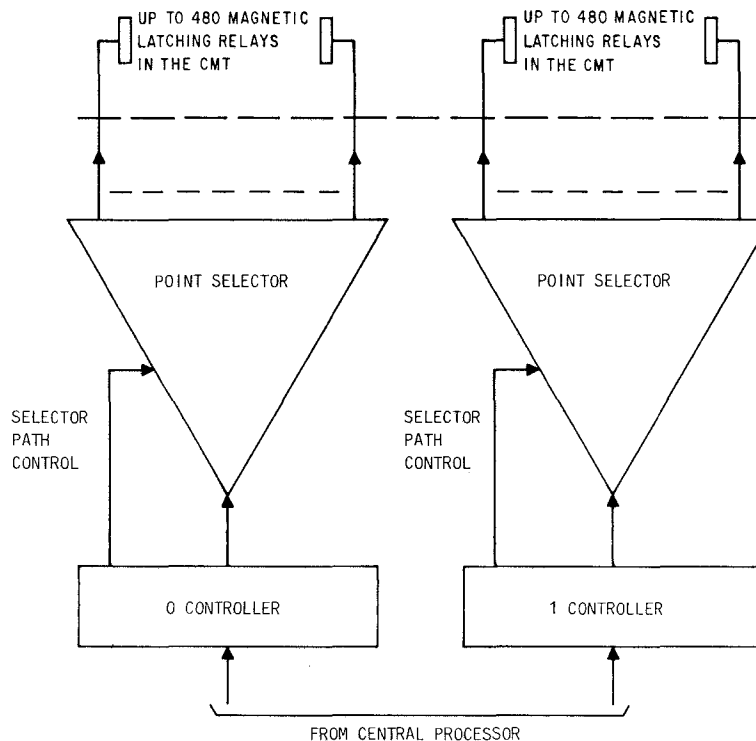


Fig. 4—Normal (Split) Mode Configuration

TABLE B

IMD CIRCUIT PACK REPLACEMENTS

NON-IMD	IMD REPLACEMENT
FA1202	FA1810
FB592	FB592B
FB593	FB698
FC300	FC661
FC322	FC664
FC323	FC665
FC324	FC666
MG7	MG7B

(talking battery current present in control windings), coupling is destroyed and the interrogate signal is not able to induce a signal into the readout windings. When no transmission path exists (no current in control windings), the interrogate signal will induce a signal in the readout winding. If the scanner seems to have functioned properly, an all-seems-well scanner (ASWS) signal is sent with the 16 interrogation replies. Each trunk circuit is scanned at an average rate of once every 0.1 second. For more information on a basic ferrod arrangement, see Section 231-030-010.

Enabling and Addressing a Scanner

- 4.12** Scanners are considered PUs. All PUs are addressed simultaneously from the control processor over the PU address bus. The particular PU that is to reply is selected by an enabling signal from the CPD.
- 4.13** All signaling to the scanner, except the control of the ferrod sensors, is done with a 0.5 μ sec pulse on duplicated peripheral address buses. Each controller of the scanner must be able to operate from either PUAB with the selection being made by

the enabling pulse via the CPD. The addressed controller replies simultaneously on both SCAB buses.

- 4.14** Associated with each controller are two enabling pairs that determine from which bus to accept addresses. The answer bus contains 16 pairs for ferrod outputs and a seventeenth pair for the ASWS signal.

- 4.15** An address bus to the scanner is divided into two groups: the least significant (LS) group and the most significant (MS) group. Both groups contain eight pairs of wires. The scanner uses an additional pair of wires of the address bus for maintenance test (MT) orders.

5. DETAILED FUNCTION DESCRIPTION

- 5.01** Figure 13 is a functional block diagram of the CMT. This figure shows the left and right SD controllers, the scanner controller, and the interconnecting leads.

PERIPHERAL BUS CIRCUIT

A. Peripheral Unit Address Bus

- 5.02** PAUB circuits 0 and 1 are physically and electrically separate; however, their functions are identical. The following description applies to both bus 0 and bus 1, unless otherwise stated.

- 5.03** There are five cable receiver circuit packs (FC 12), four of which are capable of receiving a total of 29 address or control bits. The remaining 7 bits of the PUAB are wired through the frame so the entire 36-bit PUAB is run through the frame. The fifth cable receiver pack is provided to terminate six enable cable pairs.

- 5.04** The cable receivers convert an input current pulse of 35 milliamperes (minimum) to a voltage swing on the output of the receiver, using a saturating transistor. The receiver output terminal is normally high (no pulse). An output on the receiver is a low-going voltage pulse 0.5 microseconds wide.

- 5.05** The input pick-off transformer is located on the receiver circuit pack. A bypass resistor maintains the continuity of the bus when the receiver circuit pack is pulled out and the transformer is removed.

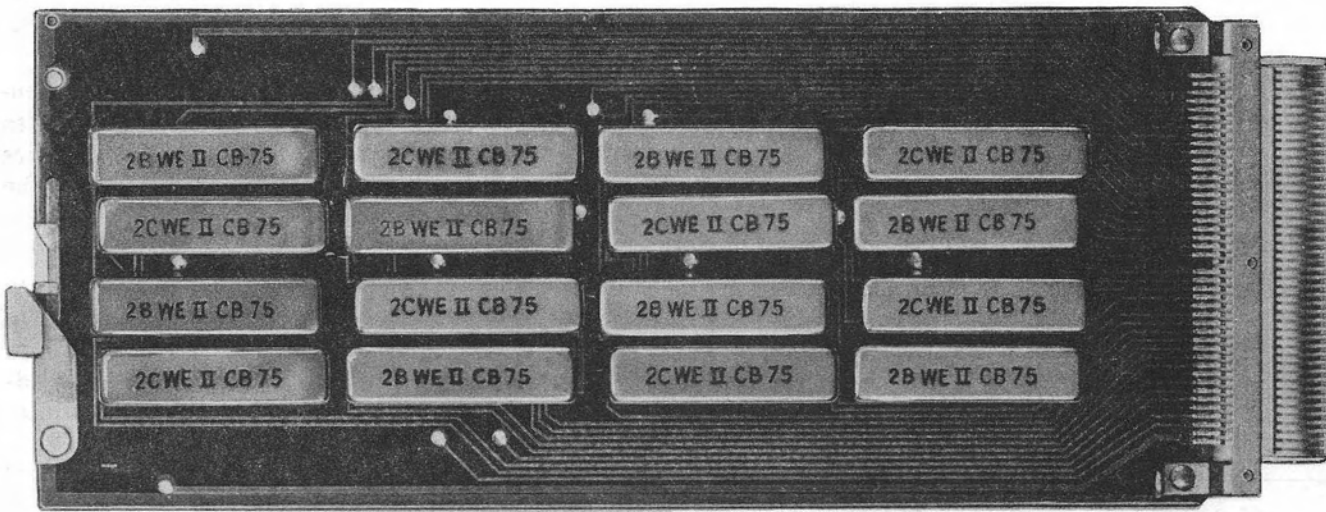


Fig. 5—Plug-In Ferrod Circuit Pack

B. Scanner Answer Bus

5.06 There are three FC 13 cable driver circuit packs, two of which are capable of terminating 16 of the 17 required answer bus pairs. The seventeenth pair is terminated by one of the eight cable drivers on the third cable driver circuit pack. Six of the remaining circuit outputs are connected to the inputs of the enable cable receiver circuit pack. These six cable drivers generate enable-verify signals on the same cable pair over which an enable signal was previously received. These enable pairs are terminated in 100 ohms.

5.07 The cable drivers convert the low voltage digital inputs into current pulses that are returned on the SCAB. The same results are sent back on both circuits (0 and 1).

5.08 The FA 776 SCAB register circuit pack stores the results of the scanner-detector circuit pack (FC 135), stores the ASW information, and provides the low voltage digital inputs to the cable drivers. The SCAB register circuits are always active and perform the same functions regardless of which scanner controller is active.

SCANNER CONTROLLER

5.09 To operate a scanner controller, an enabling pulse is sent from the CPD. This opens a gate, permitting the address to be received for 2.2 μsec or for 0.4 μsec after an address is received. At 2 μsec after the start of the enabling pulse, the previously enabled pair is pulsed for 1 μsec by the controller. This permits the CPD to verify that the enable pulses reach the correct equipment. A valid address results in a pulse on only one pair of wires in the LS and MS group of inputs (maintenance-test pair not pulsed). The PU bus circuit receives the address pulses and stores them in the address register and the access circuitry. The register and access circuitry translates LS and MS address inputs so that one of 64 rows of 16 ferrods is selected and interrogated. The outputs of the 16 ferrods are detected by the detector circuit and stored in the scanner-answer register. If there is less than sufficient current in the control windings of the ferrod, the output circuitry produces a pulse (1). If there is sufficient current in the control windings of the ferrod, the output circuitry will produce no pulse (0) when interrogated. The result of the interrogation (16 outputs) is transmitted simultaneously on both SCABs.

5.10 The maximum operate time of the scanner is 2.2 μ sec. A scanner may be addressed at a minimum interval of 7 μ sec.

C. Scanner Register and Access Circuit

5.11 The function of the scanner register and access circuit is to provide a bipolar interrogate pulse to the correct ferrod row. There are 64 rows of 16 ferrods that a scanner controller interrogates.

5.12 This circuit registers and translates the address information, provides the all-seems-well (ASW) logic, and contains the logic for the enable and enable-verify circuitry. The timing for the scanner controller is also provided by this circuit.

5.13 The ASW pulse is used to indicate that the scanner controller has interrogated only one ferrod row. If more than one row is pulsed due to faulty circuitry or because an invalid code is received, the ASW pulse is inhibited.

D. Scanner Power Circuit

5.14 The scanner power circuit converts the +24 DC frame voltage to the +3 DC volts used for logic and timing functions.

E. Ferrod Matrix Circuit

5.15 The ferrod sensors are arranged in two 16 by 32 matrices for a 1024-point scanner. The scanner matrix consists of miniaturized plug-in ferrods mounted on printed circuit packs (Fig. 5). These packs are distributed in the same housing as the trunks (Fig. 1). There is a particular scanner address associated with each row of 16 ferrods. All 16 ferrods in the row are interrogated simultaneously when an address is received from the central processor. The answers of the scanner busy/idle information for eight trunk circuits are returned to the central processor via the scanner detector circuit. If the scanner seems to have functioned properly, an ASWS signal is sent with the 16 interrogate replies. Scan points and rate of scan are provided as per SD-1A272 (assignment for master scanners). Two types of ferrod sensors are used; 2B type of line side and 2C type for trunk side of the circuit.

F. Scanner Detector Circuit

5.16 A scanner detector board contains 16 circuits that detect the readout current of an unsaturated ferrod. An unsaturated ferrod, upon interrogation, causes current to flow in the readout loop.

5.17 Scanner detector boards also contain a transformer which is activated during a maintenance test. The test verifies that the readout loop has continuity and that the detector works correctly.

SIGNAL DISTRIBUTOR CONTROLLER

G. SD Buffer And Maintenance Circuit

5.18 The SD buffer and maintenance circuit buffers the address signals from the bus circuit to the rest of the SD controller. This circuit is also used to control the state of the duplicated SD controllers (0 and 1).

5.19 Each SD cycle begins when the CC instructs the CPD to send an enable pulse to the SD controller. The enable pulse is received by the buffer circuit from either peripheral bus circuit 0 or 1. This enable sets an enable register. A pulse is sent over the control leads to the SD timing, pulse, and miscellaneous circuit which returns a pulse over the timing and pulse leads. This pulse is used as a timing window for the address registers to accept address information from the bus circuit. An enable-verify signal is sent back to the peripheral bus circuit.

5.20 System reset pulses are also sent via the peripheral bus circuit. If one of the enable registers is set, a pulse is sent to the SD timing, pulse, and miscellaneous circuit which returns pulses to reset the appropriate enable and address registers. Normally, these register reset pulses are sent at the end of the SD cycle and are caused by the armature-movement register and the end of timing pulse being set.

5.21 The address bits are divided into subgroups. Several subgroups are used to set registers which generate the horizontal and vertical select pulses sent to the interface circuit. The vertical selectors determine the location of the vertical column or trunk position of the relay to be controlled. The horizontal selection determines the horizontal mounting plate location of the relay to be controlled. One of the subgroups is used to determine whether a magnetic-

latching relay is going to receive an operate or release pulse. Another subgroup is used to determine which half of the SD (0 or 1) is to be activated. A third subgroup determines whether the controller is in the normal or maintenance mode. The operate/release pulses and the controller status information are transmitted to the SD timing, pulse, and miscellaneous circuit.

H. SD Timing, Pulse, and Miscellaneous Circuit

5.22 The SD timing, pulse, and miscellaneous circuit is used to send pulses for creating timing windows, for operating relays, and for resetting registers. This circuit also includes some scan point driving circuits.

5.23 This circuit provides timing for the enable signals, relay pulser, triac selectors, and detection circuits. A pulse is sent to the SD buffer and maintenance circuit for use as a timing window to accept address information from the bus circuit.

5.24 The SD timing, pulse, and miscellaneous circuit supplies the -48 volt operate pulses needed to operate magnetic-latching relays. It sends +24 volt pulses over the same leads to release the relays. If the triac-selection circuits have two or more relay paths selected, the operate or release pulses are removed from the selected paths before the relays have time to operate or release.

5.25 This circuit also detects relay armature movement which is required before the enable and bit register resets are generated. The armature movement detector generates a pulse which is gated with the output of a double release detector. This can set a register which results in a controller failure for the cycle. Resets are not sent to the enable and address bit registers in the case of controller failure. A system reset pulse from the SD buffer and maintenance circuit is necessary to clear the controller for the next cycle.

5.26 When the controller is put in the quarantine mode of operation, the SD timing, pulse, and miscellaneous circuit generates a pulse to operate the quarantine relay.

5.27 Another function of this circuit is to reset all the registers when power is applied to the SD circuit. The SD controller always comes up in the quarantine mode when power is restored. Register

reset pulses are also sent when a controller is placed in or out of the maintenance mode.

5.28 Each controller has three dedicated scan points. The scan point driving circuits are located on the miscellaneous circuit. Inputs to the driving circuits come from the SD buffer and maintenance circuit. The miscellaneous circuit also contains the driving circuits for five common diagnostic master scanner points associated with all SD controllers. These five scan points become active only when the controller is in the test access mode.

I. Interface Circuit

5.29 The interface circuit provides for conversion between digital logic and the +24 volt selection circuits. This circuit also provides node isolation between normal and quarantine selection.

J. SD First Stage Triac Circuit

5.30 The triac select circuit provides the triac gate current for the first and second stage supplementary triacs. It also contains the circuitry for selecting the triac gate current path in the first stage for the universal triac points. When the proper combination of inputs to the first stage triac circuit is made, a gate selection path is established for the first triac stage.

5.31 The first stage triac circuit provides the first of two stages of triac switches that make up the SD matrix. When gating occurs, a current is established through the triacs and subsequently through a magnetic relay to ground.

K. SD First Stage With IMD Feature

5.32 When the SD is equipped with option V (hardware for IMD, or when the *optional SD is equipped with option Y (IMD)*, the first stage triac circuit is replaced by first stage relays. These relays are small, mercury relays which are mounted on circuit packs. The relays provide better isolation between selection circuitry and the SD matrix than triacs.▲

L. SD Second Stage Triac Circuit

5.33 The second stage triac circuit consists of two types of circuits: the second stage triac selection and triac circuit and the second stage triac cir-

cuit. The second stage triac selection and triac circuit provides 24 second stage triacs and their associated selection circuitry. The second stage triac circuit contains 40 triacs and the associated gating circuitry for 40 SD points.

M. SD Controller Logic and Timing

5.34 The SD controller cycle begins when an enable signal is sent under direction of the central processor, via the CPD, to a specified SD controller (Fig. 6). This enable signal gates on the buffer registers via the enable network. The buffer registers store the address information for the duration of the operation cycle. Information stored in the buffer register is used to establish a path through the triac selector to a specified magnetic latching relay and to select the operate or release signal (E) from the magnetic latching relay pulser. When the relay operation or release is sensed by the relay action detector, the enable register in the enable circuit and the buffer registers are reset. The controller is now prepared to receive a new order from the central processor.

5.35 The function of the SD controller is as follows:

- (1) Receive address information from the central processor
- (2) Temporarily store address information
- (3) Check address and pulse path for errors (with IMD, also check first stage selection circuit for errors).
- (4) Inhibit continued operation of the cycle when errors are found and report errors to the central processor
- (5) Establish a path through the triac selector
- (6) Verify that relays worked as intended.

If all circuit conditions are satisfied, the controller resets and awaits the next order.

5.36 As shown in Fig. 6, the controller contains the following circuits:

- (1) Steering logic circuit
- (2) Enabler

- (3) Buffer registers
- (4) Selector interface and translation buffer
- (5) Logic error detecting circuit
- (6) Path detector circuit (point selector)
- (7) Magnetic latching relay pulser
- (8) Relay path diagnostic detectors
- (9) Strobe circuits
- (10) Reset circuit.

As shown in Fig. 7, the controller with IMD contains the above circuits and a selection circuit error detection feature.

5.37 The steering circuit is used to direct the SD buffer register circuits to the proper bus for reception of address signals.

5.38 The enabler circuit generates the time window during which address information can be received. The start of the window occurs when an enable pulse is received. The enable circuit also generates on termination of the address window an enable-verify signal that is sent to the central processor indicating that an enable signal had been properly received.

5.39 The buffer register is a 28-bit buffer used to store an address. The buffer register is broken down into seven subregisters, five of which are shown in Fig. 6. The registers are given an alpha designation with the numeric subscript indicating the number of bits in the register. The designations are A8, B8, D4, C2, E2, H2, and T2. For a proper address to exist, each of these registers must have one and only one bit set. The A, B, C, and D registers designate the path through the selector, E designates the operation or release of the magnetic latching relay, H designates which of the two selectors in an SD is to be used (this will become more significant when combined mode operation is explained), and T specifies normal or maintenance operation during the cycle. With IMD, both bits set in the T register is valid and specifies a special order used only during diagnostics.

5.40 The selector interface and translation buffer circuits convert the logic outputs from the

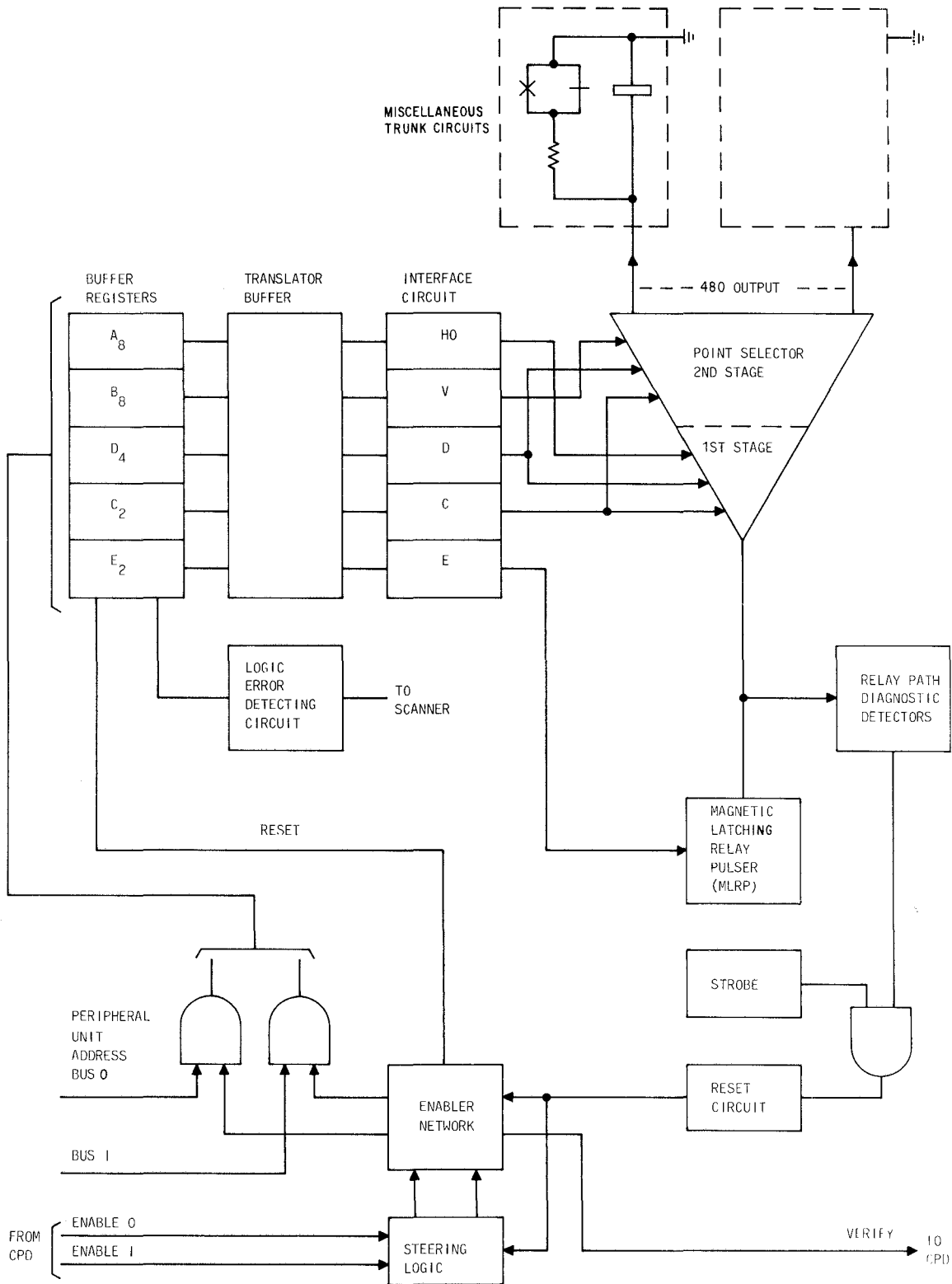


Fig. 6—Basic Signal Distributor Controller Block Diagram

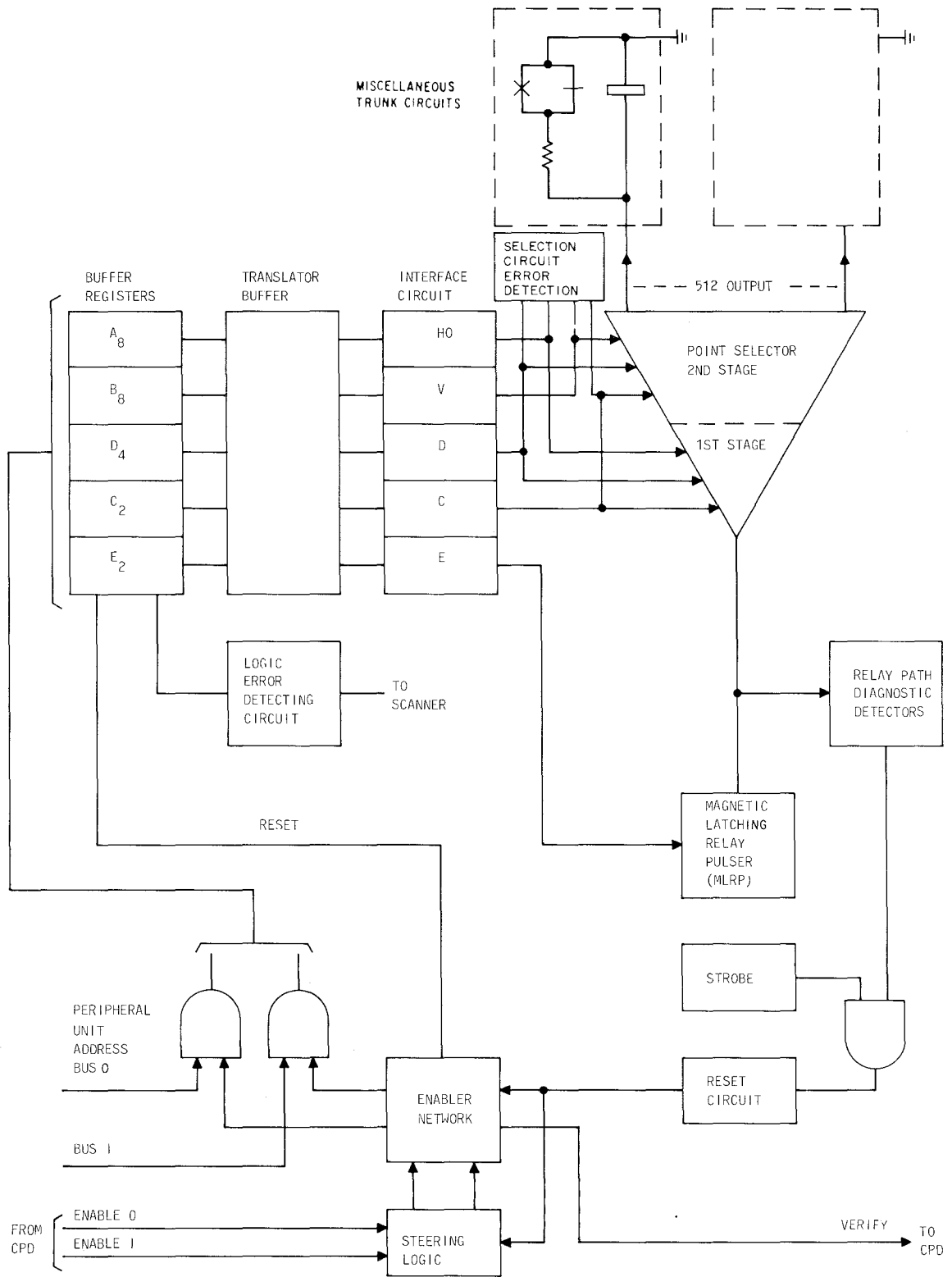


Fig. 7—Basic Signal Distributor Controller with IMD Block Diagram

buffer register into signals which are compatible with the gating of the selector circuit.

5.41 The logic error detecting circuit determines if one and only one bit has been set in the buffer register. If an error has occurred, progress through the SD cycle is interrupted and the fault is reported to the CC.

5.42 One function of the relay path diagnostic detectors is to determine if one and only one path has been established through the selector. It also determines if two or more relays have been connected to a given selector output with IMD; it also determines if no relays have been connected. If a single path with a single relay is not indicated, the SD cycle is interrupted and the fault condition is reported to the CC.

5.43 The magnetic latching relay pulser generates signals of the proper amplitude and duration for operating and releasing a magnetic latching relay. The relay path diagnostic detector has two functions in addition to the one described. One is to sense when the magnetic latching relay has worked as intended. This part of the circuit is called the armature movement detector. The detection of armature movement is used to indicate a successful cycle and to initiate the reset of the buffer registers. On the other hand, failure of armature movement indicates a faulty operation and is reported to the CC on the next cycle. The second function is used to sense when a release signal is being sent to an already released relay. This circuit is called a double release detector. Double release detection is important since second release under some circumstances, can place a magnetic latching relay in an operated state. Then the CC would consider the relay released when it is actually operated, and an intolerable situation would exist; hence, double releases must be detected and interrupted before operation of the relay can occur. The detection of double release is used to terminate the SD cycle. Since detection occurs early in the cycle, an operated relay will be avoided.

5.44 The strobe circuit shown in Fig. 6 (Fig. 7 for IMD) is used to mask out rapid voltage changes that occur on the selector path while the path is being established. These rapid voltage changes may cause false operation of the armature movement detector. The strobe gates the detector output only after sufficient time has elapsed to ensure that the chatter has disappeared.

5.45 The reset circuit is actuated if armature movement has been detected and the selection signal has been applied for a specified length of time. The reset circuit drives the enable and buffer register into a reset state.

POWER AND MISCELLANEOUS CIRCUIT

5.46 The power and miscellaneous circuit provides +24, +48, and -48 volt filters and fuses for circuits on the frame. This circuit also provides ground, high resistance ground, -48 volts, and +24 volts to test-pin jacks for frame testing.

6. MAINTENANCE AND DUPLICATION

6.A. Standard Maintenance Functions

6.01 Maintenance registers are provided for placing either of the two controllers in modes of operation other than normal. These modes are used under trouble conditions and/or to perform maintenance tests. Maintenance procedures for the CMT frame are contained in TOP 231-050-002.

6.02 Maintenance addresses are indicated when the T1 bit of the T2 register is set, as shown in Fig. 8. When the T1 bit is set, the D4 register is used to indicate what maintenance function is to be performed. The D0 bit indicates a quarantine or an out-of-service mode is to be established; the D1 bit indicates a test access mode is to be established, and the D2 bit indicates the maintenance registers are to be reset.

6.03 Note that maintenance functions to be performed on the left-half controller are addressed to the right-half buffer register and vice versa. The maintenance mode, once established, is maintained by the maintenance registers (Fig. 8) until the registers are released under the direction of the CC by simultaneously sending a T1 and D2 bit.

6.04 When a controller is placed in the test access mode, its ability to operate and release magnetic latching relays is not affected. In the test access mode, the master scanner is connected to check circuits within the SD. The check circuits of each controller are connected to the master scanner via multiples that are common to all SD controllers and are referred to as the SD diagnostic bus.

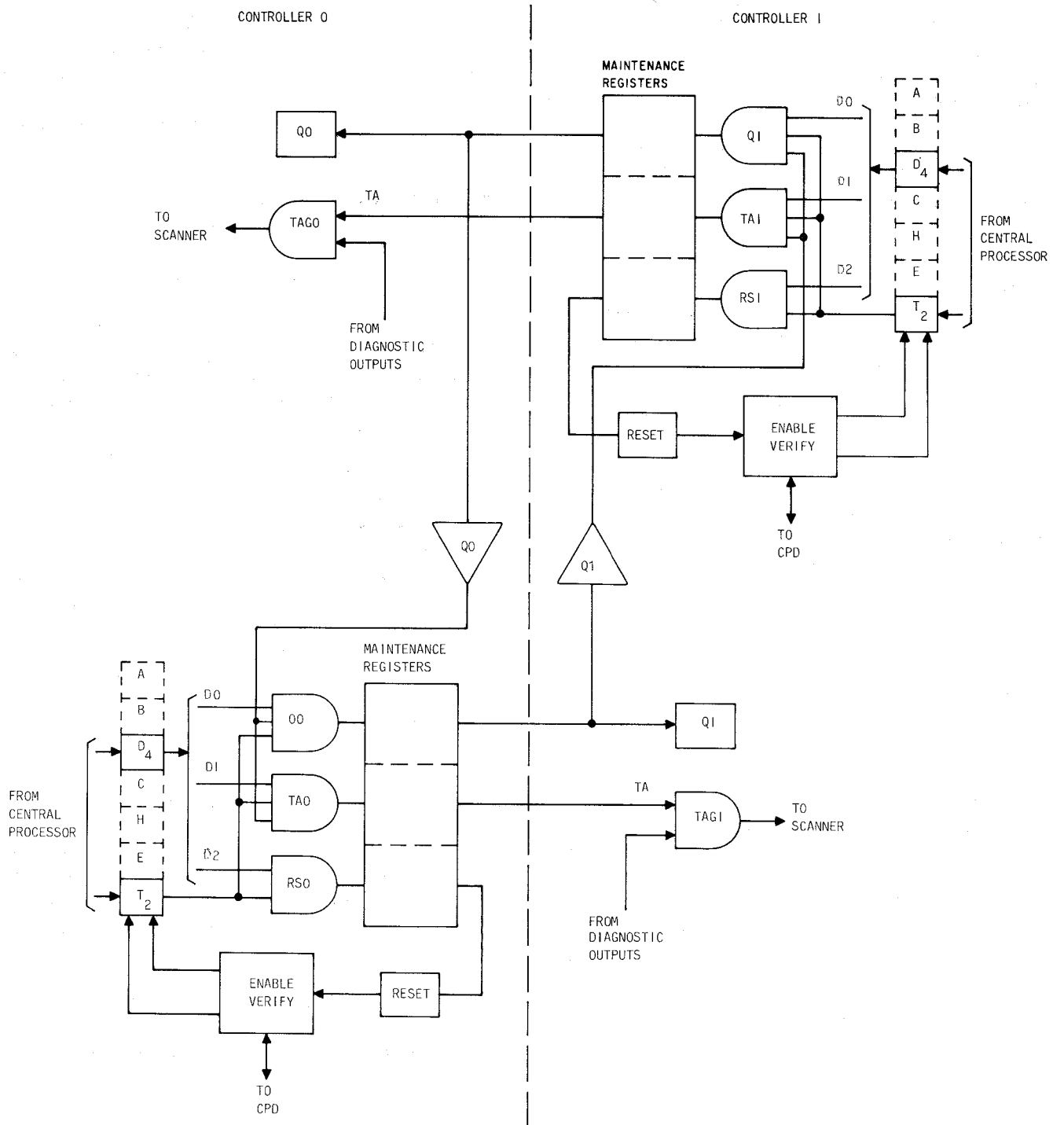


Fig. 8—Maintenance Logic

6.05 While a controller is in the test access mode, the addresses from the CC that are used for testing purposes may be incomplete, in which case no path is closed through the selector. Each of these addresses is directed to the basic SD in which the test access mode has been established. The CC then inspects the test points via the master scanner. After each test, the CC resets all circuits in the controller by signaling over an appropriate path provided in the PUAB.

6.06 When a controller is placed in quarantine, it is removed from service. The other controller is given full access to both selectors. (This is called the combined mode of operation.) The in-service controller has the capability of making a 1-out-of-960 point selection and controlling any of the magnetic latching relays connected to the two selectors. Assume the left controller is quarantined; the right controller can complete a path to any one of the 960 output terminals (Fig. 9). The H section of the buffer register controls the half of the selector in which a pulse path is established. In all modes of operation, the address from the CC contains selections of the H section of the buffer register. However, only one controller can control all of the outputs if the other controller is in quarantine. Control connections between opposite halves are established only when one of the quarantine relays, Q0 or Q1, is operated (Fig. 8 and 9).

6.07 Provisions have been made so that a controller can be manually quarantined. Manual quarantine is established automatically when power is removed from one of the controllers. A mechanical lockout feature is provided to eliminate the possibility of manually removing power from both controllers at the same time.

6.08 To return an SD from a combined mode of operation to split mode, the CC addresses the buffer register such that the D2 and T1 bits are set. This results in the maintenance registers being cleared.

6.09 The controlling circuitry of the SD is duplicated, but not in the sense that one controller operates the whole SD while the other stands by ready to take over. Normally, one controller offers access to one-half of the output terminals, while the other controller offers access to the other half.

6.10 In each controller, the buffer registers are equipped to accept an address from either of the duplicated PU buses. Each controller has two enable inputs through which the CC determines the bus from which address information is to be registered and to which SD, of the many possible SDs in an office, the address is to be sent.

◆B. IMD Maintenance Functions

6.11 When the SD is equipped with IMD (Option V for the SD and option Y for the optional SD), there are significant additions to the maintenance functions of the SD. The IMD provides improved fault detection and isolation, as well as some maintenance improvements. In addition to the maintenance functions described above, IMD also provides the functions as described in the following paragraphs. Figure 10 shows the maintenance logic of an SD equipped with IMD.

6.12 Besides maintenance states of normal, quarantine, and test access mode, IMD provides double quarantine and a second test access mode called TPA2. The original test access mode is renamed TPA1. There are also two additional reset orders. One is Release Double Quarantine, which takes the controller which is in double quarantine mode and puts it into quarantine mode. The second reset is Release TPA 2, which takes a controller out of TPA2 and puts it into TPA1.

6.13 Unlike quarantine and TPA1, maintenance functions of double quarantine and TPA2 are addressed to the controller under test. For example, the order to put controller 0 into double quarantine is sent to controller 0. These maintenance modes are maintained by maintenance registers until an appropriate reset order is sent.

6.14 It should be noted that in order to put a controller into double quarantine, it must first be in quarantine mode. Similarly, a controller must be in TPA1 before it is put into TPA2.

6.15 Double quarantine mode allows both controllers full access to all 960 SD points. It is used during SD diagnostics so that one controller can operate and release relays for call processing while the other controller is being thoroughly tested by the diagnostic program. The controller in double quarantine is considered out of service. When either controller is in double quarantine, both out-of-

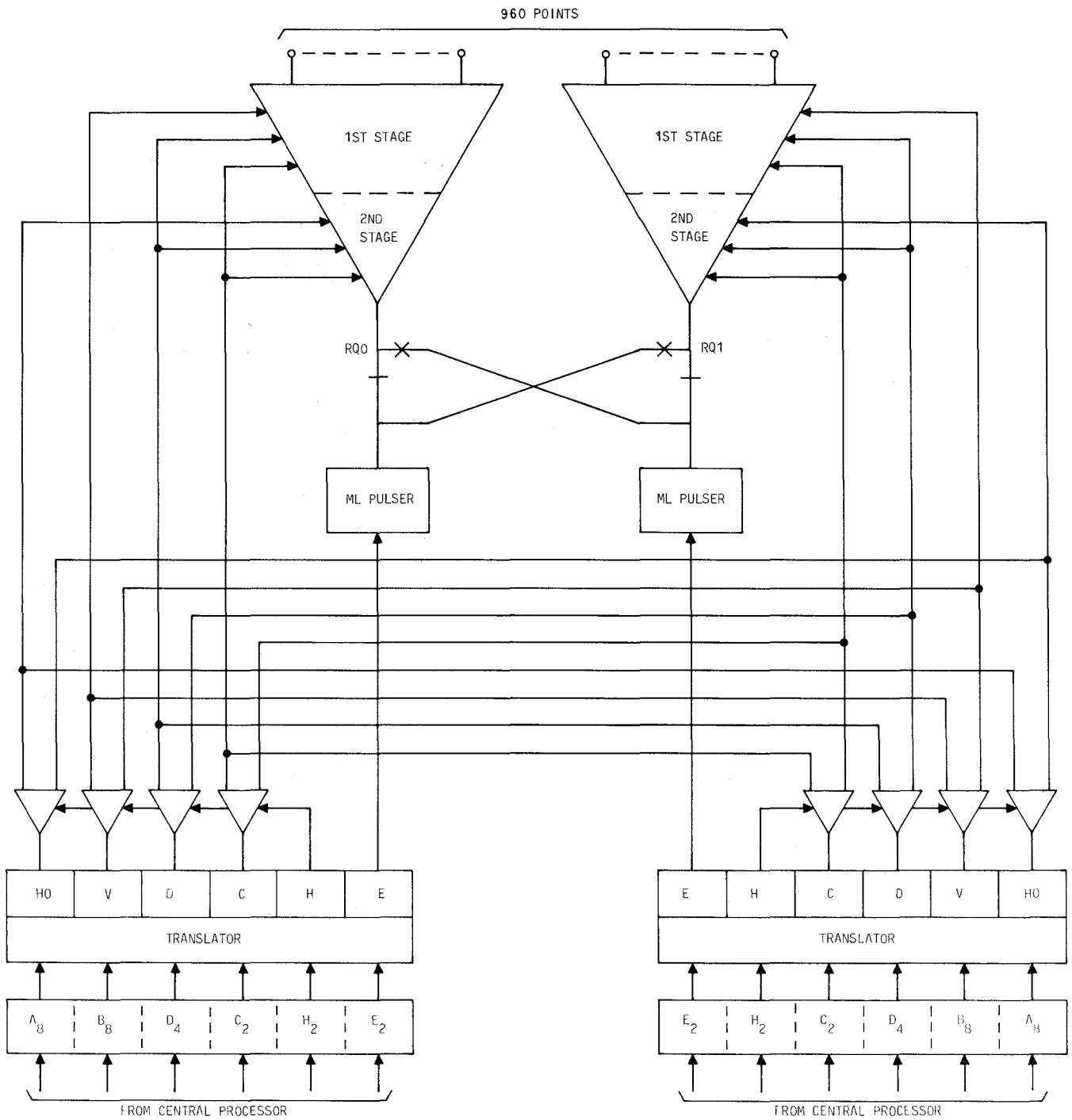


Fig. 9—960-Point Supplementary Signal Distributor with Selection and Pulse Path Required for Combined Mode Operation

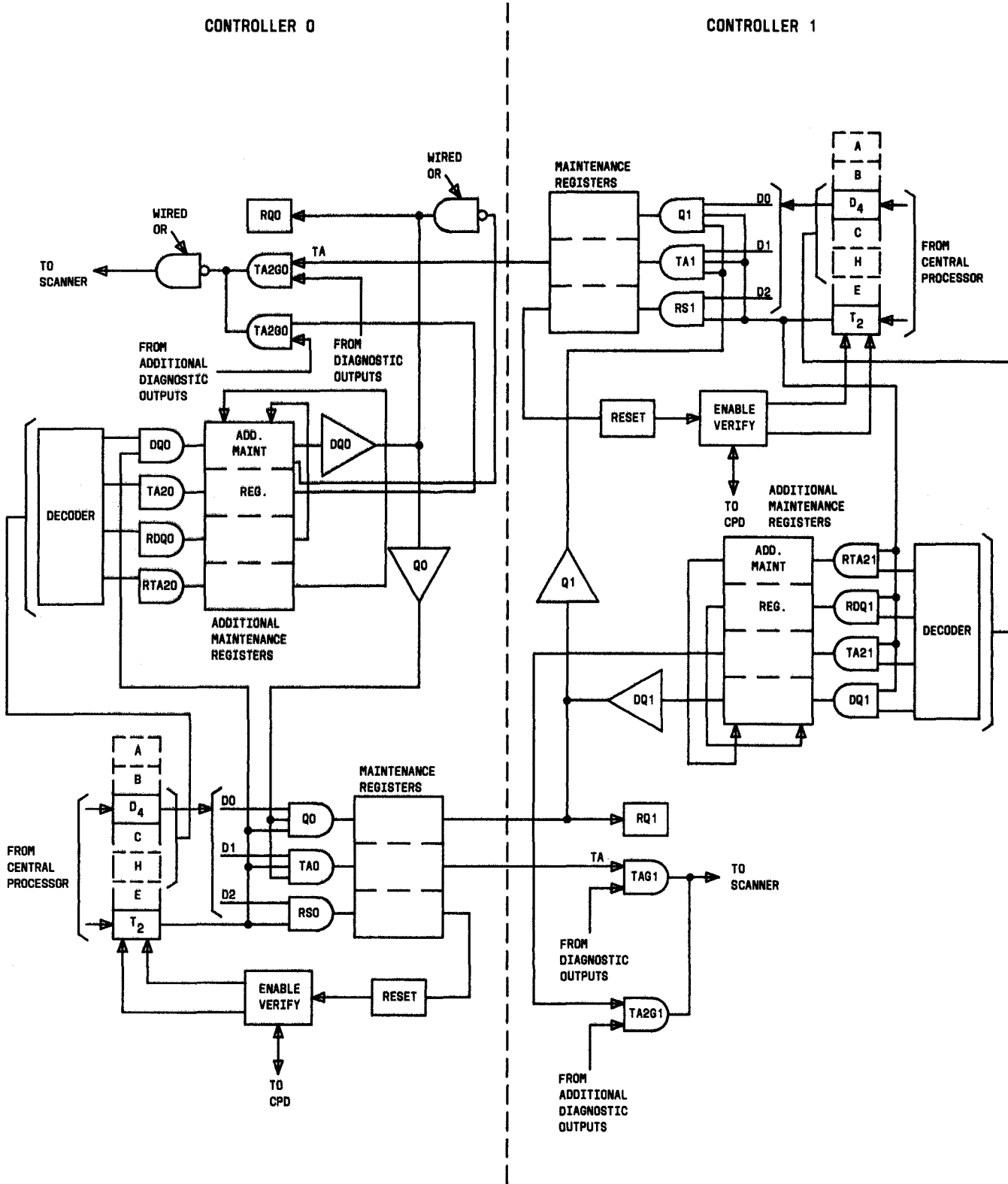


Fig. 10—Maintenance Logic with IMD

service lamps will be illuminated, and both quarantine relays will be operated.

6.16 The TPA2 mode provides more test points which can be monitored. It also uses the same SD diagnostic bus as TPA1.♦

7. POWER AND MISCELLANEOUS CIRCUITS

7.01 These circuits provide filters, fuses, and a means of applying and removing power to the CMT frame. Abnormal conditions within the CMT frame are reported to the system via scan points, and visual and audible alarms are also initiated. These circuits also provide test-pin voltage jacks and a means of communicating between frames.

FRAME LINE TELEPHONE JACKS

7.02 This circuit provides means of communicating between the CMT frame and all other frames in the ESS switch office. The telephone jacks are located on the extreme left-hand side of the left bay control panel (Fig. 1 and 11). The local frame line is located in the line and trunk test bay of the master control center. The telephone head set when plugged into the telephone jacks completes the talking path. The local frame line has no means of signaling.

SPARE JACK

7.03 This circuit provides a 3-wire belt line around the office for miscellaneous use. The jack is located on the left bay control panel next to the telephone jack (see Fig. 1 and 11).

TEST-PIN JACKS

7.04 These circuits provide ground, high resistance ground -48 volt and $+24$ volt battery for testing in the frame. These jacks are located on the left bay control panel and provide access from both front and back of the frame (Fig. 11).

FILTERS, FUSES, AND FUSE ALARM CIRCUITS

7.05 These circuits provide $+24$, $+48$ and -48 volt filters and fuses for circuits on the CMT frame. The $+24$ TBS and -48 TBS non-alarm fuses provide voltage for the test-pin jacks on the frame. The $+24$ LP non-alarm fuses provide voltage through the $+24$ LP leads, to the fuse alarm scan point SC00,

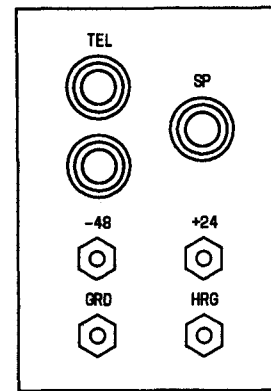


Fig. 11—Miscellaneous Circuits

to the PWR OFFL and PWR OFFR lamps, and to other lamps on the frame.

7.06 The failure of any alarmed fuse on the frame will operate the FA relay and

- (1) Light the PWR OFFL and PWR OFFR lamps
- (2) Signal the major alarm to the office alarm circuit through leads ABG and MJ
- (3) Indicate a failure via scan point SC00.

8. TAKING EQUIPMENT OUT OF SERVICE

8.01 Only one of the two controllers of an SD or scanner can be taken out of service at any time. This is accomplished by the system when it has been requested to do so via the teletypewriter. Once a controller has been removed from service, power to it can be removed by operating the appropriate FRAME CONTROL OUT-OF-SERVICE key. **The system should always be requested to remove both the left SD and scanner controllers before the HOME FRAME CONTROL OUT-OF-SERVICE key is operated** because the HOME FRAME CONTROL OUT-OF-SERVICE key controls both the left SD and both scanner controllers. The appropriate out-of-service lamp will light when the system quarantines (removes from service) the controller. The out-of-service keys override any frame condition previously established. The system is able to determine the state of the controllers by the state of the S, F, and T scan points assigned to it. The frame control panels are shown in Fig. 12.

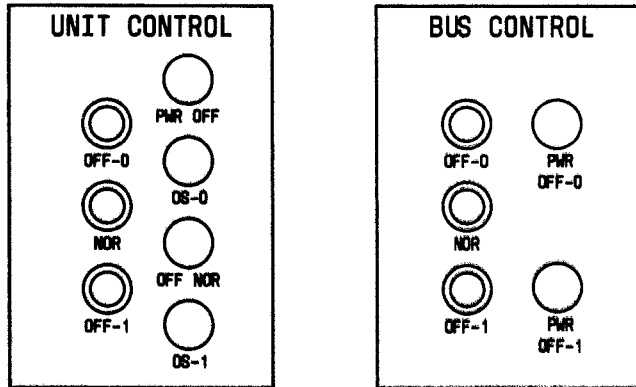


Fig. 12—Frame Control Panels

8.02 When the system has been requested to remove a controller from service, it remains out of service until a request via the TTY to restore it to service has been made. To restore controllers to service, use appropriate input message NM-RESTORE for SSD and for scanners.

8.03 Power is applied to the SSD controller and the scanner controller by the PW0 and PW1 power relays. The power relays are controlled by a 3-position locking key. In the NOR position, power is applied to both controller 0 and 1 of the SSD and scanner controllers. Depressing the OFF-0 pushbutton removes the power associated with controller 0 of both the SSD and the scanner. The OFF-1 pushbutton controls power to controller 1 of both the SSD and scanner controllers. Both controller 0 and 1 power cannot be removed at the same time. When power from either controller 0 or 1 has been removed, the POWER-OFF red lamp will light.

8.04 The bus circuit has a 3-position locking key that controls the power applied to the circuit. These three positions are designated NOR, OFF-0, and OFF-1. In the NOR position, power is applied to both 0 and 1 circuit packs for the bus circuit. Depressing the OFF-0 pushbutton removes power from all circuit packs associated with the 0 side of the bus circuit. Depressing OFF-1 pushbutton removes power from all circuit packs associated with the 1 side of the bus circuit. Power cannot be removed from both the 0 and 1 side at the same time.

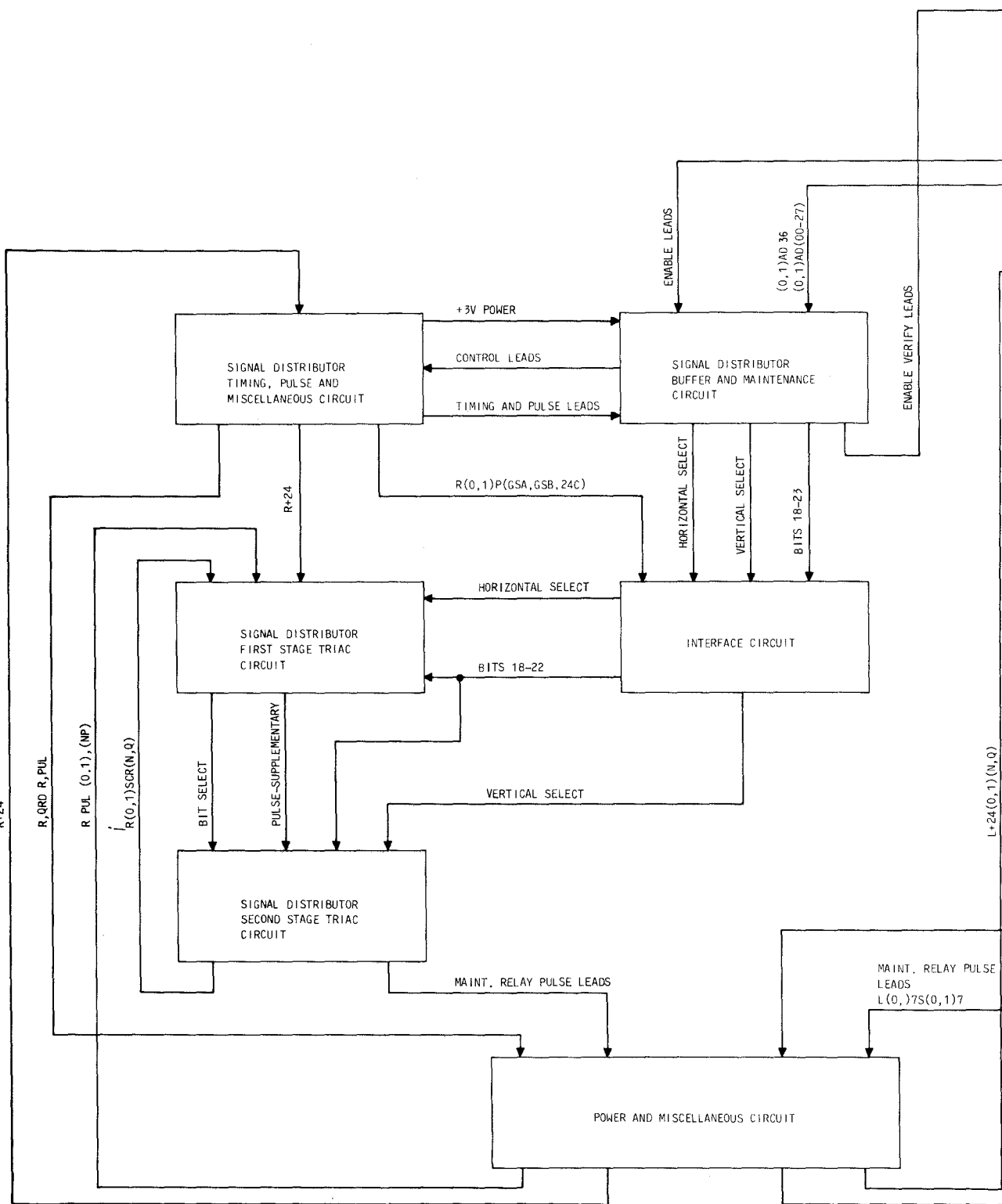
9. REFERENCE DOCUMENTATION

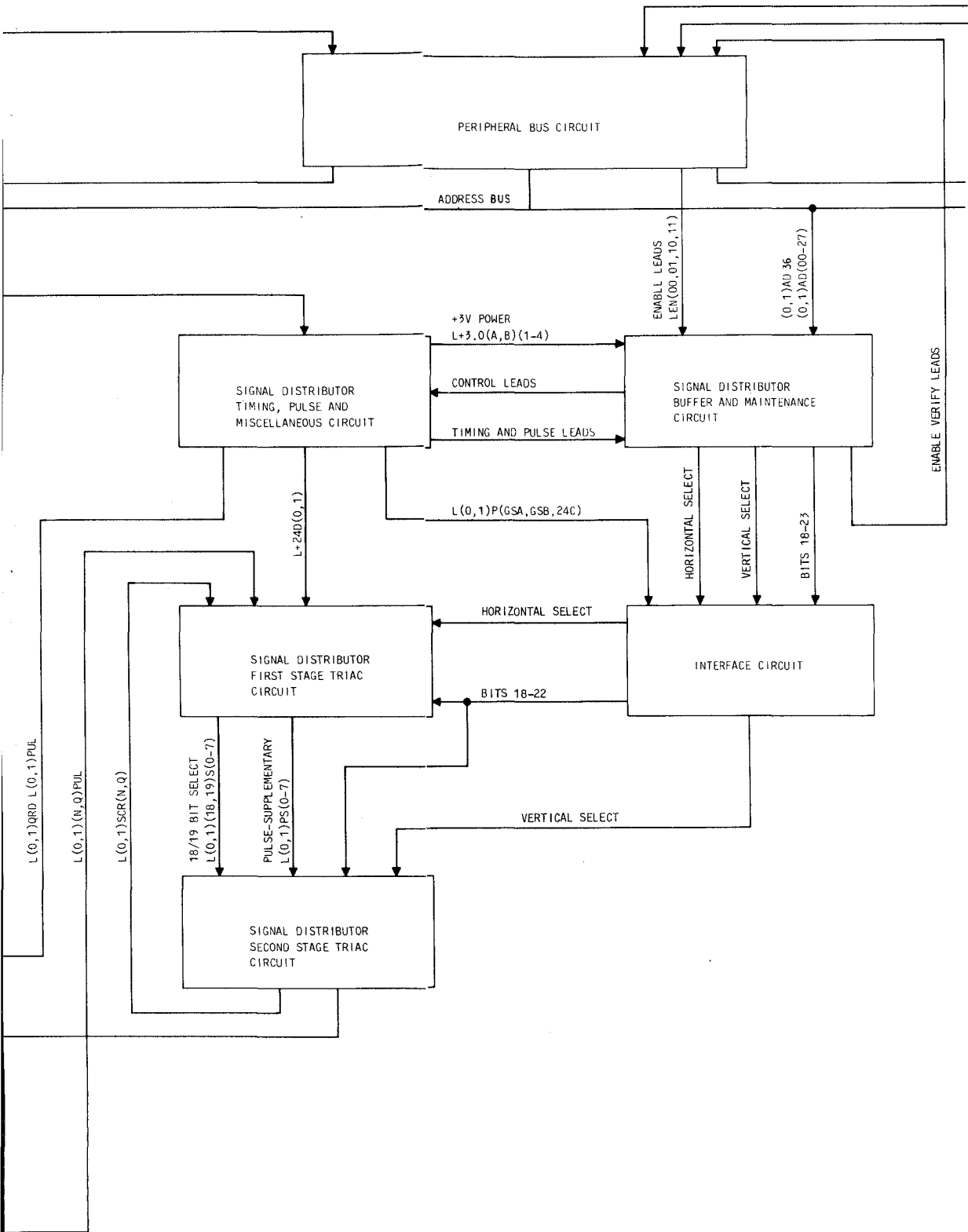
9.01 Reference documentation is listed below.

SD-1A401-01	Control Circuit for the Combined Miscellaneous Trunk Frame
SD-1A402-01	Supplementary SD for the Combined Miscellaneous Trunk Frame
SD-1A403-01	Matrix Circuit for the Combined Miscellaneous Trunk Frame
SD-1A404-1	Trunk Interconnection Circuit 1 for the Combined Miscellaneous Trunk Frame
SD-1A405-01	Power and Miscellaneous Circuit for the CMT Frame
SD-1A406-01	Cable Circuit for the CMT Frame
SD-1A407-01	Trunk Interconnection Circuit for the Plug-In Customer Dial Pulse Receiver
SD-1A408-01	Trunk Interconnection Circuit for the CMT Frame (128 SD Points and 64 MS Points)
SD-1A409-01	Trunk Interconnection Circuit for the CMT Frame (64 SD Points and 48 MS Points)
SD-1A410-01	Trunk Interconnection Circuit for the Plug-In Attendant Trunk and Loop Circuits
SD-1A411-01	Trunk Interconnection Circuit for the Plug-In 3-Port Conference Circuit
SD-1A412-01	Trunk Interconnection Circuit for the CMT Frame (96 SD Points and 32 MS Points)
SD-1A413-01	Trunk Interconnection Circuit for the CMT Frame (96 SD Points and 64 MS Points)

SD-1A414-01 Trunk Interconnection Circuit for
the CMT Frame (96 SD Points and
64 MS Points Adjacent Row As-
signment)

SD-1C650-01 Common System
TOUCH-TONE® Calling Re-
ceiving Circuit Type H.





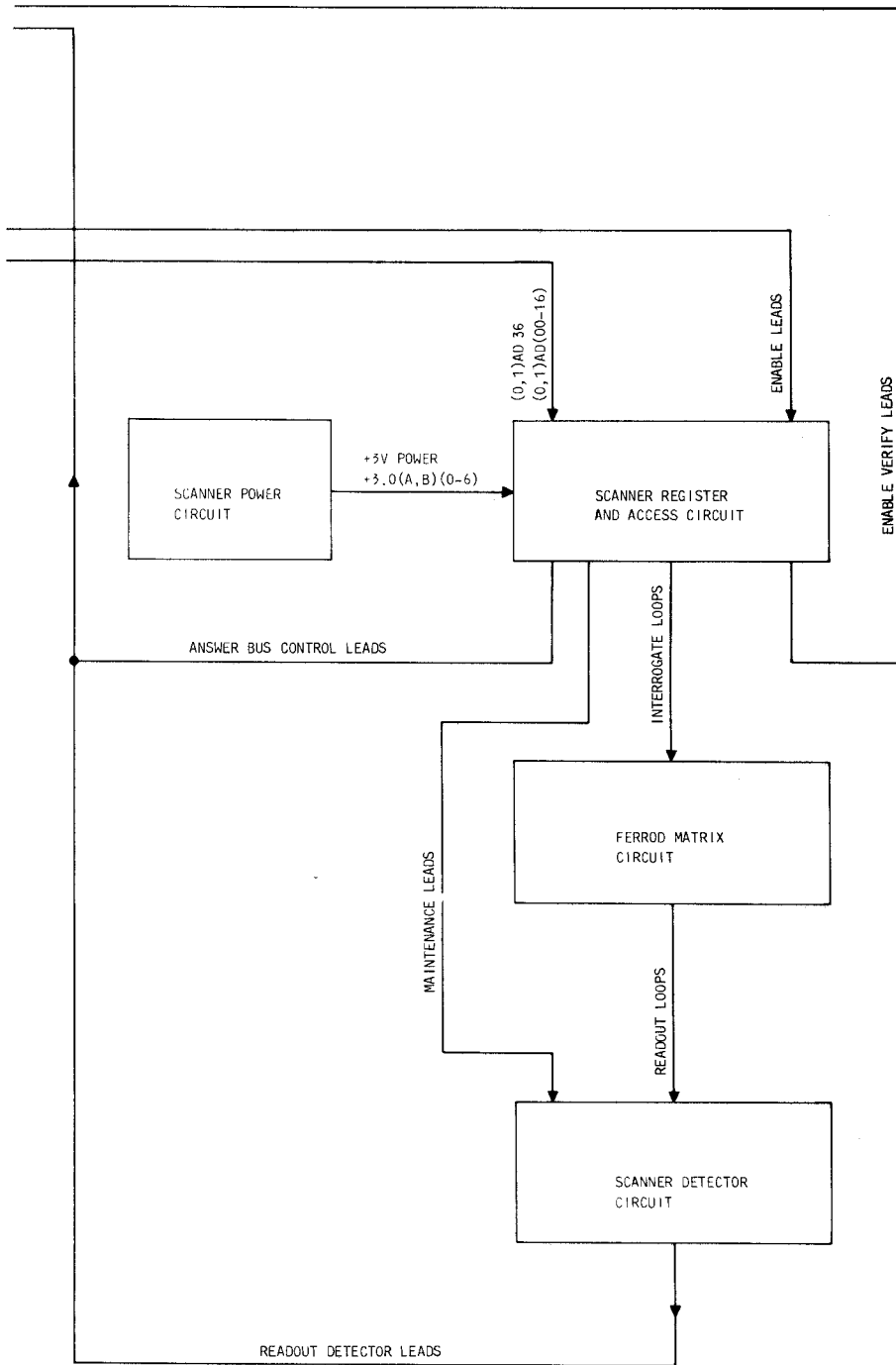


Fig. 13—CMT Functional Block Diagram