HILO UNIVERSAL TRUNK CIRCUITS AND FRAME DESCRIPTION 2-WIRE NO. 1 AND NO. 1A ELECTRONIC SWITCHING SYSTEMS WITH HILO 4-WIRE FEATURE

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1. GENERAL

1.01 This section describes and gives the theory of operation for the HILO 4-wire universal trunk (HUT) frame used in the No. 1 or No. 1A Electronic Switching System (ESS) combined local/toll offices. See Fig. 1 and 2.

1.02 Whenever this section is reissued, the reason for reissue will be listed in this paragraph.

1.03 Abbreviations used in this section are as follows:

ASW—All-seems-well

CC—Central Control

CPD—Central Pulse Distributor

ESS—Electronic Switching System

EPSCS—Enhanced Private Switched Communication Service

HILO—High out, Low input

HGF—HILO Grouping Frame

HUT—HILO Universal Trunk

LS—Least Significant

MS—Most Significant

MT—Maintenance Test

PU—Peripheral Unit

PUAB—Peripheral Unit Address Bus

SD—Signal Distributor

SP—Signal Processor

μS—Microseconds

2. PHYSICAL DESCRIPTION

2.01 The HUT frame is a standard double bay framework 7 feet 0 inches high by 6 feet 6 inches wide by 1 foot 0 inches deep. The HUT frame supports 256 plug-in trunks (512 trunk circuits) and the associated power filtering, fusing alarm, bus, scanner, and signal distributor control units. The physical location of these various J coded units within the frame work is detailed in Figures 3, 4, and 5. In general, the HUT frame layout follows the standard arrangement used for all No. 1 ESS frames. The power filters and fuses are at the bottom of the frame, communications bus circuits and terminal strips for external frame wiring are located at the top of the frame. External wiring to trunk circuits is accomplished by wiring directly to the connector of the trunk circuits. The remaining frame space is utilized to support the plug-in trunks.

3. FUNCTIONAL DESCRIPTION

A. General

3.01 The HILO 4-wire switching feature makes it possible to use the existing No. 1 and No. 1A ESS 2-wire remreed switching network to provide an equivalent 4-wire switching function. This function is accomplished by converting the 2-wire bidirectional conductor pair into two independent unidirectional unbalanced paths and using the ground path as the common return. A typical use of this frame will be for intertoll and enhanced private switched communication service (EPSCS).

3.02 In order to assure high quality transmission through the 2-wire switching network while in the unbalanced mode, the normal voltage transmission mode is converted to a current mode. A final conversion before leaving the 2-wire switching office restores the transmission to the voltage

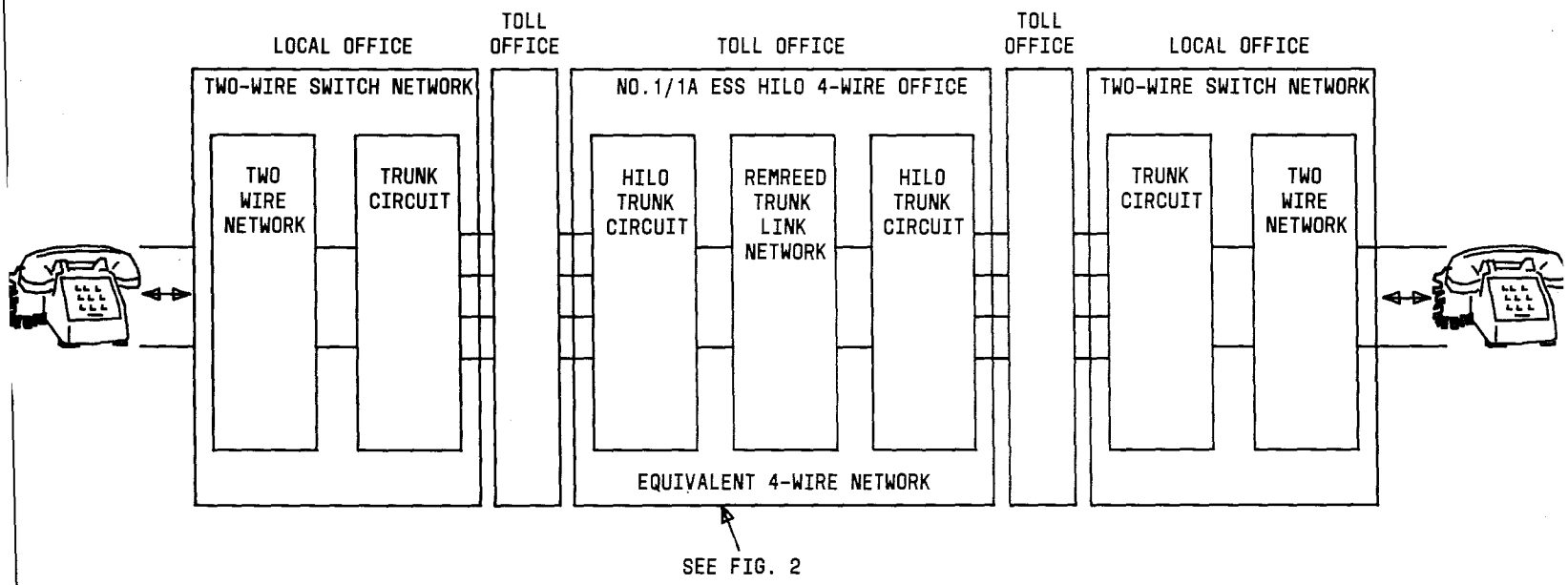


Fig. 1—Typical Toll C

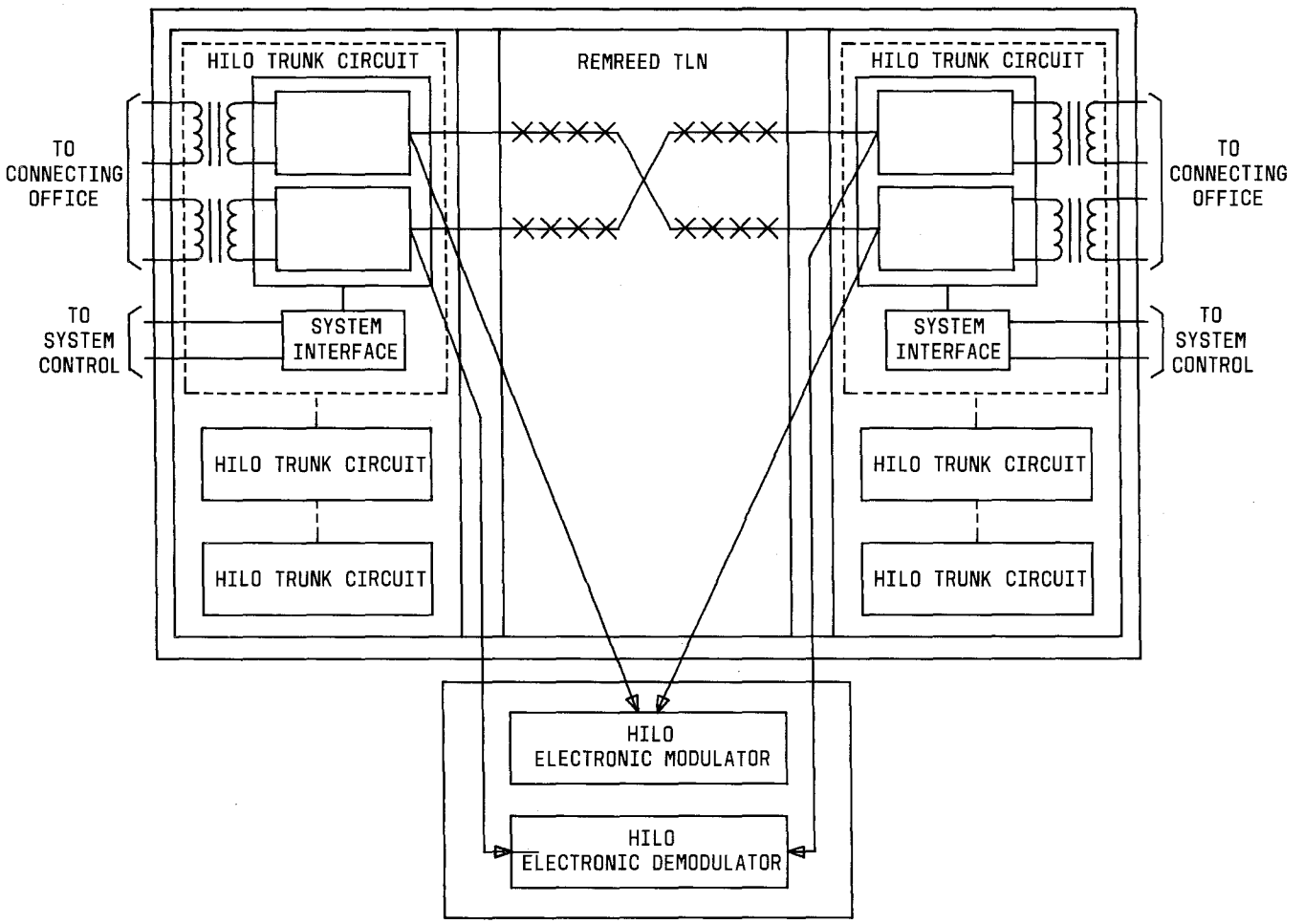


Fig. 2—No. 1/1A ESS HILO 4-Wire Office

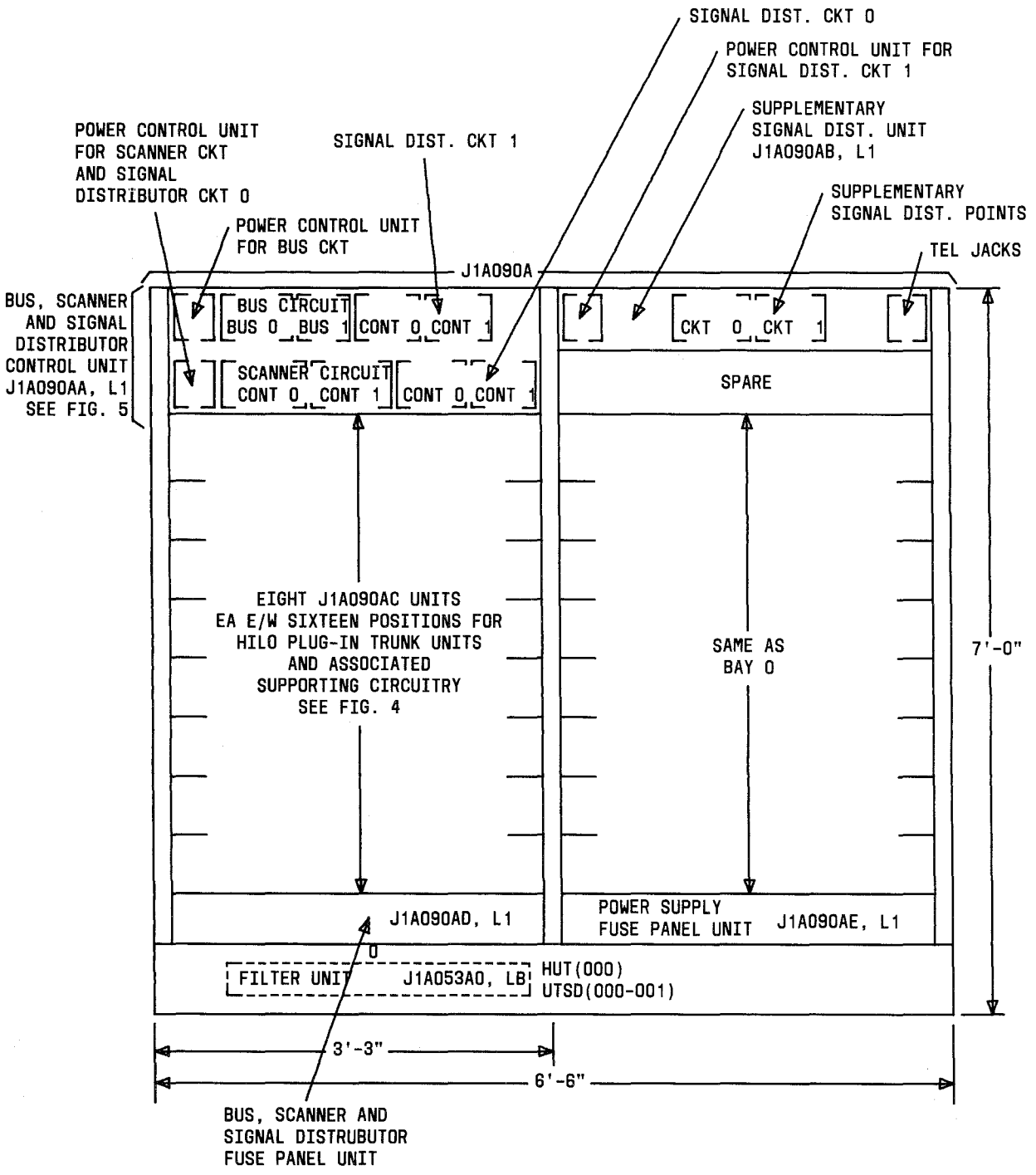


Fig. 3—HILO Universal Trunk Frame

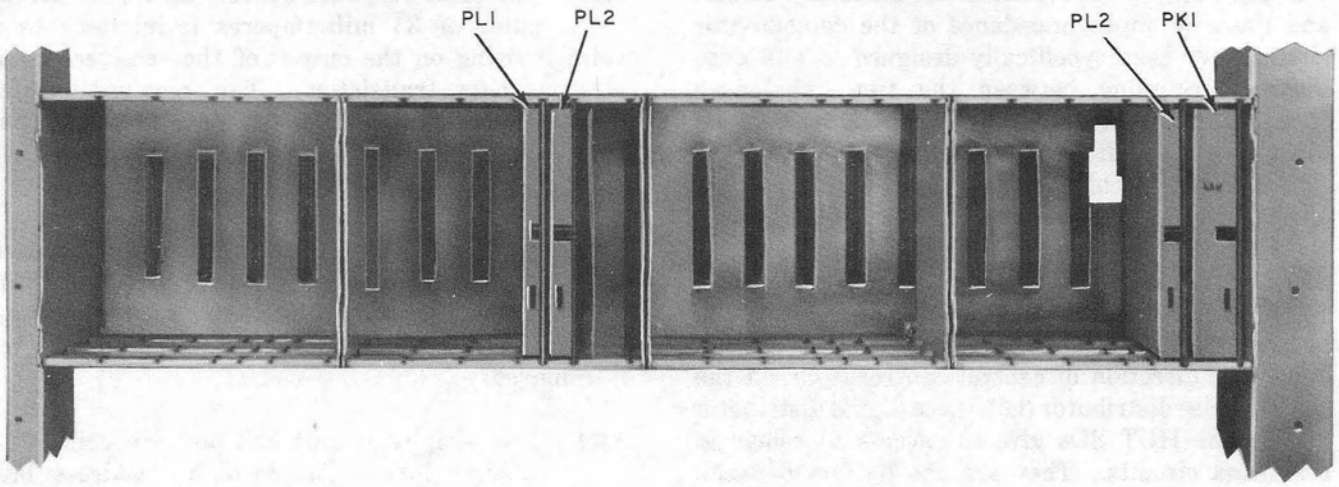


Fig. 4—HILO Plug-in Trunk Unit J1A090AC

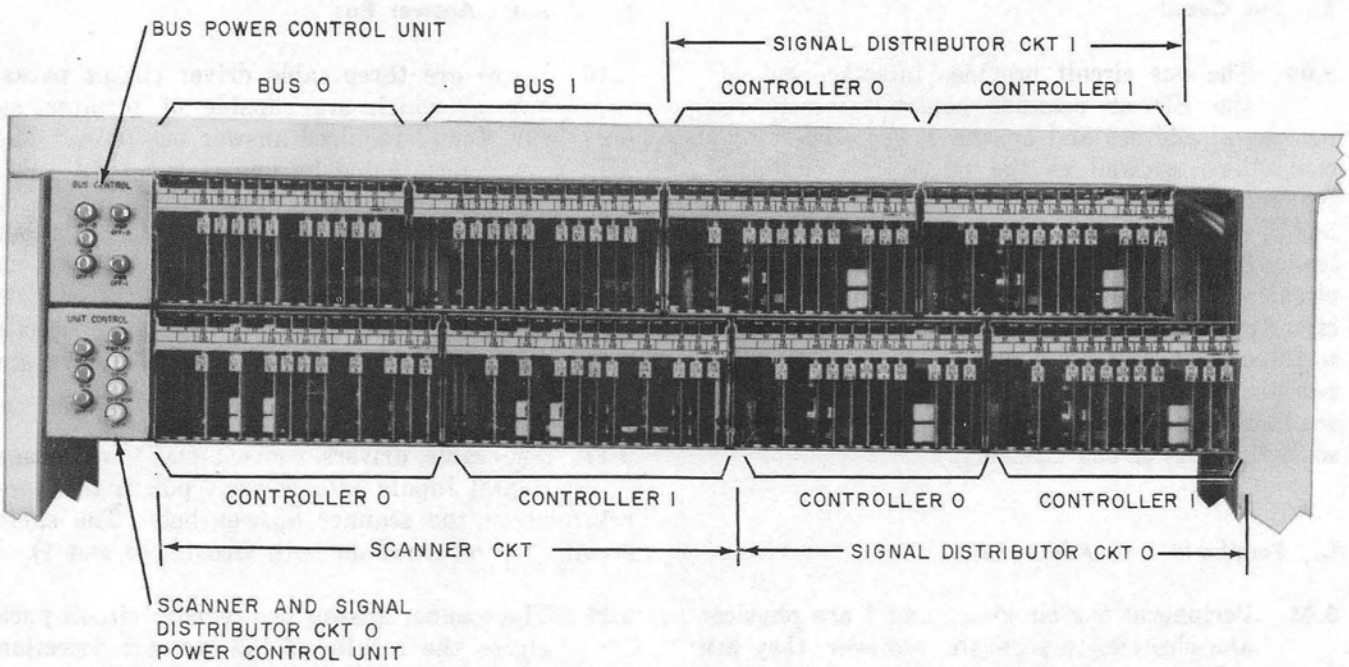


Fig. 5—Bus, Scanner, and Signal Distributor Control Unit

mode. This voltage-to-current-to-voltage conversion is accomplished by the HILO modulator and demodulator circuits located on each trunk circuit. The ***high*** output impedance of the modulator circuit and the ***low*** input impedance of the demodulator circuit have been specifically designed to minimize crosstalk coupling between the two unbalanced paths. This impedance level difference is the bases for the name HILO (***HI***gh output impedance of the modulator circuit and the ***LOw*** input impedance of the demodulator circuit).

3.03 The HUT is used to complete and supervise paths established through the switching network. Relays within the trunk circuits operate under the direction of central control (CC) via the central pulse distributor (CPD) and signal distributor (SD). The HUT SDs give CC access to relays in the trunk circuits. They are the buffers between the high-speed CC and low-speed relays. The scanner in the HUT supervises interoffice calls. Bay 0 has the control unit for a 1024-point scanner. The scanner detects and sends to the CC any change in trunk or loop conditions that results from relay operation or action from a distant office. See the functional block diagram in Fig. 6.

B. Bus Circuit

3.04 The bus circuit provides interface between the SD or scanner control circuits and peripheral address and answer buses. The circuit controllers, as well as the buses, are duplicated for reliability. The method for selecting the bus-to-controller path is provided via the enable leads from the central pulse distributor (CPD) circuitry. The bus circuitry also includes the circuitry for generating the enable-verify signals to the enable cable pairs and a scanner-answer bus register which stores the results generated by the scanner and provides the interface of the scanner with the answer-bus circuitry.

C. Peripheral Unit Address Bus

3.05 Peripheral bus circuits 0 and 1 are physical and electrically separate, however, they are functionally identical. This description will apply to both circuits, unless otherwise stated.

3.06 Included in each bus circuit are four cable receiver circuit packs which receive a total of 29 address or control bits. A fifth cable-receiver circuit pack is provided which receives six enable bits.

3.07 The cable receivers convert an input current pulse of 35 milliamperes (minimum) to a voltage swing on the output of the receiver, using a saturating transistor. The receiver output terminal is normally high (no pulse). An output on the receiver is a low going voltage pulse 0.5 microseconds wide.

3.08 The input pick-off transformer is located on the receiver circuit pack. A bypass resistor maintains the continuity of the bus when the receiver circuit pack is pulled out and the transformer is removed.

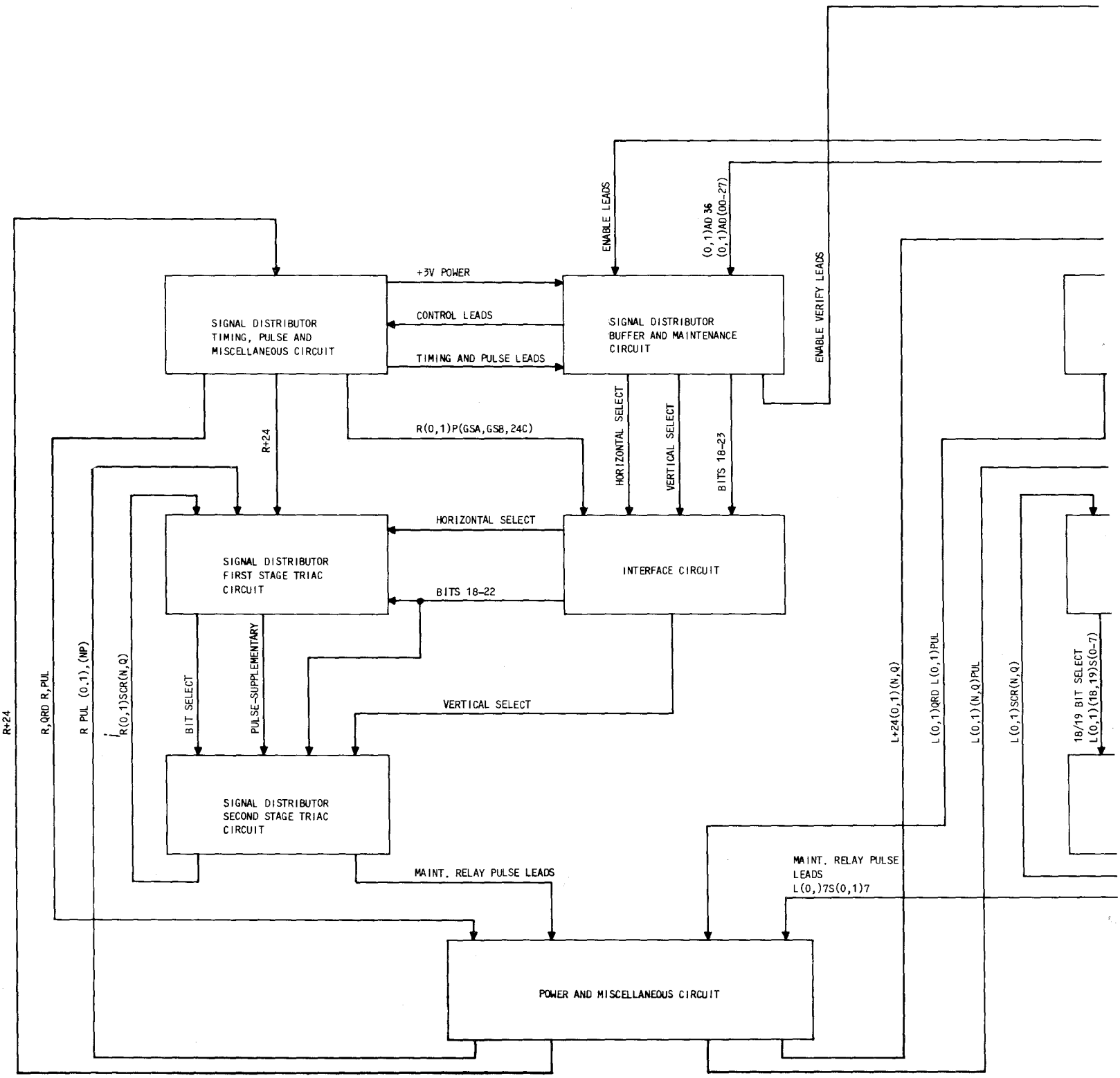
3.09 The peripheral unit bus bits are called the address bits. The incoming address bits have the letters AD in their lead designation. A 0 or 1 prefix indicates the bus number, and a P or N suffix indicates the relative voltage polarity of the wire. The remaining two digits indicate the bit number 00 through 36.

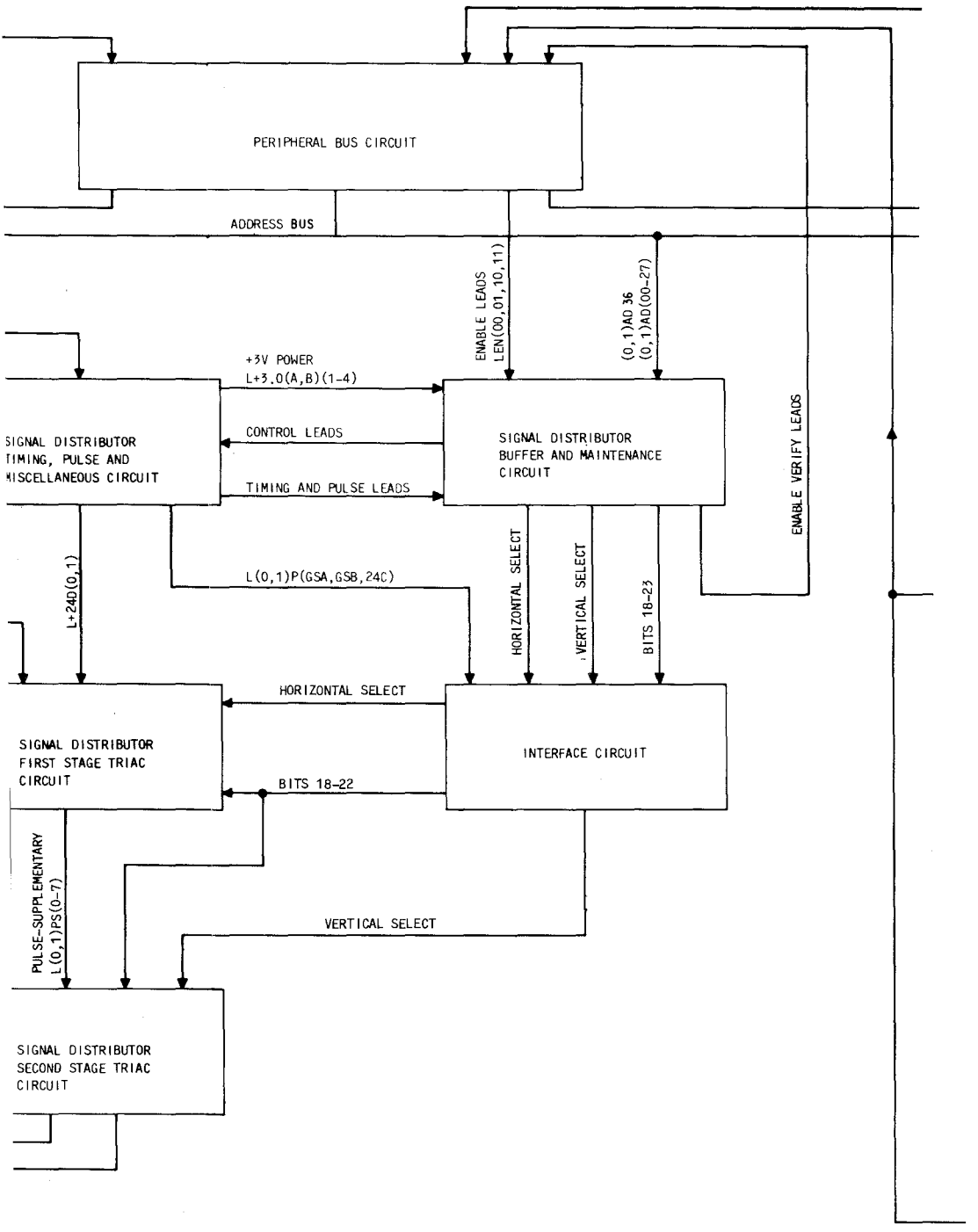
D. Scanner Answer Bus

3.10 There are three cable driver circuit packs, two of which are capable of terminating only 16 of the 17 required answer bus pairs. The 17th pair is terminated by one of the eight cable drivers on the third pack. The outputs of six of the remaining seven circuits connect to the input of the enable cable receiver pack. These six cable-driver circuits generate enable-verify signals on the same cable pair on which the enable signals were previously received. These enable pairs are terminated into 100 ohms.

3.11 The cable drivers convert the low voltage digital inputs into current pulses that are returned on the scanner answer bus. The same results are returned on both circuits (0 and 1).

3.12 The scanner answer bus register circuit pack stores the results of the scanner detection packs or stores the all-seems-well (ASW) information and provides the low voltage digital input to the cable driver. The scanner answer bus register circuits are always active and perform the same function regardless of which scanner controller is active.


ENABLE LEADS
(0,1)AD 36
(0,1)AD(00-27)
ENABLE VERIFY LEADS
+3V POWER
CONTROL LEADS
TIMING AND PULSE LEADS
SIGNAL DISTRIBUTOR TIMING, PULSE AND MISCELLANEOUS CIRCUIT
SIGNAL DISTRIBUTOR BUFFER AND MAINTENANCE CIRCUIT
R+24
R(0,1)P(GSA,GSB,24C)
HORIZONTAL SELECT
VERTICAL SELECT
BITS 18-23
HORIZONTAL SELECT
BITS 18-22
SIGNAL DISTRIBUTOR FIRST STAGE TRIAC CIRCUIT
INTERFACE CIRCUIT
R+24
R,QRD R,PUL
R PUL (0,1),(MP)
R(0,1)SCR(N,Q)
BIT SELECT
PULSE-SUPPLEMENTARY
VERTICAL SELECT
SIGNAL DISTRIBUTOR SECOND STAGE TRIAC CIRCUIT
MAINT. RELAY PULSE LEADS
MAINT. RELAY PULSE LEADS L(0,)7S(0,1)7
L+24(0,1)(N,Q)
L(0,1)QRD L(0,1)PUL
L(0,1)(N,Q)PUL
L(0,1)SCR(N,Q)
18/19 BIT SELECT L(0,1)(18,19)S(0-7)
POWER AND MISCELLANEOUS CIRCUIT


PERIPHERAL BUS CIRCUIT
ADDRESS BUS
ENABLE LEADS
LEN(00,01,10,11)
(0,1)AD 36
(0,1)AD(00-27)
+3V POWER
L+3.0(A,B)(1-4)
CONTROL LEADS
TIMING AND PULSE LEADS
SIGNAL DISTRIBUTOR
TIMING, PULSE AND
MISCELLANEOUS CIRCUIT
SIGNAL DISTRIBUTOR
BUFFER AND MAINTENANCE
CIRCUIT
ENABLE VERIFY LEADS
L+24D(0,1)
L(0,1)P(GSA,GSB,24C)
HORIZONTAL SELECT
VERTICAL SELECT
BITS 18-23
HORIZONTAL SELECT
SIGNAL DISTRIBUTOR
FIRST STAGE TRIAC
CIRCUIT
INTERFACE CIRCUIT
BITS 18-22
PULSE-SUPPLEMENTARY
L(0,1)PS(0-7)
VERTICAL SELECT
SIGNAL DISTRIBUTOR
SECOND STAGE TRIAC
CIRCUIT

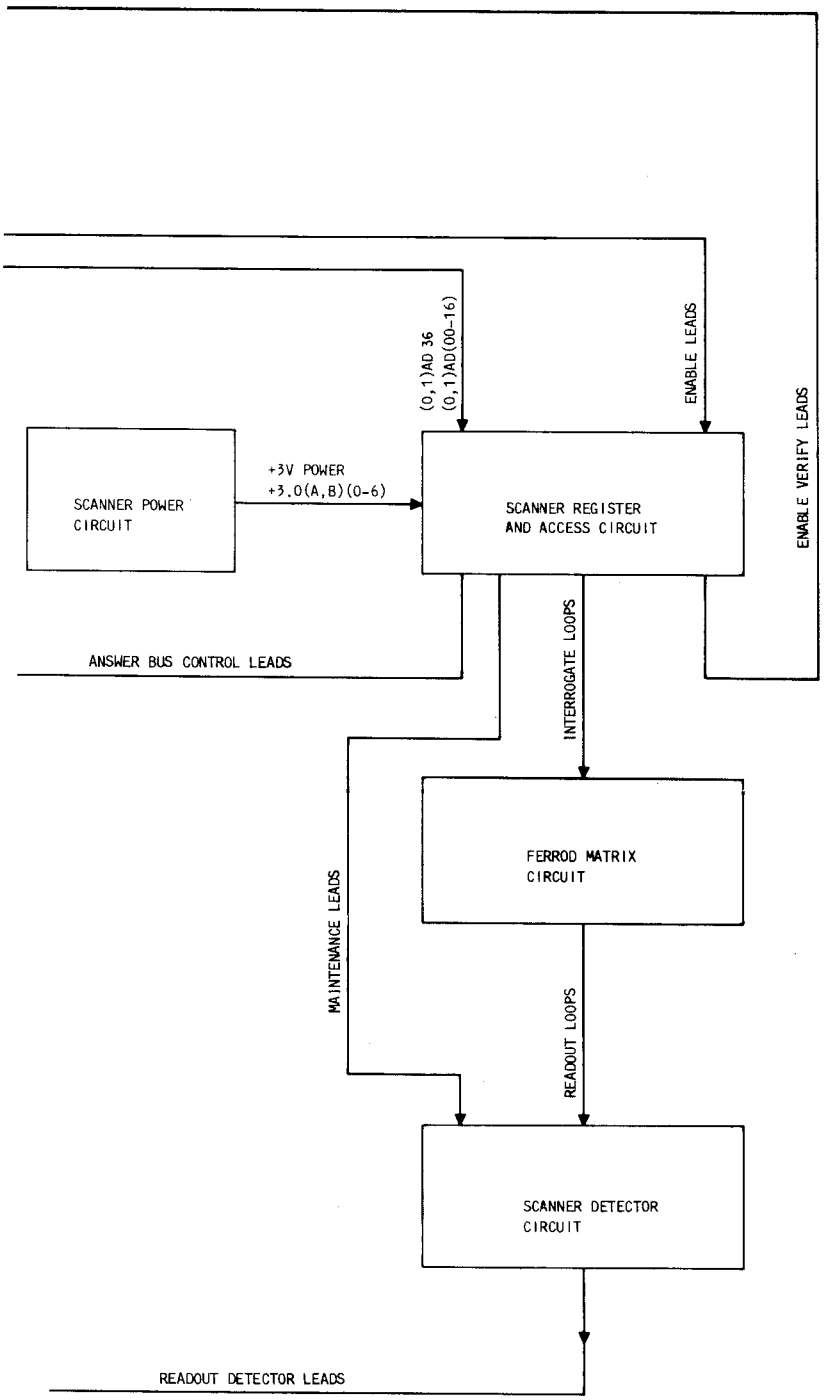


Fig. 6—HUT Function Block Diagram

E. Enable

3.13 The enable pairs have the letters EN in their lead designation followed by two numbers signifying controller and bus. The enable-verify leads have the letters EV in their lead designation preceded by a 0 or 1 indicating the bus circuit. SC0 and SC1 indicate the scanner controllers and SD00 SD01, SD10, and SD11 indicate the SD controllers.

F. Scanner

3.14 The scanner circuit provides supervision of interoffice calls and can monitor a maximum of 512 calls (1024 trunks) simultaneously. The scanner consists of a ferrod sensor matrix and a controller that is duplicated for reliability. the ferrod sensors are assigned to trunk circuits and are not duplicated. Groups of 16 ferrod sensor (Fig. 7) are scanned (interrogated) simultaneously. The average rate varies between one every 100 milliseconds and once every 200 milliseconds depending on traffic load.

G. Ferrod Sensor

3.15 The ferrod sensor is a basic unit of the scanner. it can be considered a 2-winding transformer whose coupling (the ability to induce a signal from the primary winding to the secondary winding) is controlled by current in the control windings. The primary and secondary windings of the transformer are associated with the interrogate-and-readout equipment windings respectively. If the facility is on-hook (transmission path is not established and current is not present in control windings), the interrogate signal induces a signal in the readout windings. If the facility is off-hook (transmission path is established and current is present in control windings), the coupling is destroyed and the interrogate signal is not able to induce a signal into the readout winding. The control windings are associated with either the network side or the trunk side of a trunk circuit.

H. Ferrod Sensor Matrix

3.16 The ferrod sensors, two per trunk circuit are arranged into two 16 by 32 matrices for the 1024-point scanner. There is a particular scanner address associated with each row of 16 ferrods and the 16 ferrods in the row are interrogated simultaneously when an address is received by the peripheral unit address bus. Addresses to a scanner are sent from the signal processor (SP). The answers of the scanner (busy-idle information for 16 trunks circuit, either network side or trunk side) are returned to the addressing equipment. If the scanner functions properly, an ASW signal is sent with the 16 interrogation replies.

I. Scanner Organization

3.17 The two major parts of the circuit are the ferrod sensor matrix and the interrogate-and-readout equipment. The interrogate-and-readout equipment is duplicated (scanner 0 and 1) for reliability. The ferrod sensors are assigned to the trunk circuit on a per trunk basis and are not duplicated.

J. Enabling and Addressing a Scanner

3.18 Scanners are considered peripheral units (PU). All PUs in a central office are addressed simultaneously over the peripheral unit address bus (PUAB). The particular PU that is to reply is selected by an enabling signal from the CPD.

3.19 All signaling to and from the scanners (except the control of the ferrods by the trunk circuit) is accomplished using 0.5-μs intercommunication pulses on the duplicated PUAB system. Each scanner controller must be able to operate from either PUAB, with the selection being made by the enabling pulse via the CPD. The address controller replies simultaneously on both PU reply buses.

3.20 Associated with each controller are two enabling pairs that determine from which bus to accept addresses. The answer bus contains 16 pairs for ferrod outputs and a 17th pair for the ASW signal.

3.21 An address bus to the scanner is divided into two groups: the least significant (LS) group and the most significant (MS) group. Both groups contain eight pairs of wires. The scanner uses an additional pair of wires of the address bus for maintenance test orders (MT).

K. Controller Operation

3.22 To operate a controller, an enabling pulse is sent. This opens a gate, permitting the

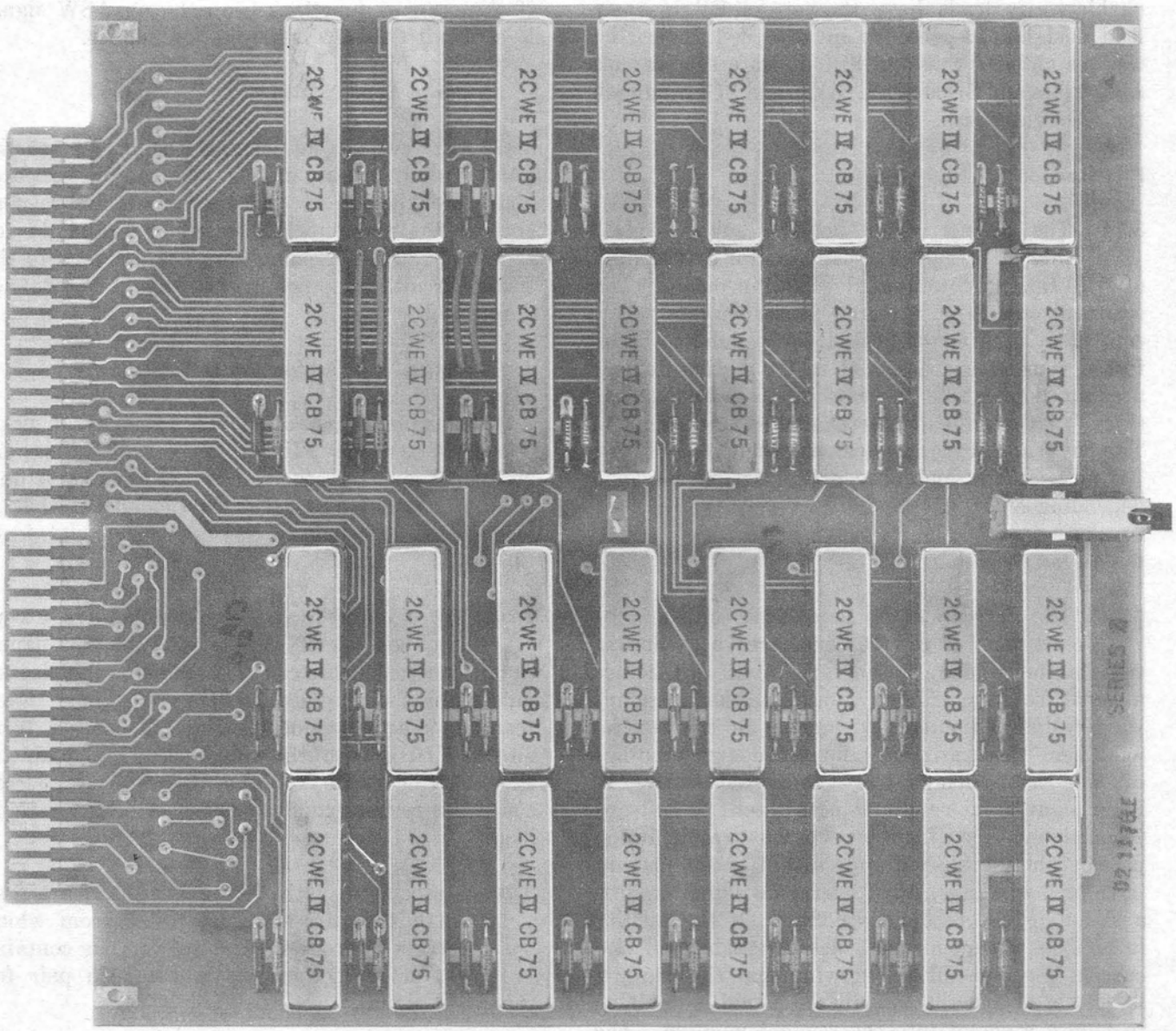


Fig. 7—Plug-in Ferrod Circuit Pack

address to be received for 2.2 μs (for 0.4 μs after an address is received). At 1.3 μs, after the start of the enabling pulse, the previously enabled pair is pulsed for 1 μs by the controller. This permits the CPD to verify that the enable pulses reach the correct equipment. A valid address results in a pulse on only one pair of wires in the LS and MS group of inputs (maintenance-test pair not pulsed). The PU bus circuit receives the address pulses and stores them in the address register and the access circuitry. The register and access circuitry translates LS and MS address inputs so that one of 64 rows of 16 ferrods is selected and interrogated. The outputs of the 16 ferrods are detected by the detector circuit and stored in the scanner-answer register. If there is no current in the control windings of the ferrod, the output circuitry produces a pulse (1). If there is current in the control windings of the ferrod, the output circuitry will produce no pulse (0) when interrogated. The result of the interrogation (16 outputs) is transmitted simultaneously on both scanner-answer buses.

3.23 The maximum operate time of the scanner is 2.2 μs. A scanner may be addressed at a minimum interval of 7-μs intervals.

L. TRIAC Signal Distributor

3.24 The signal distributor (SD) used in No. 1 and No. 1A ESS gives the central processor the ability to operate and release magnetic latching relays in trunk circuits, junctor circuits, and certain control circuits. The SD acts as a buffer between the central processor (electronic speeds) and the peripheral relays (relay speed).

3.25 There are two pairs of SD controllers in the HUT frame (Fig. 3). The two controllers of a pair are designated by 0 and 1. The SD controller pair for Bay 0 is designated SD00 and SD01. The SD controller pair for Bay 1 is designated SD10 and SD11.

3.26 The basic SD is composed of a controller and a 1-out-of-512 point selector. The SD, when directed by information sent in the form of a 28-bit address from the central processor, sets up a signal path to one of the 512 magnetic latching relays. The address also directs the controller to send a release or an operate signal to the relay. The controller detects the movement of the relay armature that initiates the reset of the controller enable and address register. Until this reset function has been accomplished, no new addresses can be registered or acted upon. Two of these units (a controller and selector) make up a 1024-point SD. Normally, they operate independently of each other as separate entities in what is known as ***split mode*** operation. In No. 1 and No. 1A ESS, they are always provided in pairs, shown in Fig. 8.

4. OPERATION

A. General

4.01 The HUT circuits have little, if any, autonomy. With few exceptions, relays within these circuits operate only under the direction of the CC via the CPD and the SD. CC detects, via a scanner, any change in the trunk or loop conditions that results from relay operation or from actions by a distant office.

B. Trunk Circuits

4.02 The HUT is part of the communication channel between two switching systems. The communication channel starts at the outgoing terminals of the originating office and ends at the incoming terminals of the switching network of the terminating office. As shown in Fig. 9, a trunk includes the transmission facility terminated in two trunk circuits, one at each end.

4.03 The simplified illustrations (Fig. 10 and 11) show the relationship of outgoing and incoming trunks to the switching network.

C. Signal Distributor

4.04 The SD cycle begins when an enable signal is sent under direction of the central processor, via the CPD, to a specified SD controller (Fig. 12). This enable signal gates on the buffer registers via the enable network. The buffer registers store the address information for the duration of the operation cycle. Information stored in the buffer register is used to establish a path through the TRIAC selector to a specified magnetic latching relay and to select the operate or release signal from the magnetic latching relay pulser. When the relay operation or release is sensed by the relay action detector, the enable registers in the enabler circuit and the buffer register are reset. The controller is now prepared to receive

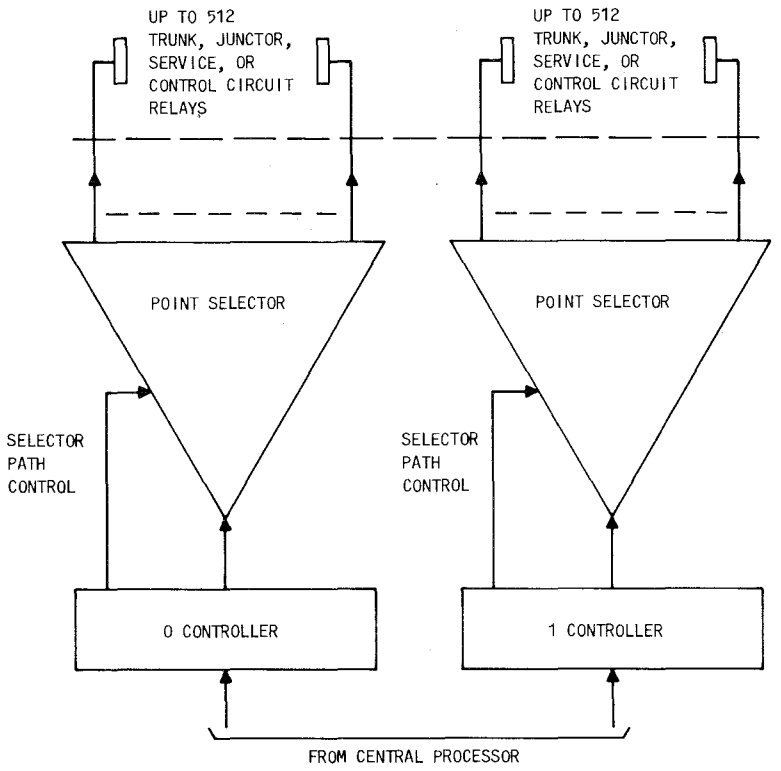


Fig. 8—Normal (Split) Mode Configuration of Signal Distributors

a new order from the central processor. Figure 13 shows the block diagram of the TRIAC signal distributor controller.

D. Signal Distributor Controller

4.05 The function of the SD controller is as follows:

(1) Receive address information from the central processor

(2) Temporarily store address information

(3) Check address and pulse path for errors

(4) Inhibit continued operation of the cycle when errors are found and report errors to the central processor

(5) Establish a path through the TRIAC selector

(6) Verify that relays worked as intended.

If all circuit conditions are satisfied, the controller resets and awaits the next order.

4.06 As shown in Fig. 12 the controller contains the following circuits:

(1) Steering logic circuit

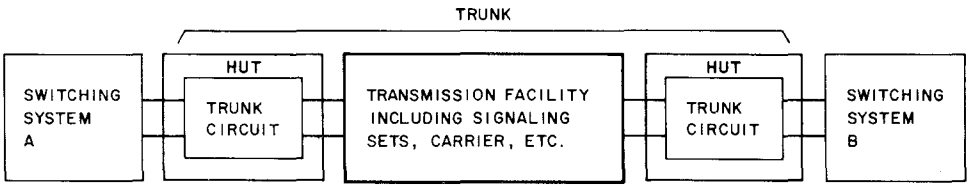


Fig. 9—Relationship of Trunk Circuit to Trunk

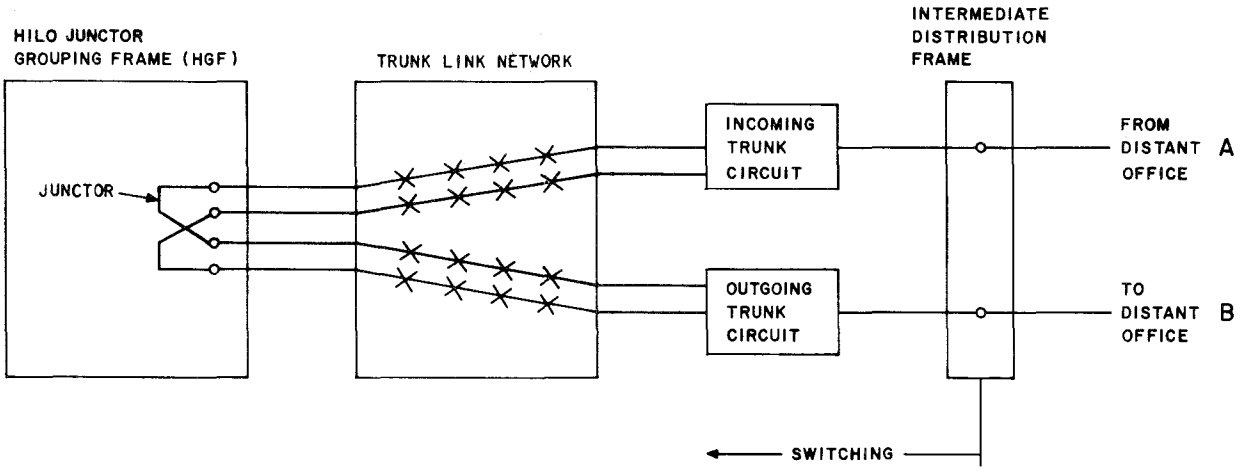


Fig. 10—Outgoing and Incoming Trunk Arrangement

(2) Enabler

(3) Buffer registers

(4) Selector interface and translation buffer

(5) Logic error detecting circuit

(6) Path detector circuit (Point Selector)

(7) Magnetic latching relay pulser

(8) Relay path diagnostic detectors

(9) Strobe circuits

(10) Reset circuit.

4.07 The steering circuit is used to direct the signal distributor buffer register circuits to the proper bus for reception of address signals.

4.08 The enabler circuit generates the time window during which address information can be received. The start of the window occurs when an enable is received. The enable circuit also generates on termination of the address window an enable verify signal that is sent to the central processor indicating that an enable signal had been properly received.

4.09 The buffer register is a 28-bit buffer used to store an address. The buffer register is broken down into seven subregisters, five of which are shown in Fig. 12. The registers are given an alpha designation with the numeric subscript indicating the number of bits in the register. The designations are A_8, B_8, D_4, C_2, E_2, H_2, and T_2. For a proper address to exist, each of these registers must have one and only one bit set. The A, B, C, and D registers designate the path through the selector, E designates the operation or release of the magnetic latching relay, H designates which of the two selectors in a signal distributor is to be used (this will become more significant when combined mode operation is explained), and T specifies normal or maintenance operation during the cycle.

4.10 The selector interface and translation buffer circuits convert the logic outputs from the buffer register into signals which are compatible with the gating of the selector circuit.

4.11 The logic error detecting circuit determines if one and only one bit has been set in the buffer register. If an error has occurred, progress through the signal distributor cycle is interrupted and the fault is reported to the central control.

4.12 One function of the relay path diagnostic detectors is to determine if one and only one path has been established through the selector. It also determines if two or more relays have been connected to a given selector output. If a single path with a single relay is not indicated, the signal distributor cycle is interrupted and the fault condition is reported to the central control.

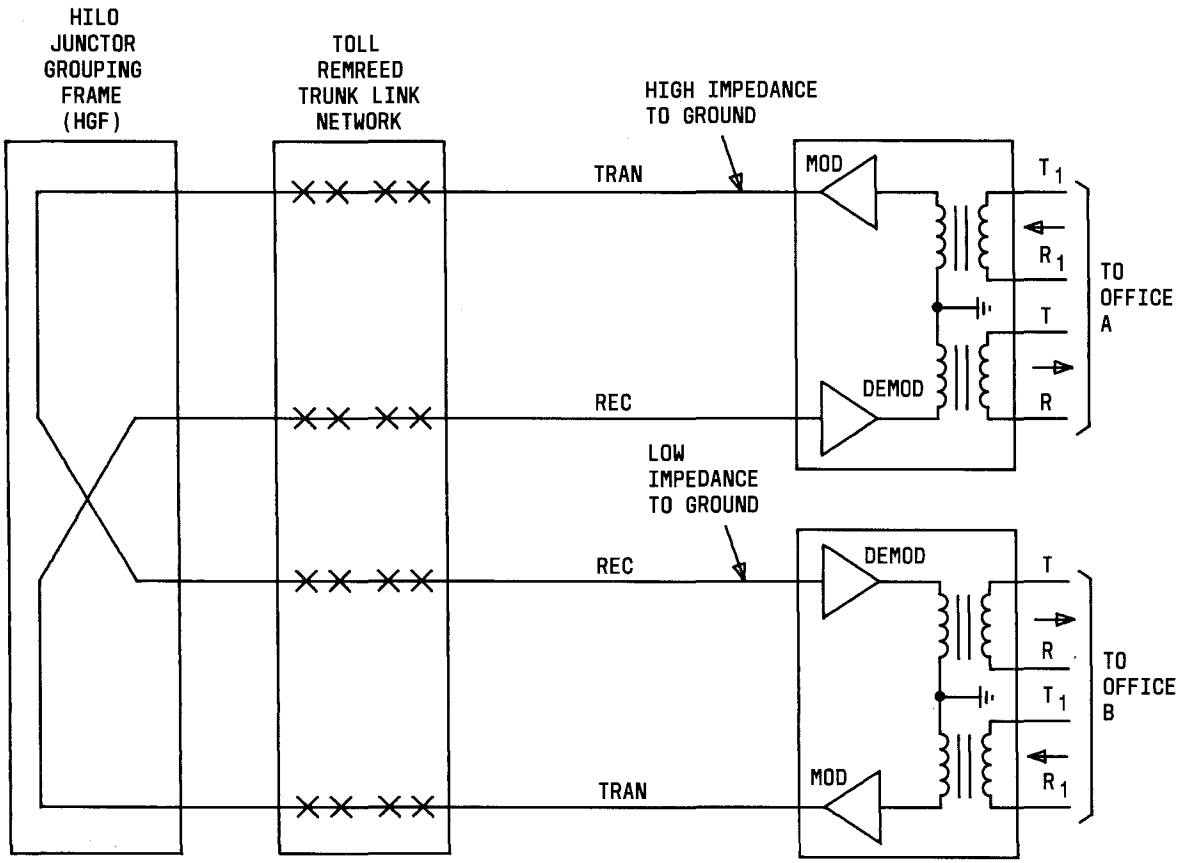


Fig. 11—HILO 4-Wire Network Using 2-Wire TLN

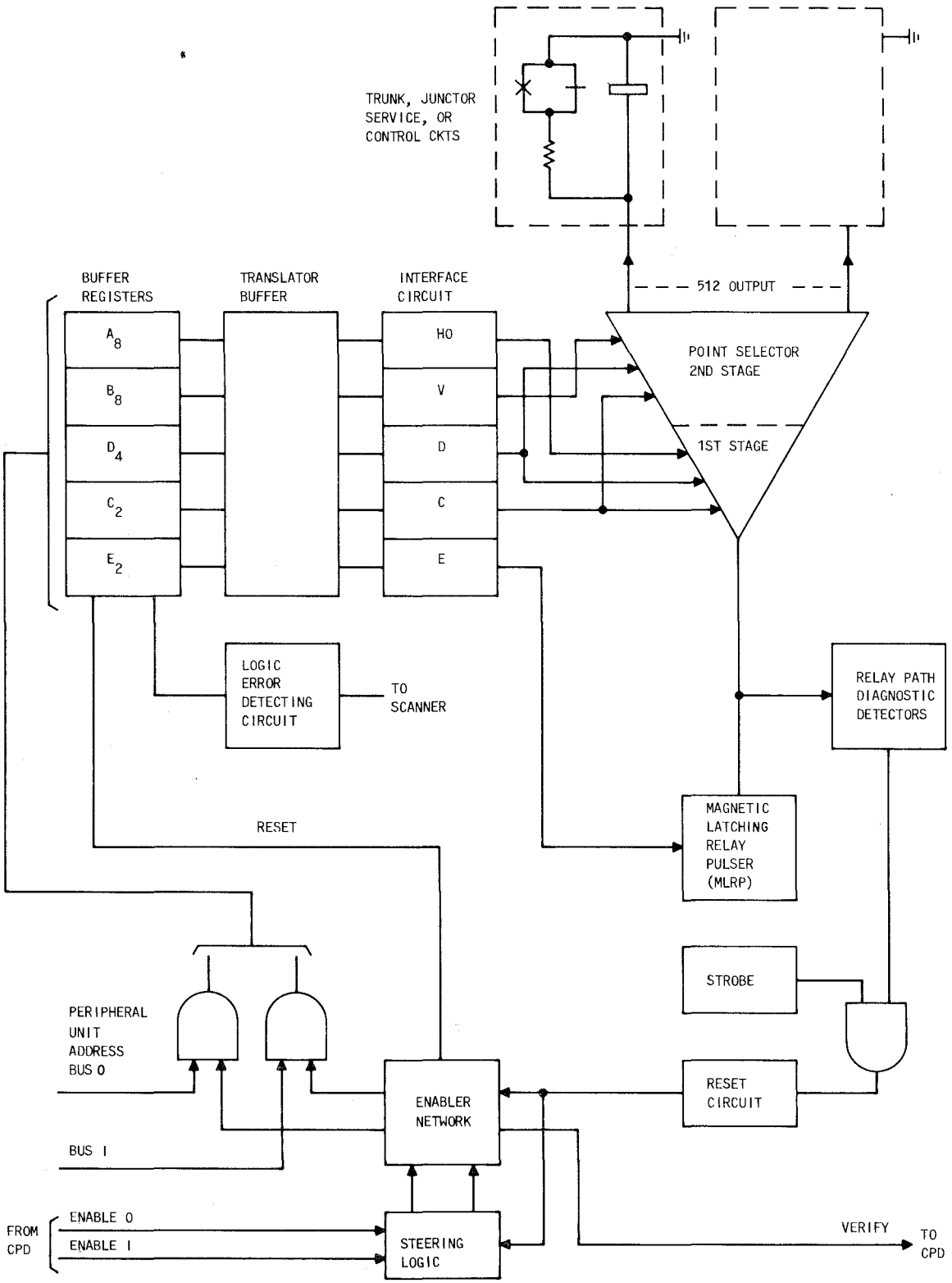


Fig. 12—Basic Signal Distributor Block Controller Diagram

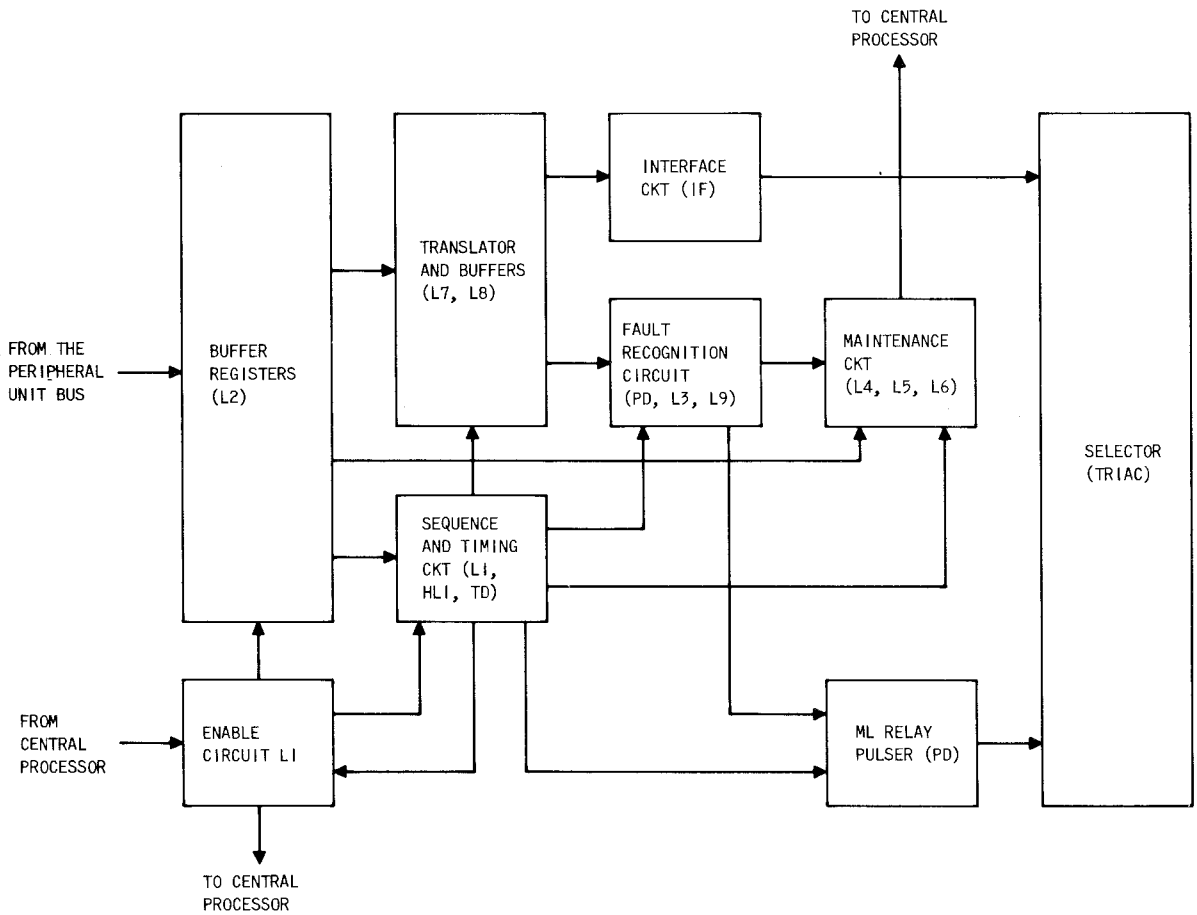


Fig. 13—TRIAC Signal Distributor Block Diagram

4.13 The magnetic latching relay pulser generates signals of the proper amplitude and duration for operating and releasing a magnetic latching relay. The relay path diagnostic detector has two functions in addition to the one described. One is to sense when the magnetic latching relay has worked as intended. This part of the circuit is called the "armature movement" detector. The detection of armature movement is used to indicate a successful cycle and to initiate the reset of the buffer registers. On the other hand, failure of armature movement indicates a faulty operation and is reported to the central control on the next cycle. The second function is used to sense when a release signal is being sent to an already released relay. This circuit is called a "double release" detector. Double release detection is important since second release under some circumstances can place a magnetic latching relay in an operated state. Then the CC would consider the relay released when it is actually operated, and an intolerable situation would exist; hence, double releases must be detected and interrupted before operation of the relay can occur. The detection of double releases is used to terminate the signal distributor cycle. Since detection occurs early in the cycle, an operated relay will be avoided.

4.14 The strobe circuit shown in Fig. 12 is used to mask out rapid voltage changes (chatter) that occur on the selector path while the path is being established. This voltage chatter may cause false operation of the armature movement detector. The strobe gates the detector output only after sufficient time has elapsed to ensure that the chatter has disappeared.

4.15 The reset circuit is actuated if armature movement has been detected and the selection signal has been applied for a specified length of time. The reset circuit drives the enable and buffer register into a reset state.

E. Scanner

Register and Access Circuit

4.16 The function of the circuitry in the register and access portion of the scanner controller is to provide a 650-mA bipolar-interrogate pulse to the correct ferrod row. There are 64 rows that the scanner controller interrogates and each row contains 16 ferrods. Each scanner controller contains one transformer for every ferrod row. The negative part of the interrogate pulse resets the ferrods and the positive part is used for readout. A normal scanner order consists of two 1-out-of-8 codes. These two bits specify which one of the 64 ferrod rows is interrogated. The register and access portion of each scanner controller is made up of one register and translator (0SCRT or 1SCRT) pack, one timing board (0ST or 1ST) pack, one interrogate current drivers (0ICD or 1ICD) pack, and four interrogate matrix (0IM0, 0IM1, 0IM2, and 0IM3 or 1IM0, 1IM1, 1IM2, and 1IM3) packs.

4.17 The register and translator pack provides the logic for the controller. The circuit pack registers the address information, translates the address information, provides the ASW logic, and contains the logic for the enable and enable-verify circuitry. All of the timing for the scanner controller is generated on the scanner timing board. The interrogate current drivers pack provides eight current sinks, two current sinks comprise a current-sink group. A 1-out-of-4 select from the register and translator pack into the interrogate current driver pack which determines which current-sink group is activated. The interrogate current driver circuit packs also contain discrete components that generate the ASW response. The interrogate matrix packs each contain 16 transformers, each of which provides an interrogate pulse, organized into a 4-by-4 matrix. The circuit pack also contains devices which are used for selection purposes.

4.18 In normal operation, the two 1-out-of-8 codes are translated by the register and translator pack into a 1-out-of-4 and a 1-out-of-16 code. There is one transformer in each scanner controller corresponding to one ferrod row (16 ferrods per row). The 64 transformers, each of which provides a bipolar-interrogate pulse, are organized in a 16-by-4 matrix. Since each interrogate matrix contains a 4-by-4 transformer matrix, four circuit packs are required to implement the 16-by-4 matrix. The 1-out-of-16 code and the 1-out-of-4 code uniquely determine which one of the 64 transformers is selected. The 1-out-of-16 code activates a 27A PNPN on the interrogate matrix circuit pack which switches +24 volts on 1 of the 16 transformer rows. The 1-out-of-4 code activates a current-sink group located on the interrogate circuit driver pack. The timing from timing interrogate circuit pack (on lead designated NPD) first activates one current sink in the group to generate the negative or reset pulse to one ferrod row. The negative pulse is 650 mA in amplitude

and 0.8 μs in duration. The second current sink in the group is activated after the first current sink becomes inactive; this generates the positive pulse used for readout. The terminal designated PPD on the timing interrogate circuit pack provides the timing for the positive pulse. The positive or interrogate pulse that follows the negative pulse is 650 mA in amplitude and 1.0 μs in duration.

4.19 The ASW pulse is used to indicate that the scanner controller has interrogated only one ferrod row. If more than one row is pulsed because of either an invalid address or faulty circuitry, the ASW signal is inhibited. The circuitry on the interrogate matrix and interrogate current driver circuit packs checks that +24 volts is applied to only one row of the 16-by-4 transformer matrix. The current sinks on interrogate current driver circuit packs are checked to ascertain that only one current sink is activated during the negative pulse and that only one current sink is activated during the positive pulse. The register and translator circuit pack contains the logic that combines the results from the individual ASW tests and interfaces with the scanner-answer bus register circuit packs.

Ferrod Matrix Wiring

4.20 The ferrods are arranged into two 32-by-16 matrices (32 rows and 16 readouts). The ferrods are mounted on ferrod circuit pack PL2 which contains 32 ferrods arranged in a 2-by-16 ferrod matrix. The PL2 circuit packs are wired together to form the two 32-by-16 matrices. Every row has a unique pair of wires used for interrogation; the interrogate pairs are DR00P and DR00N through DR63P and DR63N.

4.21 The readout wiring is the column in the 32-by-16 ferrod matrix. Each readout loop (column) which terminates on the scanner detection circuit pack is composed of 32 ferrods which are connected in series. Every column on every PL2 circuit pack is bypassed with a 15-ohm resistor which is mounted on the rear of the frame on each 940E connector in equipment locations 04-31 and 04-67. These resistors (16 per PL2 circuit pack) insure continuity of the readout loop when a ferrod circuit pack is removed or if a ferrod-readout winding should open up. At no time should more than one PL2 be removed from each loop, or bay, at one time. There are 16 PL2s per bay, two rows per PL2 or 32 rows (one loop) in each bay.

Scanner Detector Circuit

4.22 The scanner detector circuit packs contain 16 circuits that detect the readout current of the 16 ferrod columns. An unsaturated ferrod, upon interrogation, causes current to flow in the readout loop. The readout current is an input to the scanner detector and is transformer-coupled into the base of a 66S transistor, causing the transistor collector to go low. If the ferrod is saturated, insufficient current flows to cause the transistor collector on the scanner detector to go low. The collector load resistor is on the scanner-answer bus register circuit pack.

4.23 One scanner detector circuit pack in each scanner is associated with each 32-by-16 matrix. The outputs of the two scanner detector circuit packs in each scanner are combined to provide the output to the answer-bus register for the full 64-by-16 matrix.

4.24 The scanner detection board also contains a transformer that is activated during the maintenance test (bit 16). The test verifies that the readout loop has continuity and that the detector works correctly. The peripheral bus choice determines which 32-by-16 matrix readout windings are checked for continuity. When the MT order is received from peripheral bus 0, the readout windings associated with bay 0 (rows 00 through 31) are checked. The readout windings associated with bay 1 (rows 32 through 63) are checked when the maintenance order is received from peripheral bus 1.

Power

4.25 The +3 volts for each of the two scanner circuits is generated by a pair of +24 to +3 volt dc-to-dc converters, which are each powered from separate fused +24 volt power feeders (+24SA and +24SE). The +24SA and +24SB feeders also supply, respectively, the circuit 0 and circuit 1 interrogate drivers and interrogate matrix circuit packs. Power is controlled by MPC1 and is removed on an individual circuit basis. The -15.0 volts for the PL2 ferrods is provided by PK1.

5. MAINTENANCE AND DUPLICATION

5.01 Maintenance registers are provided for placing either of the two SD controllers in modes of operation other than normal. These modes are

used under trouble conditions and/or to perform maintenance tests.

5.02 Maintenance addresses are indicated when the T1 bit of the T2 register is set, as shown in Fig. 14. When the T1 bit is set, the D4 register is used to indicate what maintenance function is to be performed. The D0 bit indicates a quarantine or an out-of-service mode is to be established, the D1 bit indicates a test access mode is to be established, and the D2 bit indicates the maintenance registers are to be reset.

5.03 Note that maintenance functions to be performed on the left half controller are addressed to the right half buffer register, and vice versa. The maintenance mode, once established, is maintained by the maintenance registers (Fig. 14) until the registers are released by direction of the central control which simultaneously sends a T1 and D2 bit.

5.04 When a controller is placed in the test access mode, its ability to operate and release magnetic latching relays is not affected. In the test access mode, the master scanner is connected to check circuits within the signal distributor. The check circuits of each controller are connected to the master scanner via multiples that are common to all signal distributor controllers and are referred to as the signal distributor diagnostic bus.

5.05 While a controller is in the test access mode, the addresses from the central control that are used for testing purposes may be incomplete; in which case, no path is closed through the selector. Each of these addresses is directed to the basic signal distributor in which the test access mode has been established. The central control then inspects the test points via the master scanner. After each test, the central control resets all circuits in the controller by signaling over an appropriate path provided in the peripheral unit address bus.

5.06 When a controller is placed in quarantine, it is removed from service. The other controller is given full access to both selectors. (This is called the combined mode of operation.) The in-service controller has the capability of making a 1-out-of-1024 point selection and controlling any of the magnetic latching relays connected to the two selectors. Assume that the 0 controller is quarantined; the 1 controller can complete a path to any one of the 1024 output terminals (Fig. 15). The H section of the buffer register controls the half of the selector in which a pulse path is established. In all modes of operation, the address from the central control contains selections of the H section of the buffer register. However, only one controller can control all of the outputs if the other controller is in quarantine. Control connections between opposite halves are established only when one of the quarantine relays, Q0 or Q1, is operated (Fig. 14 and 15).

5.07 Provisions have been made so that a controller can be manually quarantined. Manual quarantine is established automatically when power is removed from one of the controllers. A mechanical lock-out feature is provided to eliminate the possibility of manually removing power from both controllers at the same time.

5.08 To return a signal distributor from a combined mode of operation to split mode, the central control addresses the buffer register such that the D2 and T1 bits are set. This results in the maintenance registers being cleared.

5.09 The controlling circuitry of the signal distributor is duplicated, but not in the sense that one controller operates the whole signal distributor while the other stands by ready to take over. Normally, one controller offers access to one half of the output terminals, while the other controller offers access to the other half.

5.10 In each controller, the buffer registers are equipped to accept an address from either of the duplicated peripheral unit buses. Each controller has two enable inputs through which the central control determines the bus from which address information is to be registered and to which signal distributor (of the many possible signal distributors in an office) the address is to be sent.

6. POWER AND MISCELLANEOUS CIRCUITS

6.01 These circuits provide filters, fuses, and a means to remove power from the HUT frame. Abnormal conditions within the frame are reported to the system via scan points, and visual and audible alarms are also initiated. These circuits also provide test pin voltage jacks and a means of communicating between frames.

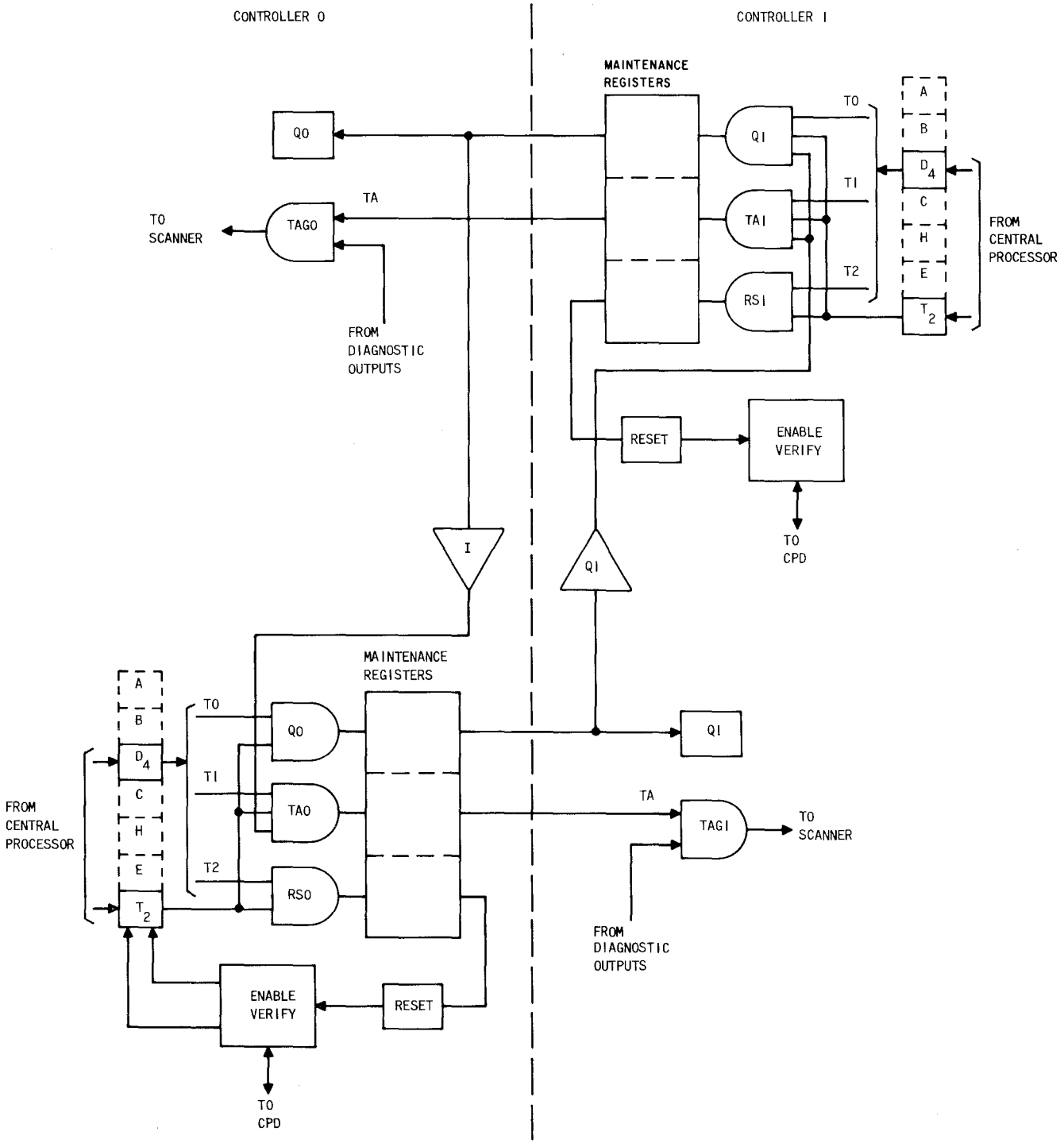


Fig. 14—Signal Distributor Maintenance Logic

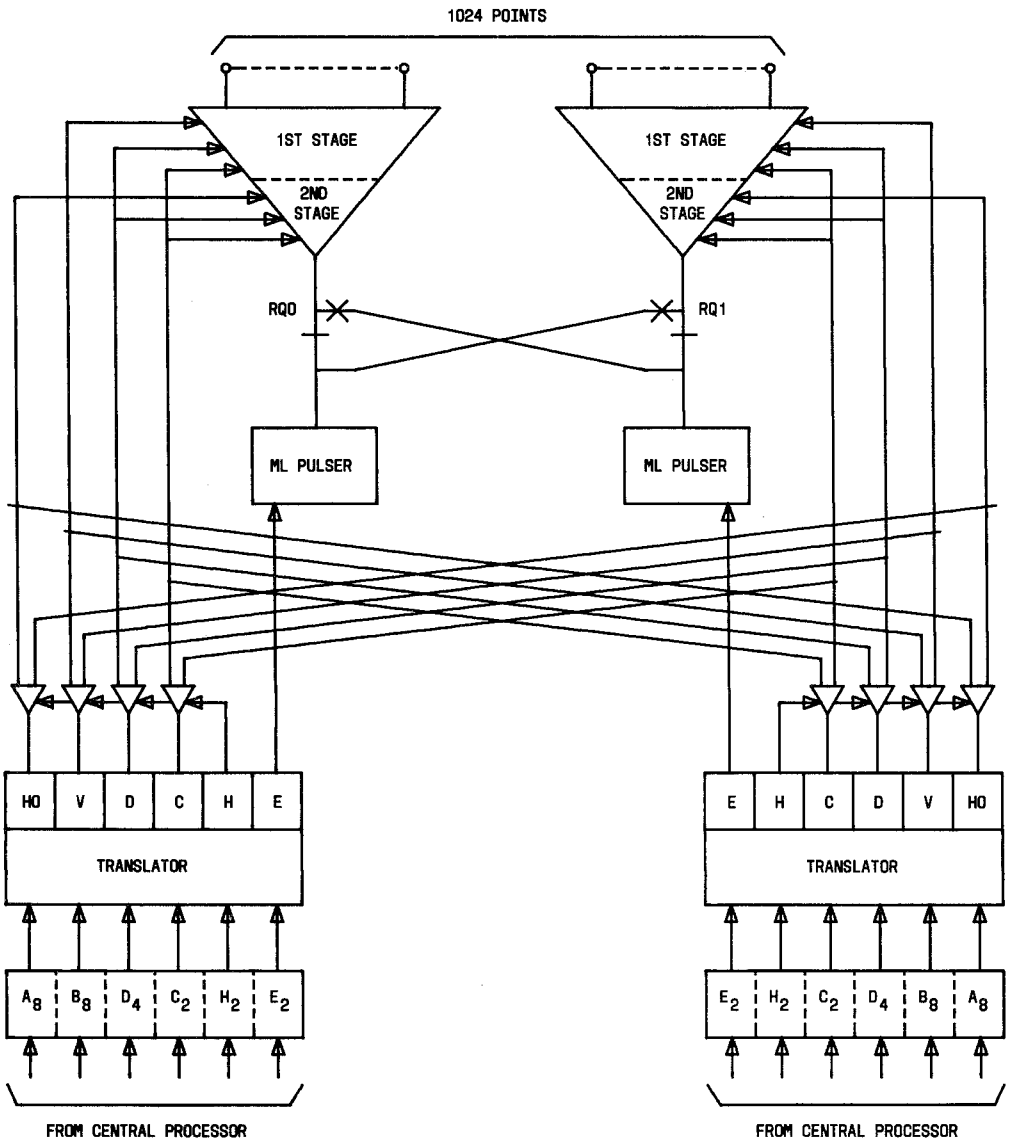


Fig. 15—1024 Point Signal Distributor With Selection and Pulse Path Required for Combined Mode Operation

FRAME LINE TELEPHONE JACKS

6.02 This circuit provides means of communicating between the HUT frame and other frames in the ESS office. The telephone jacks are located on the far left side of the supplementary signal distributor unit (Fig. 3). The local frame line is located in the line and trunk test bay of the master control center. The telephone head set, when plugged into the telephone jacks, completes the

talking path. The local frame line has no means of signaling.

SPARE JACKS

6.03 This circuit provides a 3-wire belt line around, the office for miscellaneous use. The jack is located next to the telephone jack.

TEST PIN JACKS

6.04 These circuits provide ground, high resistance ground, and -48 and +24 volt batteries for testing in the frame. These jacks can be accessed from both front and back of the frame.

FILTERS, FUSES AND FUSE ALARM CIRCUITS

6.05 These circuits provide +24, and -48 volt filters and fuses for circuits on the HUT frame. Two nonalarm fuses (+24TBS and -48TBS) provide voltage for the test pin jacks on the frame. Nonalarm fuse +24LP provides voltage through the +24LP leads, to the fuse alarm scan point SC00, to the PWR OFF 0 and PWR OFF 1 lamps, and to other lamps on the frame.

6.06 The failure of any alarmed fuse on the frame will operate the FA relay and;

(1) Light the appropriate PWR OFF lamps

(2) Signal the major alarm to the office alarm circuit through leads ABG and MJ

(3) Indicate a failure via scan point SC00.

7. TAKING EQUIPMENT OUT OF SERVICE

7.01 Only one of the two conrollers of an SD or scanner can be taken out of service at any time. This is accomplished by the system when it has been requested to do so via the teletypewriter. Once a controller has been removed from service, power to it can be removed by operating the appropriate power removal key. ***The system should always be requested to remove both the SD and scanner controllers before the power removal key is operated.*** The appropriate out of service lamp will light when the system quarantines (removes from service) the controller. The power removal keys override any frame condition previously established. The system is able to determine the state of the frame by the state of the S, F, and T scan points assigned to it.

7.02 Whenever a request has been made to take a controller out of service, it remains out of service until a request has been made to the system via the teletypewriter to restore it to service.