2400 DATA LINK - COMMON CHANNEL INTEROFFICE SIGNALING DESCRIPTION AND MAINTENANCE CONSIDERATION (1E7/1AE7 AND LATER GENERICS) 2-WIRE NO. 1 AND NO. 1A ELECTRONIC SWITCHING SYSTEMS

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1. GENERAL

INTRODUCTION

1.01 This section describes the common channel interoffice signaling (CCIS) feature of the 2-wire No. 1 and No. 1A Electronic Switching Systems (ESS).

1.02 Revision arrows are used to emphasize significant changes. The Equipment Test List is not affected. The reason for reissuing this section is to incorporate information in Section 231-138-305, Toll-CCIS Data Link Configuration and Recovery, 2-Wire No. 1 ESS. This reissue will now provide a complete single section on the description and maintenance consideration of the 2400 data link equipment with a No. 1/1A ESS.

1.03 Abbreviations used in this section are listed in Part 13.

PURPOSE OF CCIS SYSTEM

1.04 The CCIS system (Fig. 1) is a signaling system in which all telephone signals associated with a designated trunk group are passed over a common data channel instead of the individual voice paths of the No. 1 or No. 1A ESS intertoll switching network. The CCIS network is designated for the exchange of telephone signaling information between processor-equipped switching systems only. Interoffice signaling data is exchanged over a signaling link, consisting of a terminal unit and its associated modulator-demodulator (modem) located at each office, and the connecting voice-freqency link (VFL). The VFL is the wire facility or voice-frequency channel over which the signaling data is transmitted and received.

1.05 The CCIS signaling link from each office is independently connected to a signal transfer point (STP). The STP processes signaling data directly between connecting CCIS offices, within the same signaling region (Fig. 2) (eg, A-C or D-E), and forwards signaling data to a distant STP for interregional trunk groups (eg, A-D, B-E). In the latter case, incoming CCIS connecting office signaling traffic at the STP is concentrated for transmission to the next STP to achieve efficient use of signaling link capacity.

1.06 The STP function is fully duplicated and redundant in each region as shown in Fig. 2. There are two STPs located in each of the ten continental toll regions. Each CCIS office is connected to both STPs of the pair, and the STPs of all regions are interconnected by four signaling links forming quads. The STPs in each region are also connected by signaling links. This permits an STP to transfer signaling data to the mate STP if its signaling links have failed. Under normal conditions, each STP is designed to process one-half of the regional signaling traffic, which can constitute no more than one-half of its processing capacity. In the event of signaling link or STP equipment failure, all regional CCIS signaling traffic is processed by the other STP.

SIGNALING LINK DATA

1.07 The data contained within the CCIS network exists in the form of binary serial data words

called signal units (SU). These 28-bit SUs are used singly [designated lone signal units (LSU)] or in groups [designated multiple unit messages (MUM)] to transfer supervisory and control signals between switching offices handling a call. Since signaling can take place before, during, or after a call, and can take place simultaneously in both directions, much more information regarding call status can be efficiently transferred between offices.

TERMINAL OPERATION OVERVIEW

1.08 Incoming calls to a CCIS switching office may be assigned to CCIS facilities by the processor. If so, then the necessary SUs required to control the progress of these calls are reformatted by the terminal access controller (CONT) and passed to the terminal equipment. These outgoing SUs, along with outgoing link and relative priority level information, are conveyed in parallel bit form over the peripheral unit address bus (PUAB) to the terminal access controller. The terminal access controller is also known as a TAC, but in this section, CONT is used as this term reflects the schematic diagrams and circuit description terminology (Fig. 3). The SUs are then relayed in the same form from the CONT to the indicated data terminal and stored in a transmit buffer according to priority level. Each SU remains in this buffer until it has been transmitted. It is then stored in the data terminal transmit record table until the data terminal receives an acknowledgment control unit from the distant office CCIS data terminal indicating error-free reception. If any SUs are received in error by the distant office, they are retransmitted. Thus, error control consists of error detection by the decoding of check bits included in each SU and by monitoring the modem carrier failure detector. Error correction is then accomplished by retransmission of SUs.

1.09 When ready to be transmitted, each SU, in priority order, is placed in a logic register where eight check bits are added. The 28-bit SU is then passed serially to the modem for encoding and transmission over the voice-frequency link (VFL) to the distant office. The VFL is a 4-wire voice bandwidth circuit similar to a 3002-basic private line channel for data transmission. The VFL is operated full duplex; that is, both directions of transmission are used for signaling simultaneously.

1.10 Incoming 28-bit SUs are received by a modem where the encoded data is converted back into digital format and relayed serially to the receive section of the associated data terminal. There error-checking is performed on the SUs, utilizing the eight check bits. Independent of the check code, the carrier detector circuit in the modem is also used to detect erroneous SUs. An SU is considered to be in error if the carrier detector circuit indicates a loss of received carrier. Each block of 12 SUs is processed by the data terminal, and an acknowledgment control unit is generated and returned to the distant office. Error-free SUs (minus the eight check bits) are stored by relative priority level in the data terminal receive buffer. Through wired logic, the data terminal receive buffer indicates a nonpriority or a priority-signal-present condition to the processor via the CONT. When the processor is ready to receive the SUs from the data terminal, each SU is relayed in parallel-bit form through the CONT to the processor over the scanner answer bus (SCAB).

1.11 The signaling information interface with the CONT is through the PUAB and the SCAB. Power status indications of the terminal equipment are also via the scanner. The CONT operates only under direction of processor instructions; however, the terminal unit autonomously conducts self-checking routines interleaved with the data handling routines of the signaling link. Figure 3 shows the configuration of the CONTs and central control processors in the No. 1/1A ESS toll CCIS system.

EQUIPMENT CHARACTERISTICS

1.12 The data terminal, including its associated modem, is a CCIS common systems design. As a stored program-controlled processor operating autonomously, its basic functions include all operations related to the 2-way synchronous signaling link. The data and control interface between the No. 1/1A ESS central control processor and CCIS terminal units is provided by the No. 1/1A ESS CCIS CONT unit.

1.13 The modem contained in each data terminal is a plug-in 2400 bit-per-second transmission rate 201D-L1A data set designed with 5V transistor-transistor logic integrated circuits of the dual in-line package variety. All other functional units in the CCIS terminal group are designed with 1A-type 3V transistor-transistor logic circuits. Some of these are mounted on a ceramic substrate which is mounted on a plug-in card. The data terminal program memory and data memory consist of bipolar memory modules mounted on the same type plug-in cards.

1.14 Figures 4 and 26 show unit location and sizes.

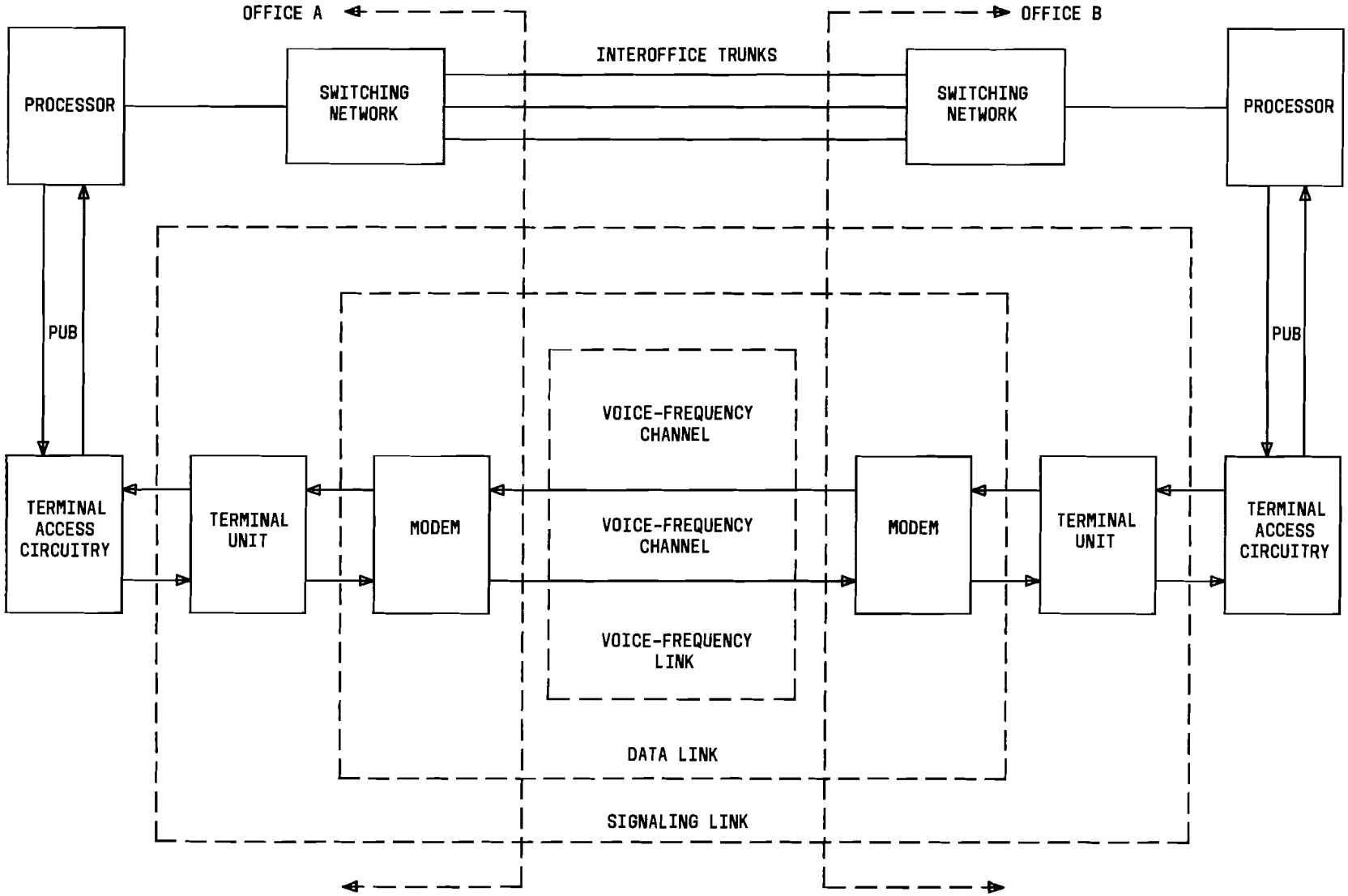


Fig. 1—Common Channel Interoffice Signal System—Block Diagram

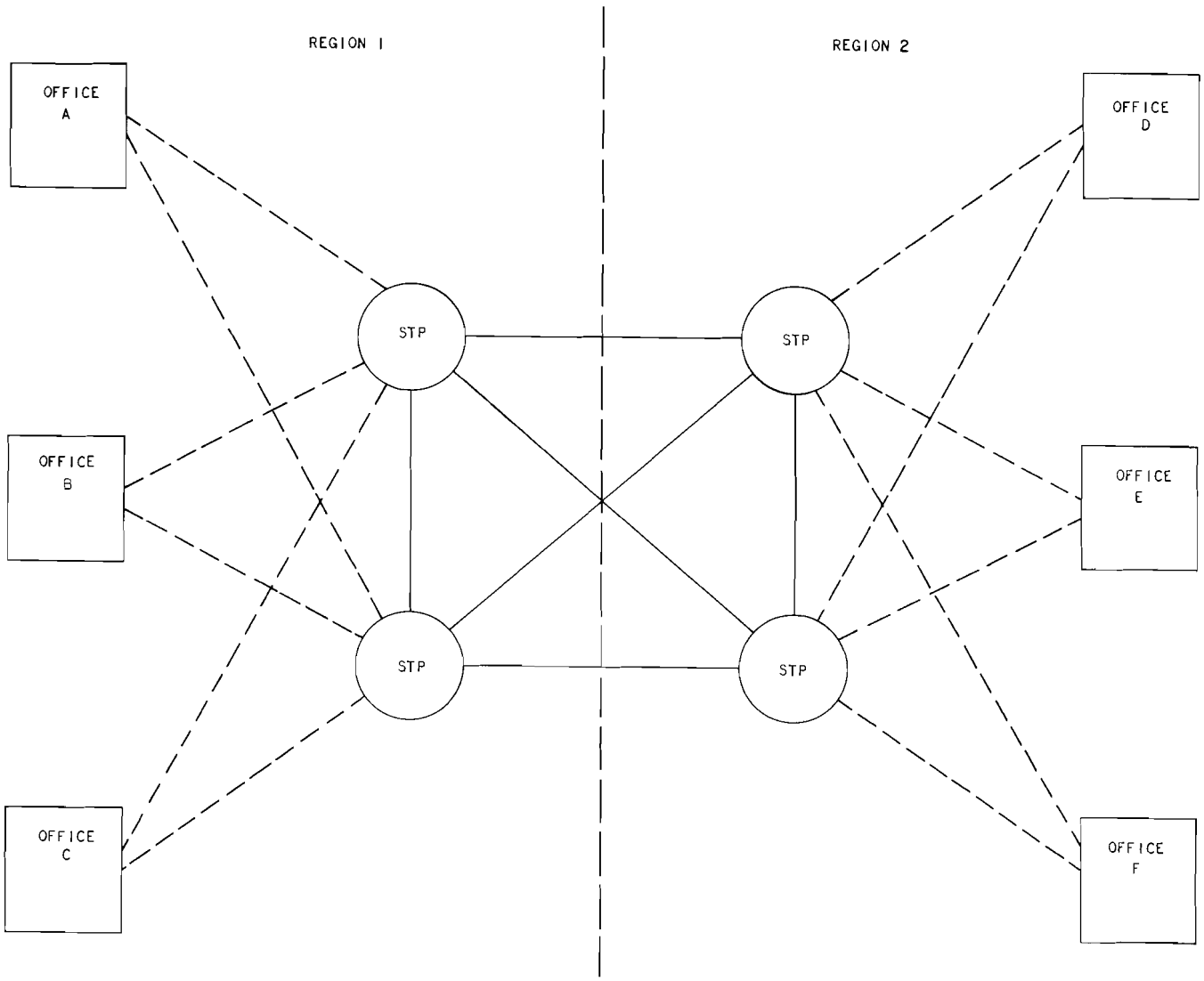


Fig. 2—CCIS Quad Network Structure—Block Diagram

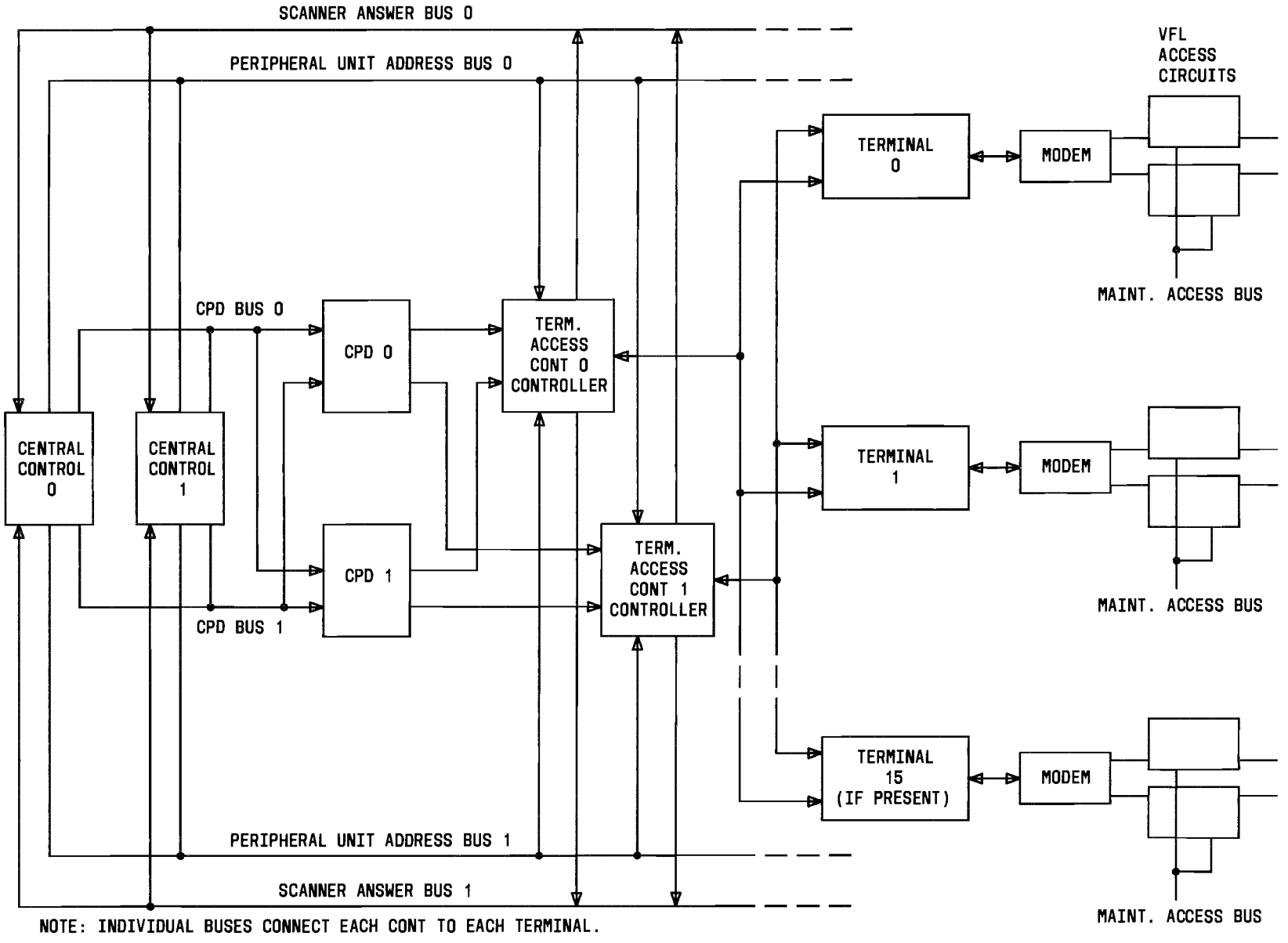
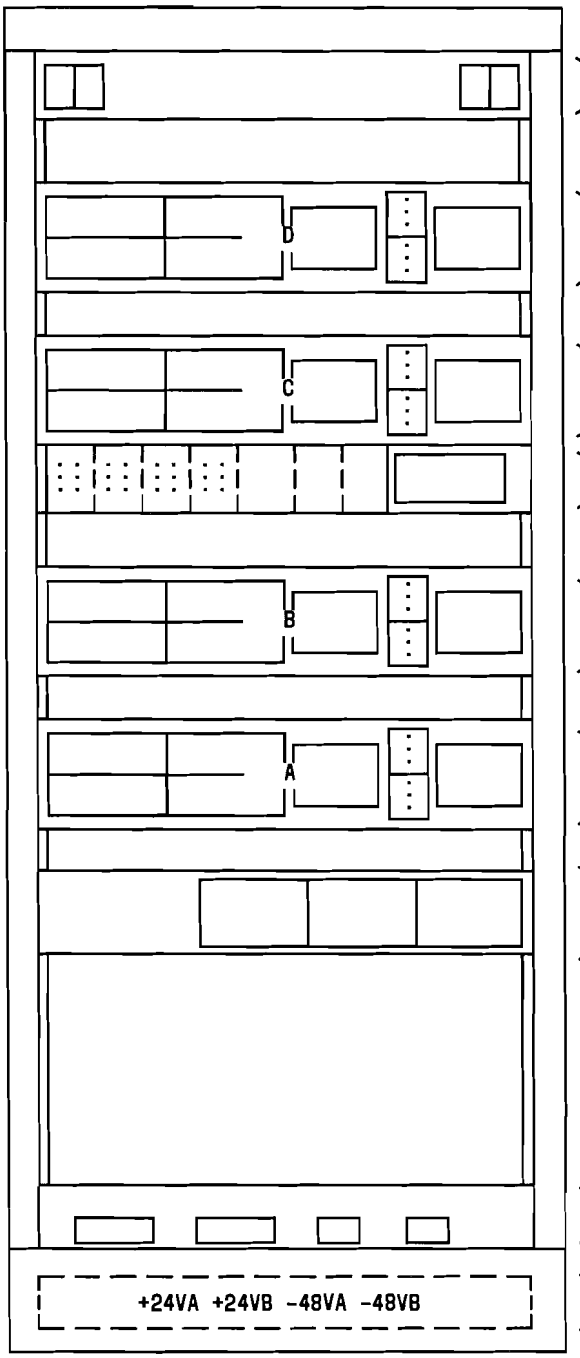


Fig. 3—No. 1/1A ESS Toll CCIS Configuration



	1ST SUPL FR	2ND SUPL FR
D	11	15
C	10	14
B	09	13
A	08	12

Fig. 4—Data Terminal Supplementary Frame J1A094B

REFERENCES

1.15 Refer to Table A for supporting documentation.

2. VOICE FREQUENCY LINK ACCESS (VFLA) UNIT

2.01 The VFLA unit allows test of a VFL from a centrally located test position such as the trunk and line test panel, supplementary trunk test panel , or the manual trunk test position in HILO 4-wire applications. The results of the tests are the same as if the test equipment used were located at the data terminal associated with the VFL under test. For this to be accomplished, the transmission levels between the test position and the VFLA, including cable loss, must match the levels present between the data terminal and the VFLA. The VFLA maintenance circuit provides adjustable gain and loss to insure that the levels at the test position and VFLA are correct and to compensate for varying amounts of cable loss.

VOICE FREQUENCY LINK ACCESS CIRCUIT

2.02 The VFLA circuit provides the required attenuation between the DS 201D modem and the

TABLE A

SUPPORTING DOCUMENTATION

CIRCUIT	SD/CD NUMBER	OTHER REFERENCES
Data Terminal Basic Frame Circuit	1A441-01	Section 820-069-151
Data Terminal Supplementary Frame Circuit	1A442-01	Section 820-069-151
Terminal Access Controller Circuit	1A443-01	—
Data Set 201D	—	Section 312-811-100
Data Terminal Circuit	1A444-01	—
Data Terminal Power Control Circuit	1A445-01	Section 231-115-501
Voice Frequency Link Access Circuit	1A446-01	—
3-Volt, 8-Amp Power Converter	82246-01	Section 231-115-501
201D Data Set	73090-01	Section 312-811-100
Central Pulse Distributor	1A109-01	
Communications Bus Circuit for Peripheral Units	1A119-01	—
Master Scanner Applique Circuit	1A133-01	—
Signal Distributor Applique Circuit	1A146-01	—
Office Alarm Circuit	1A158-01	Section 231-115-501
Power Distributing Frame Circuit	1A126-03	
Miscellaneous Circuit for All Frames	1A129-01	

voice frequency link. This attenuation is accomplished on the JW422 circuit packs by a fixed 16-dB, 600-ohm balanced attenuator located in the transmit path of the circuit and by a 4-dB attenuator located in the receive path. The JW430 circuit pack contains a 309A repeater unit with a continuously variable range of -20 to +24 dB.

2.03 The VFLA circuit also provides the VFL with line build-out capability to a test position. A local loopback transmission path is also provided. When switched into the circuit during the data terminal diagnostic routine, this path allows testing of the DS 201D transmitter output stages and the receiver input stages including carrier detect circuits.

2.04 The VFLA circuit provides a matched transmission path between:

- The duplicated VFLs and the duplicated outputs of the DS 201D-L1A.
- The VFLs and the test position.

Signaling via the DS 201D duplicated outputs (designated A and B) is mutually exclusive. The VFL not selected for connection to a data set output is available for test purpose using the VFLA circuit only, if that VFL is in the unavailable software state.

3. MODEM—VFL INTERFACE

GENERAL

3.01 The 201D data sets (DS 201D) shown in Fig. 27 are physically located within the terminal units. Each modem performs the following functions:

(a) Receives serial binary data from the terminal.

(b) Groups received binary data into bit pairs called dibits.

(c) Decodes the dibit to determine the carrier phase-shift that represents the dibit.

(d) Generates and presents to the voice-frequency channel the serial train of phase-shifted carrier pulses at a rate of 1200 baud (2400 bits per second).

(e) Receives from the voice-frequency channel the phase-shifted carrier pulses.

(f) Determines the phase shift between the previous signaling element and the present signaling element to determine the dibit represented.

(g) Generates the dibit.

(h) Presents the received data to the signaling terminal in binary form one at a time.

(i) Detects loss of carrier.

(j) Maintains synchronization for a period of 1 second during loss of carrier.

3.02 Refer to CD-1A444-01 for a complete description of the operation of the modem—VFL interface.

MODEM CHARACTERISTICS AND CONFIGURATION

3.03 The 201D modem consists of seven circuit packs (six AR-type packs, plus a 102A power unit) in a self-contained housing. The modem mounts as a single unit via four screws.

3.04 Functionally, the six AR-type packs comprise a transmitter, receiver, and a terminal and telephone line interface section. The interface unit (AR668) is the only unit that is discussed in detail by this section. The modem operates under control of the terminal.

3.05 The DS 201D uses a 4-level differential phase-shift-keying modulation scheme to transmit and receive serial binary data synchronously at the rate of 2400 bps on a facility similar to 3002-type 4-wire private line channel with basic conditioning. Synchronization is achieved by a 2400-Hz clock provided by either the data set (transmit and receive clocks) or the terminal equipment (transmit clock external only).

3.06 The data set transmitter accepts serial binary data at 2400 bps in synchronization with a 2400-Hz clock. The transmitter encodes the digital data into symbols of two bits each (dibits). These are used to modulate the phase of the 1800-Hz carrier frequency at a 1200-baud rate. The resultant differential 4-phase modulated signal is converted to an analog signal for transmission over the voice-frequency telephone line.

3.07 The receiver accepts the far-end transmitted analog signal from the telephone lines, demodulates the signal to recover the serial data and bit timing, and delivers the data and timing to the terminal through the interface connector.

MODEM—VFL CONFIGURATION

3.08 There are many possible combinations for configuring the modem-to-modem interface. These are dependent on the type of facilities linked by the CCIS system. The basic CCIS configuration between offices is shown in Fig. 28.

3.09 In the VFLA maintenance access state, ground is provided on leads 1IE and ALT (refer to Fig. 29). The 1IE and ALT relays are operated in the JW422 VFLA circuit pack associated with the line B output of the data set. In this state, the 4-wire circuit of the associated VFL and the attenuators, switches, and jacks in the VFLA circuit are connected to the 4-wire circuit of the maintenance bus. The maintenance bus is a 4-wire multiple common to all VFLAs of a basic frame bay or supplementary frame bay. Each bus requires one trunk link network appearance. It provides a transmission path to the test position via the JW430 VFLA maintenance circuit pack.

3.10 Several data terminals may be controlling VFLA circuits which have access to the test position via a common maintenance bus. Since proper termination dictates that only one VFL at a time be switched to the maintenance bus, the ALT bit of only the terminal selected should be set to logic 1 in the terminal control register.

3.11 The VFLA circuit allows test of a VFL from a test position. The results of the tests are the same as if the test equipment used were located at the data terminal unit associated with the VFL under test. To effect this situation, the transmission levels between the test position and the VFLA (including cable loss) must match those levels present between the data terminal unit and the VFLA. To ensure that the levels at the test position and VFLA are correct, and to compensate for varying amounts of cable loss, the JW430 VFLA maintenance circuit provides adjustable gain and loss.

3.12 In the transmit path of the maintenance bus (ie, direction of transmission towards the transmission facility), the VFLA maintenance circuit provides nominally 13 dB of gain. This amplifies the 0 transmission level point test signal present at the test position to the +13 transmission level point required at the 310-type jack labeled TRMT on the VFLA circuit pack. In this path of the circuit, the JW430 VFLA maintenance circuit provides gain and loss in the continously variable range of -20 to +24 dB.

3.13 In the receive path of the maintenance bus circuit (ie, direction of transmission away from the transmission facility), the JW430 circuit pack contains a 49A-type variable attenuator that provides 0 to 1.5 dB of attenuation adjustable in 0.1 dB increments. The transmission level point present at the 310-type jack of the VFLA circuit pack labeled RCV is the -3 db transmission level point. The variable attenuation provided by the JW430 and cable loss between the VFLA and test position allows adjustment of the expected receive signal at the test position to the -4 db transmission level point.

3.14 With the VFLA circuit configured to provide VFL-to-maintenance bus continuity, the output of the data set is removed from the circuits. In this state a loopback path from the data set transmitter circuit to the receive circuit is provided through a 25-dB, 600-ohm balanced attenuator (AT1). This external loopback path is used during data terminal unit diagnostic routines to test the transmitter output amplifier, output transformer, receiver input transformer, and the carrier detector circuits.

MODEM TESTS

3.15 The DS 201D provides several test features such as digital loop-back, analog loopback, line transfer, and facility test. Figure 27 shows how these test features apply to the circuitry. Also refer to Fig. 5 and Table B.

A. Digital Loopback

3.16 The control inputs establish digital loopback (Table B, state 3) by operating the receive data loop relay. This loops RD to SD and serial clock receive to serial clock transmit, external secondary clock time. Also, it opens the SD and SCTE leads at the terminal interface. An initialization pulse called GIP is allowed to pass to the transmitter to align the transmitter countdown circuitry to the same condition as the receiver countdown circuitry, thus maintaining synchronization.

3.17 The data set is processing data all the time on the SD lead except when in digital loopback. While in digital loopback, the signals on IE, SD, and SCTE leads are ignored, and serial clock transmit is phase-locked to serial clock receive.

3.18 In state 3, the line signal is 0 or -15 dBm if carrier on is high (received signal present) and is

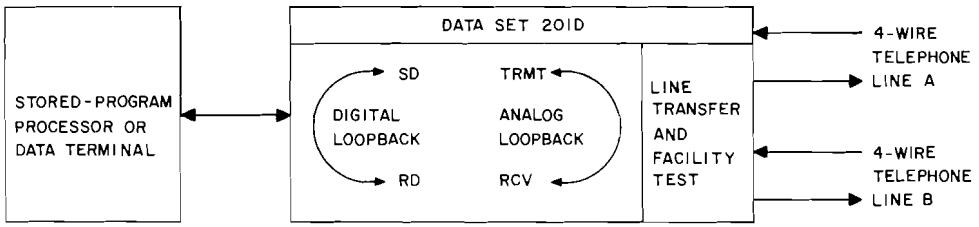


Fig. 5—Data Set DS 201D Showing Simplified Test Features

▶TABLE B◀

CONTROL INPUTS DETERMINING STATE OF DATA SET (DS)

CONTROL INPUTS (NOTE)			STATE OF DS
LC	DL	AL	
0	0	0	1 Normal on-line
1	0	0	2 Line signal power off (on-line)
0	1	0	3 DL (DS regenerator)
0	0	1	4 AL –15 dBm nominal receive level
0	1	1	5 AL –26 dBm low receive level
1	1	0	6 AL –5.5 dBm high receive level
1	1	1	7 AL –30 dBm receive level COR test
1	0	1	8 AL line signal power off, less than –40 dBm receive level

Note:
1 = High level, 0 = Low level
LC = Line Control
DL = Digital Loop-Back
AL = Analog Loop-Back

off if carrier on is low (no received signal present). This permits the near-end data set to control the transmitted line signal from the far-end data set if the latter is in digital loopback.

B. Analog Loopback

3.19 There are five analog loopback states (states 4 through 8 of Table B) with each state at a different simulated, received-signal power level. The receiver is not connected to either line A or line B when in any of the analog loopback states (RAL relay is operated). Once the RAL relay is operated, switching between the five analog loopback states is accomplished through the transistor-controlled attenuator. Transition from state 4 (-15 dBm) to state 8 (PWR-OFF) within 15 microseconds is effected and the CCIS diagnostic tests the response of carrier off reliable.

3.20 In states 4, 5, 6, and 7 (Table B), the transmitter applies the nominal 0 or -15 dBm signal (as optioned) to line A or B (as selected by line transfer) at all times. The near-end testing does disrupt transmission to the far-end data set.

C. Line Transfer

3.21 Refer to Fig. 27. Line A (AT1, AR1, AT, and AR) and line B (BT1, BR1, BT, and BR) represent two separate 4-wire private lines. The transmitter output and receiver input are normally connected to line B (line transfer is low). Switching to line A is accomplished by making line transfer high which

activates the line transfer relay K3. The data set presents a balanced 600-ohm termination to both lines except when in the facility test mode. A short circuit between any pairs or a ground fault on any lead will cause no damage to the data set.

D. Facility Test

3.22 Refer to Fig. 27. A low level on the facility test lead causes the telephone lines to be connected to the data set and terminated in 600 ohms. A high level on facility test causes the transmitter and receiver to be disconnected from the telephone lines and causes BT1-BR1 to be connected to AT-AR relay K2 and AT1-AR1 to be connected to BT-BR relay K1. A high level on facility test with line transfer low causes the transmitter and receiver to be connected to line B and the line A receive pair to be connected through a 16-dB amplifier to the line A transmit pair. A high level on facility test with line transfer high causes the transmitter and receiver to be connected to line A and the line B receive pair to be connected through the 16-dB amplifier to the line B transmit pair. The amplifier is set for 0 dB gain in CCIS. This provides a loopback (transmit-receive) on the VFL not currently connected through to the data terminal (DTRM).

3.23 A summary of modem internal analog and digital loopback tests and other modem tests that are directed by the processor include tests as follows:

(1) Tests at power levels near the upper, lower, and nominal operating range of the receiver. These tests verify adequate transmitting power levels and receiver sensitivity.

(2) Tests are at the levels designed to check the operate and nonoperate states of the carrier failure detector circuit.

(3) Tests the frequency of the transmit and receive clocks and the ability of the modem to maintain synchronization properly.

(4) Tests the capability of the various modem control signals to properly control the modem.

(5) Tests response of carrier off reliable by means of an external analog loop through the VFLA.

MODEM MAINTENANCE

3.24 The entire DS 201D modem is replaced as a single unit if a fault is detected. It mounts simply with four self-contained screws from the front of the terminal unit. This concept simplifies the resolution requirements of the modem diagnostics. Modem diagnostics are coded as separate phases of the terminal diagnostics program.

4. TERMINAL ACCESS CONTROLLER UNIT

CONT PHYSICAL DESCRIPTION

4.01 The CONT unit J1A094AB is located within the basic terminal frame as shown in Fig. 4. Circuit packs are arranged in the CONT as shown in Fig. 6.

4.02 A description of the circuit packs (CPs) is given in CD 1A443-01. Their locations and numbers were previously listed.

CONT FUNCTIONAL DESCRIPTION

4.03 The CONT controls all communication between the central controls and up to 16 associated terminals. The CONT must perform the following functions on information going from the processor to the terminal unit and then to the signaling link:

(a) Receive instructions and data from the processor.

(b) Check, decode, and analyze the information.

(c) Select the sequence to be used.

(d) Communicate the information to the proper terminal.

The following functions must be performed by the CONT on information going from the terminal unit to the CONT:

(e) Check the terminal information.

(f) Transmit the requested terminal data to the processor.

Thus, the CONT appears as the peripheral unit to the processor.

4.04 All communication between the processor and terminals is performed through the CONT. Therefore, duplicated CONTs are provided. Although

	UNIT MTG PLATE POSITION	
	02	06
14	3-VOLT CONVERTERS J87389P	
15		
16		
17		
18		
19		
20		
21	FC21	FC21
22	FB152	GRPING FIELD
23	VACANT	VACANT
24	CABLE TERMINATION FIELDS	
25		
26		
27		
28		
29	FA802	FA800
30	FA802	FA800
31	FA800	FA800
32	FA803	FB304
33	FB306	FA807
34	VACANT	FA808
35	FB300	FA819
36	SPARE	FA834
37	FA835	FB304
38	FA842	FB304
39	FA841	FB304
40	FA836	FB304
41	FA836	FB304
42	FA836	FB304
43		
44	FA836	FA800
45	FA804	FA800
46	GRPING FIELD	FA800
47	FA803	FA800
48	CABLE TERMINATION FIELDS	
49		
50		
51		
52	VACANT	VACANT
53	VACANT	VACANT
54	VACANT	VACANT
55	VACANT	VACANT
56	VACANT	VACANT
57	VACANT	VACANT

Fig. 6—Terminal Access Controller Unit—Circuit Pack Layout

the CONTs are duplicated, they are operated in the simplex mode; ie, only one CONT is active at one time. No matching is performed, but two paths are provided between the peripheral unit bus system and the terminals.

4.05 Processor-CONT communications are accomplished via the central pulse distributor (CPD), the PUAB and the SCAB (Fig. 30). The processor alerts the CONT by CPD enable pulses that data is arriving over the PUAB. Enable verification signals are returned to the CPD from the CONT. The PUAB data contains the information used by the CONT to determine the job to be done. The CONT returns data to the processor over the SCAB. Each CONT contains circuits for receiving from both peripheral unit bus 0 and 1 and for driving both SCABs 0 and 1.

4.06 The CONT performs no autonomous operations. It performs a task only in response to instructions received from the No. 1 or 1A ESS processor. These instructions are coded in 7-bit operation codes that are transmitted to the CONT over the PUAB. See Table C. The opcode is transmitted to the CONT in a 20-bit instruction that contains a 9-bit address field and a 4-bit terminal number field. The opcode indicates the particular operation to be performed; the address field indicates a particular location in the terminal to be used for some terminal operations; and the terminal number dictates the terminal to be used.

4.07 The amount of information required by the CONT to perform a job varies with the different instructions. Since the PUAB handles only 24 bits, some operations require that multiple words be transmitted to the CONT. Because of this, the CPD enable must indicate to the CONT whether an instruction word contains opcode information or data. The first word is referred to as an instruction word and the second as a data word. The enable also identifies which PUAB is being used.

(a) A we-really-mean-it (WRMI) bit is also generated by the processor and passed to the CONT via the WRMI bus associated with the PUB being used. This bit is used to direct the quarantine operations of a CONT unit. A quarantined CONT is prevented from contacting any of the terminal units by inhibiting the terminal active-standby signal. The intent is to prevent a failed CONT from blocking communications with the operating

▶TABLE C◀

CONT SEQUENCE OPCODE ASSIGNMENTS

PUAB BITS			DEFINITION
21	20 19	18 17 16 15	
1	00	0000	Spare
1	00	0001	Read Data Register Bits 1-16
1	00	0010	Read Reply Register Bits 17-24
1	00	0011	Spare
1	00	0100	Read Instruction Storage Register Bits 1-16
1	00	0101	Spare
1	00	0110	Spare
1	00	0111	Read Reply Register Bits 1-16
1	00	1000	Read Error Source Register
1	00	1001	Read Control Register
1	00	1010	Read Instruction Storage Register Bits 1-16
1	00	1011	Read False All-Seems-Well Register
1	00	1100	Read High Priority Signal Present Indicators
1	00	1101	Read Trouble Indicators
1	00	1110	Read Telephone Signal Present Indicators
1	00	1111	Read Data Register Bits 17-24
1	11	0001	Write Control Register

CONT. Without a quarantine signal, this mode of failure can occur.

(b) The enable verify signal is returned to the CPD over the same pair of leads that carried the enable to the CPD. The enable verify is applied to these leads by a cable driver circuit. Each cable driver board has a buffer protection circuit. This protection network is used to prevent the CONT from returning multiple enable verify pulses due to a failure of the CONT. A time-out feature is also used to prevent the circuit from babbling onto the enable leads.

(c) A failure of the CONT could also cause the CONT to continuously apply data to the SCAB and interfere with other processor-peripheral communications. The protection buffer provided in the cable driver is used to prevent the CONT from babbling on the SCAB.

4.08 Instructions are divided into terminal operations and CONT operations. A zero in the most significant bit of the 7-bit opcode specifies that the opcode is a terminal opcode. Thus, the 64 available opcodes received from the processor are allotted equally between CONT operations and terminal operations. Examples of CONT operations and CONT terminal interaction are described later in the section.

4.09 The CONT communicates with a terminal over two terminal dedicated buses (see Fig. 7). One of these buses is the 2-way terminal data (TD) bus. The second is the 7-bit 1-way terminal opcode bus. Twenty-three bits of data plus an odd parity bit are passed from the CONT to the terminal or from the terminal to the CONT through the TD bus. A 6-bit opcode is passed from the CONT to the terminal via the terminal opcode bus. The seventh bit passed with the opcode is an even parity bit generated over the 6-bit opcode. After the CONT has applied the data to the TD bus and terminal op code bus and the data has settled, the active CONT transmits a terminal enable signal over a dedicated lead to that terminal. (The active CONT is identified to the terminal through the active-standby lead.) The terminal returns a termi-

nal all-seems-well (TASW) signal as a verification signal to the CONT. This verification signal informs the CONT that the terminal has completed the requested operation without error and, if required, data has been placed on the TD bus. Three other leads are part of the CONT-terminal interface and are used to represent:

(1) The status of the nonpriority telephone buffer in the terminal.

(2) The status of the priority buffer in the terminal.

(3) Trouble status; ie, that a problem has been encountered in the terminal.

CONT SEQUENCES

4.10 Processor-controller communications are accomplished via the CPD, the PUAB, and the SCAB (see Fig. 3). The CONT is alerted by a CPD-ENABLE pulse that the data is arriving over the PUAB. From this data the CONT determines the job to be done. After accomplishing the requested task, the CONT returns data to the processor over the SCAB. Each CONT contains circuits for receiving from both PUAB 0 and PUAB 1 and for driving both SCAB 0 and SCAB 1. When the CONT replies to the processor, data is returned over both answer buses simultaneously.

4.11 The CONT is slaved to the processor; ie, the CONT does not perform any operation that has not been initiated by the processor. Coded instructions are used by the processor to direct the CONT operations. These instructions are passed to the CONT over the PUAB as 24-bit words. The format of a terminal instruction (one that directs the CONT to communicate a request to a terminal) contains a 7-bit opcode that defines the task to be per-

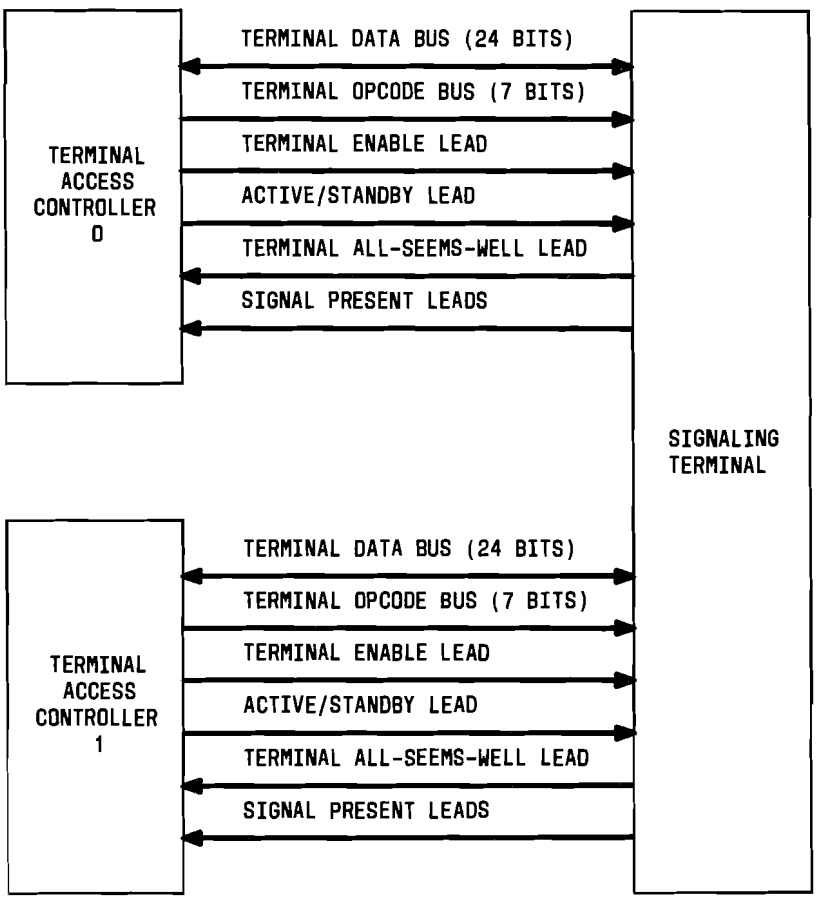


Fig. 7—Interconnection of a Terminal and the Terminal Access Controllers

formed, the address that specifies a particular register or memory location in the terminal to be used in the operation, and the terminal number that indicates the terminal to be used. The format of a CONT instruction (one that directs the CONT to perform an operation not involving a terminal) contains the 7-bit opcode that defines the task to be performed, and the data that contains information to be used during the task.

4.12 The CONT sequences can be classified as those executed strictly within the CONT and those involved in CONT-terminal interaction. The CONT opcodes of the first type contain a one in the most-significant-bit position and are used to read the various CONT registers (nine opcodes), CONT indicators (three opcodes), and to write the CONT control register (one opcode). The word format for all CONT read sequences is indicated in Fig. 8. The opcodes identifying CONT sequences are given in Table C.

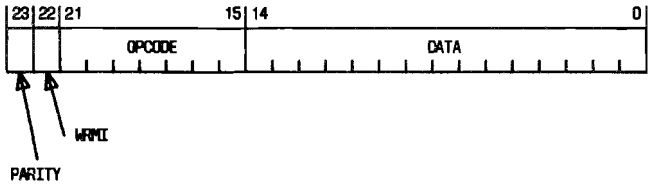


Fig. 8—CONT Word Format

4.13 The CONT write sequence (opcode 1110001) is used to write information into the CONT control register. A single opcode transfers the contents of bits 11 through 22 of the data register into the control register. The format of the CONT write word is indicated in Fig. 9. The second type of CONT sequence uses a CONT write in conjunction with the contents of the control register. The contents of the control register (loaded by the CONT write) modifies the normal CONT sequence initiated by the terminal opcode instruction paired with the CONT write. Numerous modifications of terminal sequences are possible to test the fault recognition circuitry within the CONT. These sequences are discussed in detail in CD-1A443-01 (CONT unit circuit description).

UNIT ALERT SEQUENCES

4.14 The unit alert sequence is not generally listed as one of the terminal sequences but is performed each and every time the central control needs to communicate with the CONT. Central control alerts the CONT by transmitting one enable pulse from the CPD to the CONT. A common sequence of events occurs each time the CONT receives an opcode enable or a DATA enable signal. When either the opcode or data enable arrives at the CONT, the enable verify clock is started to generate the signals to generate the enable verify signal. A translation of the received enable is started to determine the bus being used and the type of information arriving on that bus. The type of enable received is recorded in either the opcode enable or the DATA enable flip-flop. The indication as to the bus being used for transmission of the data is recorded in either the enable bus 0 or the enable bus 1 flip-flop. When the enable bus 0 flip-flop is set, the enable bus zero signal, which allows information to be gated into the data register from PUAB 0, is generated. Setting of the enable bus 1 flip-flop generates the enable bus one signal which allows information to be gated into the data register from PUAB 1. When data is stored in the data register, the master control clock is started to generate the timing pulses for the control sequences.

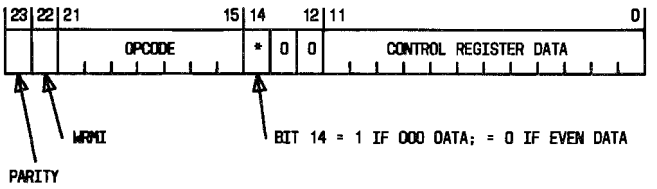


Fig. 9—CONT Write Work Format

4.15 An opcode enable, which specifies that the data register will receive an instruction word, sets the opcode enable flip-flop. This flip-flop then generates the opcode enable signal. The outputs of the flip-flops that store the 7-bit opcode in the data register are wired directly to the inputs of the opcode decoder. When opcode enable is generated, the opcode is decoded.

4.16 Each time an opcode enable is received, the opcode register is cleared and, if the opcode is a terminal instruction, the storage register gate-in signal is generated to transfer the contents of the data register into the instruction storage register.

4.17 The initialize and clear signal used to initialize all control flip-flops of the CONT is gener-

ated when both the enable verify clock and the master control clock are idle. Thus, while the CONT is in the idle state, initialize and clear signals are continuously generated. When the received enable starts the enable verify clock, the initialize and clear signal is stopped. The termination of initialize and clear initiates the generation of a group of signals that open a path between the data register and the parity circuit so that the validity of the data received over the PUAB can be checked. The signals generated are the data-register-gate-out (NADRGO and NBDRGO), the select data A, and the parity check select . The NADRGO signal gates bits 1 through 12 of the data register, and NBDRGO gates bits 13 through 24 out of the data register. The select data A signal gates the bus data through the information select network. The parity check select-one signal is a logic one to gate the data only to the parity circuit and not to the SCAB. The output of the parity circuit is monitored to determine whether the data is valid.

4.18 After the enable has been received and the WRMI bit has been received in the data register, the enable verify protection and the babble protection signals go high to unlock the buffer protection networks on the cable drivers. This allows the enable verify signal to be returned to the CPD at the proper time, and the data can be returned to the processor over the SCAB at the end of the operation.

4.19 The parity check indicates that the data is valid, and the sequence continues according to the operation required; but, if the check indicates that the data was received in error, the sequence is terminated and the circuit returns to the initial state after the enable verify clock completes its cycle.

A. CONT READ Sequence

4.20 The CONT operations are either READ operations or a WRITE of the control register. Twelve opcodes are assigned to read data from the following areas:

- Bits 1 through 16 of the data register
- Bits 17 through 24 of the data register
- Bits 1 through 16 of the reply register
- Bits 17 through 24 of the reply register
- Bits 1 through 16 of the instruction storage register
- Bits 17 through 24 of the instruction storage register
- Error source register
- Control register
- False all-seems-well register
- Trouble indicators
- Telephone signal present indicators
- Priority signal present indicators.

The CONT generates the same sequence for the READ of each of the 12 areas except for the particular gating signals for the terminal information network.

4.21 The opcode enable received in the CONT initiates the unit alert sequence. The unit alert sequence is independent of the opcode received; ie, the sequence is generated for both terminal and CONT opcodes. At the end of the unit alert sequence, the signals data-register-gate-out bits 1 through 12 (NADRGO) and data-register-gate-out bits 13 through 24 (NBDRGO) are terminated unless the instruction is a READ of the data register. However, before the end of the unit alert sequences, select data A (Read bit 1 through 16 of instruction storage register or data register) is terminated for all instructions.

4.22 The signal is initiated to select the data gated through the terminal information network. Then, the all-seems-well signal is returned over the SCAB to the processor. The circuit is initialized at master clock time (MCT) 50.

B. CONT WRITE Sequence

4.23 The CONT WRITE sequence is used to write information into the control register. Information to be written into the control register is received in bits 11 through 22 of the processor data register. When the enable signal is received, the unit alert sequence is executed. During master clock time 11, the contents of bits 11 through 22 of the data register are transferred to the control register.

4.24 During this operation, the contents of the control register are returned to the processor so

that the operation can be verified. The gating select signal for control or error source registers is a logic one gating the contents of the control register to the information select network. The read maintenance registers signal is initiated to gate the contents of the control registers through the information select network . After the information from the data register has been written into the control register, the gate-to-bus signal is generated to allow information to be gated out of the information storage register and applied to the SCAB. The all-seems-well signal is returned to the processor at clock time MCT13. Clock time MCT50 generates the initialize and clear signal to initialize the circuit.

TERMINAL SEQUENCES

4.25 Terminal opcodes and any associated data are decoded by the CONT and, if necessary, buffered for latter transmission to the proper terminal when all data has been received. The CONT enables the terminal addressed in the instruction. This terminal, in turn, decodes the opcode, checks any associated data, returns a terminal all-seems-well (TASW) signal to the CONT as an acknowledgment, and performs the indicated operation. The terminal communications unit within the CONT verifies that (1) a TASW was received from the terminal that was addressed and, (2) that a TASW was not returned from any other terminal. The false all-seems-well register within the CONT records all TASW signals from unaddressed terminals. The specific actions required by the CONT for each of the six types of terminal sequences are defined in CD-1A443-01. The six types of terminal sequences are as follows:

(1) ***PUT Sequence:*** Each PUT instruction directs the terminal to store data on one of the 16 linked lists which are assigned to a portion of data memory.

(2) ***WRITE Sequence:*** Three WRITE instructions are used to store information in the terminal data memory in areas other than the linked list area. Two others are used to clear or set the control register, and an additional two are used to perform no operation for verifying opcode parity check circuit operation.

(3) ***GET Sequence:*** Each GET instruction is a request by the processor for information from one of the linked lists which are assigned to a portion of data memory.

(4) ***READ Sequence:*** Two READ instructions are used to read information from the terminal that is in data memory areas other than the linked lists. Another READ instruction reads the terminal control register. Two other READ instructions are no operations used to verify opcode parity check circuit operation.

(5) ***Maintenance WRITE:*** Maintenance WRITE instructions are used for the following purposes:

(a) Clear or set the terminal unit mode register.

(b) Clear error indicators in the terminal unit.

(c) Initialize the terminal unit instruction address register.

(d) Load program memory starting at the instruction address register initial address.

(e) No operations for verifying parity checks.

(f) Perform daily parity check as on the terminal data (TD) bus and the input/output (I/O) data parity check circuit.

(6) ***Maintenance READ:*** Maintenance READ instructions are used to determine the status of the following circuit within the terminal.

(a) Mode register, error source register, and instruction address register.

(b) Data memory address bus, read/write A bus, and read/write B bus.

(c) Maintenance read instructions can also force all zeros or all ones (maintenance read ones) to be returned over the terminal data bus to the CONT.

As can be seen in Table D, all terminal opcodes have a zero in the most significant bit position of the opcode. The position of each bit on the PUAB is also given in the table.

4.26 In the following circuit operation, refer to Fig. 30 for the CONT block diagram. For a more detailed description of the circuitry, refer to CD- and SD-1A443-01.

A. Terminal PUT Sequence

4.27 After the processor has transmitted an opcode enable and distributed the instruction word

▶TABLE D◀

TERMINAL OPCODE ASSIGNMENTS

PUAB BITS			DEFINITION
21	20 19	18 17 16 15	
0	00	0000	Maintenance Read — Zeros
0	00	0001	Maintenance Read — Mode Register
0	00	0010	Maintenance Read — Error Source Register
0	00	0011	Maintenance Read — Data Bus
0	00	0100	Maintenance Read — Data Address Bus
0	00	0101	Maintenance Read — Spare
0	00	0110	Maintenance Read — Instruction Address Register
0	00	0111	Maintenance Read — Ones
0	00	1000	Reserved (No. 4 ESS)
0	00	1001	Read — Control Register
0	00	1010	NOP
0	00	1011	Read — Data Bits 1-24
0	00	1100	Reserved (No. 4 ESS)
0	00	1101	NOP
0	00	1110	Read — Data Bits 25-34
0	00	1111	Spare
0	01	0000	Get List 0000
0	01	0001	Get List 0001
0	01	0010	Get List 0010
0	01	0011	Get List 0011
0	01	0100	Get List 0100
0	01	0101	Get List 0101
0	01	0110	Get List 0110
0	01	0111	Get List 0111
0	01	1000	Get List 1000
0	01	1001	Get List 1001
0	01	1010	Get List 1010
0	01	1011	Get List 1011
0	01	1100	Get List 1100
0	01	1101	Get List 1101
0	01	1110	Get List 1110
0	01	1111	Get List 1111
0	10	0000	Put List 0000
0	10	0001	Put List 0001
0	10	0010	Put List 0010
0	10	0011	Put List 0011
0	10	0100	Put List 0100
0	10	0101	Put List 0101
0	10	0110	Put List 0110
0	10	0111	Put List 0111
0	10	1000	Put List 1000
0	10	1001	Put List 1001
0	10	1010	Put List 1010
0	10	1011	Put List 1011

▶TABLE D◀ (Contd)

TERMINAL OPCODE ASSIGNMENTS

PUAB BITS			DEFINITION
21	20 19	18 17 16 15	
0	10	1100	Put List 1100
0	10	1101	Put List 1101
0	10	1110	Put List 1110
0	10	1111	Put List 1111
0	11	0000	Write — Data Bits 13-24
0	11	0001	Write — Set Control Register
0	11	0010	NOP
0	11	0011	Write — Data Bits 1-12
0	11	0100	Write — Clear Control Register
0	11	0101	NOP
0	11	0110	Write — Data Bits 26-34
0	11	0111	Spare
0	11	1000	Maintenance Write — NOP
0	11	1001	Maintenance Write — Set Mode Register
0	11	1010	Maintenance Write — Clear Error Source
0	11	1011	Maintenance Write — Load Program Memory
0	11	1100	Maintenance Write — Clear Mode Register
0	11	1101	Maintenance Write — Data Parity Check
0	11	1110	Maintenance Write — Load Instruction Address Register
0	11	1111	Maintenance Write — NOP

containing a terminal PUT opcode over the PUAB, the CONT completes the unit alert sequence for an opcode enable. During the unit alert sequence, the terminal PUT signal is generated by the opcode decoder. This signal, in turn, sets the terminal PUT flip-flop of the opcode register. By the end of the unit alert sequence, as much of the sequence that can be accomplished without the data has been completed. The CONT returns an all-seems-well signal to the processor over the SCAB. The all-seems-well is approximately a one-half microsecond pulse.

4.28 Upon receipt of the data enable, the CONT executes the unit alert sequence for the data enable. During the unit alert sequence, the terminal number select signal is generated when the data enable flip-flop is set. The terminal number, which is stored in bits 17 through 20 of the instruction storage register, is translated from a binary coded decimal number to a 1 out of 16 signal. The translated terminal number is combined with the terminal number select signal to gate the contents of bits 1 through 7 (opcode) of the instruction storage register onto the terminal opcode bus for the selected terminal and to select for the specified terminal the TD bus over which data is to be transmitted and received. The parity bit generated over the opcode is an even parity bit.

4.29 Since the TD bus is a 2-way bus, a means must be provided for the CONT to gate data destined for the terminal onto the bus and to remove that data in order to receive data from that terminal. The required gating function is achieved with the release terminal data signal. This signal is initiated to place data onto the TD bus during the unit alert sequence when the data enable flip-flop is set. The generation of terminal number select, release terminal data, NADRGO, and NBDRGO, gates the contents of the data register onto the selected TD bus.

4.30 After parity over the PUAB has been checked, the data can be removed from the parity cir-

cuit input and the select data (read bits 1 through 16 of instruction register or data register) signal terminated.

4.31 The terminal enable is generated to alert the terminal that the opcode and data have been placed on the buses and should be in a stable state. The terminal can now decode the opcode. The terminal enable is transmitted to the selected terminal over the terminal enable 0 lead. The data placed on the TD bus for a PUT instruction is bits 1 through 24 of the data register. Bit 23 of the TD bus must be in the logic one state to allow the terminal to return a buffer overflow indication if the link list is full when the terminal received the PUT instruction. Since bit 23 of the data register contains the WRMI (for an operation to be performed, WRMI must equal one) this condition is fulfilled.

4.32 The terminal decodes the opcode and places the signal unit onto the selected list. If the buffer can accept the SU, the terminal returns a TASW signal. If the buffer is full, the terminal returns a TASW over the TTASW0 lead and a buffer overflow (low-going signal) on bit 23 of the TD bus.

4.33 The terminal communications network of the CONT receives the TASW from the terminal, checks to ascertain that the TASW was received from the terminal addressed and sets the valid all-seems-well flip-flop. The terminal communications network also checks that a TASW was not received from a terminal not addressed. The false all-seems-well register records all TASW from terminals not addressed and sets a bit of the error source register if a bit is set in this register.

4.34 Information arriving in the CONT over the TD bus from a terminal is deposited in the 24-bit reply register. For all terminal operations, the window to this register is opened. During the PUT sequence, the only information returned from the terminal over the TD bus is the buffer overflow when it occurs. Therefore, the information of the TD bus which is gated into the reply register is the data the CONT has transmitted to the terminal, except in bit 23.

4.35 Data and the all-seems-well signal are presented to the processor via the SCAB. The format of this data is:

- Bits 00 through 07 of the SCAB receive Bits 24 through 17 of the reply register
- Bits 08 through 15 of the SCAB receive Bits 08 through 01 of the reply register.

Bits 24 through 17 of the reply register are returned so that bit 23 can be examined. The terminal enable is ended, and initialize and clear is generated to clear the control flip-flops and the data register. Clearing the data register causes the removal of data from the TD bus and termination of the active standby signal.

B. Terminal WRITE Sequence

4.36 The WRITE instruction, which appears to the CONT very much like the PUT instruction, is a 2-distribute operation. The instruction word, which contains the 7-bit opcode and terminal number is distributed first. It contains the 9-bit address required by the terminal. The data consisting of 12 bits is distributed last.

4.37 Upon receipt of the opcode enable and the instruction word for the WRITE instruction, the CONT performs essentially the same functions performed when the opcode enable and instruction word for a PUT instruction were received. The unit alert sequence is completed. However, for this instruction, the terminal write flip-flop is set in the opcode register. The CONT returns an all-seems-well to the processor.

4.38 When the data enable is received, the CONT executes the unit alert sequence for the data enable. For the WRITE operation, the CONT must perform essentially the same tasks as for the PUT sequence. During the unit alert sequence, the terminal number select and release terminal data signals are generated. The terminal number select is combined with the translated terminal number to select and enable the proper terminal opcode code and TD buses. The opcode stored in bits 1 through 7 of the instruction storage register are transmitted to the terminal. The release terminal data opens the TD bus for data to be sent to the terminal. However, for the WRITE sequence, the CONT must construct the 24-bit word to be transmitted. This word consists of the following:

- Bits 1 through 12 from Bits 1 through 12 of the data register
- Bits 13 through 21 from Bits 8 through 16 of the instruction storage register
- Bits 22 and from Bits 19 and 20 of the data register

- Bit 24 - Generated parity

4.39 The NBDRGO signal is ended, inhibiting the gating out of bits 13 through 24 from the data register. However, bits 1 through 12 continue to be gated out of the data register by NADRGO. The stored location gate out signal is generated to gate out bits 8 through 16 of the instruction storage register (the 9-bit address) to bit locations 13 through 21 of the TD bus. Bits 19 and 20 of the data register are gated to bits 22 and 23 of the TD for a WRITE operation. The odd parity bit over 23 bits of information is gated to bit 24 of the TD bus.

4.40 The terminal enable is generated to alert the terminal that the opcode and data are on the buses and should be in a stable state. The CONT opens the circuit to the reply register. The terminal decodes the opcode, checks and stores the data in the proper location specified by the 9-bit address, and returns a TASW to the CONT. The CONT checks the TASW and sets the valid all-seems-well flip-flop which starts the secondary clock. The contents of the reply register are applied to the parity check circuitry. This action places bits 1 through 16 of the reply register on the SCAB. The CONT checks to ascertain that the terminal returned a TASW and that no erroneous TASWs were returned and that no error was incurred in the transfer of information between the terminal and CONT. During the WRITE sequence, the data loaded into the reply register is the data transmitted to the terminal by the CONT. The CONT returns an all-seems-well to the processor over the SCAB. The terminal enable is removed. The initialize and clear signal is generated to clear the control flip-flops and the data register. This action removes the active standby signal.

C. Terminal GET Sequence

4.41 In order to perform the GET operation, the CONT requires only the opcode and the terminal number. Therefore, only the instruction word is required to be distributed to the CONT.

4.42 The CONT receives the opcode enable and initiates the unit alert sequence. During the unit alert sequence for the GET instruction, the terminal GET signal is generated. The signal selects the required control signals for the GET sequence.

4.43 As soon as the opcode is decoded, the NRTN signal is generated to be combined with the translated terminal number to select the particular terminal opcode and TD buses. The opcode is gated to the terminal. For the GET operation, no data need be transmitted to the terminal over the TD bus. Therefore, release terminal data is not generated during the GET sequence. The terminal enable signal is generated to inform the terminal that the opcode is on the bus.

4.44 The CONT generates the gate reply register signal to open the reply register to receive the information from the terminal. The terminal decodes the opcode, obtains the required data from the link list, places the information on the TD bus and returns a TASW over the TTASW0 lead to the CONT. When the TASW is received in the CONT, the CONT checks the validity of the TASW and sets the valid all-seems-well flip-flop starting the secondary clock. The data placed on the TD bus by the terminal is stored in the reply register.

4.45 Upon receipt of the TASW, the contents of the reply register are gated through the information storage register to the parity check circuit. This action places bits 1 through 16 of the reply register onto the SCAB. (The data is placed on the SCAB because NGPS0 is a logic 0.) This check, which determines whether an error has been incurred during a transfer of the data from the terminal to the CONT, is made at secondary clock time 03 . If the data has been transferred without error, the terminal enable is removed immediately.

4.46 The terminal monitors the enable to determine whether the transfer was valid. If the enable is removed within 400 nanoseconds of the time the terminal returned the TASW to the CONT, the transfer is assumed valid. The terminal then updates the link list information. If an error is detected, the terminal enable is generated until master clock time (MCT) 49. The terminal determines that an error was detected and does not update the list information so that the processor can again request the data. If no error has occurred, the CONT returns an all seems well to the processor at MCT43.

4.47 The receipt of the all-seems-well by the processor is a verification that the data placed on the bus earlier is valid. The initialize and clear signal is generated to initialize the circuit. In order that the remaining half of the word be obtained from the CONT, the processor uses the CONT opcode called read reply register bits 17 through 24. Thus, a GET

opcode must be followed by the CONT opcode for reading bits 17 through 24 of the reply register.

D. Terminal READ Sequence

4.48 As with the GET operation, the CONT requires only the information word for the READ operation. When the CONT receives the opcode enable, the unit alert sequence is initiated. As soon as the opcode is decoded, the release terminal select and release terminal data signals are generated. The release terminal data signal is generated for this sequence because the 9-bit address must be transmitted to the terminal over the TD bus. The release terminal select signal is combined with the translated terminal number to select and gate data onto the terminal opcode and TD bus for the selected terminal. The opcode plus generated parity are transmitted to the terminal over the terminal opcode bus. For this sequence, the NADRGO and NBDRGO are terminated during the unit alert sequence. The stored location gate-out signal is generated to gate the 9-bit address from the instruction storage register onto the selected TD bus. A summary of the data transmitted to the terminal over the TD bus during the READ sequence is:

- Bits 1 through 12 - All zeros
- Bits 13 through 21 - Bits 8 through 16 of the instruction storage register
- Bits 22 through 23 - 1,1
- Bit 24 - Generated odd parity

4.49 The parity bit transmitted over the TD bus is odd parity calculated over the 9-bit address. The terminal enable is then transmitted to the terminal and the gating circuit is opened for data from the TD bus to be received in the reply register.

4.50 The terminal returns 23 bits of data plus an odd parity bit when the data memory is read. The terminal places the data on the TD bus and returns the terminal all-seems-well simultaneously. Receiving this signal, the CONT checks the validity of the signal and sets the valid all-seems-well flip-flop. This action starts the secondary clock and terminates the release terminal data signal. Removing this signal terminates the gating of data onto the TD bus by the CONT, and the data placed on the TD bus by the terminal is forced into the reply register. The contents of the reply register are gated through the information select network to the parity circuit. Bits 1 through 16 of the reply register are gated to the SCAB. Then the parity is checked to determine whether or not a failure occurred in the transfer of data from the terminal to the CONT. If no error occurred, the CONT returns an all-seems-well to the processor. The terminal enable is removed and an initialize and clear is generated to clear the control flip-flops and the data register. The CONT is again initialized. As with the GET instruction, this instruction must be followed by a READ reply register bits 17 through 24 in order for the processor to obtain the full word.

E. Maintenance WRITE Sequence

4.51 The mode register can be set or cleared with the maintenance write set mode register and maintenance write clear mode register operation, respectively. The TD bus data is used as a mask to select individual mode register bits. Only those register bits corresponding to ones on the bus are modified on a given operation. The maintenance write clear error source register operation clears all the error indicators in the error source register, including I/O buffer overflow. The TD bus data is ignored on this operation.

4.52 The maintenance write load instruction address register operation is used to initialize the instruction address register for the program loading or execution. This operation will be executed only if terminal stop mode register bit 4 is set. If not, an all-seems-well failure occurs and no change is made to the instruction address register. This register can be loaded directly or indirectly depending on the state of MR bit 13 (load instruction address register direct). If this bit is a one, maintenance write load instruction address register will cause the TD bus bits 1 through 11 to be loaded into the instruction address register. If the bit is zero, the contents of the program memory at the current address in the instruction address register is loaded into the register.

4.53 The terminal program memory is loaded using the maintenance write load program memory instruction. When executed, TD bus bits 1 through 12 are loaded into program memory at the current address in the instruction address register; then, the register is incremented to the next sequential address. An address is not supplied with the maintenance write load program memory operation.

Program memory is loaded sequentially, one location at a time from any starting address by first using a maintenance write load instruction address register operation followed by a series of maintenance write load program memory operations. As with maintenance write load instruction address register, this operation is executed only when terminal stop is set.

4.54 The maintenance write N0 and N7 operations are no operation instructions and are used to verify the opcode leads and the opcode parity check circuit. The TD bus data is ignored. The maintenance write data parity check instruction is similar to a no operation but requires a valid parity on the TD bus. It is used to exercise the TD bus and I/O data parity check circuit.

F. Maintenance READ ONES Sequence

4.55 The CONT performs the same sequence for all READ instructions except one. This operation is called the maintenance READ ONES. The CONT must decode the four least significant bits of the opcode to determine when this instruction is received.

4.56 The sequence for this READ operation is identical to the sequence for other READ operations except that the release terminal data signal is not generated. For the maintenance READ ONES operation, the terminal requires that the contents of the TD bus be all ones. If release terminal data is not generated, the CONT cannot gate information onto the TD bus. Thus, the leads of the TD bus are all high. The terminal should return all ones on the TD bus to the CONT. The CONT, in turn, returns all ones to the processor. This instruction must also be followed by read reply register bits 17 through 24. Refer to Table E for a listing of controller and terminal register, bus and word sizes.

5. DATA TERMINAL UNIT

TERMINAL UNIT PHYSICAL DESCRIPTION

5.01 The data terminal units J1A094AC are located within the basic and supplementary terminal frames as shown in Fig. 4 and 26. The arrangement of the circuit packs which comprise the terminal unit are shown in Fig. 10. The number, quantity, and name of the circuit packs required along with the functional schematic section of SD-1A444-01 which pertains to the CPs are given in this figure.

TERMINAL UNIT FUNCTIONAL DESCRIPTION

5.02 The terminal unit is a small, high-speed, stored program processor that has simple but specialized order structure. The basic features of the terminal unit are:

- Independent program and data memories.
- An 11-bit instruction word.
- A 560-nanosecond instruction cycle time.
- A 2032-word (maximum) program memory.
- A 23-bit data word.
- A 400-nanosecond data access time.
- A 512-word (maximum) data memory.
- Dynamically allocated, wired logic SU buffers.
- Masked insertion, rotation, and increment logic function.
- High self-checking capabilities (utilizing an internal exercise program).
- Program memory controls the internal operations of the terminal unit. Data memory provides buffering for signaling unit traffic.

A block diagram of the CCIS terminal is given in Fig. 31.

5.03 The functions performed by the terminal unit are controlled by an internal stored program and include all operations related to the 2-way synchronous signaling link. Excess real-time capacity is used by a self-test exercise program which serves as the primary fault detection mechanism in the terminal unit. Processing of the transmitted and received SUs in the primary function performed by the terminal unit; therefore, these tasks are given priority over the self-test exercise routines.

5.04 Although the processing of SUs is the prime function of the terminal unit, it normally occupies the terminal for approximately 10 percent of the time. The terminal unit autonomously conducts the self-check exercises for the remainder of the real-

TABLE E

CONTROLLER AND TERMINAL REGISTER, BUS AND WORD SIZES

REGISTER, BUS, OR WORD NAME		CONTROLLER (BITS)	TERMINAL (BITS)
Instruction Storage Register	(ISR)	24	—
Data Register	(DR)	24	23
Control Register	(CR)	12	20
Terminal Reply Register	(RR)	24	—
Error Source Register	(ESR)	10	21
False Terminal ASW Register	(FASWR)	16	—
Signal Present Register	(SPR)	16	—
Logic Register	(LR)	—	23
Address Register	(AR)	—	9
Instruction Address Register	(IAR)	—	11
Mode Register	(MR)	—	23
Scanner Answer Bus	(SCAB)	16	—
Peripheral Unit Address Bus	(PUAB)	24	—
Terminal Data Bus †	(TD)	24	24
Terminal Opcode Bus †	(TOP)	7	7
Data Address Bus		—	23*
Input/Output Bus		—	24*
Address Bus		—	9
Read/Write Bus		—	—
A			12*
B			12*
C			10*
Transfer Bus			12
Instruction Word		24	24
Program Memory Words (256 Max)		12	
Data Memory Words (512 Max)		24	

* Internal communication only.

† One bus for each CONT

CONN POS	UNIT MTG PLATE POS 06	UNIT MTG PLATE POS 02
01	J87389P +3V POWER CONVERTER	J87389P +3V POWER CONVERTER
02		
03		
04		
05		
06		
07		
08	FC21	FC21
09		FB152
10	FB300	FB306
11		
12	FA796	FA914
13	FA793	FA793
14	FA793	FA793
15	FA646B	FA646B
16	(SEE NOTE)	(SEE NOTE)
17		
18	FA646B	FA795
19	FA791	FA798
20	FA919	FA792
21	FA781	FA788
22	FA782	FA789
23	FA783	FA784
24	FA783	FA785
25	FA780	FA917
26	FA646B	FA787
27	FA646B	
28	FA646B	FA646B
29	(SEE NOTE)	FA646B
30		FA646B
31		FA646B
32		
33		
	201 D MODEM(S)	

NOTE: THREE POSITIONS ARE WIRED TO ACCEPT FA646B MEMORY PACKS FOR FUTURE EXPANSION, BUT ARE UNEQUIPPED INITIALLY.

CIRCUIT PACK NUMBERS	(QUANTITIES)		NAMES AND FS LOCATIONS	
FA 646 B	(10)	:	PROGRAM MEMORY, DATA MEMORY	FS6, FS7
FA 780	(1)	:	ROTATE CIRCUIT	FS3
FA 781	(1)	:	LOGIC A	FS3
FA 782	(1)	:	LOGIC B	FS3
FA 783	(2)	:	LOGIC C	FS3
FA 784	(1)	:	INSTRUCTION CONTROLLER	FS2
FA 785	(1)	:	INSTRUCTION DECODER	FS2
FA 787	(1)	:	INSTRUCTION ADDRESS FAN OUT	FS2
FA 788	(1)	:	DATA MEMORY TIMING CIRCUIT	FS4
FA 789	(1)	:	MEMORY OPERATION SEQUENCER	FS4
FA 791	(1)	:	LINKED LIST REGISTER	FS4
FA 792	(1)	:	ERROR SOURCE REGISTER	FS4
FA 793	(4)	:	INTERFACE CIRCUIT	FS5
FA 795	(1)	:	CONTROL REGISTER AND MODEM INTERFACE	FS1
FA 796	(1)	:	MAINTENANCE CONTROL AND MONITOR	FS1
FA 798	(1)	:	DATA ADDRESS BUS	FS4
FA 914	(1)	:	INPUT/OUTPUT CONTROLLER	FS1
FA 917	(1)	:	INSTRUCTION ADDRESS REGISTER	FS2
FA 919	(1)	:	DUAL MODEM INTERFACE	FS1
FB 152	(1)	:	12 VOLT REFERENCE SUPPLY	FS8
FB 300	(1)	:	OSCILLATOR BOARD	FS4
FB 306	(1)	:	FERROD DRIVER	FS1
FC 21	(2)	:	+3 VOLT FILTER AND REFERENCE	FS8

Fig. 10—Terminal Unit Circuit Pack Layout

time cycle. The complete set of exercises will be executed at least once during the time required to transmit or receive a single SU (28 x 1/2400 =11.67 milliseconds). Faults discovered by these test routines result in the transfer of traffic to a different link, and this link is removed from service for performance of diagnostic routines to determine the cause of the failure. Each modem clock cycle provides a signal which alerts the terminal unit program to execute the portion of program memory required to process this bit of the signaling traffic. Each clock cycle (1/2400 = 416.7 microseconds) of the modem requires the terminal unit to handle one receive and one transmit bit over the VFL interface. The terminal only requires 560 nanoseconds to complete any single operation execution sequence. Therefore, roughly 740 such instructions may be executed during the time one bit is being processed for the VFL interface. Only 10 percent of this capacity is required to process VFL traffic, and the remainder of the real time that the signaling bit is present in the VFL is dedicated to the self-check routines of the terminal, CONT, modem and VFL. Each 28th bit requires additional processing associated with a complete SU and every 12th word requires processing associated with each block of signaling traffic. Detailed description of the software processing for the receive and transmit tasks may be found in Section 231-045-405.

5.05 The terminal unit receives SUs for transmission in parallel bit form from the processor via the CONT. These SUs, which may be single-unit messages or multiunit messages, are stored according to priority level in the transmit buffer portion of data memory. Each SU, in priority order, has eight check bits added and is passed serially to the data modem for transmission. Both transmit and receive tasks are based on the processing of each bit and each 28-bit SU, and each consecutive block of 12 SUs. An acknowledgment control unit is always generated to occupy the 12th position of an outgoing block and relates to a block previously received. Synchronizing SUs are transmitted in lieu of SUs when less than the 11 SUs required for a block are available in the transmit buffer. Transmitted SU blocks are stored in the transmit record table until an acknowledgment control unit, acknowledging error-free reception, is received. The transmit tasks also include transmission of faulty-link information when instructed by the processor.

5.06 The incoming serial data from the data modem is accepted by the terminal unit where each SU is examined for errors, based on its eight check bits. Error-free SUs, minus check bits, are delivered in parallel bit form to the processor from the CONT. Included in the receive task are the following functions performed by the terminal unit:

(a) Group bits of the data stream into SUs.

(b) Generate and transmit an acknowledgment control unit in the 12th position of each block.

(c) Filter erroneous SUs and all other SUs related to the operation of the signaling link from the received data to be presented to the processor.

(d) Analyze received acknowledgment control unit to:

(1) Determine whether or not the acknowledgment control unit is received in the proper SU position

(2) Determine if an acknowledgment control unit has been skipped, repeated, or is the one expected

(3) Determine whether or not an acknowledgment control unit requests retransmission of any previously transmitted SUs.

(e) Process any required retransmission.

(f) Separate incoming data according to priority and indicate reception to the processor.

(g) Collect multiunit messages.

5.07 Correction of errors contributed by the data link is via retransmission. To accomplish this, all SUs are transmitted in blocks of 12, the first 11 of which contain signaling information or sychronizing SUs which are transmitted only in the absence of other signaling traffic. The 12th SU of each block is an acknowledgment control unit, coded to indicate the number of the block in which it is included, the number of the block being acknowledged, and bits indicating whether or not each of the 11 SUs of the acknowledged block were received without error. Primary error detection on the signaling links is achieved through the use of the eight signal unit check bits. In addition, a data carrier failure detector is provided for detection of longer error bursts. Error-free messages are used without delay while a retransmission is requested of those found in error.

5.08 Continuity of service is maintained by transfer from a faulty link to an alternate link in event of a failure condition. The terminal unit continuously monitors the data carrier and the SU error rate. Either a total failure or excessive SU errors will initiate transmission of messages over the alternate signaling link. This transfer is effected without loss of signaling information due to the retransmission method of error correction. Signaling traffic is restored to the regular route after the trouble clears. The processor is alerted to an impending overload of terminal unit signaling capacity (overflow) by means of a single scan point associated with each terminal unit.

5.09 Each terminal unit is equipped with a DS 201D which provides the transmission interface with the 4-wire VFL.

5.10 Figure 11 is a simplified block diagram of the terminal showing the controller hierarchy. There are three separate control entities within the terminal. These are the instruction controller, the data memory controller, and the I/O controller. The instruction controller provides access to the program memory and executes the internally stored program. The data memory controller provides access to the data memory for both the internal stored program and the I/O controller. It also contains a wired logic linked-list sequencer which administers the SU buffers. The I/O controller handles all communications with the CONT which include:

(a) Maintenance access to the terminal

(b) Access to the mode register which controls the operating mode to the terminal

(c) Relaying commands to the instructor controller or data memory controller for accessing the program memory or data memory respectively.

The instructor controller and data memory controller are driven by a common 12.5 Hz oscillator. No internal timing is required in the I/O controller.

5.11 The three controllers operate asynchronously with respect to each other. Interaction among the controllers is in the form of commands of bids. The solid arrows in Fig. 11 identify the various commands and indicate controller hierarchy. When one controller bids for service from another, it waits until an acknowledgment (broken line) is received from the serving controller. This indicates that the operation is in progress and that data is being transferred. For example, if the instruction controller decodes a READ instruction, it bids for the data memory controller and then waits. The data memory controller recognizes the bid and starts a memory access cycle. When the memory output is available, the continue signal is returned. The instructor controller then resumes its cycle, gating the data into a register and removing the bit. The data memory controller completes its cycle and is ready to serve another bid.

5.12 The data memory controller can receive bids from both the instruction controller and the I/O controller. If bids arrive simultaneously, the I/O bid is served first. The GET and PUT sequences are operations which require a sequence of memory reads and writes. Due to the length of these sequences and because of the need for fast response to commands from the CONT, the data memory controller will interrupt a local GET or PUT sequence to serve an I/O memory access bid. The local bid is restarted after the I/O operation has been completed. An interrupt will not occur if the local sequence has passed the point where "continue" is returned to the instruction controller.

5.13 Figure 31 is a block diagram of the terminal showing principal functional blocks of the terminal. The terminal contains 11 hardware registers. The logic register, data register, and address register are used by the internal program for logic operations and for access to the data memory. The instruction address register contains program memory addresses. Its contents can be incremented or loaded in the case of program transfers. The mode register and error source register are accessible only by the stored program control. The state of the mode register determines the operating mode of the terminal.

5.14 The error source register records the occurrence of errors detected by the various check circuits throughout the terminal. The empty list pointer register, pointer registers A and B, and the list number register are used by the data memory controller for administration of the SU buffers. The control register is a special register used for passing software control information between the stored program control and the terminal. Because it must be accessed by both the stored program control and the terminal, it appears like a pseudo data memory location.

5.15 The memory used in the terminal is a random access integrated field effect transistor

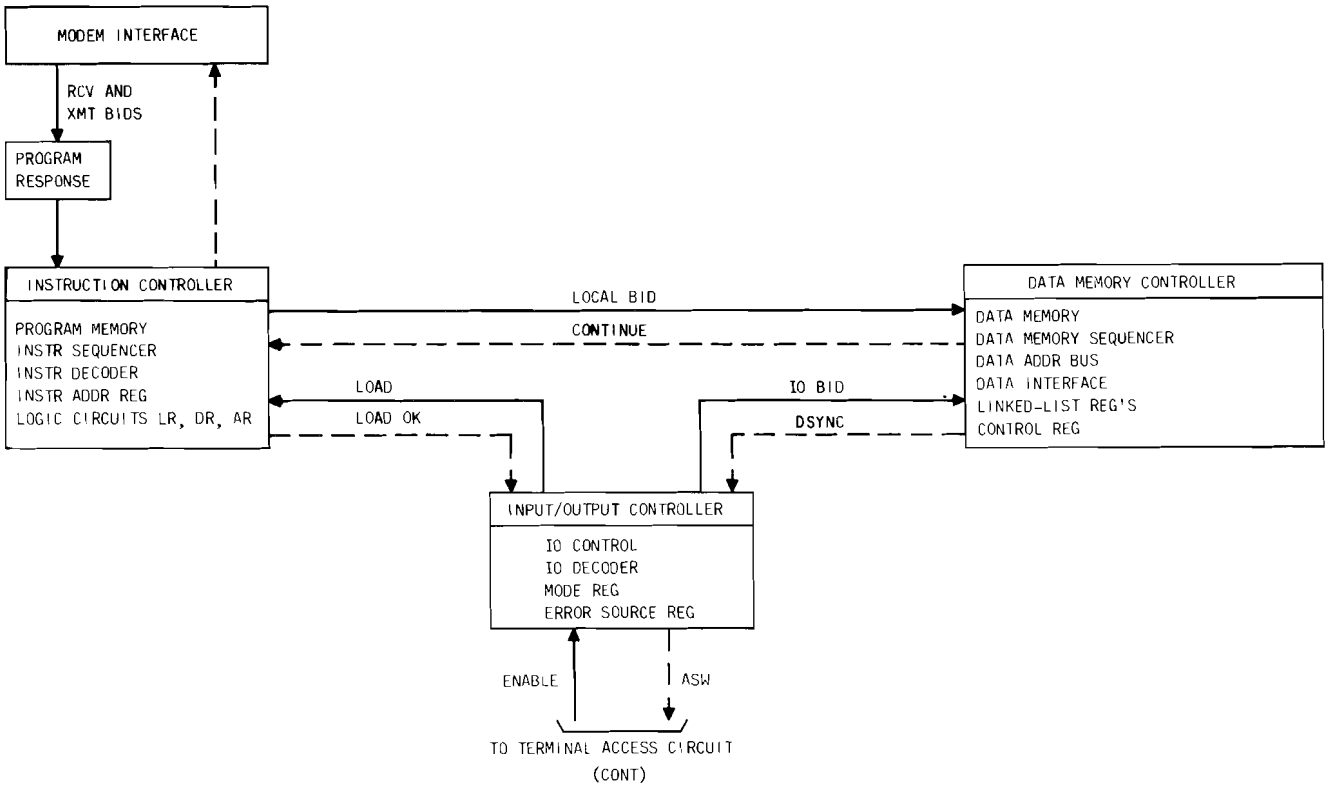


Fig. 11—Terminal Unit Controlled Hierarchy

(IGFET) memory. It is packaged in modules of 128 words by 12 bits per word. All inputs and outputs interface directly with the 1A logic used in the terminal. Timing signals required for the memories are generated in the respective controllers.

5.16 A modem interface circuit provides the I/O port for the serial bit stream to and from the modem. The interface also operates asynchronously with respect to the rest of the terminal. Bids for receive and transmit are generated in response to clock signals from the modem at the bit rate of the data link. These bids appear in the control register where they can be inspected periodically by the internal program. Special receive and transmit instructions are used to transfer data, one bit at a time, between the modem interface and the logic register. The execution of the receive or transmit instruction is used as the acknowledgment signal for the respective bid.

5.17 Bit numbering for data registers and buses starts with one for the leftmost bit. This corresponds to the numbering of CCIS SUs. Addresses for data and program memories are numbered from the right starting with zero.

5.18 The theory of operation of the CCIS signaling terminal group is discussed in Section 231-045-405 (Toll CCIS Software Processing). Part 3 of this document includes a description of the functions of the terminal unit itself, which is common to all present systems using CCIS. The principal differences in operation are in the different CONT units required to interface the terminal with the main processor. Details of terminal unit operation may be obtained from this document and CD-1A441-01, the terminal unit circuit description for No. 1 or No. 1A ESS CCIS.

5.19 The administration of the linked list portion of data memory has been referred to several times in this section. Figure 32 shows a layout of the linked list operation in data memory. It is beyond the

scope of this section to present a detailed description of its operation.

5.20 The linked list operation is common to all systems using toll CCIS. Refer to either CD-1A444-01 or CD-94833-01 for a complete detailed description of its operation.

MESSAGE FORMAT AND CODING

5.21 The format and coding associated with the various CCIS SUs are defined in Part 6 of this document and Section 781-030-100.

6. TERMINAL INPUT/OUTPUT CIRCUIT

6.01 The terminal I/O circuit is comprised of connectors and transformers and its basic functions are to:

- Handle all I/O communications between the CCIS terminal and the ESS processor via the CONT.
- Provide a digital-to-analog and an analog-to-digital interface between the near-end and far-end CCIS terminals, respectively.

6.02 The circuits located on the data terminal basic frame are interconnected with the No. 1 or No. 1A ESS processor as illustrated in Fig. 4. The processor alerts the data terminal basic frame that communication is required by means of enable pulses transmitted from the CPD. When the processor transmits data to the data terminal basic frame, the data is sent to the peripheral function translator . From the translator information is passed to the data terminal basic frame over the binary PUAB. Information requested from the circuits of the frame is returned to the No. 1 or No. 1A ESS processor over SCAB.

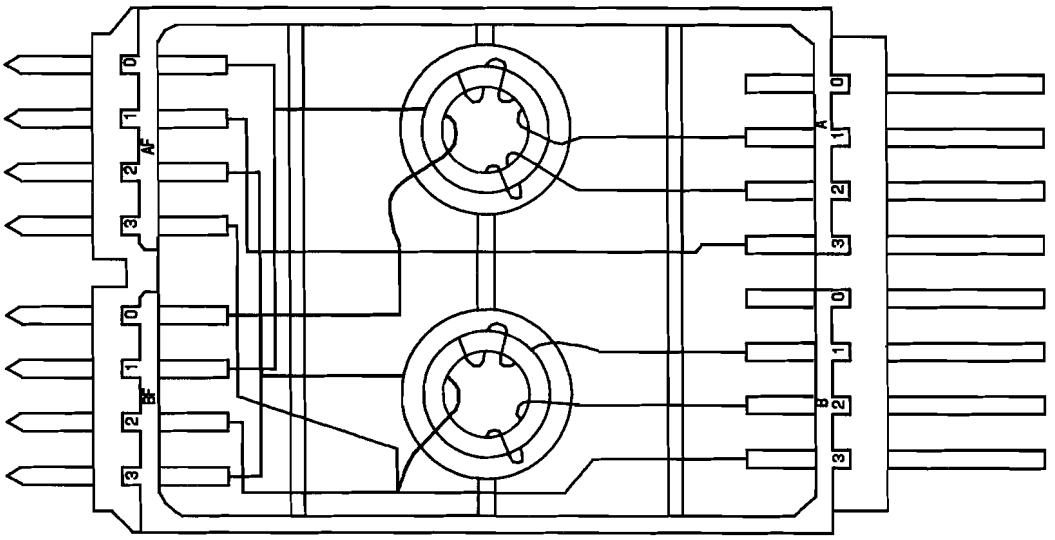
6.03 The terminal I/O circuits provide the entrance and exit ports to the data terminal basic frame for the PUAB and the SCAB plus the enables from the CPD. The I/O circuits are comprised of connectors, for interfacing the cable drivers of the frame to the SCAB, and transformers for interfacing the logic circuits of the frame to the PUAB. Each I/O circuit interfaces both the 0 and 1 PUAB and 0 and 1 SCAB to the circuits located in that bay.

6.04 The PUAB is 38 bits; however, only 24 of the 38 bits are used by the CONT of the data terminal basic frame. Each terminal I/O circuit contains the transformers to receive from both PUAB 0 and 1; therefore, each circuit contains 48 transformers. For the implementation of this circuit, the 2650A transformer unit is used. This unit consists of twelve 2645A transformer units assembled in a KS-2024, L1 mounting. The 2645A unit consists of two identical ferrite core transformers assembled into a plastic frame and connected to terminals as shown in Fig. 12A. When a 100-milliampere pulse of 0.5 microsecond duration is applied across terminals 0AF and 1AF or 2AF and 3AF, with terminals 0BF and 1BF or 2BF and 3BF connected together, the voltage across terminals 1A and 2A or 1B and 2B will be greater than 1.5 volts when connected to a 510-ohm load. If any signal should appear across terminals 0AF and 1AF or 2AF and 3AF so that the windings are series opposing, little or no output will be provided across terminals 1A and 2A or 1B and 2B. The 14 bits of the PUAB which are not used by the data terminal basic frame are wired through the frame.

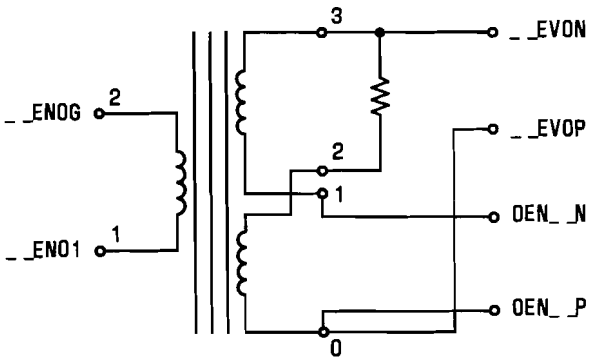
6.05 The scanner answer bus carries 17 bits of information from the data terminal basic frame to the processor. This information consists of 16 bits of data and an all-seems-well signal. The I/O circuit contains connectors to interface data from the cable drivers of the terminal access controllers of the frame to both SCAB 0 and 1.

6.06 Transformers are supplied in the I/O circuit to receive the enables from the CPDs. These transformers are part of the 2650A units. The CPD requires that enable verify signals be returned from the peripheral unit for some of the enables. In paragraph 6.04, the description of the transformer operation indicates that little or no output occurs when a signal appears across terminals 0AF and 1AF or 2AF and 3AF so that the windings are series opposing. Therefore, the transformer is wired so that the enable verify signal is returned over the same wires that carried the enable from the CPD. This wiring connection is shown in Fig. 12B. Thus, the enable verify signal is applied to the transformer to prevent a pulse on the output terminals.

6.07 Six types of enables are received by the data terminal basic frame. Two of these enables, the data terminal frame enables, are the data enable and the opcode enable. These enables are designated as DENab and OENab, where a specifies the controller number 0 or 1, and b specifies the bus number 0 or 1. When these enables are received, an enable verify must be returned to the CPD.



A. NO. 2645A TRANSFORMER



B. INTERCONNECTION OF ENABLE TRANSFORMER

Fig. 12—Input/Output Circuit Enable Transformer No. 2645A

6.08 The remaining four enables, the frame isolation enables, are the lock babble protect, the unlock babble protect, the set quarantine, and the reset quarantine enables. These enables are designated as LBPa, UBPa, SQa, and RQa, where a specifies the CPD and the controller. When these enables are received, an enable verify is not required to be sent to the CPD. The enables SQa and RQa control the quarantine functions of the terminal access controllers. When in the quarantine mode, the terminal access controller is isolated from the terminals. This mode is entered when problems are detected in the terminal access controllers. The enables LBPa and UBPa control the lockout circuitry that isolates the controllers from the SCAB.

7. SUPPORT EQUIPMENT

POWER CONTROL

A. Purpose

7.01 The purpose of the power control circuit is to:

- Provide a means of controlling power to terminals and CONTs on the data terminal frame

- Provide indications via the scanner to the processor indicating the power status of the various units on the frame
- Furnish visual indication of the power status of the terminals and CONTs
- Furnish a means of testing the power converter.

7.02 The power control circuit of the basic frame consists of:

- Five ED-1A370-30 power control units per bay
- One ED-1A370-31 timer unit per bay
- One ED-1A370-32 audible alarm unit (bay 0)
- One ED-1A370-33 minor alarm (MN) and converter test unit (bay 1)
- Four or eight ED-1A371-30 data set power control units.

These units are arranged in bays 0 and 1 of the basic frame as shown in Fig. 13.

7.03 Four ED-1A370-30 power control units are used to perform the power control functions in a supplementary terminal frame. These units are arranged in the first and second supplementary frames as shown in Fig. 13. Figures 14 and 15 are block diagrams of power control bay 0 and bay 1 of the basic frame and Fig. 16 is a block diagram of the supplementary frame. These figures show the functional arrangement of the power control circuitry within each frame, as well as the frames interaction. Refer to CD- and SD-1A445-01 for a detailed description of the power controller circuits.

B. General Description

7.04 This circuit is designed to be used for each bay of the data terminal basic frame as well as each of the two supplementary frames. The common denominator in all applications is a power control circuit pack for each data terminal and each data set. These CPs are used to turn on the converters which power their respective units and to monitor fuse alarm conditions.

7.05 Three additional circuit packs are provided on each bay of the basic frame. The first two (PC and TIMER) are used for power control and sequencing of the controller. The AUD ALM circuit pack on bay 0 is used to collect all major alarms both from the basic and supplementary frames. The MN ALM circuit pack on bay 1 is used to collect minor alarms and test the power converters on the frame. The entire circuit operates from +24 volts.

7.06 Each terminal and controller power control circuit pack consists of one KS-19223, L3 key, two relays, three lamps, and associated solid state logic. The KS key consists of three sets of contacts. Each position is mechanically held after that position is depressed. The key also has mechanical sequencing so that the outer positions can only be reached by first depressing the center position.

7.07 Each data set power control circuit pack consists of a toggle switch, one light-emitting diode, and associated solid state logic.

7.08 The TIMER circuit pack consists of two relays, one lamp, and associated solid state logic to control the turnon and turnoff time of the controller unit.

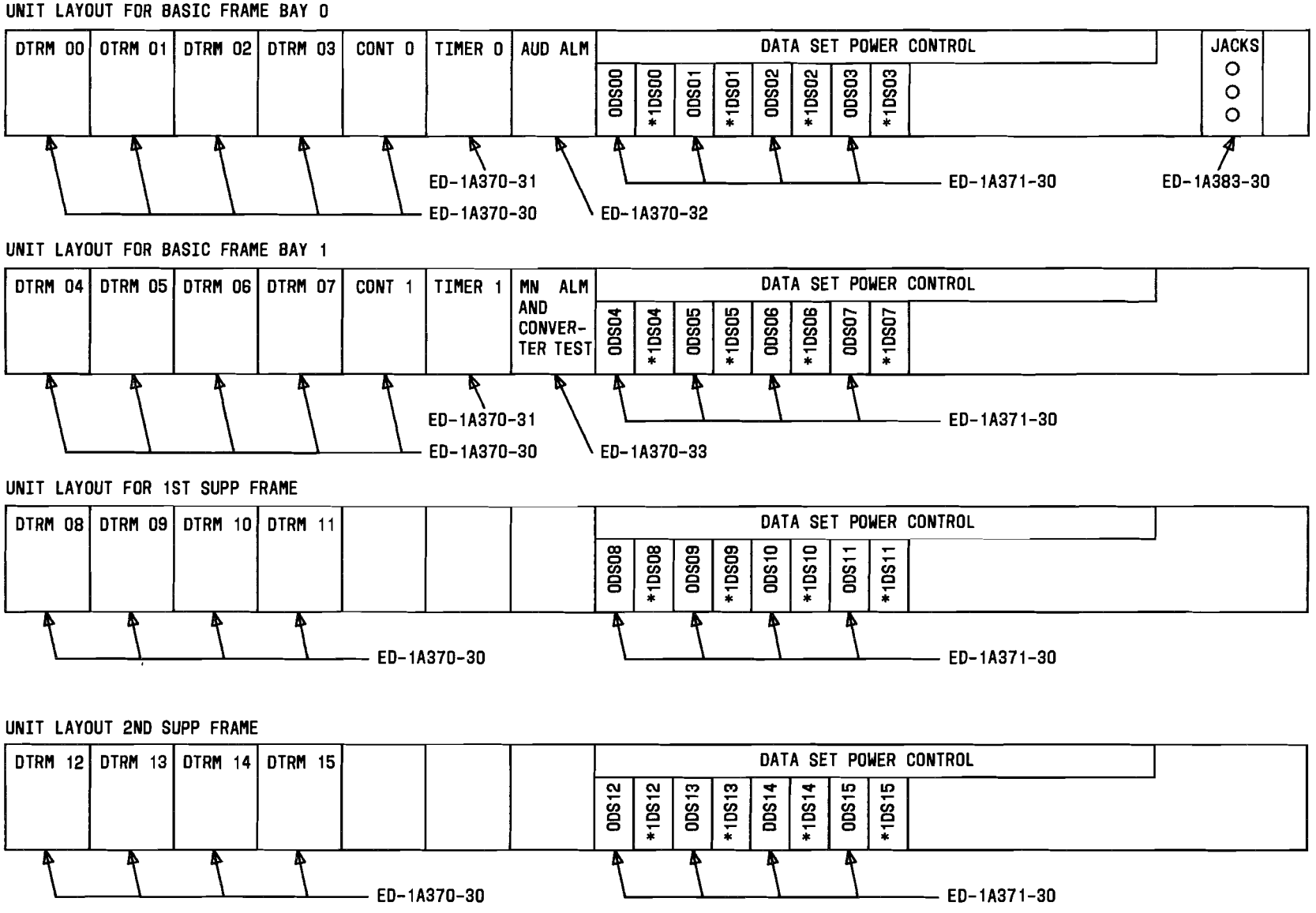
7.09 The AUD ALM circuit pack consists of one relay, two lamps, one KS-19223,L3 key, and associated solid state logic.

7.10 The MN ALM circuit pack consists of one relay, three lamps, one KS-19223,L7 key, and associated solid state logic.

C. Power Application—Data Terminal and Controller

7.11 The primary purpose of the terminal and controller power control circuit pack is to provide +24 volts to the power converters (start signal) which turn the converters on. This is accomplished through the break contact of the power relay.

7.12 When the circuit is in the off state, the power relay is energized, and the OFF NOR, OS, and PWR OFF lamps are lighted. Depressing the REQ



* DATA SET POWER CONTROLS 1DS00 THROUGH 1DS15 ARE UTILIZED IN AMPS

Fig. 13—Unit Layouts for CCIS Basic and Supplementary Frames

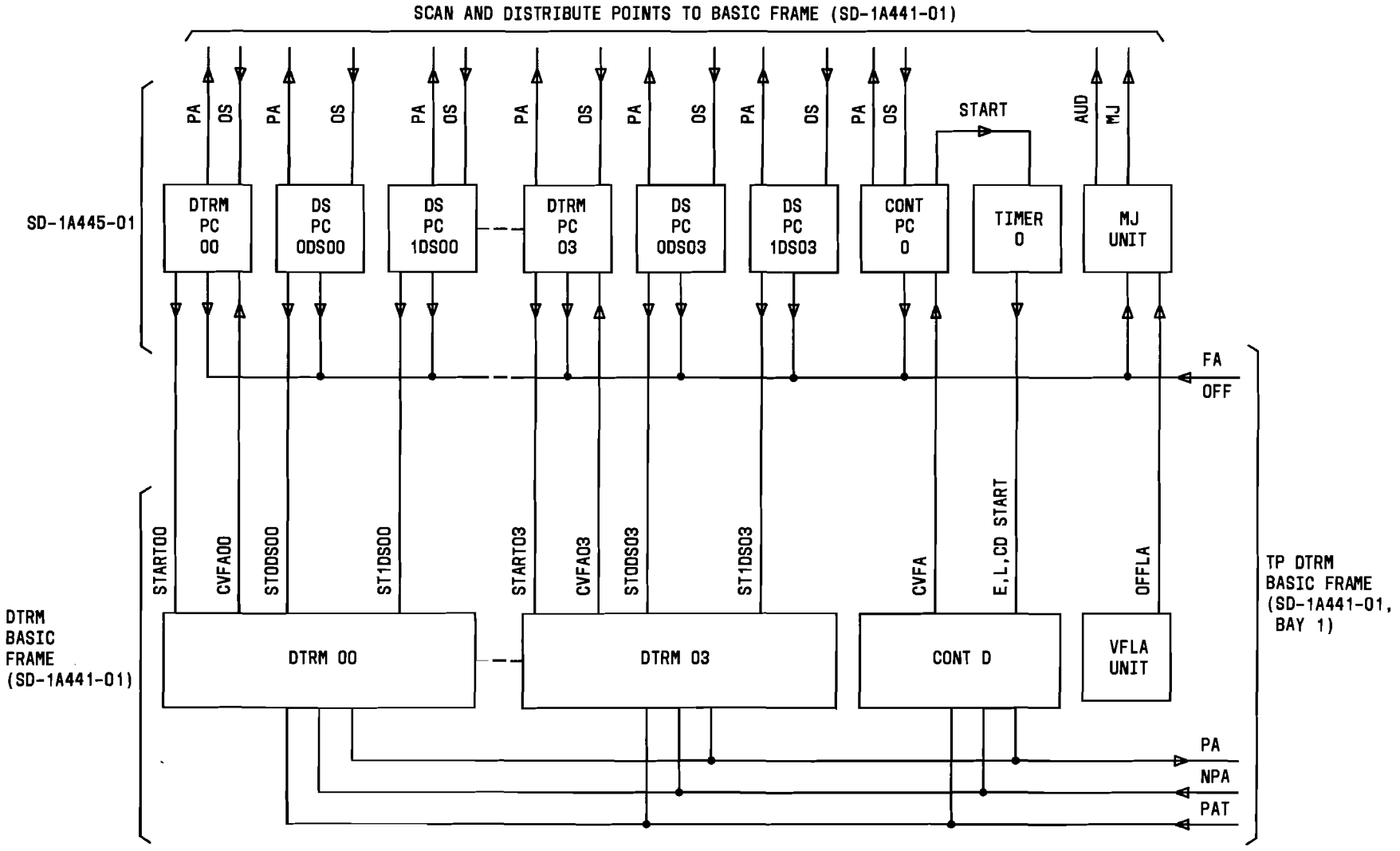


Fig. 14—Data Terminal Power Control for Basic Frame Bay 0

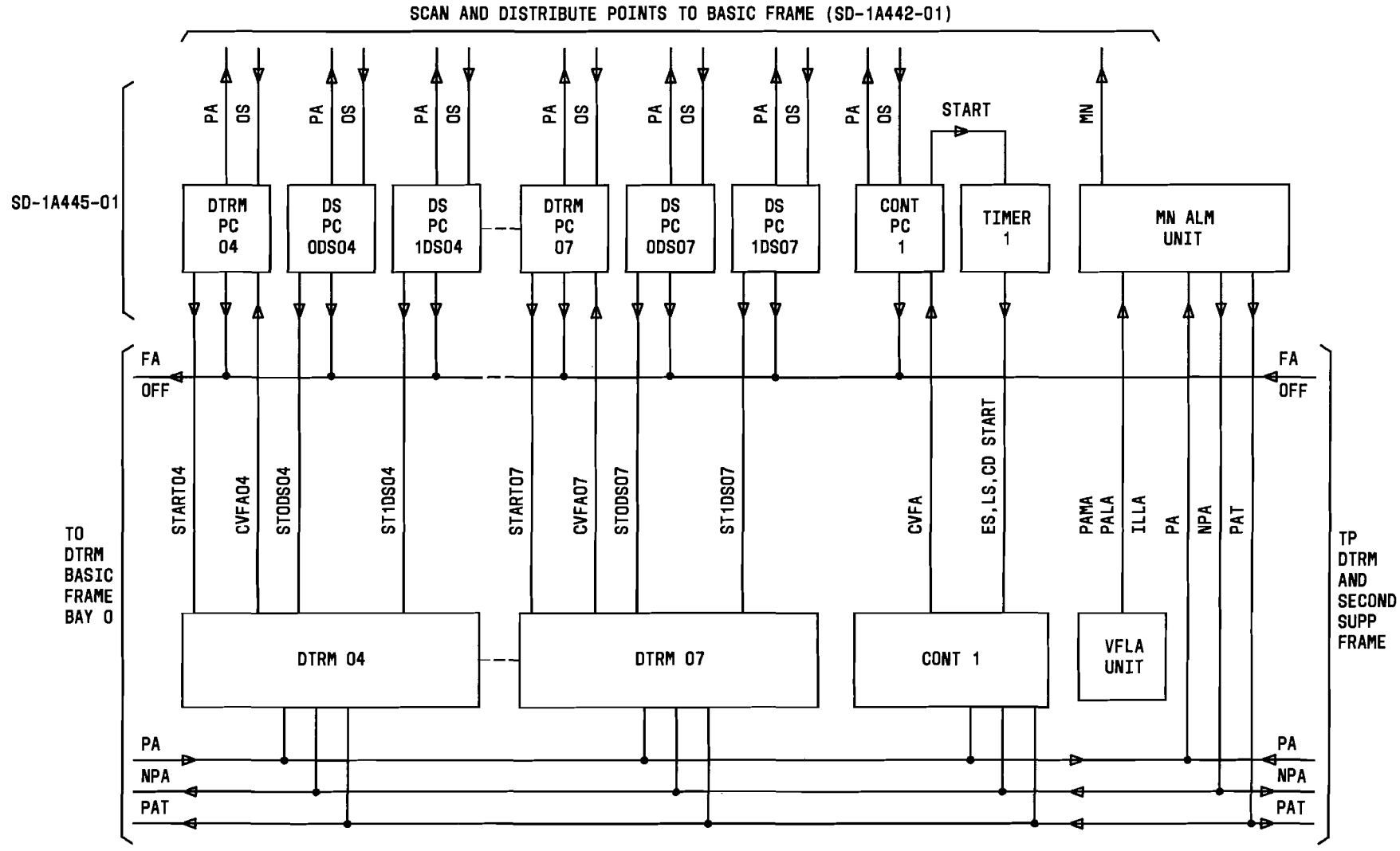


Fig. 15—Data Terminal Power Control for Basic Frame Bay 1

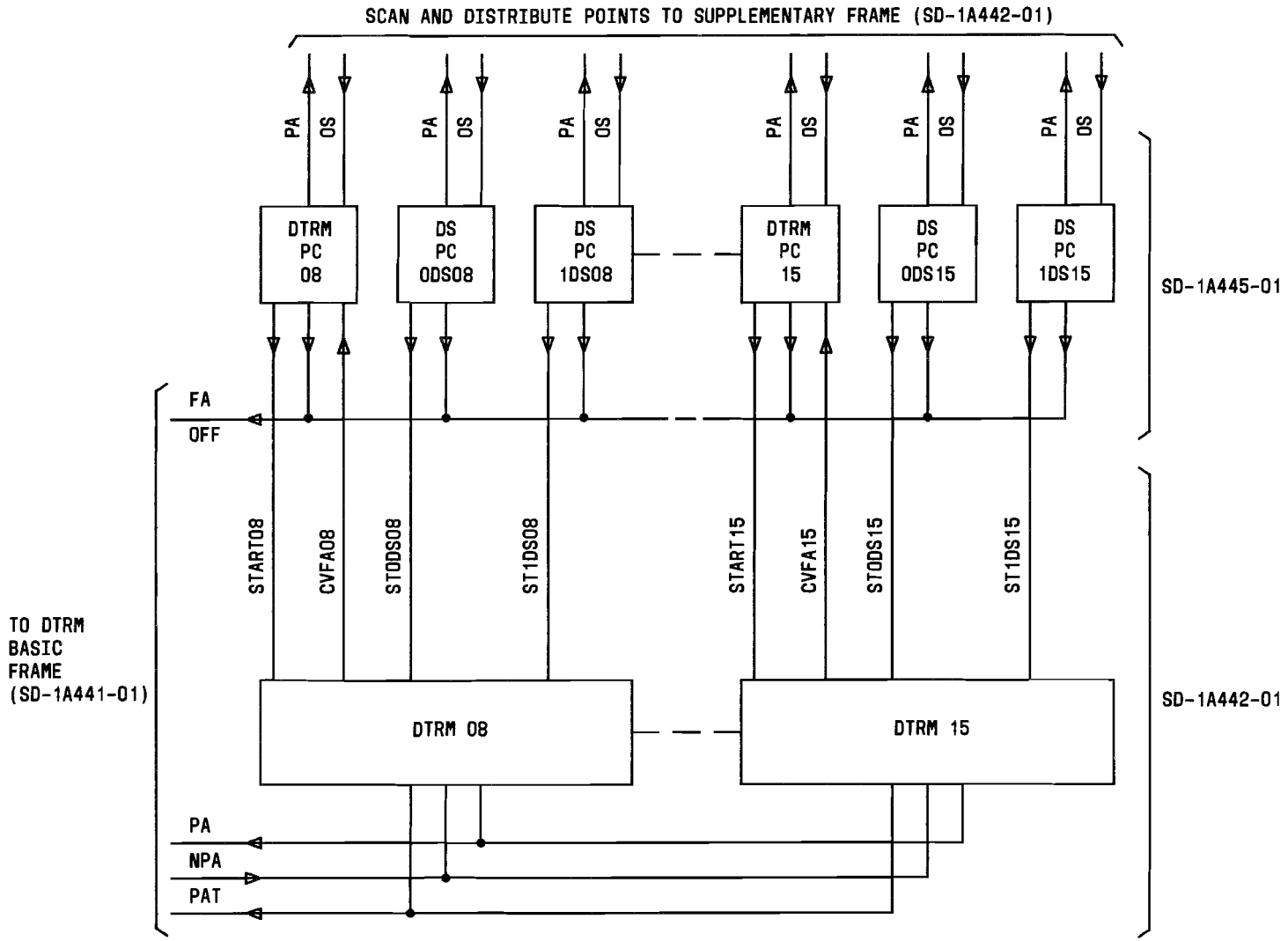


Fig. 16—Data Terminal Power Control for Supplementary Frames

INH key extinguishes the PWR OFF lamp and turns power on by dropping the power relay but does not return the unit to normal. Depressing the NOR key extinguishes the OFF NOR lamp and, via the scan point change, requests the processor to run diagnostics on the logic unit. Logic unit refers to any terminal or controller unit on the frame. If the diagnostic run is successful, the processor returns the logic unit to normal and extinguishes the out-of-service (OOS) lamp.

D. Power Removal—Data Terminal and Controller

7.13 In the normal state (ie, power on and NOR key depressed), the power and FA relays are deenergized and all lamps are off. To start the power removal sequence, the REQ INH key is depressed. This lights the OFF NOR lamp and requests the processor, via scan point changes, to take this logic unit out of service. The processor honors this request by grounding the OS lead via the signal distributor. This lights the OS lamp. Note that power has not been removed by this action. The OFF key is next depressed which removes power via the power relay. With power removed, the power relay is up and the OFF NOR, OS, and PWR OFF lamps are lighted. An OFF signal is also given to the AUD ALM circuit pack.

E. Timers

7.14 The application of 3 volts to the controller unit requires sequencing. In addition, the bus cable drivers must have 24 volts applied after the first part of the controller logic is powered. The start signal provided by the controller power control circuit pack starts charging two resistance-capacitance circuits in the timer circuit pack. The time constant of the first RC circuit is small and brings up the ES relay in about 5 milliseconds. The time constant of the second RC circuit is very large and the LS relay will operate in about 1 second.

7.15 When the start signal is removed, a diode becomes forward biased and discharges the second RC circuit. This quickly drops the LS relay. The first RC circuit slowly discharges and drops the ES relay. This time constant is set for about 1 second.

7.16 The relay will remain operated for about 1 second after the removal of the start signal. The above action provides signals which go to the controller A converter, B converter, and cable drivers. This is a first-on, last-off timer.

F. Data Set Power Control

7.17 Power to each data set is provided by the associated data set power control circuit pack. The circuit pack contains a toggle switch to apply +24 volts to the data set. Power to the data set is monitored and a scan indication is provided to the processor when power is removed or lost. In addition, an OFF indication is provided to the AUD ALM CP.

G. Scan Points

7.18 The power state of the terminal and controller is sent to the processor via the A and B scan points. Table F indicates the four possible scan states. The scanner ferrods are saturated when the circuit is in the normal state.

TABLE F

TERMINAL AND CONTROLLER POWER STATES

CONDITION	CIRCUIT STATE		LOGIC STATE	
	A	B	A	B
Normal	Closed	Closed	0	0
FA	Open	Open	1	1
Off	Open	Closed	1	0
REQ INH	Closed	Open	0	1

7.19 The data set power control circuit pack provides one scan point to the processor to indicate the power state of the data set being controlled. In NORMAL condition, the circuit state is closed and the logic state is zero (0). In the fuse alarm condition, the circuit state is open and the logic state is one (1).

7.20 The AUD ALM CP provides one scan indication to the processor to indicate that the CP is not in the NORMAL state. Depressing the NORMAL key will reset this scan point.

7.21 The MN ALARM CP provides one scan point indication to the processor to indicate a minor alarm condition exists on the data terminal frame. This scan point can be reset by removing the primary cause of the minor alarm and depressing the ALM RLS key.

H. Signal Distributor Points

7.22 The processor responds to the terminal or controller power control circuit pack by closing a signal distributor point when the REQ INH key is depressed. This lights the OOS lamp on this circuit pack as well as an OOS light emitting diode on the unit which has been taken out of service.

7.23 The send data point associated with the data set power control circuit pack is also controlled by the processor, but an OOS request for each data set must be entered via a TTY message. When this send data point is set, the lamp on the data set power control circuit pack is turned on indicating that power may now be removed. Also, this lamp will be turned on by manual data set power removal or when the data set fuse is blown.

I. Converter Alarms

7.24 The converters which power the terminal and controller units provide two types of alarms. A fuse alarm (FA) indicates that the particular converter has shut down because of an internal fault or an overvoltage or overcurrent condition. The result of this action is to drop the converter output voltage to zero, apply +24 volts on its FA lead, and light a light emitting diode on the converter. This condition can be cleared by clearing the fault and/or replacing the converter and power cycling.

7.25 One other condition can cause a 3-volt converter to shut down and give an FA alarm. This will occur if the loop resistance from converter to the 3-volt load exceeds 35 milliohms. This can be caused by cold solder joints or inadequate contact of the 3-volt distribution systems.

7.26 A power alarm condition indicates the converter output voltage is out of tolerance but not zero. Under this condition, the logic unit powered by this converter may be operational. The converter contains high- and low-voltage monitors to detect a power alarm condition and these monitors must be exercised to make sure they are operational. A power alarm condition results in lighting the light emitting diode on the converter and applying +24 volts to its power alarm lead. The complement of the power alarm lead is provided on the no-power alarm lead. The no-power alarm lead is normally high, (ie, +24 volts through a 2000-ohm resistor). The no-power alarm lead drops approximately 1 volt when a power alarm occurs. Grounding the no-power alarm lead will reset the converter light emitting diode. A power alarm test lead is also provided to permit the exercising of the converter monitors. A power alarm condition can be cleared by replacing the faulty converter and/or depressing the ALM RLS key. The power alarm features are also provided on the FB152 CP found in each terminal and controller unit. This circuit pack can be considered like a converter for power alarms.

J. Fuse Alarms

7.27 There are two categories of fuses which are used to power the data terminal frames. The first cateogry is not service affecting. These include the fuses powering the VFLA units and the power control units. A failure of any of these fuses will result only in a minor alarm. All other fuses on the frame are service affecting. The loss of any one of these fuses will result in a fuse alarm condition and an office major alarm.

7.28 When a fuse alarm condition occurs, the FA relay in the power control circuit pack sets the A and B scan points (to 1,1), energizes the power relay which removes power from the logic unit, lights the fuse alarm lamp and sounds the office major alarm via the AUD ALM circuit pack. The office major alarm can be silenced by depressing the OFF key on the AUD ALM circuit pack. The fuse alarm relay on the power control circuit pack can be energized by any of the following conditions:

(a) Blowing an associated 48-volt fuse which feeds the converters. This results in 48 volts being applied to the 48-FA lead of the power control circuit pack.

(b) Blowing an associated 24-volt alarm fuse. This results in +24 volts being applied to the 24 FA lead of the power control unit.

(c) A fuse alarm condition given by any converter which has shut down as a result of an overvoltage or overcurrent condition. This results in +24 volts being applied to the CVFA lead of the power control circuit pack.

7.29 When -48 volts is applied to the 48 FA lead, transistor Q1 cuts off. This action energizes transistor Q2 which energizes the FA relay. When +24 volts is applied to the 24 FA or CVFA lead, transis-

tor Q2 energizes which in turn energizes the FA relay.

7.30 Loss of a data set fuse will result in a major alarm by the application of +24 volts to the AUD ALM CP FA lead. The monitor on the data set power control circuit pack will sense the loss of power and set its scan point via the opto-isolator on this circuit pack.

K. Major Alarms

7.31 The AUD ALM circuit pack collects FA alarms and off indications from each logic unit. A fuse alarm condition will energize the major alarm relay which provides the office major alarm. The office major alarm can be silenced by depressing the OFF key on the AUD ALM circuit pack.

7.32 The OFF indications provided by the terminal, controller, and data set power control circuit packs (+24 volts) are used to convert the -48 volt OFF indication from the VFLA units to a +24-volt signal which in turn lights the above lamps.

L. Minor Alarms and Power Alarm Test

7.33 The MN ALM circuit pack collects all power alarm indications from all converters, FB152 circuit pack and minor fuses. In addition, this circuit pack provides a means of testing the power converters and FB152 circuit packs.

7.34 Blowing a power control fuse places +24 volts on the PAAF or PABF lead which turns on Q1, lights the PCF lamp, and sets the MN scan point. The scan point is normally closed. When Q1 turns on, the base of Q4 is pulled toward ground and turns off Q4. This action removes drive from the opto-isolator which in turn opens.

7.35 A power alarm condition from any converter or FB152 CP places +24 volts on the PAA-PAF leads. This turns on Q5, lights the CV lamp, and sets the MN scan point.

7.36 The VFLA unit can provide up to three minor alarms. Normally, when the ILLA lead is grounded, the PACA and PAMA leads are opened. Removing any VFLA CP will break a daisy chain removing the ground from the ILLA lead. This causes Q2 to turn off and Q3 to turn on; which in turn lights the LA lamp and sets the MN scan point. Blowing a VFLA fuse places -48 volts on the PALA lead turning Q2 off and Q3 on. Blowing a maintenance amplifier fuse places +24 volts on the PAMA lead turning Q3 on.

7.37 Depressing the power alarm test key on the MN ALM CP for 3 seconds tests the monitors on the FB152 CP and converters by grounding the power alarm test lead. This action does not affect the converter output voltage. All converters and all FB152 CPs on the basic frame and the two supplementary frames are tested simultaneously. A successful test will result in lighting the CV lamp, setting the MN scan point, and lighting the light-emitting diodes on all converters and all FB152 circuit packs. Any light-emitting diode which does not light indicates a faulty or marginal unit.

7.38 Depressing the ALM RLS key for 3 seconds grounds the no-power alarm lead. This action resets all light emitting diodes on the basic and two supplementary frames, extinguishes the CV lamp, and resets the MN scan point.

7.39 The no-power alarm relay is used as a slave to ground the no-power alarm leads. This relay has a larger current capacity than the ALM RLS key.

FUSE PANEL

7.40 The fuse panel in each bay of the data terminal basic frame provides dual +24 and -48 volt power buses and associated fuse holders for power distribution fuses.

FILTER UNIT

7.41 The filter units, one per 24-volt power bus and one per 48-volt power bus, contain capacitive filter circuits that filter each 24-volt and each 48-volt power feeder from the power distributing frame.

AC OUTLET

7.42 An ac outlet is located on each bay to provide 110-volt ac power.

POWER SUPPLIES

7.43 The power supplies required for the CONT and the DTRMs and their various voltages are described below.

7.44 The DTRMs require dc input power of 3VA plus or minus 1 percent, 3VB +12VA plus or

minus percent , and 24 plus or minus 10 percent ALM are supplied to the CCIS terminal by the CCIS terminal basic frame circuit. The 3-volt power is connected to separate power backplanes and the return lines are all connected to a common ground plane. The power is then distributed to two FC21 circuit packs. The 24-volt alarm power is applied to the FB152 circuit pack directly from the input connecting circuit. The 12V, 3V REG, and 3V REF are supplied by the terminal unit to the power converters. The power converters are located within the data terminal. The terminal also requires 55 watts of 3-volt power for logic and memories.

7.45 The CONT requires two 3-volt converters to supply the power required by the 3-volt logic. Power supply J87409A is a dc-to-dc converter circuit that provides a regulated nominal +3-volt ,0-to-8-ampere output from a nominal 48-volt source. Control functions of the converter receive power from a 24-volt source. Each converter feeds a portion of the backplane of the CONT. The 3-volt output of the converter is filtered by a capacitor circuit located on the FC21 circuit pack.

7.46 The 3-volt output of the converter is regulated. The regulator requires a 3.030-volt reference which is generated on the FC21 circuit pack. Reference voltage 3REFA is achieved by a resistor network that divides the regulated 12-volt reference generated on the FB152 circuit pack. In addition to generating the 3-volt reference, the circuitry on the FC21 circuit pack monitors the voltage applied to the backplane and, through a resistor, transmits this voltage to the converter as 3REGA. The regulator compares 3REFA and 3REGA and adjusts the 3-volt output that is applied to the backplane.

7.47 The converter contains test circuitry for checking the regulation limits of the converter. This test is initiated by grounding the input power alarm test lead. If the circuitry is working, this action results in a power alarm indication; ie, the signal on the power alarm lead goes high and the signal on the no-power alarm lead goes low.

7.48 If the converter shuts down because of an overvoltage or an overcurrent condition, the converter fuse alarm lead comes up.

7.49 An interlock is provided between the two converters for the CONT. This interlock prevents the powering up of only one converter. If one of the converters is not plugged in, the signal on the converter interlock lead prevents the other converter from being powered on. If one of the converters is not plugged in, the power control circuitry will bring up the fuse alarm.

8. MAINTENANCE CONSIDERATIONS

A. Link Security

8.01 ▶Link security is a module within the CCIS program concerned with CCIS data link administration and recovery. A minimum of two CCIS data links (A links) are provided per switching office. Each A link connects the switching office with one of the two signal transfer points within its direct distance dialing region. (For example, A11 and A12 from SO1 in Fig. 17.) Through translation assignment, data link pairs are formed so a link pair provides access to the CCIS signaling network via both STPs. A pair of data links has signaling capacity for up to 2250 CCIS trunks. The components of a data link pair are shown in Fig. 18.

8.02 The primary functions of link security are:

(1) Route outgoing messages from the switching office to the CCIS signaling network based on signaling network status tables.

(2) Control maintenance activity on the CCIS data links with emphasis on maintaining a viable signaling path for each CCIS trunk.

8.03 Under central control program control, a data terminal can be operated in several maintenance states, a modem can be switched between voice frequency links VFLA and VFLB, and a VFL access circuit can be used to provide maintenance access to a VFL. The A links of a pair are normally operated in a load sharing mode; that is, each link carries approximately 50 percent of the signaling load directed toward the link pair. The link pairs are engineered so a single link has enough capacity to carry all the assigned signaling load for the link pair should the other member link be removed from active service.

8.04 Five extended maintenance procedures are supported by link security:

(1) Office recovery

(2) Normal link recovery

(3) Emergency link recovery

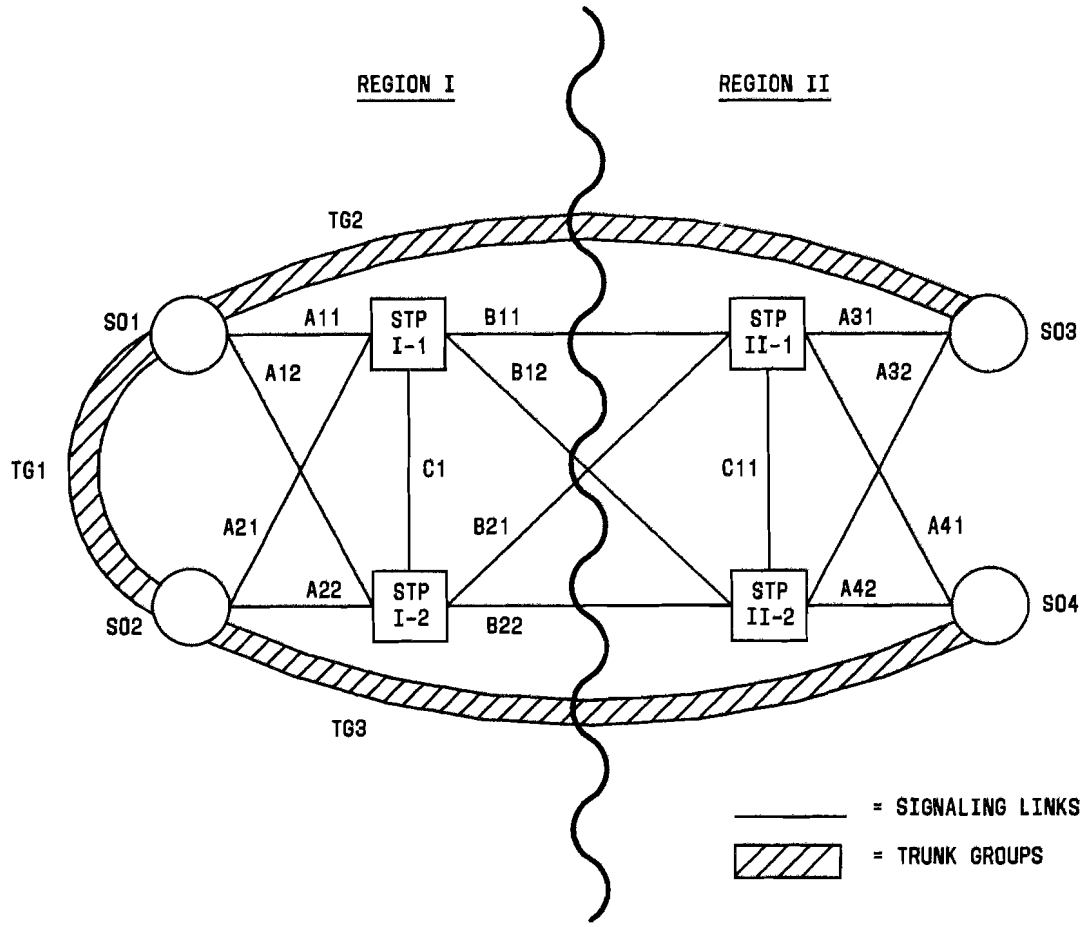


Fig. 17—Redundant CCIS Network Structure

(4) Manual link recovery

(5) Manual VFL transfer.

8.05 The office recovery procedure is automatically initiated in a switching office Phase 6 or higher; the data terminals are initialized and the data links are placed into service as quickly as possible.

8.06 The normal link recovery procedure is automatically initiated when a single link failure occurs, or when a link is released from an unavailable condition and the mate link is currently active. Before being returned to active service, the recovering link is monitored for 18 seconds to ensure acceptable transmission signaling error rates, and a CCIS signaling network status update is completed.

8.07 The emergency link recovery procedure is automatically initiated when a double link failure occurs or when a link is released from an unavailable condition and the mate link is not currently active. Before being returned to active service, the recovering link is monitored for only 3 seconds and an abbreviated restoral sequence is followed.

8.08 The manual link recovery procedure, manually initiated from either the switching office or STP, supports maintenance of the data link without normal signaling traffic.

8.09 The manual VFL transfer procedure is manually initiated from either the switching office or STP and supports changing the VFL in service between VFLA and VFLB when the link is active.

8.10 Input message DTRM-REQ- is used for manipulation of the DTRMs. Input message

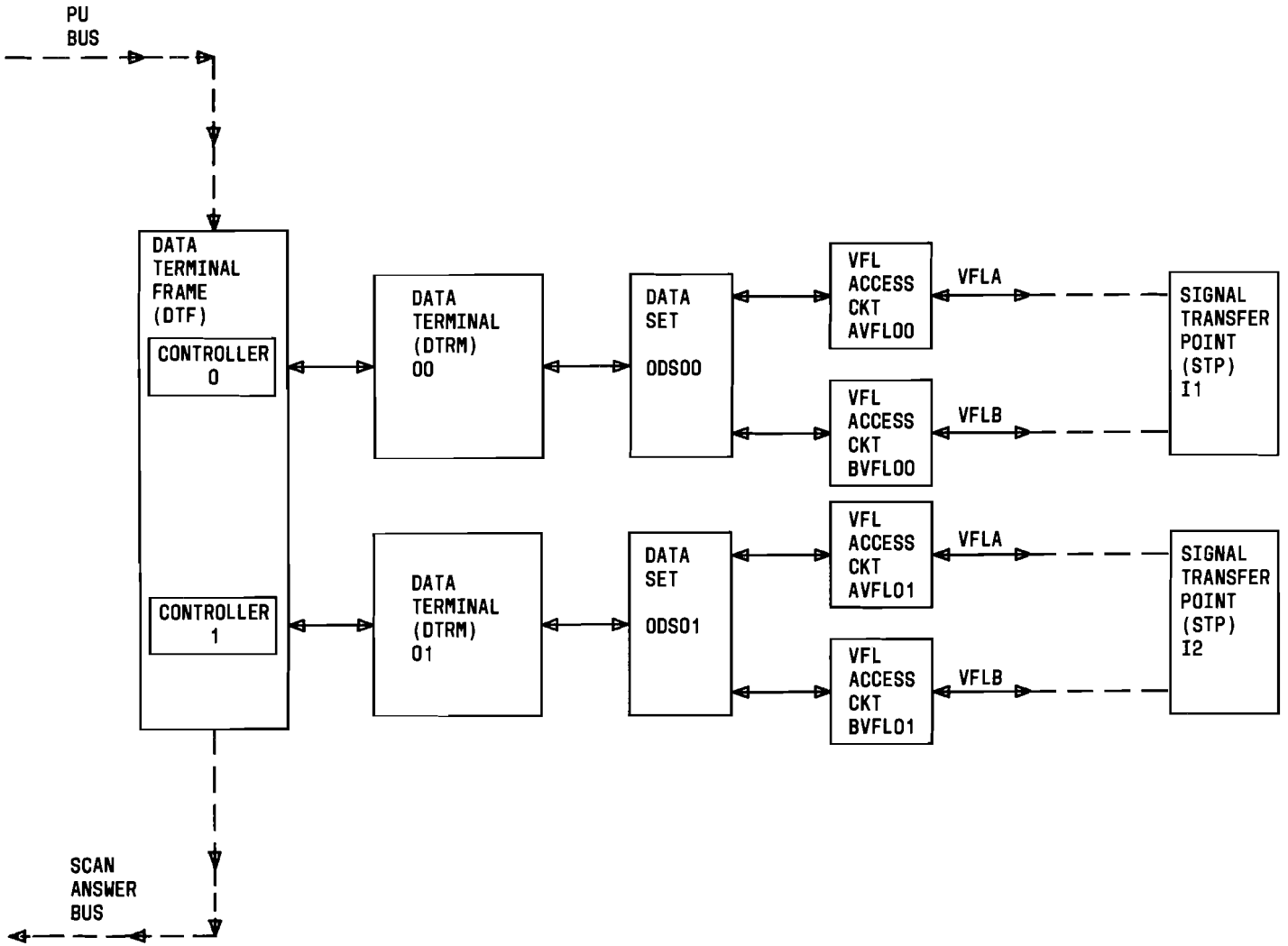


Fig. 18—CCIS Data Link (A Links)

VFLK-REQ- is used for manipulation of the modems, VFLs, and VFL access circuits.

8.11 Output message LS01 informs maintenance personnel of automatically initiated link recovery procedures, the progress of manually initiated procedures, and DTRM status changes. Output message LS02 informs maintenance personnel of high transmission error rates on active links. Output message LS03 is used to print out the contents of the link security data link status tables when requested manually. Output message LS04 is used to print out the contents of link security status and input data when a data link is reinitialized.

B. Signaling Link Maintenance Facilities

8.12 The maintenance control and coordination of the CCIS signaling network and its parts generally follow the plan currently in use in the Bell System and is commonly referred to as the control office plan. Inherent in the plan is a hierarchy of maintenance control and assignment of responsibilities that ensure orderly administration of the network. For No. 1 ESS toll CCIS, as in all toll CCIS applications, the STP has some automatic signaling link testing capabilities; however, the maintenance control office for the signaling link is the No. 1 ESS switching office.

8.13 Automatic procedures are provided to assist in recovery from data link troubles. The objectives are to sectionalize a failure to the terminal-modem combination at either end or to the interconnecting VFL without manual intervention. This permits repair and return to normal service with a minimum of human interoffice communication.

8.14 A loop-around path is provided at the ESS to allow the STP to perform VFL testing. Also, the VFL access circuit provides switched access from the switching office test panels to the VFL via a shared maintenance bus. Network access circuits (SD-1A176-2-wire or SD-1A397—HILO) are required to interface with the VFL access circuits.

8.15 Periodic testing of the standby VFLs is accomplished on a routine basis from the STP. To initiate this test, the STP sends a test-standby-VFL signal to the switching office. In response to this signal, the switching office applies a loop to the standby VFL and transmits a test-standby VFL signal to the STP. The STP then performs the test and sends the results to the switching office via a VFL test-passed signal or a VFL test-failed signal. This test can also be initiated from the switching office via TTY input. The link security routine first applies the loop and then sends a test-standby VFL signal to the STP. The STP then performs the test and returns the result.◀

9. DATA TERMINAL AND VOICE-FREQUENCY LINK STATE DESCRIPTIONS

9.01 ▶The following paragraphs describe the various maintenance states which can be established within the DTRM and/or VFL either under system control (automatically) or via TTY messages (manually).

DATA TERMINAL STATES

9.02 The DTRM may exist in one of five automatically initiated states (including the ACTIVE state) or one of four manually initiated states, as shown in Fig. 19. A summary of these states is given in Table G. These states may be determined via the maintenance TTY by using the DTRM-REQ-STS input message (see paragraph 12.09) to obtain an LS01 STATUS output message which gives the current DTRM maintenance state. A detailed explanation of each of these states is as follows. See Fig. 20 through 23 for state diagrams.

A. Automatic (AUTO) States

9.03 ***Active:*** The DTRM carries normal traffic. The mate DTRM may be either ACTIVE or in one of the other maintenance states.

9.04 ***AUTO OOS Fault:*** The DTRM failed an automatic (system requested) diagnostic. This state occurs when the system automatically removes a DTRM from the ACTIVE state and attempts a diagnostic which either fails or aborts. Once the system is in this state, if a manually requested diagnostic occurs and passes, the DTRM will be placed into the AUTO OOS REMOVE state from which normal link recovery will be initiated. If the diagnostic fails or aborts, the DTRM will return to the AUTO OOS FAULT state.

9.05 ***AUTO OOS Remove:*** This state occurs when the system automatically removes a DTRM from the ACTIVE state, as when a single or double link failure occurs. Also, if the DTRM has been manually removed from the ACTIVE state and

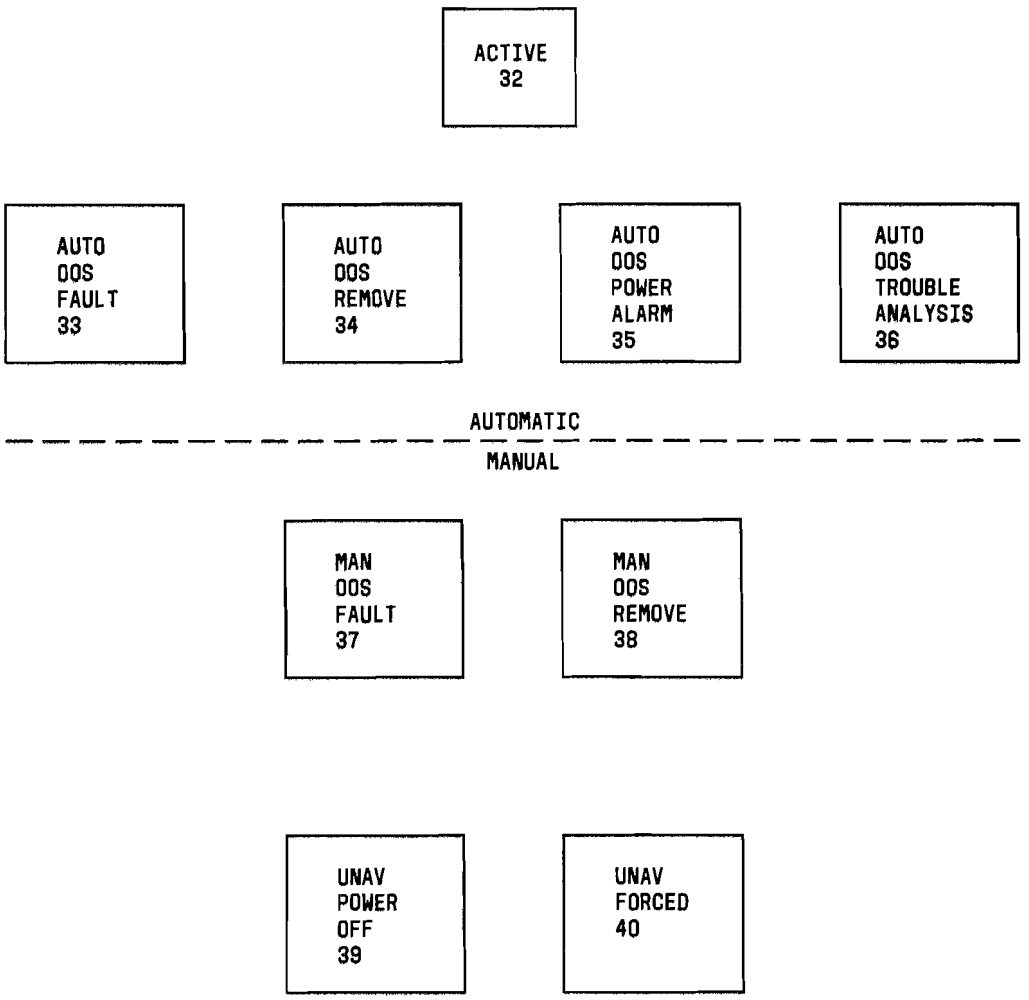


Fig. 19—DTRM States

a subsequent restoral is requested, it must first go through the AUTO OOS REMOVE state to allow restoral to the ACTIVE state via normal link recovery.

9.06 ***AUTO OOS Power Alarm:*** This state is reported automatically via the LS01 output message when a fuse alarm occurs on the DTRM. This state can be initiated from any automatic DTRM maintenance state.

9.07 ***AUTO OOS Trouble Analysis:*** The DTRM is placed in this state when an automatic diagnostic request is initiated. If the diagnostic passes, the DTRM is returned to the AUTO OOS REMOVE state; if the diagnostic fails, the DTRM is placed into the AUTO OOS FAULT state.

B. Manual (MAN) States

9.08 ***MAN OOS Fault:*** In this state, the DTRM has been manually removed from the ACTIVE state and is not operating but is available if the mate DTRM fails. To reach this state from ACTIVE, the DTRM must first be placed in the MAN OOS REMOVE state (explained in paragraph 9.09). To be restored to ACTIVE from this state, the DTRM must go through the AUTO OOS REMOVE state. From this point, the DTRM is restored to ACTIVE via normal link recovery.

9.09 ***MAN OOS Remove:*** In this state, the DTRM has been manually removed from the ACTIVE state and is operating for maintenance only, but is available if the mate DTRM fails. This state

TABLE G

DATA TERMINAL STATES

T/M STATE NUMBER	NAME	DESCRIPTION
32	Active	Carrying normal traffic
33	AUTO OOS FAULT	Failed diagnostic (automatic request)
34	AUTO OOS REMOVE	Performing automatic link recovery
35	AUTO OOS POWER ALARM	Fuse alarm
36	AUTO OOS TROUBLE ANALYSIS	Diagnostic request (automatic)
37	MANUAL OOS FAULT	Not operating; but available if mate DTRM fails
38	MANUAL OOS REMOVE	Operating for maintenance only, but available if mate DTRM fails
39	UNAVAILABLE POWER OFF	Power off
40	UNAVAILABLE FORCED	Not operating; ***not*** available if mate DTRM fails

can be reached directly from the ACTIVE mode; however, to return to the ACTIVE mode from this state, the DTRM must go through the AUTO OOS REMOVE state and be restored via normal link recovery.

9.10 ***Unavailable Power Off:*** In this state, the power has been removed from the DTRM for major maintenance or other purposes. The DTRM is not available if the mate DTRM fails. From this state, the DTRM may be placed in any of the other manual states, and, as before, the DTRM must go through the AUTO OOS REMOVE state before being restored to the ACTIVE state.

9.11 ***Unavailable Forced:*** In this state, the DTRM is not operating and is not available if the mate DTRM fails. This state is useful for maintenance functions which require power and also the assurance that the system will not attempt to place the DTRM into ACTIVE service. As for all previous manual states, it must go through the AUTO OOS REMOVE state before it can be placed in ACTIVE service via normal link recovery.

VOICE FREQUENCY LINK STATES

9.12 There are two VFLs (designated VFLA and VFLB) associated with each DTRM of a DTRM pair. Only one of these VFLs is in service at any time. Interface from the DTRM to both VFLs is accomplished through a data set to which two VFL access circuits are connected. Each VFL access circuit corresponds to a VFL (a or b). To assure a viable signaling path and to provide some automatic maintenance functions, there are several automatic maintenance states and modem/VFL access, circuit/VFL configurations that can be initiated by the system. For maintenance purposes, there are several manually initiated states which can be initiated via the VFLK-REQ-input message. The current status of the VFL, VFL access circuit, and modem may be determined by using the VFLK-REQ-STS input message to obtain an LS01 STATUS output message which gives status information. An explanation of each of the states is as follows (see Fig. 24 and 25 for VFL state diagrams). A summary of the VFL states is given in Table H.

A. Automatic States

9.13 ***ACTIVE:*** In this state, the VFL marked ACTIVE is carrying normal signaling traffic. The mate VFL is in one of the other possible states.

9.14 ***STBY/RDY (STANDBY/READY):*** The VFL identified as being in this state is not carrying call traffic but is connected to the DTRM. This

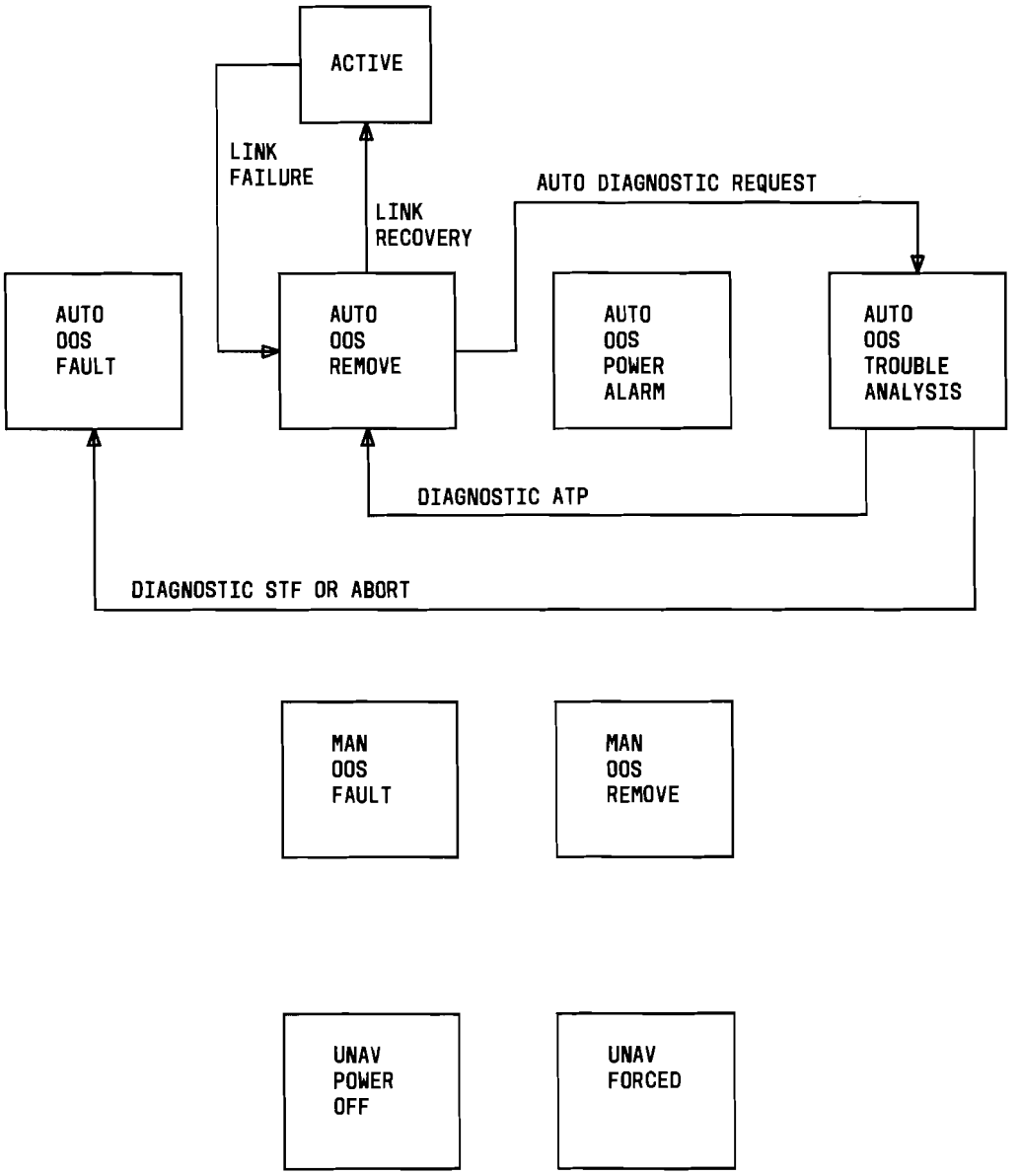


Fig. 20—Automatic DTRM State Transitions, Normal Link Recovery

is the state which a normal nonactive VFL would occupy. The nonactive VFL may be put directly into the ACTIVE state from this state via normal link restoral. Also, to be placed in the ACTIVE state from any other state, a VFL must pass through the STBY/RDY state.

9.15 ***STBY/DLY (STANDBY/DELAYED):*** The VFL identified as being in this state is not carrying call traffic and not connected to the DTRM.

B. Manual States

9.16 ***UNV/REL (UNAVAILABLE/RELEASED):*** The VFL identified as being in this state is not available for service and has its VFL access circuit released. This state is used during the manual test panel transmission test to take down the connection from the VFL to a trunk link network appearance and is initiated by the VFLK-REQ-REL input message.

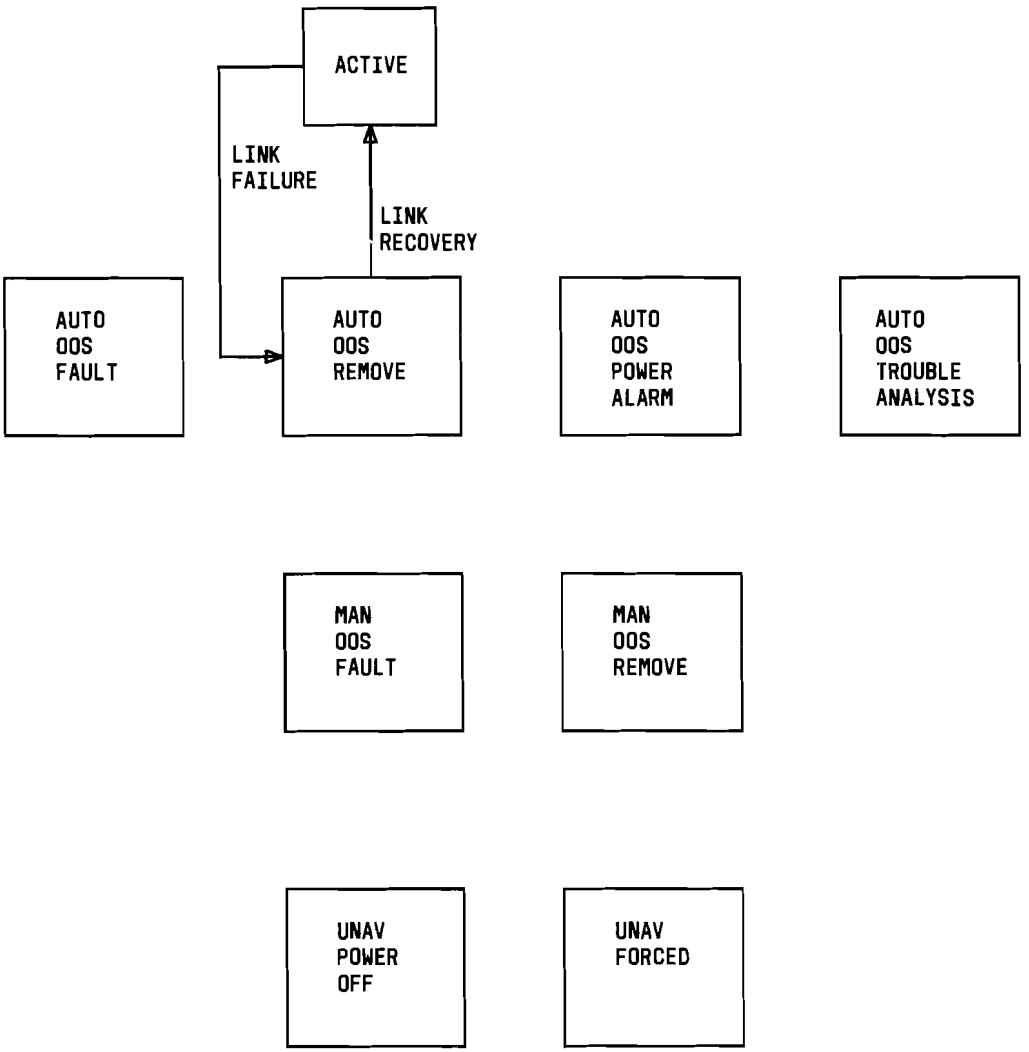


Fig. 21—Automatic DTRM State Transitions, Double Link Failure (Emergency Restart)

9.17 ***UNV/OPR (UNAVAILABLE/ OPERATED):*** The VFL identified as being in this state is not available for service and has its VFL access circuit operated. This state is used during the manual test panel transmission test to set up a connection from the VFL to a trunk link network appearance and is initiated by the VFLK-REQ-OPR input message.

10. DATA LINK FAILURE REPORTING AND ANALYSIS

10.01 The primary method for reporting failures of the CCIS data link is via TTY output messages. The LS01, 2, 3, and 4 messages are used to report the status of both automatic and manually initiated procedures and configuration changes. These messages are described in the following paragraphs.

Note: For a detailed explanation of the following message formats and associated data fields, see IM-1A001.

LS01 OUTPUT MESSAGE

10.02 The LS01 output message prints the current status and configuration of a CCIS DTRM

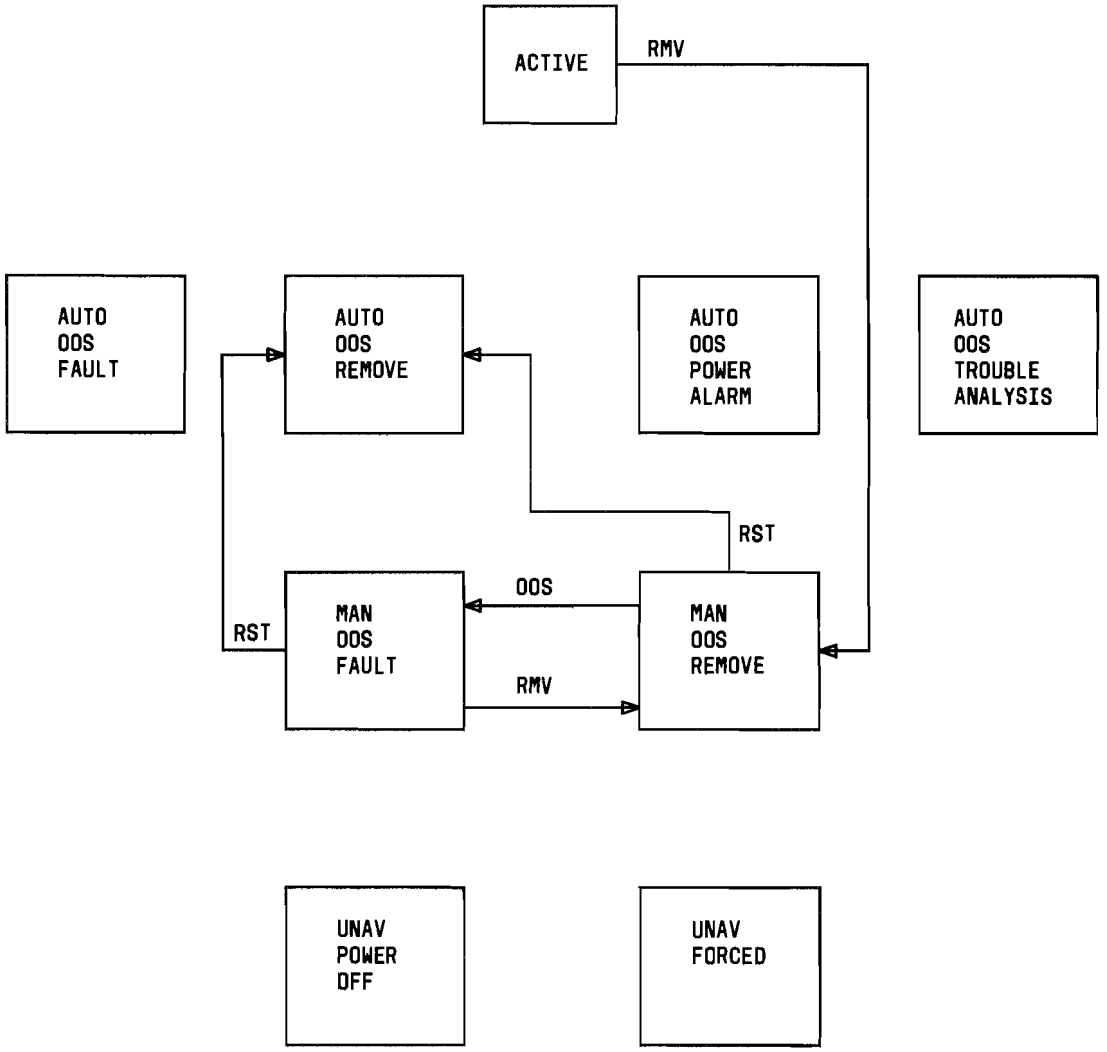


Fig. 22—Manual DTRM State Transitions

and its associated voice frequency links (VFLA and VFLB). It is printed in response to a significant manual or automatic status and/or configuration change. It is also printed in response to the DTRM-REQ-STS input message.

10.03 The following information is provided in the LS01 printout:

- Terminal pair to which the DTRM is assigned
- Member of terminal pair to which DTRM is assigned
- DTRM type indicator
- Member number of DTRM
- Which VFL (a or b) is connected through to the DTRM
- Data link maintenance procedure currently being performed or last procedure performed
- Which end of the data link is in control of the maintenance procedure being performed

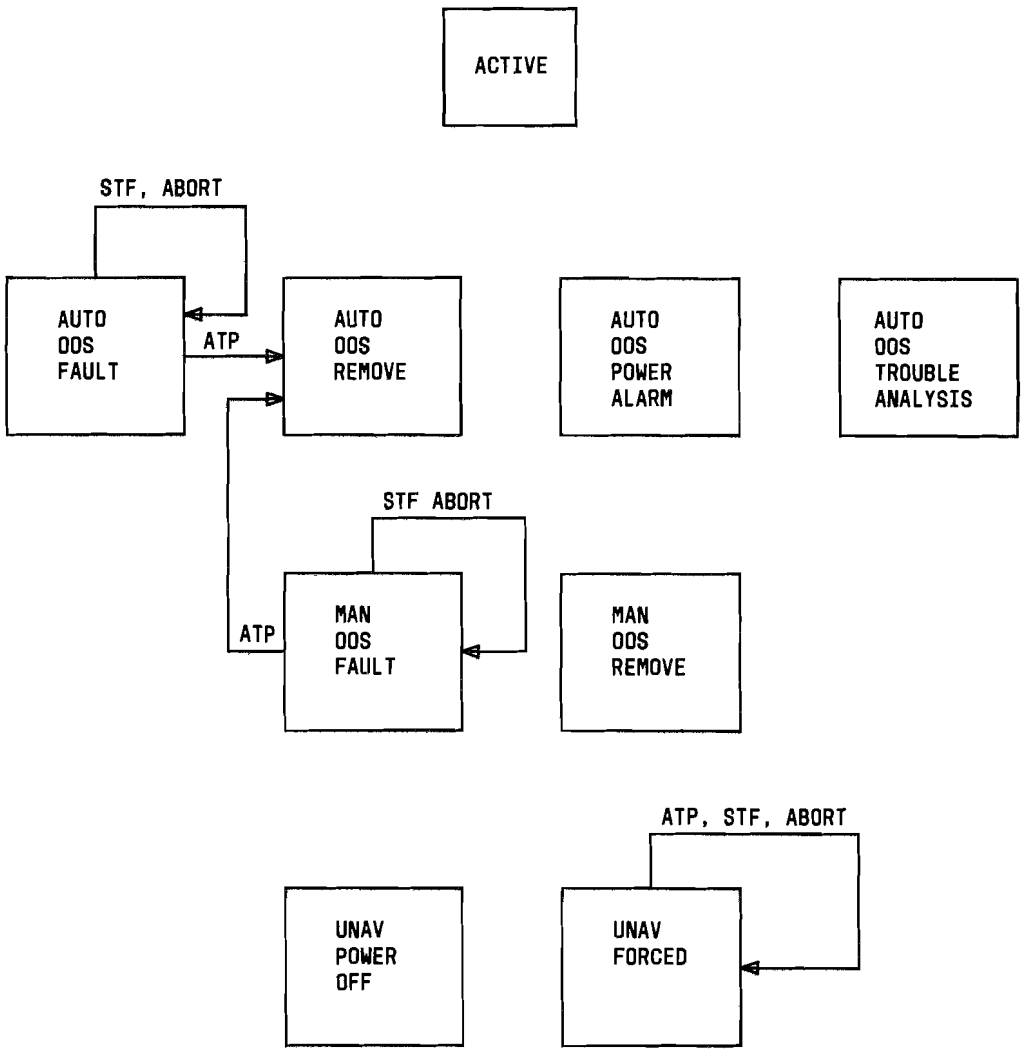


Fig. 23—Manually Requested DTRM Diagnostics

- Disposition of maintenance procedure(ie, pass, fail, in-progress, completed, etc)
- Sequence number of message
- DTRM/MODEM maintenance state
- Last processor notification processed
- VFL maintenance state
- VFL to DTRM connection indicator
- VFL transmission test status
- Whether or not VFL is in synchronization
- Whether or not VFL test relay is operated.

10.04 Using the information provided by the LS01 printout, it is possible to identify the data link in trouble. All data links should be placed in the ACTIVE state as soon as possible. Any data links out of service should be repaired and rediagnosed.

LS02 OUTPUT MESSAGE

10.05 The LS02 output message is printed each quarter hour when data link errors exceed a predetermined warning level, but are not high

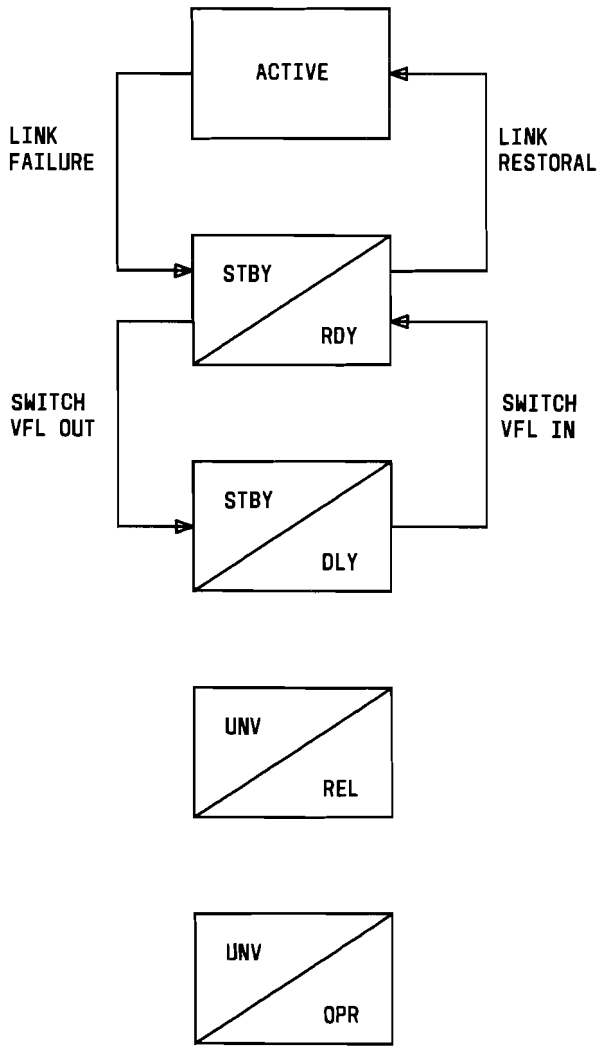


Fig. 24—Automatic VFL State Transitions

enough to cause automatic removal of the link from service.

10.06 The following information is provided in the LS02 printout.

- Terminal pair to which the DTRM is assigned
- Member of terminal pair to which the DTRM is assigned
- DTRM type indication
- Member number of DTRM
- Which VFL (a or b) is connected through to the DTRM
- Number of SUs received in error
- Number of received repeated acknowledgment control units
- Number of received skipped acknowledgment control units.

10.07 Based on the information provided by the LS02 printout, appropriate action may be taken. High error rates may indicate impending data link failure. High counts of SUs received in error and/or retransmission requests received indicate transmission problems. High counts of received repeated acknowledgment control units and/or received skipped acknowledgment control units indicate near-end and far-end modem clocks are not synchronized.

LS03 OUTPUT MESSAGE

10.08 The LS03 output message is printed in response to the DTRM-REQ-AUD input message. The printout shows those DTRM, VFL, and band status indicators that are currently being used to perform the CCIS data link I/O function in addition to data link maintenance control.

10.09 The data contained in the LS03 printout may be used to provide additional status information if the LS01 printout is not sufficient.

LS04 OUTPUT MESSAGE

10.10 The LS04 output message is printed whenever the CCIS link security bootstrap routine is entered. This can occur via an internal program request or manual request using the DTRM-REQ-FRC input message. The printout shows all the status information and current input data for the DTRM being bootstrapped before all software and hardware for that DTRM is reinitialized.

11. DTRM STATE CONTROL

11.01 Control of the DTRM maintenance states is accomplished automatically or manually. Automatic state control is initiated entirely by the system, without human intervention, based on the results of automatic transmission tests and status

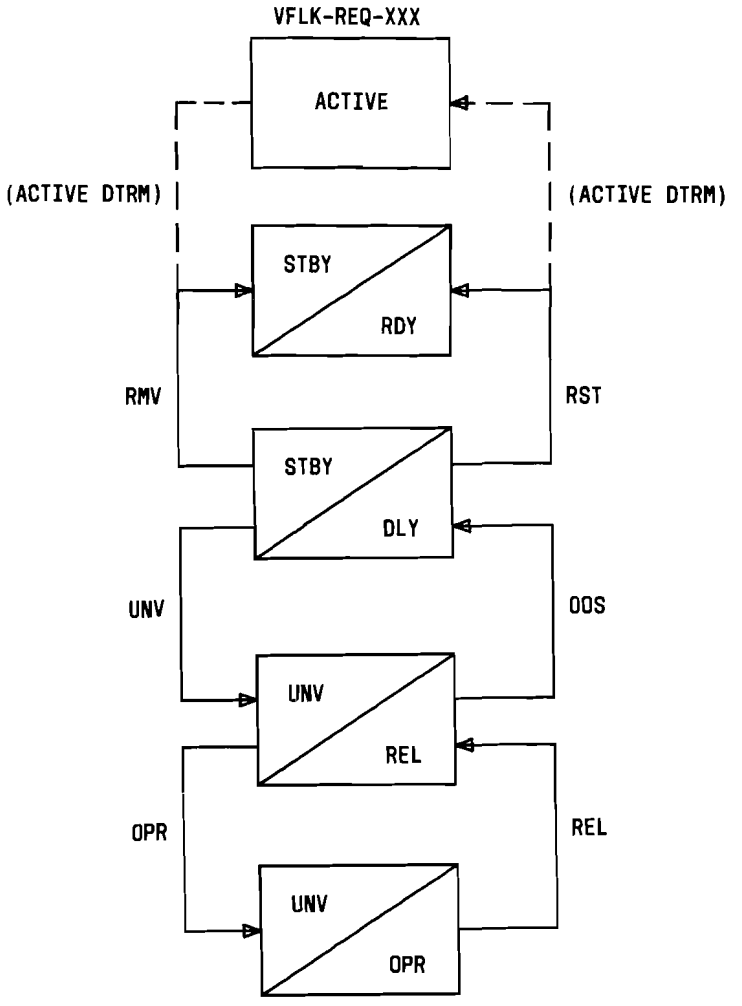


Fig. 25—Manual VFL State Transitions

TABLE H

VOICE FREQUENCY LINK (VFL) STATES

STATE	VFL FUNCTION
ACTIVE	Carrying call traffic
STBY/RDY	Standby: ***Not*** carrying call traffic
	Ready: Connected to DTRM
STBY/DLY	Standby: ***Not*** carrying call traffic
	Delay: ***Not*** connected to DTRM
UNV/REL	Unavailable: ***Not*** available for service
	Released: VFL access circuit ***released***
UNV/OPR	Unavailable: Not available for service
	Operated: VFL access circuit ***operated***

checks. Manual state control is initiated via teletypewriter input messages, frame controls, or maintenance data link messages, when configurations must be established for maintenance purposes. Table I shows the DTRM state transitions that are allowed (from one state to another).

AUTOMATIC DTRM STATE TRANSITIONS

A. Normal Link Recovery

Note: Refer to the state diagram in Fig. 20.

11.02 The normal link recovery procedure is initiated when a single link failure occurs or when a link is released from an unavailable condition and the mate link is currently active. The DTRM must always enter the AUTO OOS REMOVE state before being restored to active service. This allows the recovering link to be monitored for 18 seconds to insure acceptable transmission quality and allows a CCIS signaling network status update to be completed.

11.03 If transmission quality is found to be unacceptable for 3 minutes, the DTRM is automatically placed in the AUTO OOS TROUBLE ANALYSIS state and a diagnostic is initiated. If an all-test-pass occurs, the DTRM is returned to the AUTO OOS REMOVE state, from which the normal link recovery routine will attempt to restore it to the ACTIVE state.

11.04 If the automatically initiated diagnostic has some-tests-failing or aborts, the DTRM is placed in the AUTO OOS FAULT state. In this state, the DTRM is marked unavailable for service and manual troubleshooting procedures should be initiated as soon as possible. Manually initiated diagnostics can be run from this state. (See paragraph 11.16.)

11.05 Any automatically initiated link recovery procedures are reported on the maintenance teletypewriter via the LS01 output message.

B. Emergency Link Recovery

Note: Refer to the state diagram in Fig. 21.

11.06 The emergency link recovery procedure is automatically initiated when a double link failure occurs or when a link is released from an unavailable condition and the mate link is not currently active. The DTRM enters the AUTO OOS REMOVE state and, before being restored to ACTIVE service, the recovering link is monitored for only 3 seconds and an abbreviated restoral sequence is followed.

11.07 As for normal link recovery, emergency link recovery procedures are reported via the LS01 output message.

MANUAL DTRM STATE TRANSITIONS

Note: Refer to the state diagram in Fig. 22.

11.08 Manual control of the DTRM maintenance states is accomplished via the maintenance teletypewriter using the DTRM-REQ-XXXX input message. These messages allow maintenance personnel to establish various maintenance states or request some action to be taken on the DTRMs. The use of this message is described in the following paragraphs.

A. Removing a DTRM from Service

11.09 To manually remove a DTRM from ACTIVE service, type in:

DTRM-REQ-RMV bbbb.

bbbb = Decimal number between 0 and 1023 identifying the DTRM.

System responds with PF followed by an LS01 output message indicating the request has been implemented. The DTRM is now in the MAN OOS REMOVE state (T/M state 38) and operating for maintenance-only but is available if the mate DTRM fails.

11.10 If the problem is solved, the DTRM may be restored to ACTIVE service, using the DTRM-REQ-RST input message. (See paragraph 11.11.) If the problem is of such a nature that manually requested diagnostics are required to obtain further information, the DTRM must first be placed in the MAN OOS FAULT state using the DTRM-REQ-OOS message. (See paragraph 11.12.)

B. Restoring a DTRM to Service

11.11 To manually restore a DTRM to service, type in:

DTRM-REQ-RST bbbb.

bbbb = Decimal number between 0 and 1023 identifying the DTRM to be restored to service.

TABLE I

DTRM STATE TRANSITIONS ALLOWABLE OR NOT ALLOWED

FROM T/M STATE NO.	TO T/M STATE NO.	ACTIONS OR EVENTS CAUSING STATE CHANGE
32	32	Don't Care
	33	Not allowed
	34	Automatically initiated if single link failure or if DTRM inaccessible
	35	Blown fuse
	36	Automatically initiated if single link failure
	37	Not allowed
	38	Initiated by ***DTRM-REQ-RMV*** input message
	39	DTRM should be in one of OOS states before power removed
	40	Initiated by ***DTRM-REQ-UNV*** input message
33	32	Not allowed
	33	Don't care
	34	Automatic if diagnostic is ATP or initiated by ***DTRM-REQ-RST*** input message
	35	Blown fuse
	36	Not allowed
	37	Initiated by ***DTRM-REQ-OOS*** input message
	38	Initiated by ***DTRM-REQ-RMV*** input message
	39	Power manually removed
	40	Initiated by ***DTRM-REQ-UNV*** input message
34	32	Automatically initiated by link recovery routine
	33	Not allowed
	34	Don't care
	35	Blown fuse
	36	Automatically initiated by link recovery routine
	37	Initiated by ***DTRM-REQ-OOS*** input message
	38	Not allowed
	39	Power manually removed
	40	Initiated by ***DTRM-REQ-UNV*** input message
35	32	Not allowed
	33	Not allowed
	34	Automatically initiated if single link failure or if DTRM inaccessible
	35	Don't care
	36	Not allowed
	37	Initiated by ***DTRM-REQ-OOS*** input message
	38	Initiated by ***DTRM-REQ-RMV*** input message
	39	Power manually removed
	40	Initiated by ***DTRM-REQ-UNV*** input message

TABLE I (Contd)

DTRM STATE TRANSITIONS ALLOWABLE OR NOT ALLOWED

FROM T/M STATE NO.	TO T/M STATE NO.	ACTIONS OR EVENTS CAUSING STATE CHANGE
36	32	Not allowed
	33	Initiated automatically if diagnostics aborts or results in STF
	34	Automatic if diagnostics is ATP or initiated by ***DTRM-REQ-RST*** input message
	35	Blown fuse
	36	Don't care
	37	Initiated by ***DTRM-REQ-OOS*** input message
	38	Initiated by ***DTRM-REQ-RMV*** input message
	39	Power manually removed
	40	Initiated by ***DTRM-REQ-UNV*** input message
37	32	Not allowed
	33	Not allowed
	34	Automatic if diagnostics is ATP or initiated by ***DTRM-REQ-RST*** input message
	35	Not allowed
	36	Not allowed
	37	Don't care
	38	Initiated by ***DTRM-REQ-RMV*** input message
	39	Power manually removed
	40	Initiated by ***DTRM-REQ-UNV*** input message
38	32	Not allowed
	33	Not allowed
	34	Automatic if diagnostics is ATP
	35	Not allowed
	36	Not allowed
	37	Initiated by ***DTRM-REQ-OOS*** input message
	38	Don't care
	39	Power manually removed
	40	Initiated by ***DTRM-REQ-UNV*** input message
39	32	Not allowed
	33	Not allowed
	34	Automatic if diagnostics is ATP or initiated by ***DTRM-REQ-RST*** input message
	35	Not allowed
	36	Power manually restored; diagnostics automatically initiated
	37	Initiated by ***DTRM-REQ-OOS*** input message
	38	Initiated by ***DTRM-REQ-RMV*** input message
	39	Don't care
	40	Initiated by ***DTRM-REQ-UNV*** input message

▶TABLE I◀ (Contd)

DTRM STATE TRANSITIONS ALLOWABLE OR NOT ALLOWED

FROM T/M STATE NO.	TO T/M STATE NO.	ACTIONS OR EVENTS CAUSING STATE CHANGE
40	32	Not allowed
	33	Not allowed
	34	Initiated by ***DTRM-REQ-RST*** input message
	35	Not allowed
	36	Not allowed
	37	Initiated by ***DTRM-REQ-OOS*** input message
	38	Initiated by ***DTRM-REQ-RMV*** input message
	39	Not allowed
	40	Don't care

System responds with PF followed by an LS01 output message indicating the request has been implemented. The DTRM is placed in the AUTO OOS REMOVE (T/M state 34) from which the automatic link recovery routine will attempt to restore the unit to the ACTIVE state.

C. Taking a DTRM Out of Service

11.12 To take a unit out of service, type in:

DTRM-REQ-OOS bbbb.

bbbb = Decimal number from 0 through 1023 identifying the DTRM to be taken out of service.

This request is not honored on an active terminal. The system responds with PF followed by an LS01 output message indicating the request has been implemented. The DTRM is now in the MAN OOS FAULT state (T/M state 37). In this state, the DTRM is not operating but is available if the mate DTRM fails. Diagnostics may be run using the DTRM-REQ-DGN (paragraph 11.16) or DTRM-REQ-DGR (paragraph 11.17) input messages.

11.13 The DTRM may be restored to ACTIVE service from this state by using the DTRM-REQ-RST message as explained in paragraph 11.11. If additional maintenance is required with the DTRM operational but not carrying normal call traffic, the DTRM may be returned to the MAN OOS REMOVE state by using the DTRM-REQ-RMV input message as explained in paragraph 11.09.

D. Marking a DTRM Unavailable for Service

11.14 If major maintenance is required, a DTRM may be marked unavailable for service by typing in:

DTRM-REQ-UNV bbbb.

bbbb = Decimal number from 0 to 1023 identifying the DTRM to be marked unavailable for service.

System responds with PF followed by an LS01 output message indicating the request has been implemented. The DTRM is now in the UNAV FORCED state (T/M state 40). In this state, the DTRM is not operating and not available if the mate DTRM fails. This state is useful for major maintenance requiring power on the unit but assurance that the system will not attempt to place the unit into service.

E. Reinitializing a DTRM

11.15 If a DTRM must be fully reinitialized, type in:

DTRM-REQ-FRC bbbb.

bbbb = Decimal number between 0 and 1023 identifying the DTRM to be forced active.

System responds with an LS04 output message showing all the status information and current input data for the DTRM being forced before all software and hardware for that DTRM is reinitialized. An LS01

message is also printed indicating when the initialization is completed. Repeated LS04 messages may indicate software problems.

MANUAL DTRM DIAGNOSTICS, STATUS CHECKS AND AUDITS

Note: See Fig. 23 for a diagram indicating from which maintenance states diagnostic results will be meaningful.

A. Diagnosing a DTRM (Normal Printout)

11.16 To diagnose a DTRM and obtain a normal printout, type in:

DTRM-REQ-DGN bbbb.

bbbb = Decimal number between 0 and 1023 identifying the DTRM to be diagnosed.

System responds with a DR01 output message containing diagnostic results for the DTRM. No trouble numbers will be printed if all tests pass is printed; otherwise, use the printed trouble numbers to access the appropriate trouble locating manual section and follow the procedure indicated.

B. Diagnosing a DTRM (Raw Data Printout)

11.17 To diagnose a DTRM and obtain a raw data printout of the diagnostic results, type in:

DTRM-REQ-DGR-bbbb.

bbbb = Decimal number from 0 to 1023 identifying DTRM to be diagnosed.

System responds with a DR02 message containing the raw data of a diagnostic result in octal form. Refer to the raw data tables given in PK-xxxxx. Trouble numbers are also printed and may be matched with numbers in the appropriate trouble locating manual.

C. Requesting DTRM Status

11.18 To request a printout of the status of a DTRM, type in:

DTRM-REQ-STS bbbb.

bbbb = Decimal number between 0 and 1023 identifying the DTRM to be checked.

System responds with an LS01 message containing the current status and configuration of a DTRM and its associated voice frequency links (VFLa and VFLb).

D. Requesting an Audit of a DTRM

11.19 To request a copy of the DTRM data base, type in:

DTRM-REQ-AUD bbbb.

bbbb = Decimal number between 0 and 1023 identifying the DTRM to be audited.

The system responds with an LS03 message showing those DTRM, VFL, and band status indicators that are currently being used to perform the CCIS data link I/O function in addition to data link maintenance control.◀

12. VFL STATE CONTROL

12.01 ▶Manual control of the VFL maintenance states is accomplished via the maintenance TTY using the VFLK-REQ input message. This message is functionally similar to the DTRM-REQ message described in Part 11; ie, it can be used to establish various maintenance states and/or configurations or request some action to be taken on the VFL.

MANUAL VFL STATE TRANSITIONS

12.02 The following paragraphs describe the various VFLK-REQ input messages required to manually change the state of the VFL. There is a definite sequence which must be followed when going from one state to another, as shown in the state diagram in Fig. 25. After determining which state the VFL is in (using the VFLK-REQ-STS input message, as described in paragraph 12.09), start at that state and type in the appropriate VFLK-REQ-xxx messages to allow progression through the required number of states until the desired VFL state is reached. The following descriptions of the various VFLK-REQ-xxx input messages correspond to the sequence given in the state diagram.

A. Removing a VFL from Service

12.03 To remove a VFL from service, type in:

VFLK-REQ-RMV bbbb c.

bbbb = Decimal number between 0 and 1023 identifying the DTRM

c = A or B identifying the VFL.

System responds with a PF followed by an LS01 output message indicating the system has implemented the request. The VFL is removed from the ACTIVE state and placed in the STBY/DLY state. In this state, the VFL is not carrying call traffic and is not connected to the DTRM. The mate VFL is placed in the ACTIVE state.

B. Marking a VFL Unavailable for Service

12.04 To mark a VFL unavailable for service, type in:

VFLK-REQ-UNV bbbb c.

bbbb = Decimal number between 0 and 1023 identifying the DTRM

c = A or B identifying the VFL

System responds with OK indicating the request has been implemented. The VFL has been changed from the STBY/DLY state to the UNV/REL state. In this state, the VFL is not available for service and cannot be automatically switched into service by the system. Also, the VFL access circuit is released (not connected); however, before the access circuit can be operated (connected), the VFL must be in this state.

C. Operating a VFL Access Circuit

12.05 To operate the VFL access circuit for a specified VFL, type in:

VFLK-REQ-OPR bbbb c.

bbbb = Decimal number between 0 and 1023 identifying the DTRM

c = A or B identifying the VFL

System responds with OK indicating the specified VFL access circuit has been operated. The VFL has been moved from the UNV/REL state into the UNV/OPR state. In this state, the VFL is connected to the network appearance of the shared maintenance bus used for manual VFL testing. In this state, the VFL is not available for service and transmission tests may be performed.

D. Releasing a VFL Access Circuit

12.06 To release the VFL access circuit for a specified VFL, type in:

VFLK-REQ-REL bbbb c.

bbbb = Decimal number between 0 and 1023 identifying the DTRM

c = A or B identifying the VFL

The system responds with OK indicating the specified VFL access has been released. The VFL is now in the UNV/REL state and has been disconnected from the maintenance bus.

E. Placing a VFL in the Manual Out-of-Service State

12.07 To place the VFL in the manual OOS state, type in:

VFLK-REQ-OOS bbbb c.

bbbb = Decimal number between 0 and 1023 identifying the DTRM

c = A or B identifying the VFL.

System responds with OK indicating the request has been implemented. This causes a transition from the UNV/REL state to the STBY/DLY state. The automatic VFL test may be initiated only from this state. (See paragraph 12.10.)

F. Restoring a VFL to Service

12.08 To manually restore a VFL to service, type in:

VFLK-REQ-RST bbbb c.

bbbb = Decimal number between 0 and 1023 identifying the DTRM

c = A or B identifying the VFL.

The system responds with PF followed by an LS01 output message indicating that the request has been implemented. The VFL is restored to the ACTIVE state, carrying call traffic. If the associated DTRM is not active, the VFL is restored to the STBY/RDY state. The mate VFL is removed from service.

MANUAL VFL STATUS CHECKS, TESTS, AND AUDITS

A. Requesting VFL Status

12.09 To request a printout of the status of a VFL, type in:

VFLK-REQ-STS bbbb c.

bbbb =Decimal number between 0 and 1023 identifying the DTRM

c = A or B identifying the VFL to be checked.

The system responds with an LS01 message containing information on the current status and configuration of the specified DTRM and associated VFLs.

B. Initiating the Automatic Standby VFL Test

Note: The VFL must be in the STBY/DLY state to perform this test.

12.10 To initiate the automatic VFL test, type in:

VFLK-REQ-TST bbbb c.

bbbb = Decimal number between 0 and 1023 identifying the DTRM

c = A or B identifying the VFL to be tested.

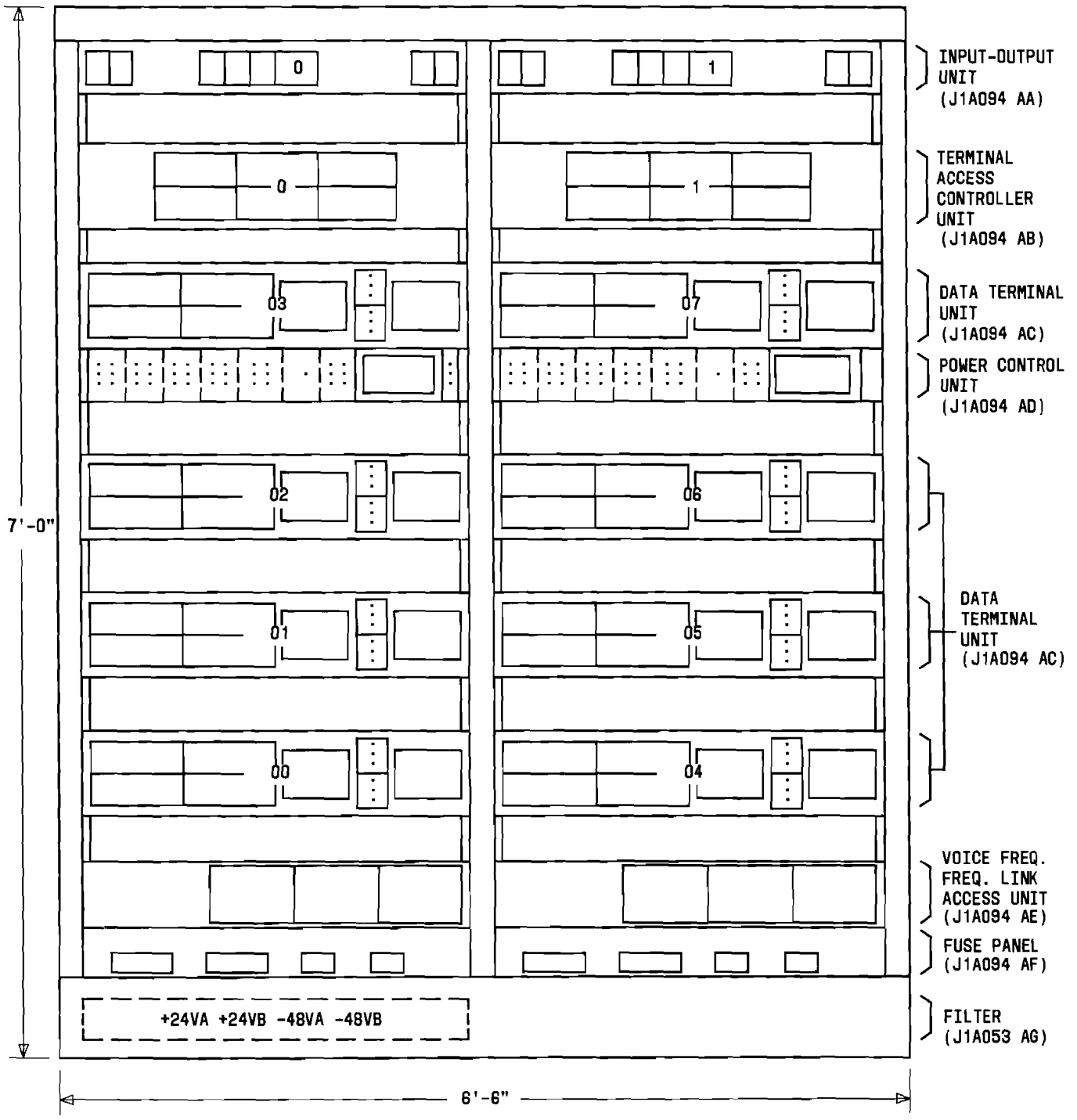
System responds with an LS01 message giving the results of the test. The switching office (via the link security routine) applies a loop to the VFL and sends a test-standby VFL signal to the STP. The STP then performs the loop-around test and returns the results to the switching office via a VFL test-passed signal or a VFL test-failed signal.◀

13. ABBREVIATIONS AND ACRONYMS

13.01 The following abbreviations and acronyms are used in this section.

ALT	Automatic Link Test
AUTO	Automatic
CCIS	Common Channel Interoffice Signaling
CONT	Controller
CP	Circuit Pack
CPD	Central Pulse Distributor
DEN	Data Enable
DS	Data Set
DTRM	Data Terminal
ESS	Electronic Switching System
FA	Fuse Alarm
IGFET	Integrated Field Effect Transistor
I/O	Input/Output
LBP	Lock Babble Protect
LSU	Lone Signal Unit
MCT	Master Clock Time
MN	Minor Alarm
MUM	Multiple Unit Message
NADRGO	Data-Register-Gate-Out(Bits 1 through 12)
NBDRGO	Data-Register-Gate-Out(Bits 13 through 24)
OEN	Opcode Enable
OOS	Out Of Service
PUAB	Peripheral Unit Address Bus
RQ	Reset Quarantine Enable
SCAB	Scanner Answer Bus
SQ	Set Quarantine Enable
STP	Signal Transfer Point
SU	Signal Unit
TASW	Terminal All-Seems-Well
TD	Terminal Data
UBP	Unlock Babble Protect

VFL	Voice Frequency Link
VFLA	Voice Frequency Link Access
WRMI	We-Really-Mean-It.


0
1
0
1
03
07
02
06
01
05
00
04
+24VA +24VB -48VA -48VB
7'-0"
6'-6"
INPUT-OUTPUT UNIT (J1A094 AA)
TERMINAL ACCESS CONTROLLER UNIT (J1A094 AB)
DATA TERMINAL UNIT (J1A094 AC)
POWER CONTROL UNIT (J1A094 AD)
DATA TERMINAL UNIT (J1A094 AC)
VOICE FREQ. FREQ. LINK ACCESS UNIT (J1A094 AE)
FUSE PANEL (J1A094 AF)
FILTER (J1A053 AG)

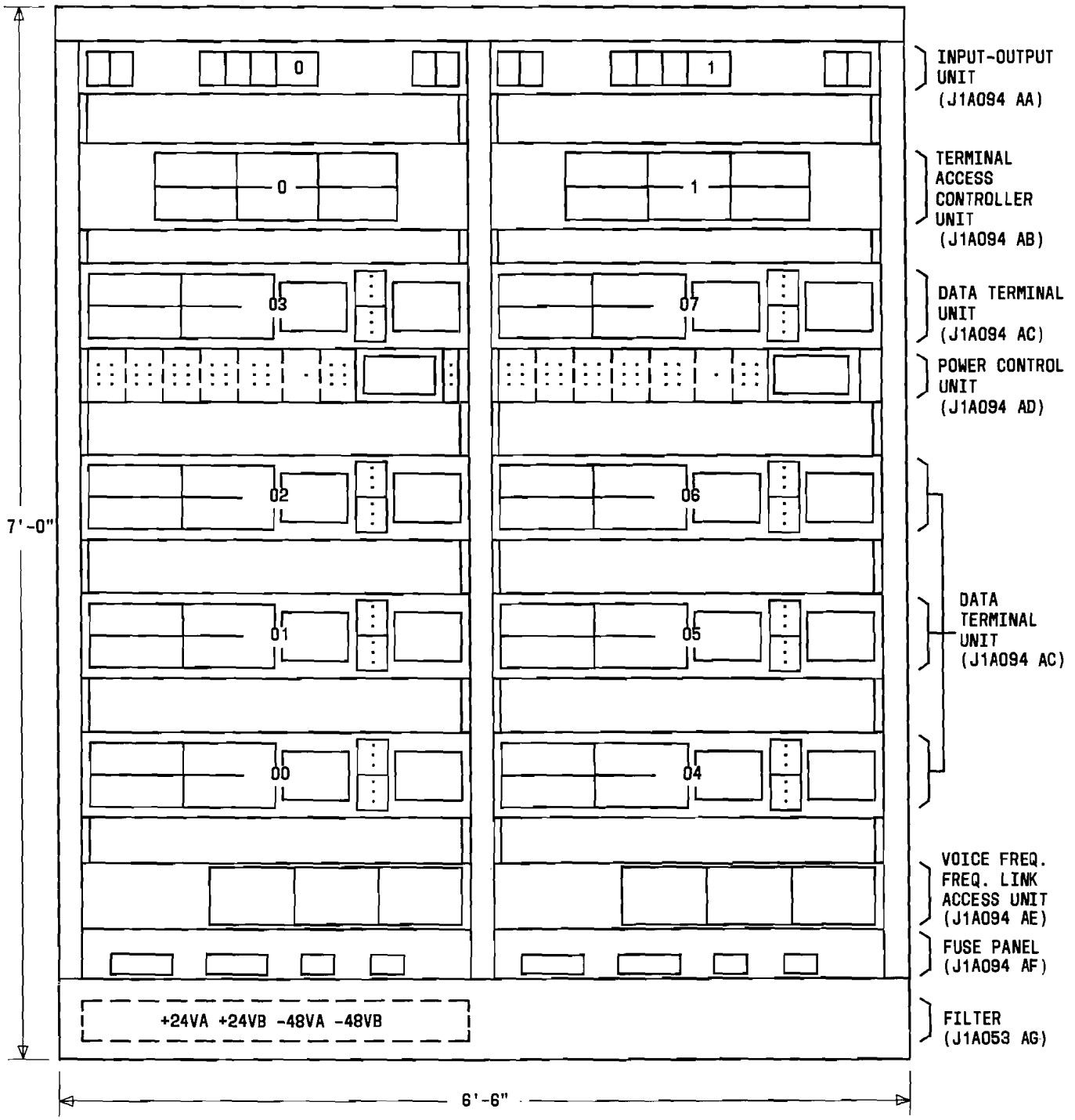
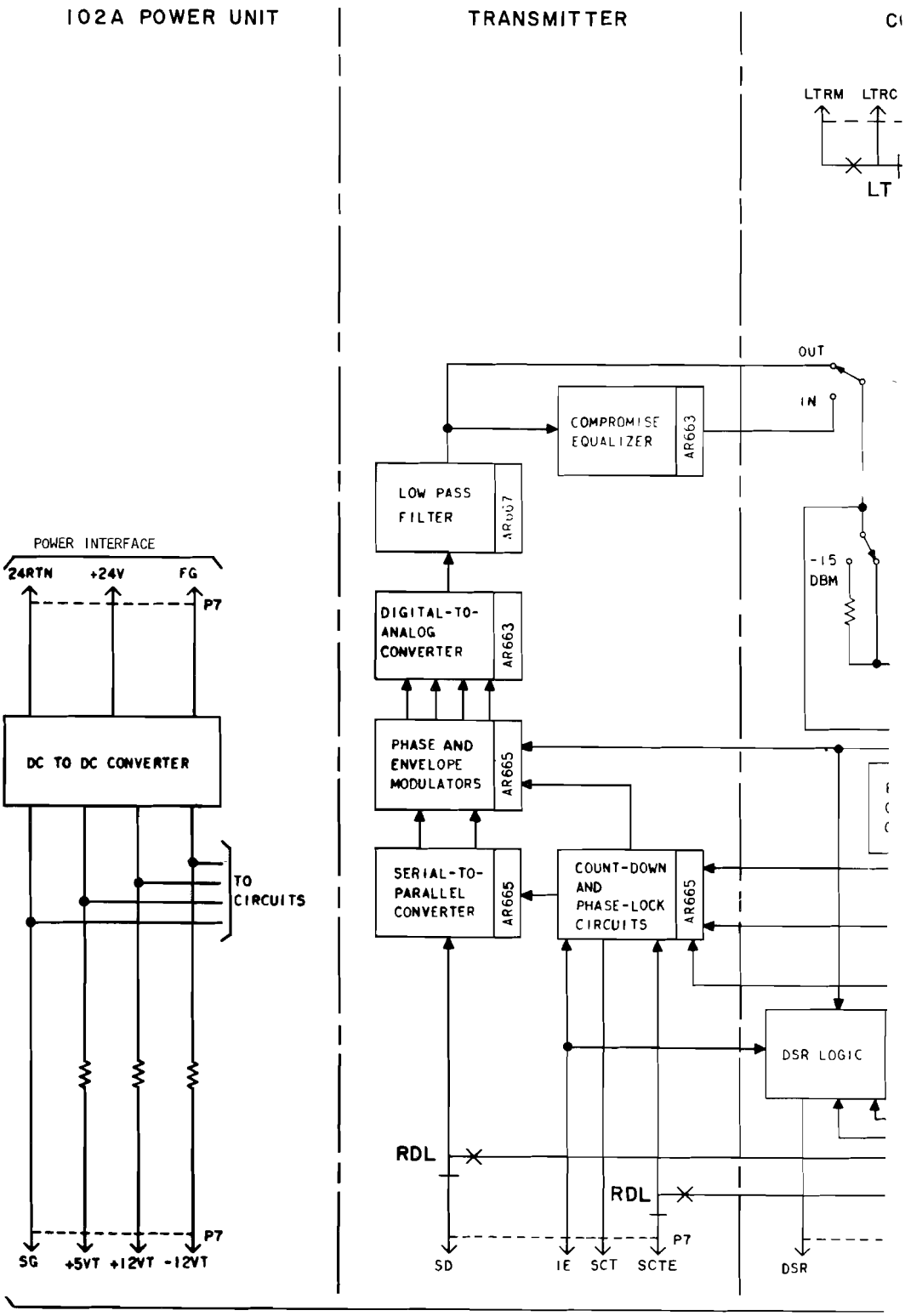


Fig. 26—Data Terminal Base Frame J1A094A


102A POWER UNIT
TRANSMITTER
POWER INTERFACE
24RTN
+24V
FG
P7
DC TO DC CONVERTER
TO CIRCUITS
P7
SG
+5VT
+12VT
-12VT
LTRM
LTRC
LT
OUT
IN
COMPROMISE EQUALIZER
AR663
LOW PASS FILTER
DIGITAL-TO-ANALOG CONVERTER
AR663
-15 DBM
PHASE AND ENVELOPE MODULATORS
AR665
SERIAL-TO-PARALLEL CONVERTER
AR665
COUNT-DOWN AND PHASE-LOCK CIRCUITS
AR665
DSR LOGIC
RDL
RDL
P7
SD
IE
SCT
SCTE
DSR

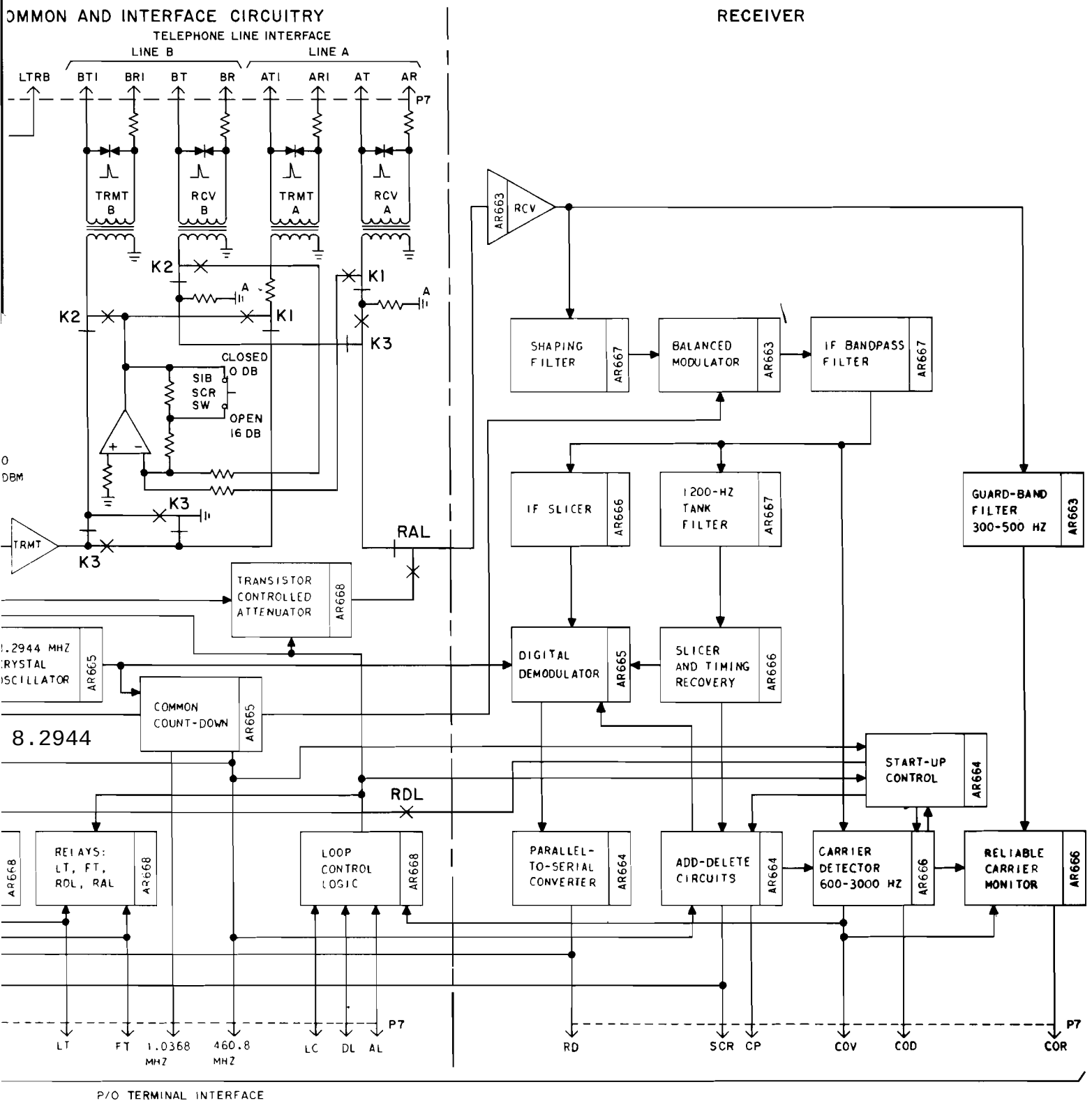
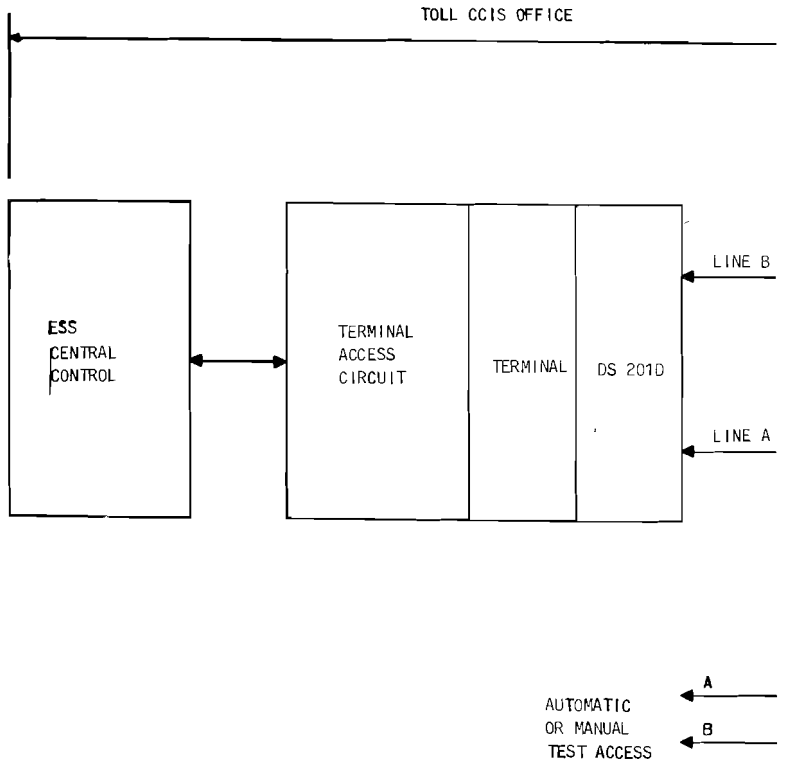


Fig. 27—Data Set DS 201D—Simplified Functional Schematic


TOLL CCIS OFFICE
ESS
CENTRAL
CONTROL
TERMINAL
ACCESS
CIRCUIT
TERMINAL
DS 201D
LINE B
LINE A
A
AUTOMATIC
OR MANUAL
TEST ACCESS
B

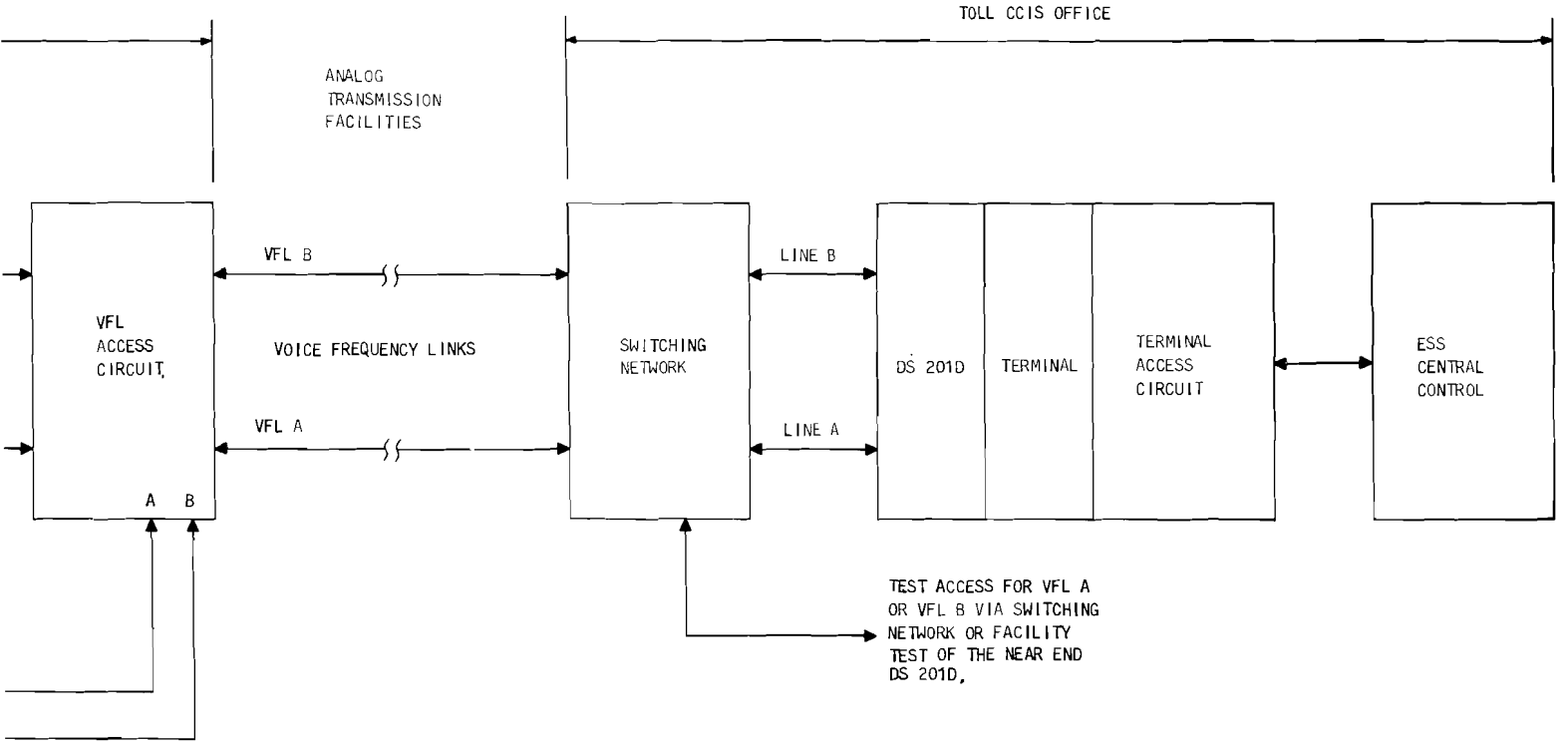
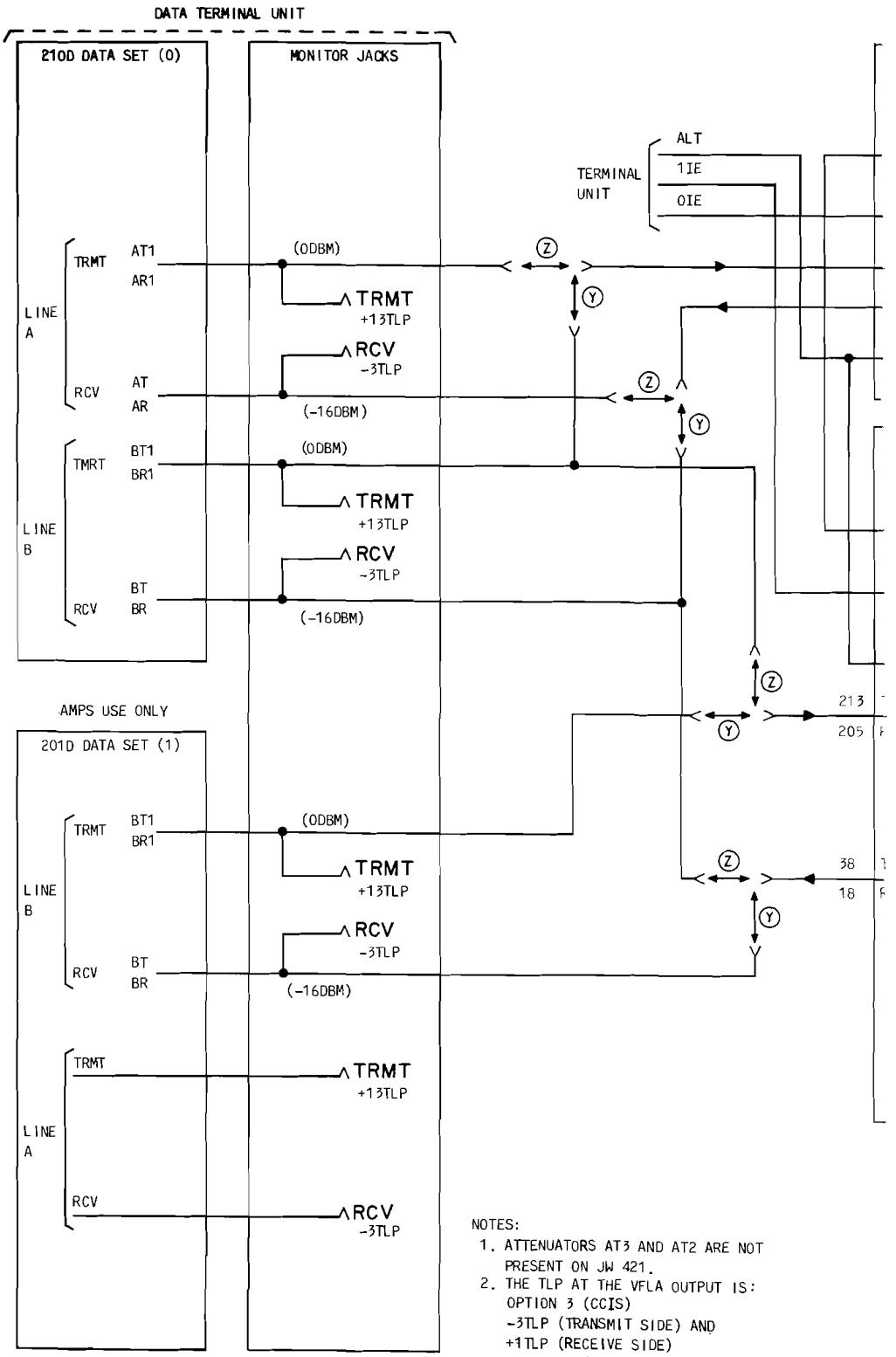


Fig. 28—Basic CCIS Configuration



NOTES:

1. ATTENUATORS AT3 AND AT2 ARE NOT PRESENT ON JW 421.
2. THE TLP AT THE VFLA OUTPUT IS:
   OPTION 3 (CCIS)
   -3TLP (TRANSMIT SIDE) AND
   +1TLP (RECEIVE SIDE)
   OPTION 2 (AMPS)
   +13TLP (TRANSMIT SIDE) AND
   -3TLP (RECEIVE SIDE)

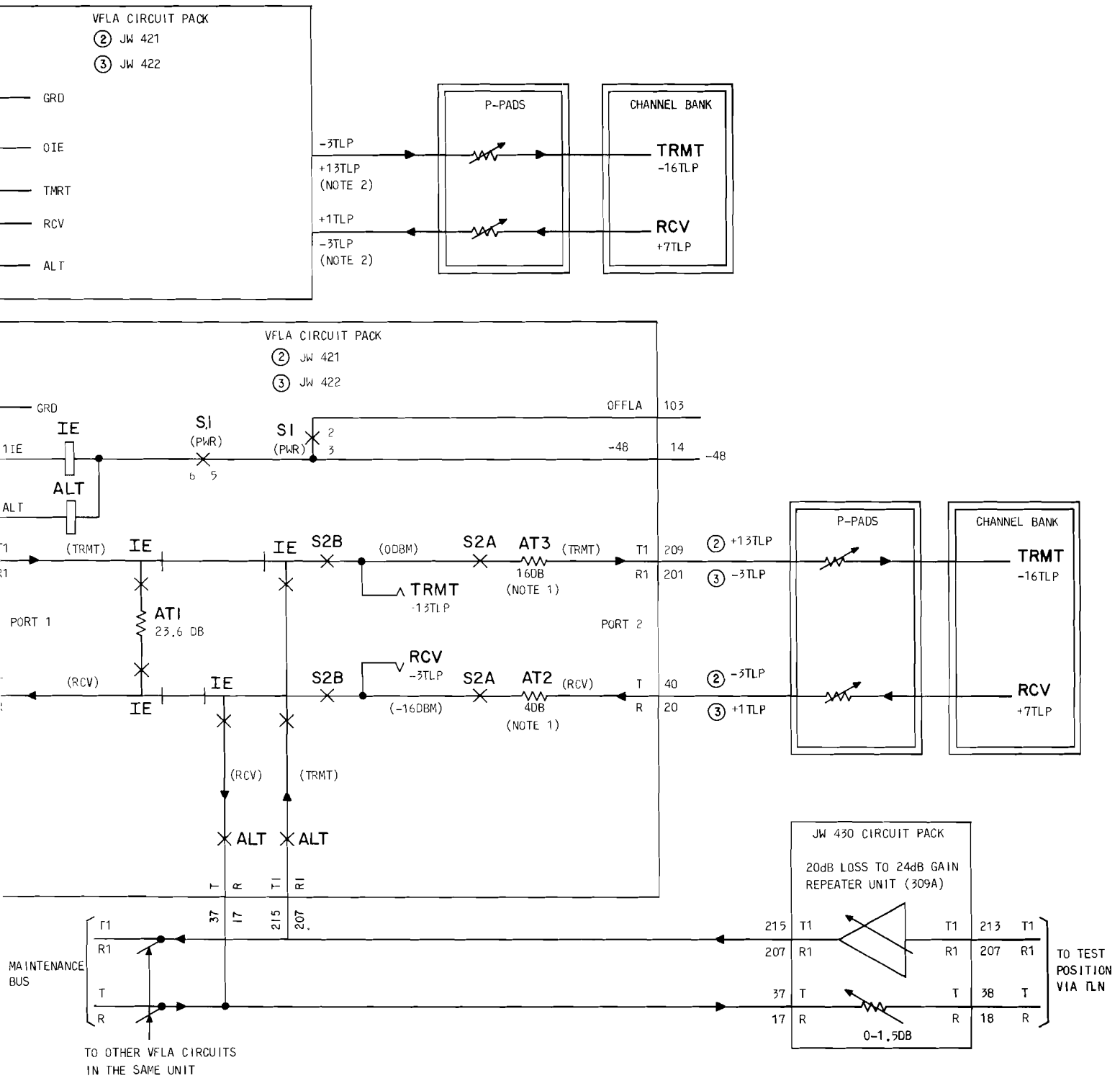
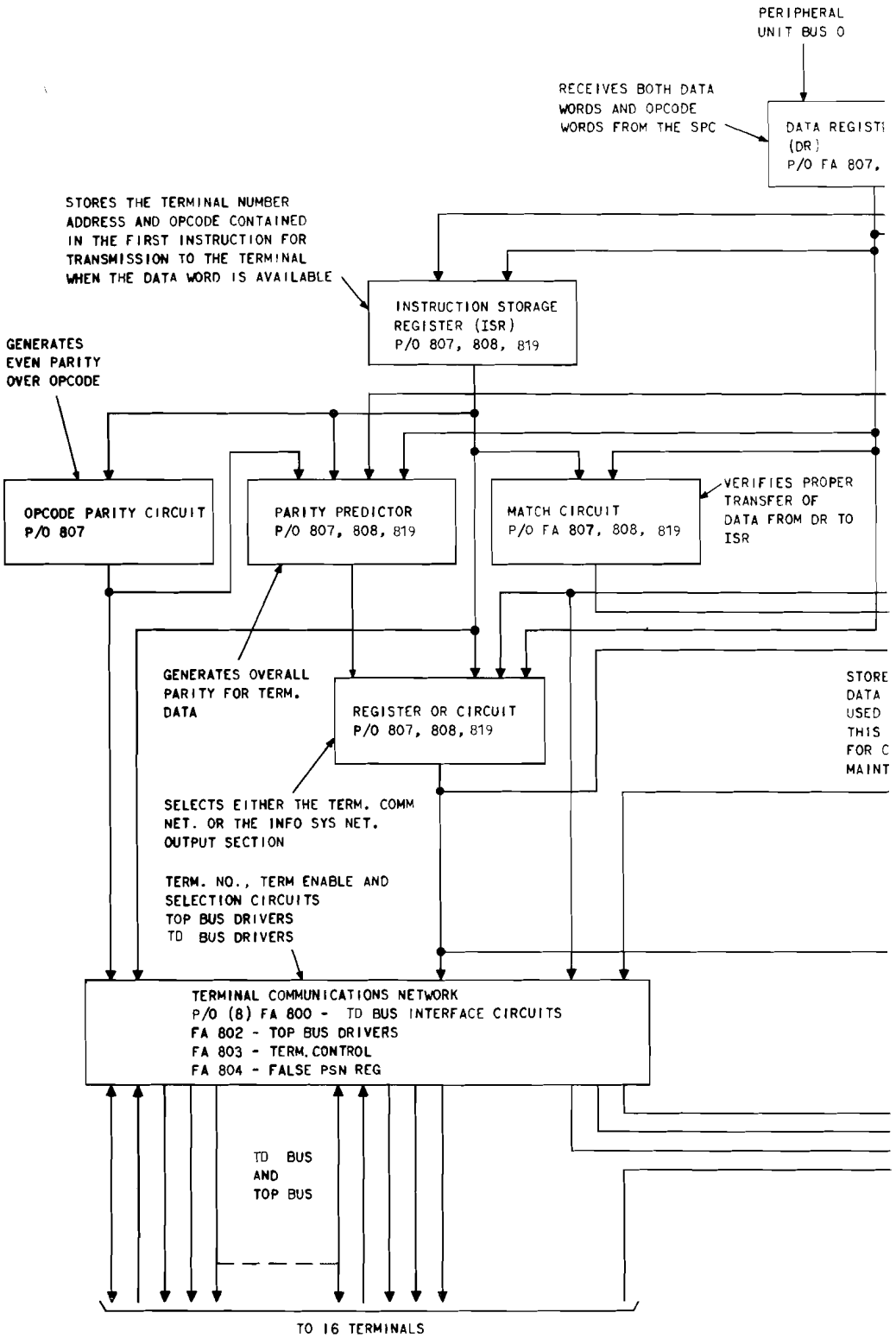


Fig. 29—Voice Frequency Link Access Unit—Block Diagram


PERIPHERAL
UNIT BUS 0
RECEIVES BOTH DATA
WORDS AND OPCODE
WORDS FROM THE SPC
DATA REGISTI
(DR)
P/O FA 807,
STORES THE TERMINAL NUMBER
ADDRESS AND OPCODE CONTAINED
IN THE FIRST INSTRUCTION FOR
TRANSMISSION TO THE TERMINAL
WHEN THE DATA WORD IS AVAILABLE
INSTRUCTION STORAGE
REGISTER (ISR)
P/O 807, 808, 819
GENERATES
EVEN PARITY
OVER OPCODE
OPCODE PARITY CIRCUIT
P/O 807
PARITY PREDICTOR
P/O 807, 808, 819
MATCH CIRCUIT
P/O FA 807, 808, 819
VERIFIES PROPER
TRANSFER OF
DATA FROM DR TO
ISR
GENERATES OVERALL
PARITY FOR TERM.
DATA
REGISTER OR CIRCUIT
P/O 807, 808, 819
STORE
DATA
USED
THIS
FOR C
MAINT
SELECTS EITHER THE TERM. COMM
NET. OR THE INFO SYS NET.
OUTPUT SECTION
TERM. NO., TERM ENABLE AND
SELECTION CIRCUITS
TOP BUS DRIVERS
TD BUS DRIVERS
TERMINAL COMMUNICATIONS NETWORK
P/O (8) FA 800 - TD BUS INTERFACE CIRCUITS
FA 802 - TOP BUS DRIVERS
FA 803 - TERM. CONTROL
FA 804 - FALSE PSN REG
TD BUS
AND
TOP BUS
TO 16 TERMINALS

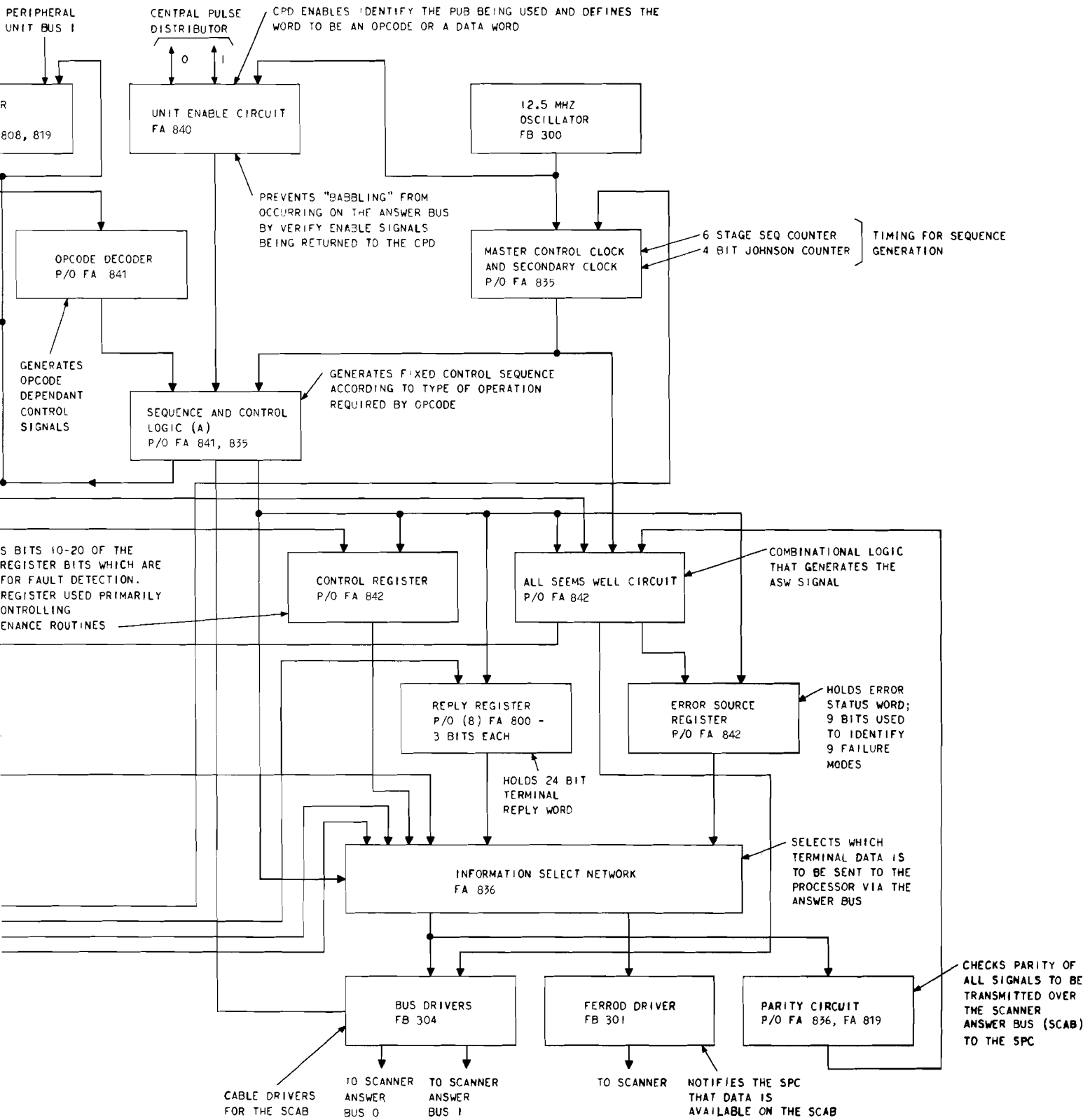
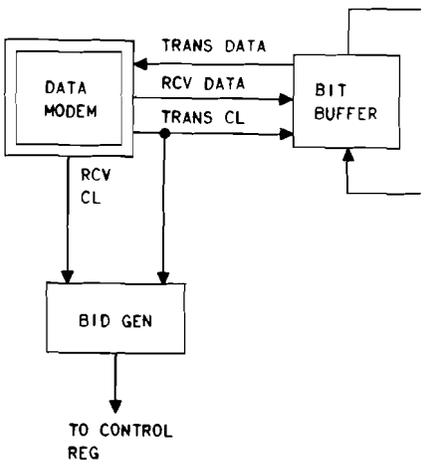
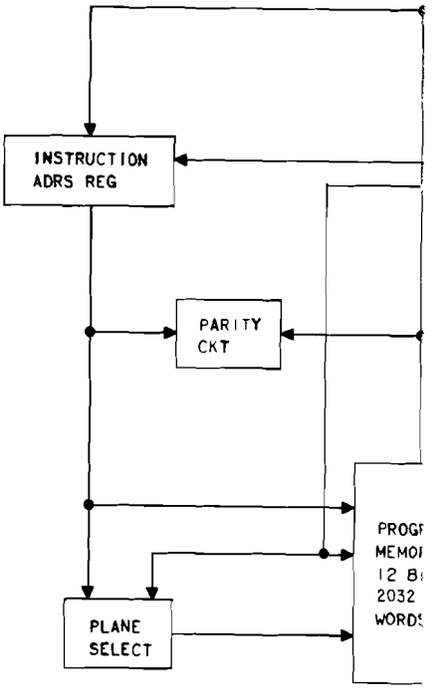


Fig. 30—CONT Functional Block Diagram


TRANS DATA
RCV DATA
TRANS CL
DATA MODEM
BIT BUFFER
RCV CL
BID GEN
TO CONTROL REG


INSTRUCTION ADRS REG
PARITY CKT
PLANE SELECT

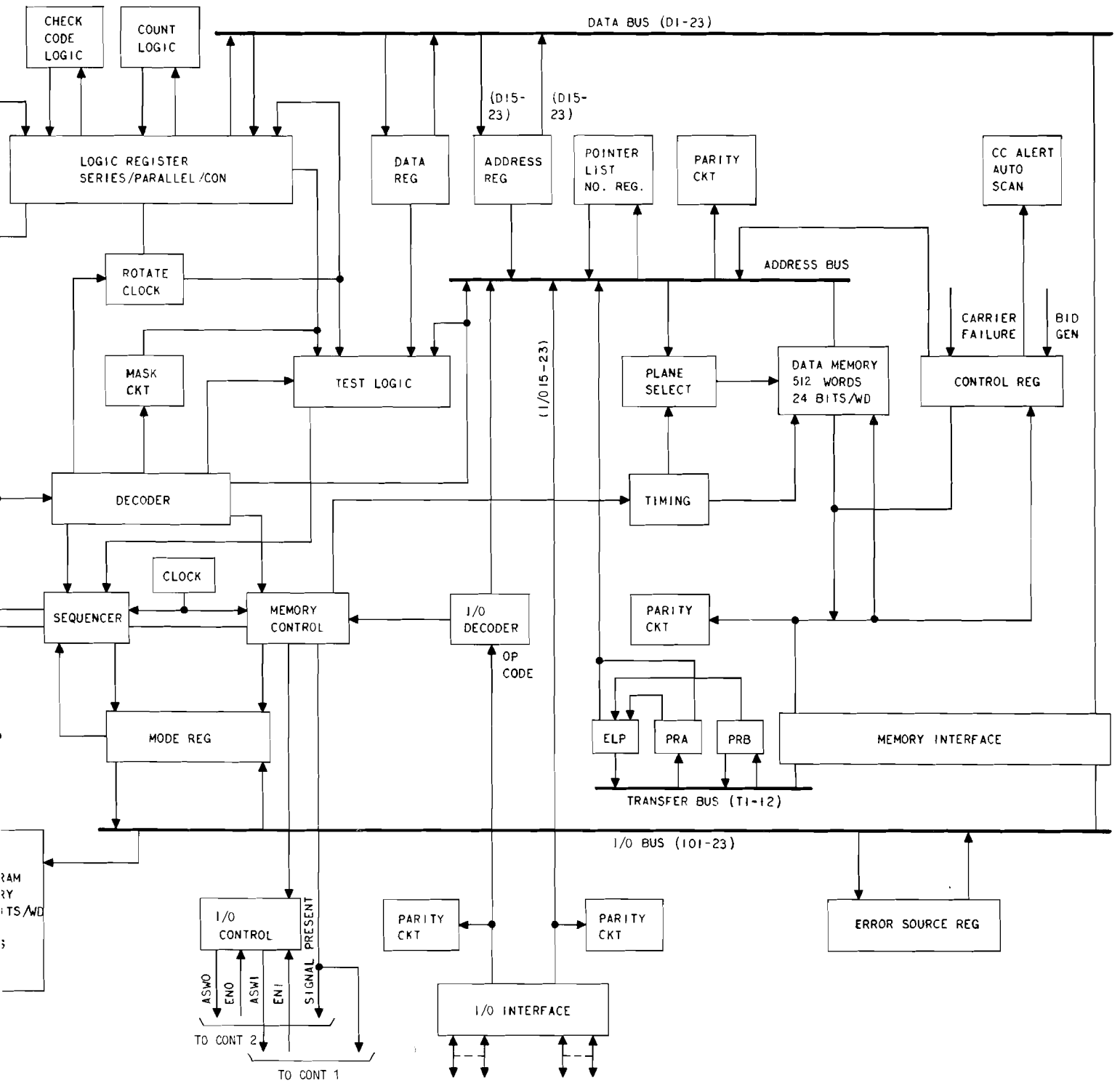


Fig. 31—CCIS Terminal—Block Diagram