5ESS® Switch
Hardware Description
5E16(2) and later

Document: 235-100-200
Issue Date: December 2003
Issue Number: 3.02a

Legal Notice

Notice

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This *5ESS*® switch document may contain references to the *5ESS*® switch, the *5ESS*®-2000 switch, and the *5ESS*® *AnyMedia*® Switch. The official name of the product has been changed back to the *5ESS*® switch. The documentation will not be totally reissued to change these references. Instead, the changes will be made over time, as technical changes to the document are required. In the interim, assume that any reference to the *5ESS*®-2000 switch or the *5ESS*® *AnyMedia*® Switch is also applicable to the *5ESS*® switch. It should be noted that this name change may not have been carried forward into software-influenced items such as input and output messages, master control center screens, and recent change/verify screens.

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Acknowledgment

Developed by Lucent Technologies.

1. HARDWARE DESCRIPTION INTRODUCTION

1.1 PURPOSE

The 235-100-200 Hardware Description Information Product (IP) provides descriptions of the hardware components that are included in the *5ESS*® Switch.

The purpose of this information product (IP) is to describe *5ESS*® switch hardware components through six predefined categories. The target population for this IP is telephone company personnel who:

- Regularly operate and maintain the *5ESS*® switch,
- Have completed basic *5ESS*® switch maintenance training, or
- Have equivalent *5ESS*® switch maintenance experience and knowledge.

1.2 UPDATE INFORMATION

1.2.1 Reason For Update

This section is for update information specific to the *Hardware Description*, 235-100-200, Issue 3.02. The **8. SWITCHING MODULE LINE PERIPHERALS** section *Packet Switching Unit, Model 2 (PSU2)* was updated due to the new **OIU-SIP-T** feature.

1.2.2 Supported Software Releases

This information product supports 5E14 through 5E16.2 software releases. In accordance with the *5ESS*® Switch Software Support Plan, the 5E13 software release is rated Discontinued Availability (DA) as of ***January*** 1, 2002. Information supporting software releases 5E13 and earlier will be removed from all documentation. If you support offices that use software release 5E13 or earlier, and you need that information, keep the associated pages as they are removed from the information products, or keep the earlier copy of the CD-ROM.

All release specific information for software releases rated DA is archived. This information can be provided from our archives in the event of a customer's need. When a software release is rated DA, a level of essential technical support is maintained. Essential technical support is defined as supporting critical problems, as mutually defined by the customer and Lucent Technologies. Additional technical support may be negotiated through service contracts, if desired.

1.2.3 Terminology

1.2.3.1 Communication Module Name Change

The term Communication Module (CM) has been changed to the Global Messaging Server (GMS), representing the new portfolio name of this particular module. The current names of the specific types of the GMS (the CM2 and CM3) have not been changed. Where the CM name has been used in a generic way within this information product, the name will be changed to GMS. Where the specific version of GMS (CM2 or CM3) is being described or mentioned, the name will not be changed. However, the GMS name may be added to the description in certain places as a reminder of the change, and that the particular version is a part of the overall portfolio. The following list provides some examples of how you may see these names used together:

- Global Messaging Server (formerly Communication Module)
- GMS (formerly CM) Global Messaging Server-CM2

- GMS-CM2
- Global Messaging Server-CM3
- GMS-CM3.

These name changes will be made over time as other technical changes are required. Also these changes may not be reflected in all software interfaces (input and output messages, master control center screens, and recent change and verify screens). Where the information product references these areas, the names are used as they are within the software interface.

1.2.3.2 *5ESS*®-2000 Switch Name Change

This *5ESS*® switch document may contain references to the 5ESS switch, the *5ESS*®-2000 switch, and the *5ESS*® *AnyMedia*® Switch. The official name of the product has been changed back to the *5ESS*® switch. In the interim, assume that any reference to the *5ESS*®-2000 switch or the *5ESS*® *AnyMedia*® Switch is also applicable to the *5ESS*® switch. It should be noted that this name change may not have been carried forward into software-influenced items such as input and output messages, master control center screens, and recent change/verify screens.

1.3 ORGANIZATION

This section describes how this information product is organized into sections, with a brief description of each.

- **1. INTRODUCTION**: This section contains information about this document and other general information about *5ESS*® switch documentation.
- **2. ADMINISTRATIVE MODULE**: This section describes the Administrative Module (AM) hardware units in the *5ESS*® switch documentation.
- **3. COMMUNICATION MODULE, MODEL 2**: This section describes the Communication Module, Model 2 (CM2) hardware units in the *5ESS*® switch documentation.
- **4. COMMUNICATION MODULE, MODEL 3**: This section describes the Communication Module, Model 3 (CM3) hardware units in the *5ESS*® switch documentation.
- **5. SWITCHING MODULE AND SWITCHING MODULE 2000**: This section describes the Switching Module and Switching Module-2000 hardware units in the *5ESS*® switch documentation.
- **6. SWITCHING MODULE APPLICATIONS**: This section describes the Switching Module Applications hardware units in the *5ESS*® switch documentation.
- **7. SWITCHING MODULE CONTROL UNITS**: This section describes the Switching Module Control hardware units in the *5ESS*® switch documentation.
- **8. SWITCHING MODULE LINE PERIPHERALS**: This section describes the Switching Module Line Peripheral hardware units in the *5ESS*® switch documentation.
- **9. SWITCHING MODULE TRUNK UNITS**: This section describes the Switching Module Trunk hardware units in the *5ESS*® switch documentation.
- **10. SWITCHING MODULE SERVICE PERIPHERAL UNITS**: This section describes the SM Service Peripheral hardware units in the *5ESS*® switch documentation.

- **11. LINKS AND BUSES**: This section describes the Links and Buses hardware in the *5ESS*® switch documentation.
- **12. CABINET POWER**: This section describes the Cabinet Power hardware units in the *5ESS*® switch documentation.
- **13. HARDWARE ACRONYM EXPANSIONS**: This section provides the hardware acronym expansion table expands all acronyms that are used in this IP. Each diagnosable component acronym described in this IP is expanded in the Table of Contents. Each non-diagnosable component acronym is expanded in the table only.

1.4 USER COMMENTS

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1.6 TECHNICAL ASSISTANCE

For technical assistance, call Technical Support Services (TSS) at:

- **1-866-LUCENT8 (1-866-582-3688)**; from inside the continental United States
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Technical Support Services is staffed 24 hours a day, 7 days a week.

2. ADMINISTRATIVE MODULE (AM)

2.1 3B21D Computer Administrative Module (AM)

2.1.1 Basic Description

The 3B21D Administrative Module (AM) is a multi-unit component. The AM is located in the processor shelves of the Computer System Processor cabinet.

The primary job of the AM is to control *5ESS*® switch functions and to monitor the operations and maintenance of the switching modules.

2.1.2 Electrical Power

The Administrative Module (AM) has a fuse and filter unit that acts as an interface between the DC power supply cables from the Global Power Distribution Frame (GPDF) and the DC/DC voltage converters that provide the units of the AM with the required voltage levels.

The Administrative Module has three fault groups: the CU, DFC, and IOP. The power for each fault group is controlled independently.

2.1.3 Shelf and Circuit Pack Arrangement

The Administrative Module (AM) is located in the processor shelf of the Computer System Processor cabinet. In the maximum configuration, the AM occupies three Computer System Processor cabinets.

Figure 2-1 depicts the shelf and circuit pack arrangement of the AM.

Figure 2-1 AM Shelf and Circuit Pack Arrangement

The following table details the shelf arrangement of the AM. For circuit pack information, go to the CU, IOP, and DFC sections.

EQL			
Vertical	**Horizontal**	**Component Name**	**Component Number**
49	Processor 1	**CU**	N/A

		IOP	
		DFC	
24	Processor 0	**CU**	N/A
		IOP	
		DFC	

2.1.4 Configuration

The following table details the configuration of the Administrative Module (AM).

Sub Modules	Link/Bus	Connects to...	Method of Operation	State of Operation
CU	DSCH	CM, DFC, CNI , and ASM	Duplex	ACT/STBY
	EAI	IOP		
DFC	DSCH	CU	Duplex	ACT/ACT
	SCSI bus	Disk and tape drives		
IOP	DSCH	CU	Go to the IOP hardware description document.	ACT/ACT
	Metallic wire	Peripherals		
NOTE: This table applies only to the 3B21D computer system. Other processors may be used.				

The following table details the hardware that the AM contains.

Diagnosable Units	Shelf Units	Diagnosable Components
CU	Processor Unit 0 and Processor Unit 1	CC
		CH
		CSU
		DMA
		MASC
		SAT
DFC	Processor Unit 0 and Processor Unit 1	DFC
IOP	Processor Unit 0 and Processor Unit 1	IOP
		MTTYC
		SCSDC
		TTYC
		SDLC
		PSSDB

2.1.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Administrative Module (AM) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
AM	One side	Major	No service impact.	No service impact.
	Both sides	Critical	Removes all CCS trunks from service.	Removes all Operations, Administrative, and Maintenance (OA&M) peripherals from service, except the EAI.

2.1.6 Detailed Description

The following table details the functions of the sub-units in the Administrative Module (AM).

Part	Function
CU	Controls the operations of the *5ESS*® switch.
	Executes software program instructions.
	Stores software programs and Office Dependent Data (ODD).
	Passes program instructions and ODD for all AM components.
DFC	Controls the disks that store data from the CU.
IOP	Connects Operations, Administration, and Maintenance (OA&M) peripheral devices that communicate with the *5ESS*®switch.

2.1.7 Functional Description

2.1.7.1 Functions

The Administrative Module (AM):

- Controls the *5ESS*® switch:
  - Provides programs, instructions, and data to operate the switch.
  - Stores records.
  - Schedules routine diagnostic tests.
  - Alerts users when the maintenance state of any component changes.
- Allows users to communicate with the switch by the Input/Output peripherals.
- Connects the Input/Output peripherals for orders, instructions, and data retrieval.
- Connects the CM and CNI processors for trunk signaling.
- Connects the CM and ASM processors for administration and maintenance messages.

2.1.7.2 Operation

The AM interacts with other components to operate the switch.

Figure 2-2 depicts the operation of the AM.

Figure 2-2 AM Block Diagram

The following table details the operations of the AM. The AM handles the following operations simultaneously.

Stage	Description

1	Receives orders from users through the ASM by the DSCH and the Input/Output peripherals by the metallic wires.
2	Sends the orders to the AM components, CNI , and ASM by the DSCHs.
3	Sends messages (data, address, select and control) to the CM, CNI , and ASM by the DSCHs.
4	Receives messages (data and response) from the CM, CNI , and ASM by the DSCHs.

2.2 Control Unit (CU)

2.2.1 Basic Description

The Control Unit (CU) is a multi-circuit pack component. The CU is located in the processor shelf of the Computer System Processor cabinet.

The primary job of the CU is to control the operations of the *5ESS*® switch.

2.2.2 Electrical Power

The CUPS circuit pack controls power for the CU. The CUPS circuit pack is located in the processor shelf of the Computer System Processor cabinet. The following table details the power groups for the CU.

CU Power			
Circuit Pack	**Location**		**Function**
CUPS	Vertical	Horizontal	The CUPS controls the following two 410AA packs: □ The TN1821B supports Auto Restart. □ The TN1821 does not support Auto Restart.
	53	060	
	28	060	
CONVA	Vertical	Horizontal	410AA Powers all the circuit packs in the CU.
	53	052	
	28	052	
NOTE: Vertical slot 53 refers to CU 1. Vertical slot 28 refers to CU 0.			

2.2.3 Shelf and Circuit Pack Arrangement

The CU is located in the processor shelf of the Computer System Processor cabinet.

Figure 2-3 depicts the shelf and circuit pack arrangement of the CU.

Figure 2-3 CU Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the CU circuit packs. The following EQL locations reference the following:

- Vertical locations 45, 49, and 53 refers to CU 1.
- Vertical locations 19, 24, and 28 refers to CU 0.

EQL		Component Name	Component Number
Vertical	Horizontal		
049	008	**MM**	KLW32, KLW40, KLW48, KLW64, KLW128, or KLW256
024	008		
049	038	**CC**	KLW31
024	038		
053	052	**CONVA**	410AA
028	052		
053	060	**CUPS**	TN1821 or TN1821B
028	060		
053	075	**DMA 0**	KBN15 or KBN415
028	075		
045	050	**Utility Circuit (Office dependent)**	UN379
019	050		
049	018	**EX 0**	KLW size circuit pack for future growth
049	028	**EX 1**	
024	018	**EX 0**	
024	028	**EX 1**	

2.2.4 Configuration

The following table details the configuration of the CU.

Circuit Pack	Link/Bus	Connects to ...	Method of Operation	State of Operation

CC	MCHL	Mate CU	Duplex	ACT/STBY
	CCIO	DMA		
	MASB	MM		
	EAI	MTTYC/IOP		
	Backplane	UC		
MM	Update Bus	Mate CUs	Duplex	ACT/STBY
	MASB	CC		
		DMA		
		EX		
DMA	MASB	Mate DMA	Duplex	ACT/STBY
	CCIO	CC		
	DSCH	DFC, IOP, CM, CNI, and ASM		
UC*	Backplane	CC	Duplex	ACT/STBY
NOTE: ******* Office Dependent.				

2.2.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the CU components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
CU	One side	Major	No impact.	Reduces the AM to the simplex mode.
	Both sides	Critical	Removes local and long-distance calls from service.	Stops inter-switching module call processing.
NOTE: The CU is a fault group. When the CC, DMA, or MM goes Out-Of-Service (OOS), then the CU goes OOS.				

2.2.6 Detailed Description

The following table details the functions of the circuit packs in the Control Unit (CU).

Part	Function
CC	Executes the software program instructions
MM	Stores the software programs and ODD that are most frequently used by the AM
DMA	Allows the switch to communicate by routing messages between the CC, MM, DFC, IOP, CNI, CM, and ASM
UC	Interfaces the CC (Bell Labs Only, Office Dependent)

2.2.7 Functional Description

2.2.7.1 Functions

The Control Unit (CU) consist of the following circuit packs:

- **CC**: Executes the software program instructions.
- **MM**: Stores software programs and Office Dependent Data (ODD) that are the most frequently used by the AM.
- **DMA**: Enables the switch to communicate by routing message between the CC, MM, DFC, IOP, CNI, CM, and ASM.
- **UC**: Interfaces the CC. (Bell Labs Only, Office Dependent)

2.2.7.2 Operation

The CU interacts with other components to operate the switch.

Figure 2-4 depicts the operation of the CU.

Figure 2-4 CU Block Diagram

The following table details the operation of the CU. The CU does the following:

Stage	Description
1	Sends Operations, Administration, and Maintenance (OA&M) messages (data, address, select, and control) to the CNI, ASM, CM, IOP, and DFC by the DSCHs.
2	Receives messages (data, response) from the CNI, ASM, CM, IOP, and DFC by the DSCHs.
3	Receives intervention orders from users that are operating the MCC and SCCS terminals by the EAI.

2.3 Central Control (CC)

2.3.1 Basic Description

The Central Control (CC) is a one circuit pack component. The CC is located in the CU processor shelf of the Computer System Processor cabinet.

The primary job of the CC is to execute software program instructions.

2.3.2 Electrical Power

The Central Control (CC) is part of the CU power group. The CUPS circuit pack controls power for the CU. The CUPS circuit pack is located in the CU processor shelf of the Computer System Processor cabinet.

2.3.3 Shelf and Circuit Pack Arrangement

The Central Control (CC) 0 is located in the lower processor shelf of the Administrative Module (AM) cabinet. The CC 1 is located in the upper processor shelf.

The Figure 2-5 depicts the shelf and circuit pack arrangement of the CC.

Figure 2-5 CC Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the CC circuit packs.

EQL		Component Name	Component Number
Vertical	Horizontal		
049	038	**CC 1**	KLW31
024	038	**CC 0**	KLW31

2.3.4 Configuration

The following table details the configuration of the Central Control (CC).

Circuit Pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
CC	MCHL	Mate CC	Duplex	ACT/STBY
	CCIO	DMA		
	MASB	MM		
	EAI	MTTYC		
	Backplane	UC		

2.3.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Central Control (CC) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
CC	One side	Major	No impact.	Reduces the AM to the simplex mode.
	Both sides	Critical	Removes all long-distance calls from service.	Removes the AM and CCS trunks from service.
NOTE: The CU is a fault group. When the CC, DMA, or MM goes OOS, then the CU goes OOS.				

2.3.6 Detailed Description

The following table details the functions of the diagnosable components in the Central Control (CC).

Part	Function
CC	The CC consist of the following circuits that performs software program instructions: □ **CSU (Cache Store Unit):**Stores the most recent program instructions and ODD. □ **CC (Central Control):**Executes program instructions for the CU.

2.3.7 Functional Description

2.3.7.1 Functions

The Central Control (CC) controls the operation of the *5ESS*® switch.

2.3.7.2 Operation

The CC interacts with other components to operate the switch.

Figure 2-6 depicts the operation of the CC.

Figure 2-6 CC Block Diagram

The following table details the operation of the CC.

Stage	Description
1	Receives ODD and ECD from the DMA by the CCIO.
2	Generates and sends an OA&M control message to the DMA by the CCIO.
3	Receives interrupts from the DMA by the CCIO.
4	Receives copies of the ODD and ECD that were most recently used by the AM by the Main Store Bus.
5	Receives intervention orders from users at the MCC or SCCS terminals by the EAI.
6	Sends the most recent configuration information about the 3B21D to the IOP by the EAI.
7	Sends maintenance messages to the standby CU for diagnostics by the maintenance channel.
8	Sends orders to the standby CU by the maintenance channel to take control of *5ESS*® switch operations.

2.4 Main Memory (MM)

2.4.1 Basic Description

The Main Memory (MM) is a one circuit pack component. The MM is located in the CU processor shelf of the Computer System Processor cabinet.

The primary job of the MM is to store software programs and Office Dependent Data (ODD).

2.4.2 Electrical Power

The Main Memory (MM) is part of the CU power group. The CUPS pack controls power for the CU. The CUPS pack is located in the CU processor shelf of the Computer System Processor cabinet.

2.4.3 Shelf and Circuit Pack Arrangement

The Main Memory (MM) 0 is located in the lower processor shelf of the Computer System Processor cabinet. The MM 1 is located in the upper processor shelf of the Computer System Processor cabinet.

Figure 2-7 depicts the shelf and circuit pack arrangement for the MM.

Figure 2-7 MM Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the MM.

EQL		Component Name	Component Number
Vertical	Horizontal		
24	008	**MM**	KLW32, KLW40, KLW48, KLW64, KLW128, or KLW256
49	008		

2.4.4 Configuration

The following table details the configuration of the Main Memory (MM).

Circuit Pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
MM	Update Bus	Mate MM	Duplex	ACT/ACT
	MASB	CC		
	MASB	DMA		
	MASB	EX		

2.4.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Main Memory (MM) is not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
MM	One side	Major	No impact.	Reduces the AM to the simplex mode.
	Both sides	Critical	Removes all long-distance calls from service.	Removes the AM and CCS trunks from service.
NOTE: The CU is a fault group. When the CC, DMA, or MM goes Out-Of-Service (OOS), then the CU goes OOS.				

2.4.6 Detailed Description

The following table details the functions of the diagnosable components in the Main Memory (MM).

Part	Function
MM	The MM consist of the following circuits that stores software programs and Office Dependent Data (ODD): □ **MAS**: Stores ODD and program instructions that are most frequently used by the MM. □ **MASC**: Controls the MM. □ **MASU**: Updates the MM in the standby CU.

2.4.7 Functional Description

2.4.7.1 Functions

The Main Memory (MM) stores programs and data that are most frequently used by the AM.

2.4.7.2 Operation

The MM interacts with other components to operate the switch.

Figure 2-8 depicts the operation of the MM.

Figure 2-8 MM Block Diagram

The following table details the operation of the MM.

Stage	Description
1	The MM receives program instructions, ODD, and ECD from the CC, DMA, or mate MM by the Main Store or Main Store Update Bus.
2	The MM stores program instructions (call processing and call record storage) and copies of the ODD and ECD.
3	The MM sends the program instructions, ODD, and ECD to the CC, DMA, or mate MM by the Main Store or Main Store Update Bus.

2.5 Direct Memory Access (DMA)

2.5.1 Basic Description

The Direct Memory Access (DMA) is a one circuit pack component. The DMA is located in the CU processor shelf of the Computer System Processor cabinet.

The primary job of the DMA is to pass program instructions and Office Dependent Data (ODD) to all of the components in the AM.

2.5.2 Electrical Power

The Direct Memory Access (DMA) is part of the CU power group. The CUPS circuit pack controls power for the CU. The CUPS circuit pack is located in the CU processor shelf of the Computer System Processor cabinet.

2.5.3 Shelf and Circuit Pack Arrangement

The Direct Memory Access (DMA) 0 is located in the lower processor shelf of the Computer System Processor cabinet. The DMA 1 is located in the upper processor shelf of the Computer System Processor cabinet.

Figure 2-9 depicts the shelf and circuit pack arrangement of the DMA.

Figure 2-9 DMA Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the DMA.

EQL		Component Name	Component Number
Vertical	Horizontal		
49	075	**DMA 0 (CU 1)**	KBN15 or KBN415
24	075	**DMA 0 (CU 0)**	KBN15 or KBN415
49	065	**DMA 1 (CU 1)**	KBN15 or KBN415
24	065	**DMA 1 (CU 0)**	KBN15 or KBN415

2.5.4 Configuration

The following table details the configuration of the Direct Memory Access (DMA).

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
DMA	CCIO	CC	ACT/ACT	Duplex
	MASB	MM		
	DSCH	Peripherals		

2.5.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Direct Memory Access (DMA) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
DMA	CU 0	Major	No impact.	Reduces the AM to the simplex mode.
	CU 0 and CU 1	Critical	Removes all long-distance calls from service.	Removes the AM and CCS trunks from service.

2.5.6 Detailed Description

The following table details the function of the diagnosable components in the Direct Memory Access (DMA).

Part	Function
DMA	The DMA consist of the following program instructions and ODD to all the components in the AM:

	□ **CU DMACH**: Connects the AM peripherals to the DMA.

2.5.7 Functional Description

2.5.7.1 Functions

The Direct Memory Access (DMA) enables the switch to communicate by routing messages between the CC, MM, DFC, IOP, CNI, CM, and ASM.

2.5.7.2 Operation

The DMA interacts with other components to operate the switch.

Figure 2-10 depicts the operation of the DMA.

Figure 2-10 DMA Block Diagram

The following table details the operation of the DMA.

Stage	Description
1	The DMA routes control messages (Operations, Administration, and Maintenance [OA&M]) for the CC, MM, CNI, ASM, DFC, IOP, and for CM between the MSGS and the DFC, IOP, ASM, and CNI by the DSCH.
2	The DMA receives the (CC, MM, CNI, ASM, DFC, IOP, and CM) control messages from the MSGS of the CM.
3	The DMA sends the control messages to the CC or the MM by the Main Store Bus.

2.6 Disk File Controller (DFC)

2.6.1 Basic Description

The Disk File Controller (DFC) is a one circuit pack component. The DFC is located in the Control Unit (CU) processor shelves of the Computer System Processor cabinet.

The primary job of the DFC is to control the disks that store data for the CU.

2.6.2 Electrical Power

Each Disk File Controller (DFC) circuit pack contains a Display and Control Interface circuit that controls power for the circuit pack.

NOTE: The UN373 and TN2116 DFC packs require a 410AA power converter pack.

2.6.3 Shelf and Circuit Pack Arrangement

The Disk File Controller (DFC)0 is located in the upper Control Unit (CU) processor unit shelf of the Computer System Processor cabinet. The DFC 1 is located in the lower CU processor unit shelf of the Computer System Processor cabinet.

Figure 2-11 depicts the shelf and circuit pack arrangement for the DFC.

Figure 2-11 DFC Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the DFC hardware components.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
28	178	**DFC 0**	UN580B
53	178	**DFC 1**	UN580B

2.6.4 Configuration

The following table details the configuration of the Disk File Controller (DFC).

Circuit Pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
DFC	SCSI Bus	Disk Drive	Simplex	ACT
	SCSI Bus	Tape Drive		
	DSCH	DMA	Duplex	ACT/ ACT
NOTE: Prior to 1/1/1995, 3B21D shipments of the DFC contained two circuit packs: UN373 and TN2116.				

2.6.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Disk File Controller (DFC) components are not available.

Unavailable Component	Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
DFC	Major	No impact.	No impact, unless the DFC connects to the tape drive.
	Critical	Stops change orders during the outage.	Reduces the switching modules to stand-alone billing. Loses call records as the outage duration increases.

2.6.6 Detailed Description

The following table details the functions of the Disk File Controller (DFC).

Part	Function
DFC	Controls the tape drive and disks that store data from the CU.
	Routes data between the CU and the disks.

2.6.7 Functional Description

2.6.7.1 Functions

The Disk File Controller (DFC) provide the following:

- Controls the tape drive and disks that store information from the CU.
- Routes control messages between the CU and the tape drive and/or disks.

2.6.7.2 Operation

The DFC interacts with other components to operate the switch.

Figure 2-12 depicts the operation of the DFC.

Figure 2-12 DFC Block Diagram

The following table details the operation of the DFC.

Stage	Description
1	The DFC receives control information (data, control, and address) from the CU by the DSCH.

2	The DFC sends the control information OA&M to the disks and tape drive by the SCSI bus.
3	The disks and tape drive either store the messages (program instructions, ODD, ECD, and call records) or send data to the DFC by the SCSI bus.

2.7 Input/Output Processor (IOP)

2.7.1 Basic Description

The Input/Output Processor (IOP) is a multi-circuit pack component. The IOP is located in the processor unit shelf(s) of the Computer System Processor cabinet.

The primary job of the IOP is to handle the transfer of control messages between the CU and peripheral devices.

2.7.2 Electrical Power

The IOPPS power pack controls power for the Input/Output Processor (IOP).

2.7.3 Shelf and Circuit Pack Arrangement

The Input/Output Processor (IOP) 0 is located in the lower processor unit shelf of the Computer System Processor cabinet. The IOP 1 is located in the upper processor unit shelf of the Computer System Processor cabinet.

Figure 2-13 depicts the shelf and circuit pack arrangement for the IOP.

Figure 2-13 IOP Shelf and Circuit Pack Arrangement

The following tables detail the shelf and circuit pack arrangement of the IOP hardware components.

EQL PU0			
Vertical	**Horizontal**	**Component Name**	**Component Number**
19	065	**IOP Controller**	KBN10
19	080	**IOPPS Power**	TN1820B,C,or D
19	094	**MTTYC**	UN583 or UN597
19	102 - 152	**SCSDC**	UN33D or UN933
28	94 - 146	**TTYC and SDLC**	UN582

EQL PU1		Component Name	Component Number
Vertical	**Horizontal**		
45	065	**IOP Controller**	KBN10
45	080	**IOPPS Power**	TN1820B,C,or D
45	094	**MTTYC**	UN583 or UN597
45	102 - 152	**SCSDC**	UN33D or UN933
53	094 - 146	**TTYC and SDLC**	UN582
45	180	**PSSDB**	UN377

EQL		Component Name	Component Number
Vertical	**Horizontal**		
11	011	**IOP**	KBN10
62	011		
11	026	**IOPPS Power**	TN 1820B, C, or D
62	026		
11	006	**Power Converters**	410AA
11	034		
62	006		
62	034		
11	040 - 164	**TTYC and SDLC**	UN582
62	040 - 164		
NOTE: Vertical slot 11 applies to IOP2. Vertical slot 62 applies to IOP3.			

2.7.4 Configuration

The Input/Output Processor (IOP) contains four communities. Each community can contain four circuit packs.

The following table details the configuration of the IOP.

Circuit Pack	Link/Bus	Connects to...	Method of Operation	State of Operation
IOPC	IOMI	PC	Duplex	ACT/ACT
	DSCH	DMA		
MTTYC Peripheral Controller	IOMI	IOPC		
	EAI	CC		
	Metallic Wire	PSSDB		
SCSDC Peripheral Controller	IOMI	IOP Controller	Duplex	ACT/ACT
	Metallic Wire	Office Alarm Unit		
TTYC and SDLC Peripheral Controller	IOMI	IOP Controller	Simplex	ACT
	Metallic wire	Peripherals		
PSSDB	Metallic wire	MTTY	Simplex	ACT
	Metallic wire	ROP		
	Backplane	Other IOP		

2.7.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Input/Output Processor (IOP) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
IOP	One side	Major	No impact.	Removes Input/Output devices that are connected to the IOP from service. Reduces the MCC to the simplex mode.
	Both sides	Critical		Removes all Input/Output devices that are connected to the IOP and the MCC from service.
MTTYC	One side	Major	No impact.	Reduces the MCC to the simplex mode.
	Both sides	Critical		Removes the MCC from service.
SCSDC	One side	Major	No impact.	Reduces some office alarms to the simplex mode.
	Both sides	Critical		Prevents office alarms from operating.
TTYC and SDLC	One side	Major	No impact.	Removes the peripherals that are assigned to the IOP from service.

2.7.6 Detailed Description

The following table details the functions of the circuit packs in the Input/Output Processor (IOP).

Part		Function
IOPC		Connects the CU to the peripheral controllers.
PSSDB		Switches the MCC between the MTTYCs in the IOP 0/1.
Peripheral Controllers	**MTTYC**	Interfaces the MCC.
	SCSDC	Interfaces the office alarms.
	TTYC and SDLC	Interfaces optional input/output devices.

2.7.7 Functional Description

2.7.7.1 Functions

The Input/Output Processor (IOP) does the following:

- Connects all *5ESS*® switch OA&M input and output devices with the AM.
- Connects technicians with the *5ESS*® switch to perform OA&M tasks.

2.7.7.2 Operation

The IOP interacts with other components to operate the switch.

Figure 2-14 depicts the operation of the IOP.

Figure 2-14 IOP Block Diagram

The following table details the operation of the IOP.

Stage	Description
1	The interface devices (such as the MTTY and ROP) receive OA&M requests (recent change, maintenance, data query, and CM, SM, power, and fuse alarms) from users of terminals and from operating systems by the metallic wires.

2	The interface devices send the OA&M requests to the peripheral controllers by the I/O ports.
3	The peripheral controllers convert and send the OA&M requests to the IOP controller by the IOMI.
4	The IOP Controller combines and sends the OA&M requests to the CU by the DSCH.
5	The IOP Controller receives OA&M control messages (configuration, status, alarms, and reports) from the CU by the DSCH.
6	The IOP Controller separates and sends the control messages to the peripheral controllers by the IOMI.
7	The peripheral controllers convert and send the control messages to the interface devices by the I/O ports.
8	The interface devices send the control messages to the operating systems and terminal devices by the metallic wires.

2.8 Common Network Interface (CNI) Ring

2.8.1 Basic Description

The Common Network Interface (CNI) Ring is one cabinet in the *5ESS*® switch.

The primary job of the CNI Ring is to receive and transmit signaling messages between the *5ESS*® switch and the Common Channel Signaling (CCS) network.

2.8.2 Electrical Power

Each Power Converter pack controls power for one-half of the Common Network Interface (CNI) Ring shelf. Power is fed to each shelf-mounted node through the MFFU panel. There are two power converters per shelf.

2.8.3 Shelf and Circuit Pack Arrangement

The Common Network Interface (CNI) Ring is one cabinet in the *5ESS*® switch that consists of a power panel, control panel, shelves for ring nodes and fan assembly. The Ring Node cabinet may contain from two to six shelves.

The following tables detail the shelf and circuit pack arrangement of the CNI Ring hardware components.

- The following table details the first CNI Ring that installed in an office.

EQL				
Vertical	**Horizontal**	**Component Name, Initial Shelf**	**Component Number**	
Various	008	**Power Supply (+5 Volts)**	410AA2	
Various	016	**IFB**	TN1803	RPCN
Various	024	**IRN2**	UN304B	
Various	034	**Blank**		
Various	042	**3BI**	TN914	
Various	050	**DDSBS**	TN69B	
Various	058	**IRN2**	UN304B	LN - 1
Various		**Blank**		
Various	076	**LI**	TN916	
Various	084	**IRN2**	UN304B	DLN
Various	094	**Blank**		
Various	102	**AP**	TN1630B	
Various	110	**3BI**	TN914	
Various	118	**DDSBS**	TN69B	
Various	126	**IRN2**	UN304B	LN - 3
Various	136	**Blank**		
Various	144	**LI**	TN916	
Various	152	**IRN2**	UN304B	LN - 4
Various	162	**LI**	TN916	
Various	170	**IFB**	TN1803	
Various	178	**Power Supply (+5 Volts)**	410AA	

- The following table details a CNI Ring that is installed to provide additional support in the office.

EQL				
Vertical	**Horizontal**	**Component Name, Growth Shelf**	**Component Number**	
Various	008	**Power Supply (+5, Volts)**	410AA	
Various	016	**IFB**	TN1803	

Various	024	**IRN2**	UN304	LN - 0
Various	034	**LI**	TN916	
Various	042	**IRN2**	UN304	LN - 1
Various	052	**LI**	TN916	
Various	060	**IRN2**	UN304	LN - 2
Various	070	**LI**	TN916	
Various	078	**IRN2**	UN304	LN - 3
Various	090	**LI**	TN916	
Various	098	**IRN2**	UN304	LN - 4
Various	108	**LI**	TN916	
Various	116	**IRN2**	UN304	LN - 5
Various	126	**LI**	TN916	
Various	134	**IRN2**	UN304	LN - 6
Various	144	**LI**	TN916	
Various	152	**IRN2**	UB304	LN - 7
Various	162	**LI**	TN916	
Various	170	**IFB**	TN1803	
Various	178	**Power Supply (+5 Volts)**	410AA	

2.8.4 Configuration

The following table details the configuration of the Common Network Interface (CNI) Ring.

Sub-Modules	Link/Bus	Connects to ...	Method of Operation	State of Operation
RPCN	Dual Ring Bus	LN	ACT/ACT	Duplex
	DSCH	AM		
DLN	Dual Ring Bus	LN	ACT/ACT	Duplex
	DSCH	AM		
LN	Dual Ring Bus	DLN	ACT/ACT	Duplex
		RPCN		
	Tip/Ring Wire	DFA or BAT		
LI	Dual Ring Bus	Next Link	ACT/ACT	Duplex

2.8.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Common Network Interface (CNI) Ring components are not available.

Unavailable Component	Alarm Level	Impact on Subscriber service	Impact on Switch Performance
RPCN	Critical	Subscribers can ONLY make local calls.	Loses CSS trunking and communication links.
LN	Critical	Subscribers can ONLY make local calls.	Loses CSS trunking and communication links.
DLN	Critical	Subscribers can ONLY make local calls.	Loses CSS trunking and communication links.

2.8.6 Detailed Description

The following table details the functions of the Common Network Interface (CNI) Ring components.

Part	Function
RPCN	The RPCN connects the AM CU to the CNI Ring for maintenance and high-level CCS messaging. The RPCN consists of the following circuit packs: □ **IRN2 pack** - Performs node processor and ring interface functions. □ **3BI pack** - Converts the 16-bit node point bus to the 32-bit peripheral bus interface on the DDSBS. □ **DDSBS pack** - Converts the 32-bit parallel format from the 3BI and the serial format of the DSCH to connect with the AM.
DLN	The DLN connects the AM DMA to the CNI ring for low-level CCS messaging. The DLN consists of the following circuit packs:

	□ **IRN2 pack** - Performs node processor and ring interface functions. □ **AP pack** - Translates ISDN User Part routing labels and Q.931 trunk identifiers into trunk scanner numbers. □ **3BI pack** - Converts the 16-bit node point bus to the 32-bit peripheral bus interface on the DDSBS. □ **DDSBS pack** - Converts the 32-bit parallel format from the 3BI and the serial format of the DSCH to connect with the AM.
LN	The LN connects the CCS network to the CNI Ring by a Signaling Link through the BAT board. The LN consists of the following circuit packs: □ **IRN2 pack** - Performs node processor and ring interface functions. □ **LI pack** - Transfers messages between the LN node processor and the BAT board.
BAT	The BAT board converts LN protocol to signaling link protocol on the backplane of the Ring Node Cabinet shelf and connects the LN to the STP by a carrier channel. The BAT board consists of a single pack.

2.8.7 Functional Description

2.8.7.1 Functions

The Common Network Interface (CNI) Ring transmits and receives CCS signaling messages between the *5ESS*® switch and the CCS network as follows:

- The RPCN connects the AM and the CNI Ring for CNI Ring maintenance activities.
- The DLN connects the AM and the CNI Ring for CCS signaling messages.
- The LN connects the CCS network and the CNI Ring for CCS signaling messages.
- The IUN connects sequential elements of the CNI Ring and acts as a place holder for future LN growth.

2.8.7.2 Operation

The CNI Ring interacts with other components to operate the switch.

Figures 2-15 , 2-16 , 2-17 , 2-18 , and 2-19 depict the operation of the CNI Ring.

Figure 2-15 CNI Ring Block Diagram

Figure 2-16 RCPN Block Diagram

Figure 2-17 DLN Block Diagram

Figure 2-18 LN Block Diagram

Figure 2-19 IUN Block Diagram

The following tables detail the operation of the CNI Ring.

When the RPCN receives a maintenance message from the AM:

Stage	RPCN Description
1	The DDSBS receives the message from the DMA by the DSCH and sends the message to the 3BI.
2	The 3BI receives the message from the DDSBS by the backplane and sends the message to the IRN2.
3	The IRN2 receives the message from the 3BI by the backplane, adds the destination token address, and sends the message by the ring to the LNs.
4	The addressed LN receives the message by the ring and executes the message.

When the DLN receives a call processing related CCS signaling message from the AM:

Stage	DLN Description
1	The DDSBS receives the message from the DMA by the DSCH and sends the message to the 3BI by the backplane.
2	The 3BI receives the message by the backplane and sends the message to the AP30 by the backplane.
3	The AP30 executes the message and either: □ Forwards the message to the IRN2 by the ring. □ Returns the result of the executed message to the DMA by the original path.
4	The IRN2 receives a message from the AP30 by the backplane, adds the destination token address, and sends the message by the ring to the LNs.
5	The addressed LN receives the message by the ring and sends the message to the CCS network by the signaling link.
When an LN receives a CCS call processing signaling message from the CCS network by the signaling link:	
1	The LN sends the message to the DLN by the ring.
2	The IRN2 receives the message by the ring and sends the message to the AP by the backplane.

3	The AP receives the message by the backplane and sends the message to the 3BI by the backplane.
4	The 3BI receives the message from the AP by the backplane and the 3BI sends the message to the DDSBS by the backplane.
5	The DDSBS receives the message from the 3BI by the backplane and the DDSBS sends the message to the DMA by the DSCH.

When the LN receives a call processing related CCS signaling message from the DLN:

Stage	LN Description
1	The IRN2 in the LN receives the message from the IRN2 in the DLN by the ring and sends the message to the LI by the backplane.
2	The LI receives the message by the backplane and sends the message to the BAT by the backplane.
3	The BAT receives the message by the backplane and sends the message to the CCS network by the signaling link.
When the LN receives a call processing CCS message from the CCS network by the signaling link	
1	The BAT receives the message from the CCS network by the signaling link and sends the message to the LI by the backplane.
2	The LI receives the message from the BAT by the backplane and sends the message to the IRN2 by the backplane.
3	The IRN2 in the LN receives the message from the LI by the backplane and sends the message to the IRN2 in the DLN by the ring.

3. COMMUNICATION MODULE, MODEL 2 (CM2)

3.1 Communication Module, Model 2 (CM2)

3.1.1 Basic Description

The Communications Module, Model 2 (CM2) is a multi-unit module. The CM2 is located in the *5ESS*® switch.

The primary job of the CM2 is to switch calls between the switching modules.

3.1.2 Electrical Power

Power for the Communications Module, Model 2 (CM2) is removed at the unit and sub-unit levels.

3.1.3 Shelf and Circuit Pack Arrangement

The Communications Module, Model 2 (CM2) is located in the *5ESS*® switch.

Figure 3-1 depicts the shelf arrangement of the CM2.

Figure 3-1 CM2 Shelf Arrangement

The following tables detail the shelf arrangement of the CM2 hardware components.

In the minimum configuration, the CM2 occupies CM cabinets 5 and 6. CM2 cabinets 5 and 6 each contain six shelves.

Vertical EQL	Component Name
62	**CMPU**
53	**MSPU**
45	**MSCU**
36	**TMSU**

28	**CMCU**
19	**TMSU**

In the maximum configuration, the CM2 occupies CM cabinets 0 through 11. CM2 cabinets 0 through 4 and 7 through 11 each contain five shelves.

Vertical EQL	Component Name
53	**MSPU**
45	**EBUS**
36	**TMSU**
28	**EBUS**
19	**TMSU**

3.1.4 Configuration

The following table details the configuration of the Communications Module, Model 2 (CM2).

Sub-Modules	Link/Bus	Connects to ...	Method of Operation	State of Operation
MSGS	DSCH	AM	Duplex	ACT/ACT
	MIB	ONTCCOM		
	CDAL			
	QGL			
ONTCCOM	MIB	MSGS	Duplex	ACT MAJ/ ACT MIN
	CDAL			
	QGL			
	NCT/ NCT2	SM/ SM-2000		
	Clock Reference Leads	Misc. Frame		
NOTE: The *5ESS*® switch can be configured with other CM models. This table details the configuration of the CM2.				

The following table details the units that the CM2 are contained in.

Diagnosable Units	Shelf Units	Diagnosable Components
MSGS	MSCU	FPC, PPC, and MSC
	MSPU	MMP
	CMPU	CMP and QGP
ONTC	CMCU, TMSU3, and EBUS	ONTCCOM and QLPS
	MCTU2 or MCTU3	DLI
	TSIU4 or TSIU5	NLI
ONTCCOM	CMCU	NCLK, MI, and Control part of the TMS
	TMSU3	Part of the TMS and QLPS (not part of ONTCCOM diagnostic)
	EBUS	Part of the TMS
QLPSNW	TMSU3	QLPS
	CMPU	QGP
	SMPU4 or SMPU5	MH (SM-2000)
	PSU	QPH (SM-2000)

The following table details the link that the switch uses to route call processing control messages.

Hardware Unit Links and Buses	Shelf Unit	Diagnosable Components
C-Link	TSIU4 or TSIU5	CTSNS (SM-2000 only)
		NLI
	MCTU2 or MCTU3	DIP switch (SM only)
	NCT/NCT2 links	
	CMCU, TMSU3, and EBUS	TMS
	MIB	
	CMCU	MI
	MSPU	MMP

3.1.5 Service Impacts

Go to the diagnosable hardware maintenance groupings □ MSGS and ONTCCOM.

3.1.6 Detailed Description

The following table details the functions of diagnosable sub-units in the Communications Module, Model 2 (CM2).

Sub-Module	Function
MSGS	Routes control messages between all switching module, CM, and AM processors.
ONTCCOM	The ONTCCOM perform the following: □ Switch subscriber calls between the switching modules. □ Switch control messages. □ Distribute clock pulses from the Network Clock.

3.1.7 Functional Description

3.1.7.1 Functions

The Communications Module, Model 2 (CM2) does the following:

- Switches the subscriber data between the switching modules.
- Routes control messages between the switching modules, CM, and AM processors.
- Generates and sends control messages in the MSGS to the ONTCCOM and the switching modules.
- Receives timing signals from sources external to the *5ESS*® switch.
- Generates and sends Network Clock pulses in the ONTCCOM to the MSGS and the switching modules.

3.1.7.2 Operation

Figure 3-2 depicts the operation of the CM2.

Figure 3-2 CM2 Block Diagram

The following tables detail the operation of the CM.

The CM handles subscriber data and control messages between the switching modules.

Stage	Description
1	The CM receives subscriber data and control messages from switching modules by the NCT/NCT2 links.
2	The CM performs the following: □ When the message is data-specific, then the CM sends the subscriber data to a switching module by the NCT/NCT2 links. □ When the message is control-specific, then the CM either: A. Executes the control message, B. Routes the message to the switching module by the NCT/NCT2 links, or C. Routes the message to the AM by the DSCH.

The CM handles control messages from the AM.

Stage	Description
1	The CM receives control messages from the AM by the DSCH.
2	The CM preforms either of the following: A. Executes the control message, or B. Routes the message to the switching module by the NCT/NCT2 links.

The CM handles external timing references.

Stage	Description
1	The CM receives a timing signal by the external clock leads.
2	The CM performs the following: □ Adjusts the internal clock to synchronize with the timing signal. □ Generates a clock pulse. □ Distributes the clock pulse to the switching modules.

3.2 Message Switch (MSGS)

3.2.1 Basic Description

The Message Switch (MSGS) is a database that is used to diagnose a group of individually diagnosable components. That include, the FPC, PPC, MMP, CMP, QGP and MSC/MSCU.

NOTE: The term MSGS appears only on the MCC screen.

3.2.2 Service Impacts

The functions of the MSGS components are related. When one component in the MSGS goes out-of-service, then all components in the MSGS are impacted as detailed in the following table:

Unavailable Component	Alarm Level	Impact on Subscriber Service	Impact on Switch Performance

MSGS	One side	Major	No impact.	Reduces the MSGS to the simplex mode.
	Both Sides	Critical	No new inter-SM calls. Stable calls may be lost.	Isolates the ONTCCOM from the AM. Causes an AM initialization.

3.3 Message Switch Controller Unit (MSCU)

3.3.1 Basic Description

The Message Switch Controller Unit (MSCU) is a one to four-circuit pack component. The MSCU is located in the MSCU3 shelf of the CM2 cabinets 5 and 6.

The primary job of the MSCU is to route control messages between the MSGS peripherals - MMP, FPC, PPC, QGP, and CMP.

NOTE: The term MSCU refers to the diagnosable component. The term MSCU3 refers to the shelf that contains the MSCU.

3.3.2 Electrical Power

The SN516 Control and Display circuit pack controls power for the Message Switch Controller Unit (MSCU).

3.3.3 Shelf and Circuit Pack Arrangement

The Message Switch Controller Unit (MSCU) is located in the MSCU3 shelf which also contains the Pump Peripheral Controller (PPC), and the Foundation Peripheral Controller (FPC).

Figure 3-3 depicts the shelf and circuit pack arrangement of the MSCU.

Figure 3-3 MSCU Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the MSCU hardware components.

EQL			
Vertical	**Horizontal**	**Component Name**	**Component Number**
45	056	**Control and Display**	SN516
45	082	**Power Supply**	495FB
45	106	**IOMI D**	UN25B
45	120	**IOMI C**	UN25B
45	134	**IOMI B**	UN25B
45	156	**IOP2**	KBN10

3.3.4 Configuration

The following table details the configuration of the Message Switch Controller Unit (MSCU).

Circuit pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
IOP2	IOMI Bus 0	CMP, QGP, MMP, PPC, and FPC	Duplex	ACT/ ACT
	DSCH	AM		
	Backplane	IOMI B, C, and D		
IOMI C	IOMI Bus 2	QGP	Duplex	ACT/ACT
		MMPs		
IOMI B and D	IOMI Busses 1 and 3	MMPs	Duplex	ACT/ACT

3.3.5 Detailed Description

The following table details the functions of the circuit packs in the Message Switch Controller Unit (MSCU).

Part	Function
IOP2	The IOP2 perform the following: □ Uses CM peripherals to route control messages between the switching modules. □ Processes data and instructions from the MSGS peripherals and the AM. □ Connects the AM to the CM. □ Connects MSGS peripherals - MMP, FPC, PPC, and CMP. ***NOTE:*** The MSCU contains a circuit that functions as an IOMI circuit pack.
IOMI	Connects MSGS peripherals for communication between the QGP and growth MMPs.

3.3.6 Functional Description

3.3.6.1 Functions

The Message Switch Controller Unit (MSCU) preforms the following:

- Routes control messages between the MSGS peripherals - MMP, FPC, PPC, QGP, and CMP.
- Connects the CM to the AM.
- Connects the MSGS peripherals for communication between the switching modules, and between the switching modules and the AM.
- Controls the operation of the MSGS peripherals.

3.3.6.2 Operation

Figure 3-4 depicts the operation of the MSCU.

Figure 3-4 MSCU Block Diagram

The following tables detail the operation of the MSCU.

The MSCU handles control messages from the AM.

Stage	Description
1	The IOP2 pack receives a control message from the AM by the DSCH.
2	The IOP2 pack reads the address and either executes or sends the message to the IOMI pack by the backplane or an internal circuit.
3	The IOMI pack or internal circuit receives and sends the message to the FPC, PPC, MMP, CMP or QGP.

The MSCU handles control messages between the MSGS peripherals.

Stage	Description
1	The IOMI pack or the internal circuit of the MSCU pack receives a control message from the MMP, FPC, PPC, CMP or QGP by the IOMI bus.
2	When the IOMI pack receives the message, then the IOMI pack sends the message to the MSCU pack by the backplane.
3	The IOP2 pack receives and routes the message to the MMP, FPC, PPC, CMP, QGP or AM.

3.4 Message Switch Control Unit, Model 3 (MSCU3)

3.4.1 Basic Description

The Message Switch Control Unit, Model 3 (MSCU3) is a shelf. The MSCU3 shelf is located in CM2 cabinets 5 and 6.

The MSCU3 shelf contains the diagnosable components: the PPC, FPC and MSCU.

3.4.2 Shelf and Circuit Pack Arrangement

The Message Switch Control Unit, Model 3 (MSCU3) is located in CM cabinets 5 and 6.

Figure 3-5 depicts the shelf and circuit pack arrangement of the MSCU3.

Figure 3-5 MSCU3 Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the MSCU3 shelf hardware components.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
45	032 and 040	**PPC**	*
45	048 and 056	**FPC**	*
45	106 to 156	**MSCU**	*
45	008 and 066	**Control and Display**	SN516
45	024 and 082	**Power Converter**	495FB
NOTE: ******* Go to the PPC, FPC, and MSCU hardware descriptions for circuit pack numbers.			

3.5 Foundation Peripheral Controller (FPC)

3.5.1 Basic Description

The Foundation Peripheral Controller (FPC) is a two-circuit pack component. The FPC is located in the MSCU3 shelf of the CM2 cabinets 5 and 6.

The primary job of the FPC is to send network time slot control messages to the TMS.

3.5.2 Electrical Power

The Control and Display pack is located at the left end of the MSCU3 shelf and controls power for the Foundation Peripheral Controller (FPC) and the Pump Peripheral Controller (PPC).

3.5.3 Shelf and Circuit Pack Arrangement

The Foundation Peripheral Controller (FPC) is located in the MSCU3 shelf of the CM. CM cabinets 5 and 6 each contain one MSCU3 shelf.

Figure 3-6 depicts the shelf and circuit pack arrangement of the FPC.

Figure 3-6 FPC Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the FPC hardware components.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
45	008	**Control and Display**	SN516
45	024	**Power Converter**	495FB
45	048	**MSPP**	TN856B and TN856C
45	056	**FPC**	UN173

3.5.4 Configuration

The following table details the configuration of the Foundation Peripheral Controller (FPC).

Circuit Pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
MSPP	Internal to shelf or backplane	IOP2	Duplex	ACT/STBY
		FPC Pack		
FPC	Internal to shelf or backplane	MSPP Pack	Duplex	ACT/STBY
	CDAL	DMI		

3.5.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Foundation Peripheral Controller (FPC) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
FPC	One side	Major	No impact.	Reduces the FPC to the simplex mode.
	Both sides	Critical	Removes all inter-switching module calls from service.	Stops processing of all inter-switching module call.

3.5.6 Detailed Description

The following table details the functions of the circuit packs in the Foundation Peripheral Controller (FPC).

Part	Function
MSPP	Sends control messages between IOMI bus 0 and the FPC pack.
FPC	Converts messages between the MSPP pack and the DMI Controller.

3.5.7 Functional Description

3.5.7.1 Functions

The Foundation Peripheral Controller (FPC) performs the following:

- Routes network time slot control messages.
- Routes, stores, and executes control messages for the ONTCCOM.
- Enables two processors (the MSCU and DMI) of different protocols to exchange control messages.

3.5.7.2 Operation

The FPC interacts with other components to operate the switch.

Figure 3-7 depicts the operation of the FPC.

Figure 3-7 FPC Block Diagram

The following tables detail the operation of the FPC.

The FPC handles control messages from the MSCU.

Stage	Description
1	The FPC receives an control message from the MSCU by the IOMI.
2	The FPC performs the following: - When the control message from the SM is call processing-specific, then the FPC sends the message to the DMI by the CDAL. - When the control message from the AM is maintenance-specific, then the FPC either executes or sends the message to the DMI by the CDAL.

The FPC handles control messages from the DMI.

Stage	Description

1	The FPC receives an ONTCCOM control message from the DMI by the CDAL.
2	The FPC sends the message to the MSCU by the IOMI.

3.6 Pump Peripheral Controller (PPC)

3.6.1 Basic Description

The Pump Peripheral Controller (PPC) is a two-pack component. The PPC is located in an MSCU3 shelf of CM2 cabinets 5 and 6.

The primary job of the PPC is to rapidly reload SM software. The PPC temporarily stores and sends a high volume of control messages from the AM to the switching modules.

3.6.2 Electrical Power

The Control and Display circuit pack is located at the left end of the MSCU3 shelf and controls power for the Pump Peripheral Controller (PPC) and Foundation Peripheral Controller (FPC).

3.6.3 Shelf and Circuit Pack Arrangement

The Pump Peripheral Controller (PPC) is located in the MSCU3 shelf of the CM. CM cabinets 5 and 6 each contain one MSCU3 shelf.

Figure 3-8 depicts the shelf and circuit pack arrangement of the PPC.

Figure 3-8 PPC Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the PPC hardware components.

EQL		Component Name	Component Number
Vertical	Horizontal		
45	008	**Control and Display**	SN516
45	024	**Power Converter**	495FB
45	032	**MSPP**	TN856B or TN856C
45	040	**PPC**	TN886

3.6.4 Configuration

The following table details the configuration of the Pump Peripheral Controller (PPC).

Circuit Pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
MSPP	Internal to shelf or backplane	MSCU IOMI 0 PPC Pack	Duplex	ACT/STBY
PPC	Internal to shelf or	MSPP Pack	Duplex	ACT/STBY

	backplane			
	MIB	DMI		

3.6.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Pump Peripheral Controller (PPC) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
PPC	One side	Major	No impact.	Reduces the PPC to the simplex mode.
	Both sides	Critical	Slows recovery of circuits in the impacted SMCs.	Increases the time that is required to reload a switching module by 16 times.

3.6.6 Detailed Description

The following table details the functions of the circuit packs in the Pump Peripheral Controller (PPC).

Part	Function
MSPP	Processes control messages.
PPC	Converts control messages between the MSPP and the DMI in the CMCU.

3.6.7 Functional Description

3.6.7.1 Functions

The Pump Peripheral Controller (PPC) performs the following:

- Rapidly reloads the SM software via a high volume of control messages from the AM.
- Enables two processors (the MSCU and DMI) of different protocols to exchange control messages.

3.6.7.2 Operation

The PPC interacts with other components to operate the switch.

Figure 3-9 depicts the operation of the PPC.

Figure 3-9 PPC Block Diagram

The following table details the operation of the PPC.

The PPC handles control messages from the AM.

Stage	Description
1	The PPC receives a control message from the AM through MSCU by the IOMI.
2	The PPC temporarily stores and then sends the message to the DMI by the MIB.

3.7 Message Switch Processor Unit (MSPU)

3.7.1 Basic Description

The Message Switch Peripheral Unit, Model 3 (MSPU3) is a shelf. The MSPU3 is located in each CM2 cabinet.

The MSPU3 contains the diagnosable component: the MMP.

3.7.2 Shelf and Circuit Pack Arrangement

The Message Switch Peripheral Unit, Model 3 (MSPU3) is located in each CM cabinet. Each CM cabinet contains one MSPU3 shelf.

Figure 3-10 depicts the shelf and circuit pack arrangement of the MSPU3.

Figure 3-10 MSPU3 Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the MSPU3 hardware components.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
53	032 - 176	**MMP**	*
53	008	**Control and Display**	SN516
53	024	**Power Converter**	495FB
NOTE: ******* MMP circuit pack numbers are detailed in the MMP hardware description.			

3.8 Module Message Processor (MMP)

3.8.1 Basic Description

The Module Message Processor (MMP) is a two-circuit pack component. The MMP is located in the MSPU shelves of all CM2 cabinets.

The primary job of the MMP is to route control messages between the SMs and the SM-2000, QGP, AM, CNI, and FPC.

3.8.2 Electrical Power

Two Control and Display circuit packs control power for all the MMPs:

- The circuit pack at the left end of the MSPU3 shelf controls power for the MMPs on the left side of the MSPU3 shelf.
- If equipped, the circuit pack in the center of the MSPU3 shelf controls power for the MMPs on the right side of the MSPU3 shelf.

3.8.3 Shelf and Circuit Pack Arrangement

The Module Message Processor (MMP) is located in the MSPU3 shelf of all CM2 cabinets. Each CM2 cabinet contains one MSPU3 shelf.

Figure 3-11 depicts the shelf and circuit pack arrangement of the MMP.

Figure 3-11 MMP Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the MMP.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
Various	Various	**MSPP**	TN856B or TN856C
Various	Various	**MMP**	TN870

3.8.4 Configuration

In the minimum MMP configuration, an MSPU3 shelf contains between one and four MMPs. In the maximum MMP configuration, with Dual MMPs, an MSPU3 shelf contains between two and eight MMPs. The Dual MMP configuration is an engineering decision that does not impact the normal operation of the MSPU3/MMP.

The following table details the configuration of the Module Message Processor (MMP).

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
MSPP	IOMI	MSCU	Duplex	ACT/ACT, STBY/STBY*****
	Internal to shelf or backplane	MIBC		
MIBC	Internal to shelf or backplane	MSPP		
	MIB	CMCU		
***NOTE:* *** Maximum configuration only.				

3.8.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Module Message Processor (MMP) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
MMP	One side	Major	No impact.	Reduces the MMP to the simplex mode.
	Both sides	Critical	Stops inter-SM call processing for up to eight SMs.	Stops system communication between up to eight SMs and the rest of the switch.

3.8.6 Detailed Description

The following table details the functions of the circuit packs in the Module Message Processor (MMP).

Part	Function
MSPP	Routes control messages.
MIBC	Converts control messages between the MSPP pack and the DMI.

3.8.7 Functional Description

3.8.7.1 Functions

The Module Message Processor (MMP) performs the following:

- Routes control messages between the:
  - switching modules, or
  - switching modules and SM-2000, AM, CNI, and FPC.
- Allows two processors (the MSCU and DMI) of different protocols to exchange control messages.

3.8.7.2 Operation

Each MMP interacts with other components to operate the switch.

Figure 3-12 depicts the operation of the MMP.

Figure 3-12 MMP Block Diagram

The following tables detail the operation of the MMP.

The MMP handles control messages from the DMI.

Stage	Description
1	The MMP receives a control message from the DMI by the MIB.
2	The MMP performs the following: - When the control message is call processing-specific for the SM-2000, then the MMP sends the message to the DMI by the MIB.

	□ When the control message is maintenance- specific, then the MMP sends the message to the MSCU by the IOMI.

The MMP handles control messages from the MSCU.

Stage	Description
1	The MMP receives a control message from the MSCU by the IOMI.
2	The MMP performs the following: □ When the control message is call processing-specific, then the MMP sends the message to the DMI by the MIB. □ When the control message is maintenance-specific, then the MMP either executes or sends the message to the DMI by the MIB.

3.9 Communications Module Processor Unit (CMPU)

3.9.1 Basic Description

The Communications Module Processor Unit (CMPU) is a shelf. The CMPU is located in the CM cabinets 5 and 6.

The CMPU contains the diagnosable components: the CMP and the QGP.

3.9.2 Shelf and Circuit Pack Arrangement

The Communications Module Processor Unit (CMPU) is located in the CM cabinet.

Figure 3-13 depicts the shelf and circuit pack arrangement of the CMPU.

Figure 3-13 CMPU Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the CMPU hardware components.

EQL		Component Name	Component Number
Vertical	Horizontal		
62	096 - 136	**CMP**	*
62	008 - 040	**QGP**	*
62	008 and 096	**Control and Display**	SN516
62	024 and 112	**Converter**	410AA
NOTE: * See the CMP and QGP hardware descriptions for the CMP and QGP circuit pack numbers.			

3.10 Communications Module Processor (CMP)

3.10.1 Basic Description

The Communications Module Processor (CMP) is a six-circuit pack component. The CMP is located in the CMPU shelf of CM2 cabinets 5 and 6.

The primary job of the CMP is to assign network time slots for each inter-switching module subscriber call.

3.10.2 Electrical Power

The Power Control and Display circuit pack controls power for the Communications Module Processor (CMP). The Power Control and Display circuit pack is located in the right half of the CMPU shelf.

3.10.3 Shelf and Circuit Pack Arrangement

The Communications Module Processor (CMP) is located in the right half of the CMPU shelf.

Figure 3-14 depicts the shelf and circuit pack arrangement of the CMP.

Figure 3-14 CMP Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the CMP hardware components.

EQL		Component Name	Component Number
Vertical	Horizontal		
62	096	**Power Control and Display**	SN516
62	112	**Power Converter**	410AA
62	120	**CMP**	TN1368 or TN1800
62	128	**Memory**	TN1369

3.10.4 Configuration

The following table details the configuration of the Communications Module Processor (CMP).

Circuit Pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
CMP	IOMI Bus 2	MSCU	Duplex	ACT/STBY
	Backplane	Memory		
Memory	Backplane	CMP		

3.10.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Communications Module Processor (CMP) components are not available.

		Impact on Subscriber	

Unavailable Component		Alarm Level	Service	Impact on Switch Performance
CMP	One side	Major	May have a minor impact.	MSGS operates in the simplex mode.
	Both sides	Critical	Interrupts service.	Stops new inter-switching module calls.

3.10.6 Detailed Description

The following table details the functions of the circuit packs in the Communications Module Processor (CMP).

Part	Function
CMP	Monitors and distributes ODD recent changes and (network time slot) control messages.
Memory	Stores ODD recent change control messages (trunk or routing specific).

3.10.7 Functional Description

3.10.7.1 Functions

The Communications Module Processor (CMP) performs the following:

- Monitors and distributes (network time slot) control messages for inter-switching module calls.
- Monitors and distributes ODD [recent change] control messages.
- Stores trunk routing tables, identities, and the structure of the CM and switching modules.

3.10.7.2 Operation

The CMP interacts with other components to operate the switch.

Figure 3-15 depicts the operation of the CMP.

Figure 3-15 CMP Block Diagram

The following tables detail the operation of the CMP.

The CMP handles requests for network time slot .

Stage	Description
1	The CMP receives a request for a network time slot from the MSCU by the IOMI.
2	The CMP assigns a network time slot control message to the MSCU by the IOMI.

The CMP handles ODD recent change control messages.

Stage	Description
1	The CMP receives an (ODD recent change) control message through the AM from the MSCU by the IOMI.
2	The CMP either stores the (ODD recent change) control message (trunk or routing specific) or sends the message (line specific) to the switching module through the MSCU by the IOMI. (Periodically, the CMP automatically sends the message to the DFC for long-term storage through the DMA.)

3.11 QLPS Gateway Processor (QGP)

3.11.1 Basic Description

The QLPS Gateway Processor (QGP) is a two-circuit pack component. The QGP is located in the CMPU shelf of CM2 cabinets 5 and 6.

The primary job of the QGP is to enable the MSCU and QLPS to exchange control messages.

3.11.2 Electrical Power

The Control and Display circuit pack controls power for the QLPS Gateway Processor (QGP). The Power Control and Display circuit pack is located in the left end of the CMPU shelf.

3.11.3 Shelf and Circuit Pack Arrangement

The QLPS Gateway Processor (QGP) is located in the CMPU shelf of CM2 cabinets 5 and 6. The QGP circuit packs are located in the CMPU shelf of CM2 cabinets 5 and 6.

Figure 3-16 depicts the shelf and circuit pack arrangement of the QGP.

Figure 3-16 QGP Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the QGP hardware components.

EQL			
Vertical	Horizontal	Component Name	Component Number
62	008	**Power Control and Display**	SN516
	024	**Power Unit**	410AA

	032	**QLPS Gateway Processor**	TN1683
	040	**Gateway Interface**	TN1684

3.11.4 Configuration

The following table details the configuration of the QLPS Gateway Processor (QGP).

Circuit Pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
QGP	IOMI	IOMI-C pack in MSCU	Duplex	ACT/STBY
	Backplane	GWI		
GWI	IOMI	IOMI-C pack in MSCU		
	Q-Link	Four QLPS packs		

3.11.5 Service Impacts

The following table details the impact on subscriber service and switch performance when QLPS Gateway Processor (QGP) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
QGP	One side	Major	No impact.	No impact .
	Both sides	Critical	May deny service.	MMPs handle messages normally routed through the QGP until all of the capacity of the MMP is used.

3.11.6 Detailed Description

The following table details the functions of circuit packs in the QLPS Gateway Processor (QGP).

Part	Function
QGP	The QGP performs the following: □ Handles messages between the QLPS and AM. □ Handles CCS control messages between QLPS and CNI/DLN through the AM. □ Handles control messages between the QLPS and SM through the MMP. □ Handles control messages between the SM-2000 and the FPC.
GWI	Connects the QGP and the QLPS.

3.11.7 Functional Description

3.11.7.1 Functions

The QLPS Gateway Processor (QGP)enables the MSCU and QLPS to exchange control messages.

3.11.7.2 Operation

The QGP interacts with other components to operate the switch.

Figure 3-17 depicts the operation of the QGP.

Figure 3-17 QGP Block Diagram

The following tables detail the operation of the QGP.

- The QGP handles control messages from the QLPS.

Stage	Description
1	The QGP receives a control message from the QLPS by the Q-link.
2	The QGP sends the message to the MSCU by the IOMI.

- The QGP handles control messages from the MSCU.

Stage	Description
1	The QGP receives a control message from the MSCU by the IOMI.
2	The QGP also performs the following: - When the control message is call processing-specific, then the QGP sends the message to the QLPS by the Q-Link. - When the control message is maintenance-specific, then the QGP executes the message.

3.12 Office Network Timing Complex (ONTC)

3.12.1 Basic Description

The Office Network Timing Complex (ONTC) is a hardware maintenance grouping that is a group of individually diagnosable components. That include: the ONTCCOM***** (MI, NC and TMS), DLI******, NLI****** and QLPS.

The term ONTC appears only on the MCC screen.

***NOTE:* *** The ONTCCOM is also a software name used only on the MCC screen.

NOTE:* * The DLI and NLI are individually diagnosable. The DLI and NLI are located in the switching

module cabinets but are functionally part of the ONTC.

3.12.2 Service Impacts

The operations of the Office Network Timing Complex (ONTC) components inter-dependent. When one component in the ONTC goes out-of-service, then the service of all other components in the ONTC is impacted.

3.13 Communications Module Control Unit (CMCU)

3.13.1 Basic Description

The Communications Module Control Unit (CMCU) is a shelf. The CMCU is located in CM cabinets 5 and 6.

The CMCU contains the diagnosable components: the NCLK, MI, and the control part of the TMS.

3.13.2 Shelf and Circuit Pack Arrangement

The Communications Module Control Unit (CMCU) is located in CM cabinets 5 and 6.

Figure 3-18 depicts the shelf and circuit pack arrangement of the CMCU.

Figure 3-18 CMCU Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the CMCU hardware components.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
28	146 to 178	**DMI/MI**	*
28	048 to 080	**NCLK**	*
28	008	**Control and Display**	SN516
28	024, 088, and 104	**Power Converter**	495KA, 410AA, and 495MA
28	112 to 138	**Control part of the TMS**	*
NOTE: ***** See the DMI, NCLK, and TMS hardware descriptions for circuit pack numbers.			

3.14 Dual Message Interface (DMI)

3.14.1 Basic Description

The Dual Message Interface (DMI) is a five circuit-pack component. The DMI is located in the CMCU shelves of the CM2 cabinets 5 and 6.

The primary job of the DMI is to route multiplexed, serial data control messages between the TMSU and

the MMPs.

NOTE: The MCC screen and I/O printouts refer to the DMI as the MI.

3.14.2 Electrical Power

The Control and Display circuit pack controls power for the Dual Message Interface (DMI). The Control and Display circuit pack is located at the left end of the CMCU shelf.

3.14.3 Shelf and Circuit Pack Arrangement

The Dual Message Interface (DMI) is located in the CMCU shelf of the CM2 cabinets 5 and 6. Each CM2 cabinet contains one CMCU shelf.

Figure 3-19 depicts the shelf and circuit pack arrangement of the DMI.

Figure 3-19 DMI Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the DMI circuit packs.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
28	008	**Control and Display**	SN516
28	024	**Power Converter**	495KA
28	146 and 178	**DMI Receiver**	TN1034
28	162	**DMI Controller**	UN187
28	170 and 154	**DMI Transmitter**	UN186

3.14.4 Configuration

The following table details the configuration of the Dual Message Interface (DMI).

Circuit Pack	Link/ Bus	Connects to...	Method of Operation	State of Operation
DMI Receiver	MIB	MMP	Duplex	ACT Major/ACT Minor
		PPC		
	FLI Bus	FLI		
	Internal to shelf or backplane	DMI Controller		
		DMI Transmitter		
DMI Controller	Internal to shelf or backplane	DMI Receiver	Duplex	ACT Major/ACT Minor
		DMI Transmitter		
		TMS Controller		
		Network Clock		
	CDAL	FPC		
DMI Transmitter	MIB	MMP	Duplex	ACT Major/ACT Minor

		PPC		
	FLI Bus	FLI		
	Internal to shelf or backplane	DMI Controller		
		DMI Transmitter		

3.14.5 Service Impacts

The DMI is part of the: the ONTCCOM. When the DMI is out-of-service, then the NCLK and TMS go are impacted. For service impact information, go to the ONTCCOM.

3.14.6 Detailed Description

The following table details the functions of the circuit packs in the Dual Message Interface (DMI).

Part	Function
DMI	Distributes control messages between: □ MSGS □ SM and SM-2000 □ TMS controller.
	Distributes time signals to the: □ TMS controller □ MSGS.

3.14.7 Functional Description

3.14.7.1 Functions

The Dual Message Interface (DMI) performs the following:

- Routes control messages between the switching modules and MMPs for call processing and maintenance.
- Routes control messages between the TMSC and FPC to set up network time slots for customer calls.
- Routes [maintenance] control messages for the NCLK.
- Routes [maintenance] control messages that are used to rapidly reload switching module software from the PPC.
- Enables processors of different protocols to exchange control messages.

3.14.7.2 Operation

The DMI interacts with other components to operate the switch.

Figure 3-20 depicts the operation of the DMI.

Figure 3-20 DMI Block Diagram

The following tables detail the operation of the DMI.

The DMI Receiver pack handles control messages from the MMP and PPC.

Stage	Description
1	The DMI Receiver performs the following: □ Receives [call processing and maintenance] control messages from the MMP by the MIB, or □ Receives [maintenance] control messages from the AM through the PPC by the MIB.
2	The DMI Receiver combines the messages from the multiple bit streams into a single bit stream.
3	The DMI Receiver sends a single bit stream control message to the TMSU by the FLI bus.

The DMI Transmitter handles control messages from the TMSU.

Stage	Description
1	The DMI Transmitter receives [call processing and maintenance] control messages from the TMSU by the FLI bus.
2	The DMI Transmitter splits the messages from a single bit stream into multiple bit streams.
3	The DMI Transmitter sends multiple bit stream control messages to the MMPs by the MIBs.

The DMI controller pack handles control messages from the FPC.

Stage	Description
1	The DMI Controller pack receives [call processing] control messages from the FPC by the CDAL.
2	The DMI Controller pack also performs the following: □ When the message is call processing-specific, then the DMI Controller pack routes the message to the TMS Controller by the backplane. □ When the message is maintenance-specific, then the DMI Controller pack either executes or routes the message to the following:

	A. The TMS Controller by the backplane, or B. The NCLK by the backplane.

The DMI handles timing pulses from the NCLK.

Stage	Description
1	The DMI Receiver and DMI Transmitter packs receive a timing signal from the NCLK by the EBUS.
2	The DMI Receiver packs and the DMI Transmitter packs use the timing signal to adjust their internal timing signals.
3	The DMI Receiver and DMI Transmitter packs send the timing signal to the DMI Controller by the backplane.
4	The DMI Controller receives and uses the timing signal to adjust the internal timing signals.

3.15 Network Clock (NCLK)

3.15.1 Basic Description

The Network Clock (NCLK) is a three-circuit pack component. The NCLK is located in the CMCU shelf of CM2 cabinets 5 and 6.

The primary job of the NCLK is to generate the clock pulses that are used to synchronize time in the TMS controller and MSGS.

3.15.2 Electrical Power

The Control and Display circuit pack controls power for all Network Clock (NCLK) circuit packs, except the oscillator pack. The Control and Display circuit pack is located at the left end of the CMCU shelf.

The Modular Fuse/Filter Unit (MFFU) controls power for the oscillator pack.

3.15.3 Shelf and Circuit Pack Arrangement

The Network Clock (NCLK) is located in the CMCU shelf of the CM2 cabinets 5 and 6.

Figure 3-21 depicts the shelf and circuit pack arrangement of the NCLK.

Figure 3-21 NCLK Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the NCLK hardware components.

EQL		Component Name	Component Number
Vertical	Horizontal		
28	048	**NCLK Oscillator**	TN1283, TN1284, TN1285, and TN1286
28	058	**NCLK Synchronizer**	TN1274B and TN1275B
28	070	**NCLK Controller**	TN1276
28	080	**NCLK Synchronizer (Optional)**	TN1275B

3.15.4 Configuration

The following table details the configuration of the Network Clock (NCLK).

Circuit Pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
NCLK Oscillator	Backplane	NCLK Controller	Duplex	ACT/ ACT
NCLK Synchronizer	Metallic cable	External timing source	Duplex	ACT/ ACT
	Backplane	DLTU to Bridging Repeater		
		NCLK Controller		
NCLK Controller	Backplane	NCLK Oscillator and Synchronizer	Duplex	ACT/ ACT
		TMS Controller		
		DMI Controller		

3.15.5 Service Impacts

The NCLK is part of the ONTCCOM. When the NCLK goes out-of-service, then the TMS and MI are impacted. For service impact information, go the ONTCCOM.

3.15.6 Detailed Description

The following table details the functions of circuit packs in the Network Clock (NCLK).

Part	Function
NCLK Oscillator	Generates clock pulses.
NCLK Synchronizer	Uses external reference and backup signals to generate clock pulses.
NCLK Controller	Synchronizes the oscillator clock pulses with the synchronizer clock pulses.

3.15.7 Functional Description

3.15.7.1 Functions

The Network Clock (NCLK) performs the following:

- Synchronizes internal oscillator clock pulses with network reference sources.
- Generates clock pulses for the TMS controller and the MSGS.

3.15.7.2 Operation

The NCLK interacts with other components to operate the switch.

Figure 3-22 depicts the operation of the NCLK.

Figure 3-22 NCLK Block Diagram

The following tables detail the operation of the NCLK.

The NCLK generates clock pulses for the TMS controller.

Stage	Description	
1	The oscillator packs generate clock pulses.	
2	The cross-coupled oscillator packs send the pulses to the controller packs by the TB0 or TB1.	
3	The controller pack sends the time base signals TB0 and TB1 to the synchronizer pack.	
4	The synchronizer packs receive reference timing signals.	
	When	**Then**
	The synchronizer pack receives an analog pulse by the office timing supply,	1. The synchronizer pack temporarily stores each pulse. 2. The synchronizer pack counts the reference time base signal in each external clock interval and sends the pulse count to the controller pack by the TBA or TBB.
	The synchronizer pack receives a backup digital pulse from either the office repeater bay or the DFI in the DLTUs,	1. The synchronizer pack temporarily stores each pulse. 2. The synchronizer pack counts the reference time base signal in each external clock interval and sends the pulse count to the controller pack by the TBA or TBB.
	The controller packs performs the following:	

	□ Receive pulse counts from the synchronizer packs. □ Calculate the average difference. □ Use this data to control a Digital Phase Lock Loop (DPLL).
6	The DPLL generates and sends an 8 KHz pulse to the following: □ The TMS clock by the backplane. □ The mate NCLK Controller by the NCOSXC bus.

The NCLK handles control messages.

Stage	Description
1	The controller pack receives control messages through the DMI from the FPC by the CDAL.
2	The controller pack executes the messages.
3	The controller pack sends messages through the DMI to the FPC by the CDAL.

The NCLK generates [maintenance] control messages.

Stage	Description
1	When an error occurs in the NCLK, then the controller pack generates and sends a [maintenance] control message through the DMI to the FPC by the CDAL.

3.16 Office Network Timing Complex Common (ONTCCOM)

3.16.1 Basic Description

The Office Network Timing Complex Common (ONTCCOM) is in the MCC database that is used to diagnose a group of individually diagnosable components in the MCC database. That include: the MI, NC and TMS.

The ONTCCOM is viewed only from the MCC screen.

3.16.2 Service Impacts

The functions of the Office Network Timing Complex Common (ONTCCOM) components are related. When one component in the ONTCCOM (MI, NCLK or TMS) goes out-of-service, then all components in the ONTCCOM are impacted.

The ONTCCOM is part of the ONTC. When the ONTCCOM goes out-of-service, then all the ONTC components are impacted.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
ONTCCOM	One side	Major	No impact.	Reduces the ONTC to the simplex mode . Marks the ONTC as DGRD minor state.
	Both sides	Critical	No new inter-switching module calls. Stops all in-progress inter-switching module calls.	Isolates the switching modules.

3.17 Time Multiplexed Switch (TMS)

3.17.1 Basic Description

The Time Multiplexed Switch (TMS) is a multi-circuit pack component. The TMS is located in the CMCU, TMSU, and EBUS shelves of all CM cabinets.

The primary job of the TMS is to switch network time slots.

3.17.2 Electrical Power

CMCU shelf □ The SN516 Control and Display circuit pack controls power for the Time Multiplexed Switch (TMS) circuit packs that are contained in the CMCU shelf. The Control and Display circuit pack is located at the left end of the CMCU shelf.

TMSU shelf □ The SN516 Control and Display circuit pack controls power for the TMS circuit packs that are contained in the TMSU shelf. The Control and Display circuit pack is located in the TMSU shelf.

EBUS shelf □ The TMS circuit packs and EBUS cable that are contained in the EBUS shelf have no separate power supply circuit packs. The SN516 Control and Display circuit pack in the TMSU shelf controls power for the TMS circuit packs and EBUS cable in the EBUS shelf.

3.17.3 Shelf and Circuit Pack Arrangement

Depending upon configuration, the Time Multiplexed Switch (TMS) is located in the CMCU, TMSU, and EBUS shelves of the CM cabinets.

The following tables detail the shelf and circuit pack arrangement of the TMS hardware components.

The following table details the shelf and circuit pack arrangement of the TMS circuit packs that are contained in the CMCU shelf.

EQL			
Vertical	**Horizontal**	**Component Name**	**Component Number**
28	112	**TMS Clock**	TN881
28	116	**Data End Tap**	UN310 (Used in CM2 applications with no growth cabinets.)
28	122	**TMS Interface**	UN183
28	130	**TMS Controller**	TN884
28	138	**TMS Control Interface**	TN882

The following table details the shelf and circuit pack arrangement of the TMS circuit packs that are contained in the TMSU shelf.

EQL			
Vertical	**Horizontal**	**Component Name**	**Component Number**
36	008	**Control and Display Pack**	SN516
36	024	**Power Converter**	410CA
36	032 through 080	**QLI, QLI2, and QLPS**	TN888, TN1681, and TN1682
36	088	**FLI***	TN883
36	096	**Power Converter**	410AA
36	104	**Power Converter**	410AA
36	112	**SUB**	UN182
36	131	**FAB**	KBN5
***NOTE:* *** Cabinets 5 and 6 only.			

The following table details the shelf and circuit pack arrangement of the TMS circuit packs that are contained in the EBUS shelf.

EQL			
Vertical	**Horizontal**	**Component Name**	**Component Number**
Various	Various	**Multiplex Control**	UN197
Various	Various	**Loop Board**	UN198
Various	Various	**Data End Tap Board**	UN310
Various	Various	**Data End Board**	UN311

Various	Various	**Clock End Tap Board**	UN312
Various	Various	**Clock Tap**	UN313
Various	Various	**Transmit Data Repeater**	UN500
Various	Various	**Transmit Control Repeater**	UN501
Various	Various	**Receive Data Repeater**	UN503
Various	Various	**Receive Control Repeater**	UN504

3.17.4 Configuration

The following tables detail the configuration of the Time Multiplexed Switch (TMS). In the minimum configuration, the TMS consists of an EBUS cable and circuit packs in the CMCU and TMSU shelves. In the maximum configuration, the TMS consists of an EBUS cable and circuit packs in the CMCU, TMSU, and EBUS shelves.

The following table details the TMS circuit packs that are contained in the CMCU shelf.

Circuit Pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
TMS Controller	Backplane	TMS Clock, TMS Control Interface, and TMS Interface	Duplex	ACT MAJ/ ACT MIN
TMS Control Interface	Backplane	TMS Clock, TMS Controller, and TMS Interface	Duplex	ACT MAJ/ ACT MIN
TMS Interface	Backplane	TMS Clock, TMS Control Interface, and TMS Controller	Duplex	ACT MAJ/ ACT MIN
	CDAL	FPC		
	EBUS	Even TMSUs		
		Odd TMSUs		
TMS Clock Interface	Backplane	TMS Controller and TMS Interface	Duplex	ACT MAJ/ ACT MIN
		Network Clock		
	EBUS	TMSUs		

The following table details the TMS circuit packs that are contained in the TMSU shelf.

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
FLI	Metallic Bus	DMI	Duplex	ACT MAJ/ACT MIN
	NCT	SM		
	Backplane	SUB FAB		
QLI	NCT	SM	Duplex	ACT MAJ/ACT MIN
	Backplane	SUB FAB		
QLI2	NCT2	SM-2000	Duplex	ACT MAJ/ACT MIN
	Backplane	SUB FAB		
QLPS	Backplane	SUB FAB	Duplex	ACT MAJ/ACT MIN
SUB	E-BUS	FAB	Duplex	ACT MAJ/ACT MIN
	Backplane	FLI		
		QLI		
		QLI2		
		QLPS		
FAB	E-BUS	FLI	Duplex	ACT MAJ/ACT MIN

The following table details the TMS circuit packs in the EBUS shelf.

Circuit Pack	Link/Bus	Connect to ...	Method of Operation	State of Operation
Multiplex Control Board	Backplane	CMCU	Duplex	ACT MAJ/ACT MIN
		TMSU		
		EBUS cable		
Loop Board	Backplane	Transmit Data Circuit	Duplex	ACT/ACT
Data End Tap Board	Backplane	CMCU	Duplex	ACT/ACT
		TMSU		
		EBUS		
Data Tap Board	Backplane	CMCU	Duplex	ACT/ACT
		TMSU		
		EBUS		
Clock End Tap Board	Backplane	CMCU	Duplex	ACT/ACT
		TMSU		
		EBUS		
Clock Tap	Backplane	CMCU	Duplex	ACT/ACT
		TMSU		
		EBUS		

Transmit Data Repeater	Backplane	CMCU TMSU EBUS	Duplex	ACT/ACT
Transmit Control Repeater	Backplane	TMSU EBUS	Duplex	ACT/ACT
Receive Data Repeater	Backplane	TMSU EBUS	Duplex	ACT/ACT
Receive Control Repeater	Backplane	TMSU EBUS	Duplex	ACT/ACT
NOTE: The number of CM2 cabinets in the office determines the circuit packs that are contained in the EBUS shelves.				

3.17.5 Service Impacts

The TMS is part of the maintenance hardware grouping: the ONTCCOM. If the TMS goes out-of-service, then the MI and NCLK goes out-of-service. For service impact, go to the ONTCCOM.

3.17.6 Detailed Description

The following tables detail the functions of the circuit packs in the Time Multiplexed Switch (TMS).

The following table details the functions of the TMS circuit packs that are contained in the CMCU shelf.

Part	Function
TMS Controller	Generates control messages for the circuit packs in the TMSU shelves.
TMS Control Interface	Converts control messages to send to the EBUS cable.
TMS Interface	Connects the TMS Controller with the EBUS and DMI.
Data End Tap	Connects the TMS interface with the TMSU 0 and 1 (Office dependent: In a growth configuration, the Data End Tap appears in the EBUS shelves of CM cabinets 4 and 7).
Paddle-Board Circuit	Connects the TMS Interface to Transmit Data Tap (CM2 growth configuration only).
TMS Clock Interface	Generates clock pulses for the circuit packs in the TMSU shelves.

The following table details the functions of the TMS circuit packs that are contained in the TMSU shelf.

Part	Function
FLI	The FLI performs the following: □ Temporarily stores and sends control messages and data messages from the DMI and the SM-2000s. □ Connects NCT links for up to two SMs.
QLI	Connects NCT links for up to four SM-2000s.
QLI2	Connects NCT2 link for up to two SM-2000s.
QLPS	Switches control messages between the following: □ SM-2000s □ SM-2000s and the QGP.
SUB	Connects the QLI/QLI2 to the receive side of the EBUS.
FAB	Switches control messages and subscriber data.

The following table details the functions of the TMS circuit packs that are contained in the EBUS shelf.

Part	Function
Multiplex Control	Routes control messages and clock pulses between the receive side of the EBUS cable and the SUB in the TMSU shelves.
Loop	Routes [data and call processing] control messages between the receive and transmit sides of the EBUS.
Data End Tap	The Data End Tap performs the following: □ Extracts [data and call processing] control messages from the EBUS cable. □ Sends [data and call processing] control messages to the FAB in the TMSU shelf.

Data Tap Board	The Data Tap Board performs the following: □ Extracts [data and call processing] control messages from the EBUS cable. □ Sends [data and call processing] control messages to the FAB in the TMS.
Clock End Tap	The Clock End Tap performs the following: □ Extracts clock pulses from the EBUS cable. □ Sends clock pulses to the circuit packs in the TMSU shelves.
Clock Tap	The Clock Tap performs the following: □ Extracts clock pulses from the EBUS cable. □ Sends clock pulses to the circuit packs in the TMSU shelves.
Transmit Control Repeater	The Transmit Control Repeater performs the following: □ Receives clock pulses and control messages from the transmit side of the EBUS. □ Reclocks and/or temporarily stores clock pulses and control messages. □ Reamplifies and sends clock pulses and control messages back to the transmit side of the EBUS.
Transmit Data Repeater	The Transmit Data Repeater performs the following: □ Receives, and temporarily stores, [call processing] control messages from the transmit side of the EBUS. □ Reamplifies [call processing] control messages and sends the control messages back by the transmit side of the EBUS.
Receive Data Repeater	The Receive Data Repeater performs the following: □ Receives [call processing] control messages from the receive side of the EBUS cable. □ Repeats the [call processing] control messages. □ Sends the [call processing] control messages back to the receive side of the EBUS cable.
Receive Control Repeater	The Receive Control Repeater performs the following: □ Receives clock pulses and control messages on the receive side of the EBUS cable. □ Reclocks and temporarily stores clock pulses and control messages. □ Reamplifies and sends clock pulses and control messages back to the receive side of the EBUS cable.

3.17.7 Functional Description

3.17.7.1 Functions

The Time Multiplexed Switch (TMS) performs the following:

□ Switches Network Time Slots to provide a data path for inter-switching module customer calls.

- Switches control Time Slots to provide a control path between the switching modules and MMPs.
- Switches control Time Slots to provide a control path between the SM-2000s and the QLPS Network.
- Provides a path to rapidly reload SM software, between the Switching Modules and the PPC.

3.17.7.2 Operation

The following figures depict the operations of the TMS.

Figures 3-23 , 3-24 , 3-25 , and 3-26 depict the operation of the TMS in a CM2 consisting of 2 cabinets.

Figures 3-27 , 3-28 , 3-29 , 3-30 , and 3-31 depict the operation of the TMS in a CM2 consisting of multiple cabinets.

Figure 3-23 TMS Block Diagram 1

Figure 3-24 TMS Block Diagram 2

Figure 3-25 TMS Block Diagram 3

Figure 3-26 TMS Block Diagram 4

Figure 3-27 TMS Block Diagram 5

Figure 3-28 TMS Block Diagram 6

Figure 3-29 TMS Block Diagram 7

Figure 3-30 TMS Block Diagram 8

Figure 3-31 TMS Block Diagram 9

The following tables detail the operation of the TMS.

The TMS executes control messages from the FPC to set up a path for time slot information.

Stage	Description
1	The TMS Interface pack receives control messages from the FPC through the DMI by the CDAL.
2	The TMS Interface pack sends the message to the TMS Controller pack.
3	The TMS Controller pack generates and sends a control message for the FAB to the TMS Control Interface by the backplane.
4	The TMS Control Interface sends the message to the SUB by the EBUS.*

5	The SUB receives and sends the message to the FAB by the backplane.
6	The FAB receives and switches the message to the SM-2000, QLPSNW or MMP.
NOTE: ******* The circuit packs used to operate the EBUS depend on the office configuration.	

The TMS switches control messages between switching modules and the MMPs to provide a path for control time slot information.

Stage	Description
1	The QLI/QLI2 receives a control message from the switching module by the NCT/NCT2 link.
2	The SUB receives the message from the QLI/QLI2 by the backplane
3	The SUB sends the message to the FAB by the EBUS.*****
4	The FAB switches and sends the message to the FLI by the backplane.
5	The FLI receives and sends the message to the MMP through the DMI by Foundation Link and MIB.
NOTE: ******* The circuit packs used to operate the EBUS depend on the office configuration.	

The TMS switches control messages between the switching module and QLPS to provide a path for control time slot information.

Stage	Description
1	The QLI2 receives the control message from the SM-2000 by the NCT2 link.
2	The QLI2 sends the message to the SUB board by the backplane.
3	The SUB receives and sends the message to the FAB by the EBUS.*****
4	The FAB receives and switches the message to the QLPS by the backplane.
NOTE: ******* The circuit packs used to operate the EBUS depend on the office configuration.	

The TMS distributes clock pulses from the Network Clock to the FPC and switching modules.

Stage	Description
1	The TMS clock receives clock pulses from both Network Clocks by the backplane.
2	The TMS clock sends the clock pulses to the SUB and FAB by the EBUS***** and the TMS Interface by the Backplane.
3	A. The TMS Interface receives and sends the clock pulses through the DMI to the FPC by the CDAL.
	B. The SUB receives and sends the clock pulses to the QLI/QLI2 and QLPS by the backplane.
	C. The FAB receives the pulses and synchronizes the internal clock. Note: The FAB receives clock pulses after the pulses travel through the receive and transmit sides of the EBUS cable.
NOTE: ******* The circuit packs used to operate the EBUS depend on the office configuration.	

The TMS switches data between the switching modules.

Stage	Description
1	The QLI/QLI2 receives data from the switching modules by the NCT/NCT2 link.
2	The QLI/QLI2 receives and sends the data to the SUB by the backplane.
3	The SUB receives and sends the data to the FAB by the EBUS.*****
4	The FAB receives and switches the data to the QLI/QLI2 by the backplane.
5	The QLI/QLI2 receives and sends the data to the switching module by the NCT/NCT2 link.
NOTE: ******* The circuit packs used to operate the EBUS depend on the office configuration.	

The TMS switches switching module software control messages from the PPC to the switching modules.

Stage	Description
1	The FLI receives the control messages from the PPC through the DMI by the Foundation Link.
2	The FLI sends the message to the SUB by the backplane.
3	The SUB receives and sends the message to the FAB by the EBUS.*****
4	The FAB receives and switches the messages to the QLI/QLI2 by the backplane.
5	The QLI/QLI2 receives and sends the message to the switching module by the NCT/NCT2 link.
NOTE: ******* The circuit packs used to operate the EBUS depend on the office configuration.	

3.18 Time Multiplexed Switch Unit (TMSU)

3.18.1 Basic Description

The Time Multiplexed Switch Unit, Model 3 (TMSU3) is a shelf. The TMSU3 is located in the CM cabinet.

The TMSU3 contains part of the diagnosable component, the TMS.

3.18.2 Shelf and Circuit Pack Arrangement

The Time Multiplexed Switch Unit, Model 3 (TMSU3) is located in each CM cabinet.

Figure 3-32 depicts the shelf and circuit pack arrangement of the TMSU3.

Figure 3-32 TMSU3 Shelf and Circuit Pack Arrangement

The following table details the shelf and circuit pack arrangement of the TMSU3 hardware components.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
19 and 36		**TMS**	*****
19 and 36	008	**Control and Display**	SN516
19 and 36	024, 096, and 104	**Power Converter**	410CA
NOTE: ***** Refer to the TMS hardware description for circuit pack numbers.			

3.19 Emitter□Coupled Bus (EBUS)

3.19.1 Basic Description

The Emitter-Coupled Logic Bus Unit (EBUS) is a shelf. The EBUS is located in the growth cabinets of a CM2.

The EBUS contains part of the diagnosable component, the TMS.

3.19.2 Shelf and Circuit Pack Arrangement

The Emitter-Coupled Logic Bus Unit (EBUS) is located in the growth cabinets of the CM2.

The following table details the shelf and circuit pack arrangement of the TMS hardware components that contained in the EBUS shelf.

EQL		Component Name	Component Number	Cabinet
Vertical	**Horizontal**			
Various	Various	**Multiplex Control**	UN197	All growth cabinets
Various	Various	**Loop Board**	UN198	Cabinets 4, 2, or 0; and cabinets 7, 9, or 11, when the above cabinets are the last CM cabinet.
Various	Various	**Data End Tap Board**	UN310	***Cabinets 4 and 7 in a growth cabinet office.
Various	Various	**Data End Board**	UN311	0 through 3 and 8

				through 11
Various	Various	**Clock End Tap Board**	UN312	4 and 7
Various	Various	**Clock Tap**	UN313	0 through 3 and 8 through 11
Various	Various	**Transmit Data Repeater**	UN500	1, 3, 8, and 10
Various	Various	**Transmit Control Repeater**	UN501	
Various	Various	**Receive Data Repeater**	UN503	0, 2, 9, and 11
Various	Various	**Receive Control Repeater**	UN504	
NOTE: *******The UN310 is equipped in the CMCU shelf in a two-cabinet CM2.				

3.20 Quad-Link Packet Switch (QLPS)

3.20.1 Basic Description

The Quad-Link Packet Switch (QLPS) is a one-circuit pack component. The QLPS is located in the TMSU shelves of the CM2.

The primary job of the QLPS pack is to route [call processing] control messages for the SM-2000s.

3.20.2 Electrical Power

The Power Control and Display circuit pack controls power for the Quad-Link Packet Switch (QLPS).

3.20.3 Shelf and Circuit Pack Arrangement

The Quad-Link Packet Switch (QLPS) is located in the TMSU shelves.

Figure 3-33 depicts the shelf and circuit pack arrangement of the QLPS.

Figure 3-33 QLPS Shelf and Circuit Pack Arrangement

The following table details the possible shelf and circuit pack arrangement of the QLPS.

EQL			
Vertical	**Horizontal**	**Component Name**	**Component Number**
19 and 36	008	**Power Control and Display**	SN516
	024	**Power Converter**	410CA

	032, 040, 048, 056, 064, 072, 080, and 088**	**QLPS***	TN1682
Various	096	**Power Converter -5A**	410AA
NOTE: * If equipped, the QLPS consists of four QLPS circuit packs. The four packs of QLPS are contained in the same EQL slot of each of the four TMSU shelves.			
NOTE: ** QLPS cannot be in location 088 in cabinets 5 and 6.			

3.20.4 Configuration

The following table details the configuration of the Quad-Link Packet Switch (QLPS) circuit pack.

Component	Link/Bus	Connects to ...	Method of Operation	State of Operation
QLPS	QGL	GWI	Duplex	ACT/STBY
	Backplane	SUB	Quadruplex*	ACT/STBY
	Backplane	FAB	Quadruplex*	ACT/STBY
NOTE: * Four QLPS packs are equipped, each of which can carry the maximum load.				

3.20.5 Service Impacts

The following table details the impact on subscriber service and switch performance when one or more Quad-Link Packet Switch (QLPS) circuit packs are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
QLPS	One to three QLPS packs	Major	No impact.	No impact.
	Four QLPS packs	Critical	May deny service.	Removes the QLPS network from service. Routes messages through the MMP network until all of the capacity of the MMP is used.

3.20.6 Detailed Description

The Quad-Link Packet Switch (QLPS) routes [call processing, recent change administration, and maintenance] control messages.

3.20.7 Functional Description

3.20.7.1 Functions

The Quad-Link Packet Switch (QLPS) routes control messages between:

- The SM-2000s (call processing-specific).
- The SM-2000 and AM (call processing and maintenance-specific).
- The SM-2000 and CMP (call processing and recent change administration-specific).
- The SM-2000 and SM (call processing-specific).
- The SM-2000 and PSU QPH (call processing-specific).
- The SM-2000 and FPC (call processing-specific).

3.20.7.2 Operation

The QLPS interacts with other components to operate the switch.

Figure 3-34 depicts the operation of the MMP.

Figure 3-34 QLPS Block Diagram

The following tables detail the operation of the Quad-Link Packet Switch (QLPS).

The QLPS handles control messages from the FAB.

Stage	Description
1	The QLPS receives a call processing control message from the FAB by the backplane.
2	The QLPS sends the message to either of the following: A. The SUB by the backplane, or B. The QGP by the Quad-Link.

The QLPS handles control messages from the QGP.

Stage	Description
1	The QLPS receives a control message from the GWI by the Quad-Link.
2	The QLPS sends the message to the SUB by the backplane.

3.21 Quad-Link Packet Switch (QLPS) Network

3.21.1 Basic Description

The QLPSNW is a software name that the MCC database used to diagnose QLPSNW. The QLPSNW MCC screen is used to view a group of components that are independently diagnosable or part of a diagnosable component, that include: the QLPS, QGP, SM-2000 MH and SM-2000 QPH.

The QLPSNW is viewed only from the MCC screen. The MCC page that contains the QLPSNW is displayed before the MCC page that contains the QLPS and QGP diagnostic commands.

3.21.2 Service Impacts

The operations of the components in the QLPSNW are inter-dependent. The QLPSNW component the QGP is part of the MSGS. If one component in the MSGS goes out-of-service, then components in the QLPSNW may be impacted.

4. COMMUNICATION MODULE, MODEL 3 (CM3)

4.1 Description, CM3

Figure 4-1 depicts a high-level diagram of the CM3.

Figure 4-1 CM3 High Level Diagram

Communication Module Model 3 (CM3) provides the following functionality:

- Inter-processor communications (SM-to-SM, SM-to-CM, CM-to-SM, AM-to-CM, CM-to-AM, SM-to-AM, and AM-to-SM) for control, packet, and voice time slots over NCT2 links for SM-2000s or NCT links for SMs.
- Connects the SM to the AM for maintenance and various administrative functions (such as, updates and storage).
- Terminates external timing reference which provides switch synchronization.

The NxTMS feature increases the number of CM3 cabinets from one base cabinet to one base cabinet plus three growth cabinets as shown in figure 4-2 . Each cabinet contains one TMS fabric pair (TMSFP) consisting of an even fabric and an odd fabric.

Figure 4-2 CM3 NxTMS Diagram

The CM3 Base cabinet provides the connections to the:

- Administrative Module (AM) - Dual Serial Channel (DSCH).
- Switching Modules (SM) - NCT Links or Switching Modules-2000 (SM-2000) - NCT2 Links (Primary and Secondary).
- CM3 Growth cabinets - Control and Synchronization Interface (CSI).
- Network clock timing references.

The CM3 Base cabinet provides the control and timing for the CM3 Growth Cabinets.

The CM3 Growth cabinets provides the:

- Additional connections for SM-2000 Secondary NCT2 Links only.
- Interprocessor communication (voice and data) between SM-2000s connected by NCT2 Links to the same growth cabinet.

4.1.1 Availability, CM3

The availability of the:

- CM2 to CM3 conversion is the 5E15 Software Release.

- CM3 Base is the 5E15 SU4 Software Release which supports only SM-2000s.
- CM3 with Classic SM is the 5E15 FR5 Software Release which supports SMs and SM-2000s.
- CM3 NxTMS is the 5E16.2 Software Release.

4.1.2 Frame/Cabinet Arrangement, CM3

The CM3 is located in the CM Cabinet of the *5ESS*® Switch.

The cabinets that make up the CM3 are the Base Cabinet and from zero to three Growth Cabinets.

Figure 4-3 depicts the cabinet and shelf arrangement of a base CM3 cabinet.

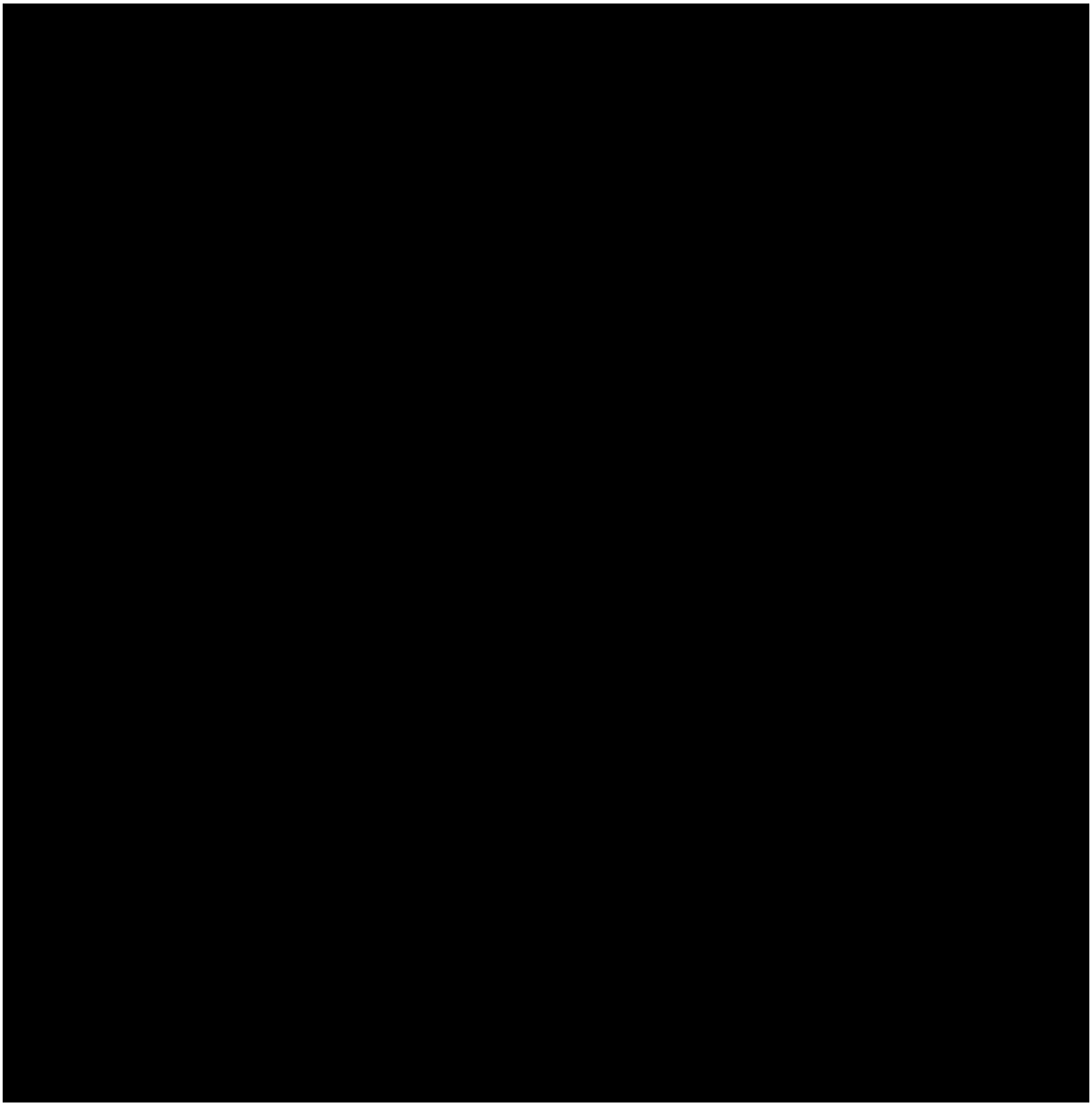

Figure 4-3 CM3 Base Cabinet Arrangement

The CM3 is contained in a Front Access Cabling (FAC) cabinet to better utilize space. The Modular Fuse

and Filter Unit (MFFU) and side "0" of the CM3 faces the front (Equipment Aisle) and side "1" faces the rear (Wiring Aisle).

Table 4-1 details the shelf arrangement of the CM3.

Table 4-1 CM3 Shelf Arrangement

EQL	Shelf Unit	Configuration
68	Modular Fuse and Filter Unit (MFFU)	Fuse and Filter Unit
55	Time Multiplexed Switch Unit, Model 4 (TMSU4)	Third Expansion Unit
45	Time Multiplexed Switch Unit, Model 4 (TMSU4)	Second Expansion Unit
35	Time Multiplexed Switch Unit, Model 4 (TMSU4)	First Expansion Unit
24	Communication Module Unit, Model 2 (CMU2)	Base Unit
11	Fan	Fan Unit

The CM3 growth cabinets provide SM-2000 interprocessor communication for voice and data time slots over NCT2 Links located on the same growth cabinet.

The CM3 growth cabinets like the base cabinet are FACs (Front Access Cabinets). Side 0 faces the Front of the Aisle and side 1 faces the wiring aisle. The CM3 cabinets do not need to be adjacent, growth cabinets can reside 100 cable ft from the base cabinet.

The cabinets are designated as shown in figure 4-4 .

Figure 4-4 CM3 Base and Growth Cabinets

The growth cabinets include the same shelf hardware as the base cabinet:

- An MFFU
- One CMU2
- Up to 3 TMSU4s
- And a fan unit.

4.1.3 Shelf and Circuit Pack Arrangement, CM3

The CM3 Base Cabinet consists of a Communication Module Unit, Model 2 (CMU2) and up to three Time Multiplexed Switch Unit, Model 4 (TMSU4)s.

The CM3 Growth Cabinet can have up to three additional bays with the same shelf equipage as the base cabinet with different circuit pack equipage.

4.1.3.1 CMU2 Shelf and Circuit Pack Arrangement

The Communication Module Unit, Model 2 (CMU2) is the base unit of the CM3. Figure 4-5 depicts the CMU2 shelf location and pack arrangement (refer to CMU2 Basic Description section 4.1.5.1 for a detailed description of the CMU2 packs) of the CM3 Base Cabinet.

Figure 4-5 CMU2 Shelf and Circuit Pack Arrangement in a CM3 Base Cabinet Table 4-2 details the horizontal EQL, Component Position, Component Name, and Pack Code of the CMU2.

Table 4-2 CMU2 Shelf and Circuit Pack Arrangement in a CM3 Base Cabinet

Horizontal EQL	Component Position	Component Name	Pack Code
424B	015B	Time Multiplexed Switch Foundation (TMSF) - Even Time Slots	MMC100
449B	016B	TMSF - Odd Time Slots	
394T	016T	Oscillator (OSC) - Stratum 2	MMB100
501	017	Network Clock and Control (NCC)	MMD101
541	018	Message Switch (MSGS)	MMD100
093 - 273	001 - 010	Optical Paddleboard	MMA1, MMA2, or MMA3

The CM3 Growth Cabinet contain only the TMSF in the CMU2 as shown in figure 4-6 .

Figure 4-6 CMU2 Unit Equipped in a CM3 Growth Cabinet Table 4-3 details the horizontal EQL, Component Position, Component Name, and Pack Code of the CMU2.

Table 4-3 CMU2 Unit Equipped in a CM3 Growth Cabinet

Horizontal EQL	Component Position	Component Name	Pack Code
424B	015B	Time Multiplexed Switch Foundation (TMSF) - Even Time Slots	MMC100
449B	016B	TMSF - Odd Time Slots	
093 - 273	001 - 010	Optical Paddleboard	MMA1, MMA2, or MMA3

4.1.3.2 TMSU4 Shelf and Circuit Pack Arrangement

The Time Multiplexed Switch Unit, Model 4 (TMSU4) is the expansion unit of a CM3 cabinet. Figure 4-7 depicts the shelf arrangement of a fully equipped CM3 Cabinet that consists of three TMSU4s (refer to TMSU4 Basic Description section 4.1.5.7 for a detailed description of the TMSU4 packs).

Figure 4-7 TMSU4 Shelf and Circuit Pack Arrangement (Fully Configured CM3 Cabinet)

Table 4-4 details the horizontal EQL, Component Position, Component Name, and Pack Code of the TMSU4.

Table 4-4 TMSU4 Shelf and Circuit Pack Arrangement

Horizontal EQL	Component Position	Component Name	Pack Code
258F	008	Time Multiplexed Switch Expansion (TMSX) - Even Time Slots	MMC101
283R	009	TMSX - Odd Time Slots	
093 - 193 and 365 - 545	001 - 006 and 011 - 020	Optical Paddleboards	MMA1, MMA2, or MMA3

4.1.4 Power, CM3

The CM3 terminates eight -48V DC power feeders from the Global Power Distribution Frame (GPDF). The power feeders are terminated at the rear of the CM3 cabinet. Four of the power feeders are terminated to the "A" power bus and four power feeders are terminated to the "B" power bus. The A power bus supplies power to side 0 (front) and the B power bus supplies power to side 1 (rear). The power feeders terminate to the locations listed in the following table.

Power Bus A	Power Bus B
68-017	68-108
68-032	68-123
68-063	68-154
68-078	68-169

After the power is filtered and fused, it is cabled to the individual shelf units and fans. Figure 4-8 depicts the fuse assignments for the base cabinet and figure 4-9 depicts the fuse assignments for the growth cabinet. Fuses for CM3 can only be accessed from the front of the CM3 cabinet.

WARNING: The NCC/OSC and TMSF/TMSX even and odd boards share a fuse, as shown in figure 4-8 and 4-9 .

Figure 4-8 CM3 Fuse Assignments for a CM3 Base Cabinet

Figure 4-9 CM3 Fuse Assignments for a CM3 Growth Cabinet

The following tables provide a cross reference between the fuses and the corresponding circuit packs and paddle boards for side 0 of the CM3.

Fuse Position	Fuse Amperage	Cable Termination	Unit Fused	Protects ...
014C	7	24-112 -48V 24-112 -RTN	CMU2	OPBs
014D	7	24-126 -48V 24-126 -RTN	CMU2	TMSF
023B	7	24-143 -48V 24-143 -RTN	CMU2	NCC/OSC*
014B	7	24-158 -48V 24-158 -RTN	CMU2	MSGS*

NOTE: *******The CM3 base and growth cabinet fuse layouts are the same except there are no MSGS or OSC/NCC fuses in the growth cabinets.

Fuse Position	Fuse Amperage	Cable Termination	Unit Fused	Protects ...
023C	7	35-103 -48V 35-103 -RTN	TMSU4	OPBs
023D	7	35-101 -48V 35-101 -RTN	TMSU4	TMSX

Fuse Position	Fuse Amperage	Cable Termination	Unit Fused	Protects ...
032C	7	45-103 -48V 45-103 -RTN	TMSU4	OPBs
032D	7	45-101 -48V 45-101 -RTN	TMSU4	TMSX

Fuse Position	Fuse Amperage	Cable Termination	Unit Fused	Protects ...
041C	7	55-103 -48V 55-103 -RTN	TMSU4	OPBs
041D	7	55-101 -48V	TMSU4	TMSX

		55-101 -RTN		

The following tables provide a cross reference between the fuses and the corresponding circuit packs and paddle boards for side 1 of the CM3.

Fuse Position	Fuse Amperage	Cable Termination	Unit Fused	Protects ...
118C	7	24-112 -48V 24-112 -RTN	CMU2	OPBs
118D	7	24-126 -48V 24-126 -RTN	CMU2	TMSF
127B	7	24-143 -48V 24-143 -RTN	CMU2	NCC/OSC*
118B	7	24-158 -48V 24-158 -RTN	CMU2	MSGS*

NOTE: *******The CM3 base and growth cabinet fuse layouts are the same except there are no MSGS or OSC/NCC fuses in the growth cabinets.

Fuse Position	Fuse Amperage	Cable Termination	Unit Fused	Protects ...
127C	7	35-103 -48V 35-103 -RTN	TMSU4	OPBs
127D	7	35-101 -48V 35-101 -RTN	TMSU4	TMSX

Fuse Position	Fuse Amperage	Cable Termination	Unit Fused	Protects ...
141C	7	45-103 -48V 45-103 -RTN	TMSU4	OPBs
141D	7	45-101 -48V 45-101 -RTN	TMSU4	TMSX

Fuse Position	Fuse Amperage	Cable Termination	Unit Fused	Protects ...
150C	7	55-103 -48V 55-103 -RTN	TMSU4	OPBs
150D	7	55-101 -48V 55-101 -RTN	TMSU4	TMSX

Figure 4-10 depicts the fan unit of the CM3.

Figure 4-10 CM3 Fan Unit

The alarm circuit contains 2 push-button switches and eight status LEDs. The following tables provides a cross reference between the buttons and LEDs.

Button Label	Description
R	Reset
T	Test

LED Label	Description
OT	Over Temperature
G	Fan G
F	Fan F
E	Fan E
C	Fan C
B	Fan B
A	Fan A
S	Status

The following table provides a cross reference between the fuses and the fans in the CM3. The fan unit power equipment location is: 11-162.

Fuse Position	Fuse Amperage	Terminals	Unit Fused	Protects ...
041A	3	1 and 2	FAN	FAN CNT
014A	3	3 and 4	FAN	FAN A
023A	3	5 and 6	FAN	FAN B
032A	3	7 and 8	FAN	FAN C
118A	3	9 and 10	FAN	FAN E
127A	3	11 and 12	FAN	FAN F
141A	3	13 and 14	FAN	FAN G

4.1.5 Basic Description, CM3

The CM3 consists of three components - the Message Switch (MSGS), Office Network Timing Complex (ONTC), and the Oscillator (OSC) that:

- Supports SMs/SM-2000s by terminating NCT and NCT2 links.
- Provides internal Stratum 2 oscillator.
- Supports external references of Stratum 2 or 3.
- Supports SS7 through the PSU.
- Performs space division switching.
- Terminates and provides an 8 kHz timing signal.
- Interfaces to the AM through the Dual Serial Channel (DSCH).
- Routes messages between different SMs and between SMs and the AM and CMP.
- Provides a mechanism to perform a normal or backup pump.

4.1.5.1 Communication Module Unit, Model 2 Basic Description

Figure 4-11 depicts a basic configuration of a CM3 that is only equipped with a Communication Module Unit, Model 2 (CMU2).

Figure 4-11 CM3 Minimal Configuration

The Communication Module Unit, Model 2 (CMU2) performs the control message switching, voice/data space switching, and network clock functions of the CM3. The CMU2 consists of the following sub-units:

In the CM3 Base Cabinet, the CMU2 consists of the following sub-units:

- Message Switch (MSGS)
- Network Clock and Control (NCC)
- Oscillator (OSC)
- Time Multiplexed Switch Foundation (TMSF)
- Optical Paddle Boards (OPBs).

In a CM3 Growth Cabinet, the CMU2 consists of the following sub-units:

- Time Multiplexed Switch Foundation (TMSF)
- Optical Paddle Boards (OPBs).

4.1.5.2 Message Switch Basic Description

The Message Switch (MSGS) performs the following functions:

- Sends and receives messages and data through the Direct Memory Access (DMA) from the AM over the Dual Serial Channel (DSCH).
- Provides cross-coupled connections to the TMSF for the transfer of pump, control, and QLPS gateway time slots.
- Provides cross-coupled connections through the Control and Diagnostic Access Link (CDAL) interface to each NCC for communication and control.

The MSGS contains two on-board processors:

- The Application Processor (AP) that performs the following functions:
  - Provides communication between the AP and IP which is a Message Switch Control Unit (MSCU) functionality.
  - Provides the interface to the ONTC for maintenance and call processing which is a Foundation Peripheral Controller (FPC) functionality.
  - Provides Global resource allocation and manages Recent Change and Verify (RC/V) which is a Communication Module Processor (CMP) functionality (such as, network time slot assignments).
  - Routes control messages by Communication Links (CLNKs) which is an Module Message Processor (MMP) functionality. The MMP utilize control time slots to get to/from the ONTC.
  - Handles control messages between the MSCU and the SM by QLNKs which is an QLPS Gateway Processor (QGP) functionality. The QGP utilize QLPS Pipes (QPIPEs) to get to/from the QLPS units in the ONTC.
- The I/O Processor (IP) that performs the following functions:

- Communicates with the DSCH which is an Message Switch Control Unit (MSCU) functionality.
- Provides SM and SM-2000 normal pump which is a Pump Peripheral Controller (PPC) functionality.

4.1.5.3 Network Clock and Control Basic Description

The Network Clock and Control (NCC) performs the following functions:

- Provides timing to the ONTC and MSGS, and using NCT and NCT2 links, provides synchronization and timing to the SMs and SM-2000s.
- Provides the interface with the OSC to maintain timing if all references are lost.
- Controls the call processing, maintenance, and error reporting for the TMS fabric through Control and Synchronization Interface (CSI).

4.1.5.4 Oscillator Basic Description

The Oscillator (OSC) performs the following functions:

- Provides high stability clock synchronization oscillator (stratum 2) for the Network Clock.
- Maintains timing for the Network Clock functions when external references are lost.

4.1.5.5 Time Multiplexed Switch Foundation Basic Description

The Time Multiplexed Switch Foundation (TMSF) performs the following functions:

- Distributes clock synchronization and control to the Time Multiplexed Switch Expansion (TMSX) boards on the same side.
- Terminates 40 TMS link pairs (one even and one odd TMSLNK) coming into the CM3. Each NCT link pair requires 1 TMS link pair and each NCT2 link pair requires 2 TMS link pairs.
- QLPS functionality supporting packet pipes to the SM-2000 Message Handlers (MHs) and QLPS gateway processors (QGPs) for OSDS messaging, and to the QLPS Protocol Handlers (QPHs) for PSU-based SS7 signaling. The QLPS functionality is only used in the primary TMSFP in an NxTMS office.
- Supplies Central Processor Intervention (CPI), idle code, and test functions in each side of the CM3.
- Provides the Fabric (FAB) that interconnects two SM's for the duration of a time slot (space switching).

4.1.5.6 Optical Paddle Boards Basic Description

The Optical Paddle Boards (OPBs) perform the following functions:

- Terminates the optical fibers, each link consists of two fibers (transmit and receive), that comprise the NCT or NCT2 Links.
- Terminates an even and odd link that originate in an SM or SM-2000.
- Converts electrical to optical and optical to electrical.

4.1.5.7 Time Multiplexed Switch Unit, Model 4 Basic Description

Figure 4-12 depicts a maximum configured CM3 Cabinet that consists of the CMU2 with a total of three Time Multiplexed Switch Unit, Model 4 (TMSU4)s.

Figure 4-12 CM3 Cabinet Maximum Configuration

The Time Multiplexed Switch Unit, Model 4 (TMSU4) is the expansion unit of the CM3 Cabinet. Each TMSU4 can terminate an additional 48 even and 48 odd TMS links. The TMSU4 consists of the following sub-units:

- Time Multiplexed Switch Expansion (TMSX)
- Optical Paddle Boards (OPBs).

4.1.5.8 Time Multiplexed Switch Expansion Basic Description

Each Time Multiplexed Switch Expansion (TMSX) performs the following functions:

- Terminates 48 TMS link pairs coming into the CM3 (48 NCT or 24 NCT2 link pairs or a combination of both).
- Multiplexes receive links together at a higher speed and connects to the TMSF.
- Converts transmit links from the TMSF pack to NCT and NCT2 link format.

4.1.5.9 Optical Paddle Boards Basic Description

The Optical Paddle Boards (OPBs) perform the following functions:

- Terminates the optical fibers, each link consists of two fibers (transmit and receive), that comprise an NCT or NCT2 Link.
- Terminates an even and odd link that originate in an SM or SM-2000.
- Converts electrical to optical and optical to electrical.

4.1.5.10 Office Network Timing Complex Basic Description

The Office Network Timing Complex (ONTC) has the primary responsibility of providing the call paths between the SM/SM-2000s, performing the time division switching, and providing uniform timing within the switch by the network clock. To perform these functions, the ONTC:

- Receives and responds to call setup messages from the Switching Modules.
- Provides the physical paths for the transfer of call data between Switching Modules.
- Provides the gating and timing pulses for the time division switching of call data.

Figure 4-13 depicts the logical grouping of the ONTC.

Figure 4-13 ONTC Logical Group

Prior to 5E16.2 the CM3 ONTC is made up of the following functional groups:

- ONTC Common - ONTCCOM

- Message Link Interface - MLI
- Network Clock - NC
- Time Multiplexed Switch - TMS

- Dual Link Interface (DLI)/Network Link Interface (NLI)
- Quad Link Packet Switch (QLPS).

In 5E16.2 and later the CM3 ONTC is made up of the following functional groups:

- ONTC Common - ONTCCOM
  - Message Link Interface - MLI
  - Network Clock - NC
  - TMS Controller (part of the NCC board)
- Quad Link Packet Switch (QLPS).
- Time Multiplexed Switch Fabric Pair (TMSFP)
- Dual Link Interface (DLI)/Network Link Interface (NLI)

4.1.5.11 Office Network Timing Complex Common Basic Description

Figure 4-14 depicts the logical grouping of the Office Network Timing Complex Common (ONTCCOM).

Figure 4-14 ONTCCOM Logical Group

The ONTCCOM consists of the following logical grouping:

- Message Link Interface (MLI)
- Network Clock (NC)
- Time Multiplexed Switch (TMS)

4.1.5.12 Detailed Description(5E16.2 and Later), CM3 NxTMS

A CM3 is made up of between 1 and 4 TMS fabric pairs (TMSFP). Each fabric pair is numbered by:

- ONTC side (0 or 1)
- TMSFP number (0, 1, 2, or 3)

The `N' in NxTMS equals the number of fabric pairs in the CM3. Refer to table 4-5 for details.

TMSFP 0 is referred to as the "primary" TMSFP because it is the only one that supports inter-processor communication between the AM and SMs/SM-2000s by CLNKs and/or QLPS. Other equipped TMSFPs are referred to as "secondary" TMSFPs. The terms "primary" and "secondary" have the same meaning for SM-2000 NLIs -- only primary NLIs support CLNK and QLPS communication.

Figure 4-15 details the TMSFP cabinet arrangement.

Table 4-5 TMSFP Cabinet Arrangement

N=	Cabinet	TMS fabric pair (TMSFP)	
1	0 (Base)	0-0	side 0
		1-0	side 1
2	1 (Growth)	0-1	side 0
		1-1	side 1
3	2 (Growth)	0-2	side 0
		1-2	side 1
4	3 (Growth)	0-3	side 0
		1-3	side 1

Figure 4-15 TMSFP Cabinet Arrangement

Network Control and Timing (NCT) links connect switching modules (SM/SM-2000s) to the TMS fabric pairs. The base cabinet supports NCT links, Primary NCT2 links and Secondary NCT2 links.

NOTE: The primary links carry control as well as voice/data, whereas the secondary links only carry voice/data.

The growth cabinets support Secondary NCT2/NCT(from TRCU2) links. Control and Synchronization Interface (CSI) cables fan out from the Network Clock and Control (NCC) circuit pack in the base cabinet out to each even or odd fabric in every CM3 cabinet. This is the only connection to the growth cabinets from the base cabinet. Each TMS fabric pair operates independently. Each fabric pair contains even and odd fabrics.

Figure 4-16 shows one side of a four bay CM3.

Figure 4-16 One Side of a Four Bay CM3

Since each CM3 fabric pair is independent of each other, NCT2 links need to be spread across all available fabrics. For example, assume an SM-2000 with 11 NCT2 pairs.

To distribute these links appropriately across all equipped fabric pairs, engineering rules must be followed.

If this is not done, there will be a higher probability of inter-SM call blocking.

SM NCT links and SM-2000 primary NCT/NCT2 links must be located in the base cabinet, which also supports secondary SM-2000 NCT/NCT2 links. Only secondary SM-2000 NCT/NCT2 links can be supported by the CM3 growth cabinets.

4.1.5.13 Time Multiplexed Switch Fabric Pair Basic Description

In 5E16.2 and later, Time Multiplexed Switch Fabric Pairs (TMSFPs) were added as new configurable units for CM3. Each TMSFP consists of one even and one odd TMS fabric. TMSFPs can be removed, restored, and diagnosed independently of other TMSFPs. Except for the common "TMS controller" functionality which resides on the NCC board, all TMS functionality that was formerly (prior to 5E16.2) part of the ONTCCOM is now associated with TMSFP units. Up to four TMSFPs (0 through 3) can be equipped, with a minimum-sized CM3 office having only TMSFP 0 as follows:

- TMSFP 0 performs the function of the TMS for SM and SM-2000s (primary and secondary NLIs).
- TMSFP 1 through 3 provides the Link Interfaces for only Secondary NLIs.

4.1.6 Connecting Circuits, CM3

The CM3 consists of the following external connecting interfaces:

- CM3 to SM and SM-2000 external interfaces.
- CM3 to AM external interfaces.

4.1.6.1 CM3 To SM And SM-2000 External Interfaces

Figure 4-17 depicts the external interfaces of the CM3 to the SM and SM-2000.

Figure 4-17 CM to SM External Interfaces

The external interfaces of the CM3 are:

- Even and Odd NCT2 links between CM3 side 0 and the SM-2000.
- Even and Odd NCT2 links between CM3 side 1 and the SM-2000.
- Even and Odd NCT links between CM3 side 0 and the SM.
- Even and Odd NCT links between CM3 side 1 and the SM.

NOTE: Each OPB terminates transmit and receive fibers for an even and an odd NCT link in an SM and NCT2 link in an SM-2000.

4.1.6.2 CM3 To AM External Interfaces

Figure 4-18 depicts the external interfaces between the CM3 to AM.

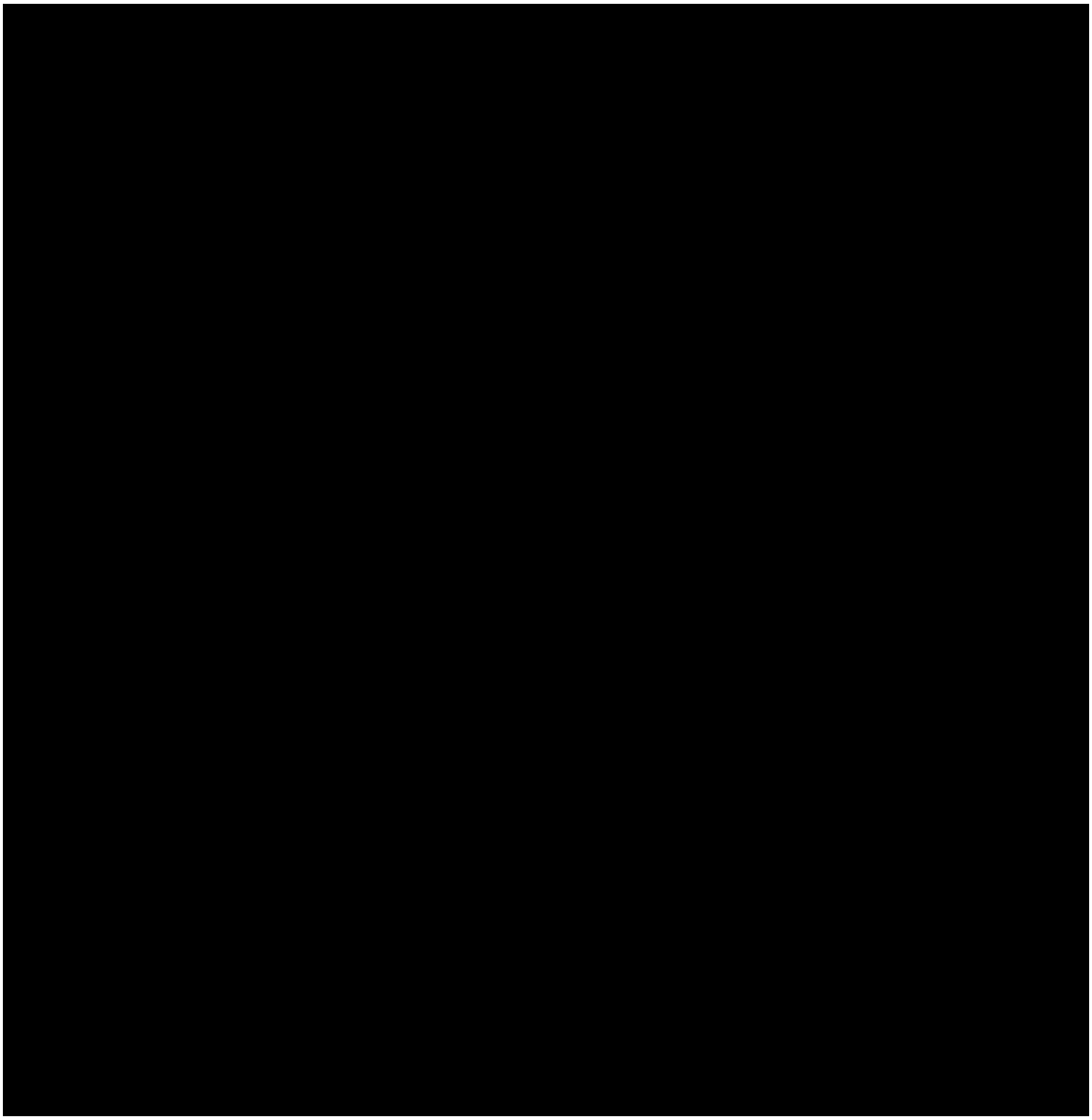

Figure 4-18 CM3 to AM External Interfaces

The external interfaces between the CM3 to AM are:

- Dual Serial Channel (DSCH) 12 to CM Side 0.
- Dual Serial Channel (DSCH) 14 to CM Side 1.
- Scan and Distribute Cables.

4.1.7 Functional Description, CM3

The Communication Module, Model 3 (CM3) provides the communication paths for:

- Inter-SM/SM-2000 voice/data
- Inter-SM/SM-2000 messaging
- Messaging between SM/SM-2000 to AM

- Normal Pump between CM3 and SM/SM-2000
- Backup Pump (CTS Pump) between CM3 and SM/SM-2000.
- The CM3 also provides the communication path for Central Processor Intervention (CPI).

4.1.7.1 Inter-SM/SM-2000 Voice/Data

The Figure 4-19 depicts the operation of an inter-SM/SM-2000 voice/data flow of a CM3. (CMU2 and up to three TMSU4s equipped)

Figure 4-19 Inter-SM/SM-2000 Voice/Data Path

Table 4-6 details the operation of an inter-SM/SM-2000 voice/data flow of a CM3.

Following an origination, digit analysis and resource allocation, a path is established through the CM3 for an inter-SM/SM-2000 voice/data call.

Table 4-6 Inter-SM/SM-2000 Voice/Data Path

Stage	Description
1	Voice/Data switched onto the PIDB time slot in the interface unit.
2	PIDB time slot switched onto network time slot in TSI.
3	NLI performs electrical to optical conversion.
4	Network time slot travels on NCT2 link from an SM-2000 to the corresponding Optical Paddle Board (OPB).
5	The OPB performs optical to electrical conversion.
6	Data from the OPB is sent through the backplane to the proper TMSF or TMSX pack.
7	The data is checked and reformatted before being sent to the TMSF pack, if necessary.
8	The data is switched by the fabric in the TMSF pack.
9	The data is again checked, multiplexed and reformatted before being sent to the proper OPB.
10	The OPB, which may be associated with either a TMSF or TMSX, performs the proper conversion and sends the

	data, through the NCT/NCT2 link, to the destination SM/SM-2000.
11	At this point the data is converted back to an electrical format by the DLI, switched through the TSI, and sent out to the target peripheral unit to the subscriber.

4.1.7.2 CM3 Inter-SM-2000 Message Path

Figure 4-20 depicts the operation of an inter-SM-2000 message path of the CM3.

Figure 4-20 CM3 Inter-SM-2000 Message Path Diagram

Table 4-7 detail the operation of an inter-SM-2000 message flow in the CM3.

An inter-SM-2000 control message is being sent between two SM-2000s. The message will travel over the QLPS network. This type of message exchange can occur during call processing when directory number routing information is required.

Table 4-7 CM3 Inter-SM-2000 Message Path

Stage	Description
1	The Message Handler (MH) in an SM-2000 assembles a message that will be sent to another SM-2000 through the QLPS network.
2	The message is sent through the MCP link to the TSI where the message is then inserted into outgoing QLPS time slots.
3	The message is sent to a primary Network Link Interface (NLI) for electrical to optical conversion.
4	The message is sent over the primary NCT2 link to the corresponding Optical Paddle Board (OPB) in the CM3.
5	The OPB performs optical to electrical conversion.

6	The data is sent through the backplane to the proper TMSX pack.
7	The data is checked and reformatted before being sent to the TMSF pack.
8	The data is switched through the TMSF fabric and sent to the QLPS functionality of the TMSF.
9	The QLPS functionality examines the message destination and forwards the message to the proper SM-2000.
10	The message is reformatted, sent back through the TMSF fabric and switched to the proper OPB.
11	The OPB performs the electrical to optical conversion and sends the data through a primary NCT2 link to the proper destination SM-2000.
12	The NLI performs optical to electrical conversion, sends the data to the TSI and over the MCP link to the MH for processing.

4.1.7.3 CM3 Inter-SM Message Path

Figure 4-21 depicts the operation of an inter-SM message path of the CM3.

Figure 4-21 CM3 Inter-SM Message Path Diagram

Table 4-8 detail the operation of an inter-SM message flow in the CM3.

An inter-SM control message is being sent between two SMs. The message will travel over the CLNKs and use the MMPs. This type of message exchange can occur during call processing when directory number routing information is required.

Table 4-8 CM3 Inter-SM Message Path

Stage	Description
1	The Protocol circuitry on the Application Pack (APPL) in the SM assembles a message to be sent to another SM.
2	The message is sent over the Link Interface Bus (LIB) to the Dual Link Interface (DLI).

3	The DLI inserts the message into the Control Time Slot (CTS) and on to the transceiver which performs electrical to optical conversion.
4	The transceiver sends the CTS over the NCT link to the corresponding Optical Paddle Board (OPB) in the CM3.
5	The OPB performs the required optical to electrical conversion.
6	The message is sent through the backplane to the proper TMSX pack.
7	The message is checked and reformatted before being sent over the backplane to the TMSF pack.
8	The message is switched through the TMSF fabric and sent over the Control Time Slot Pump Link (CTPL) to the Module Message Processor (MMP).
9	The MMP checks the protocol and forwards the message to the MSCU function.
10	The MSCU function examines the message destination and sends the message to the MMP for reformatting.
11	The MMP applies the proper protocol and forwards the message over the CTPL to the TMSF fabric.
12	The TMSF fabric reformats the messages and switches it to the proper CTS and OPB.
13	The OPB performs the electrical to optical conversion and sends the data over the NCT link to the corresponding transceiver in the SM.
14	The transceiver performs the optical to electrical conversion and forwards the CTS to the DLI.
15	Circuitry in the DLI picks off the assigned CTS and sends it over the LIB to the APPL pack.
16	The APPL pack performs the required protocol work and formatting to prepare the message for the SMP processor.

4.1.7.4 SM-2000 to AM Message Path Through The CM3

Figure 4-22 depicts the operation of an SM-2000 to AM message path through the CM3.

Figure 4-22 SM-2000 to AM Message Path Diagram

Table 4-9 steps provide a high-level example of the message flow between the SM-2000 and AM using the QLPS network functionality of the CM3. The path can be used to send billing data, retrieve diagnostics, and other read/write operations to disk.

Table 4-9 SM-2000 to AM Message Path

Stage	Description
1	The Message Handler (MH) in the SM-2000 assembles a message that will be sent to the AM using the QLPS network.
2	The message is sent through the MCP link to the TSI where the message is inserted into an outgoing QLPS time

	slot.
3	The message is sent to a primary Network Link Interface (NLI) for electrical to optical conversion.
4	The message is sent over the primary NCT2 link to the corresponding Optical Paddle Board (OPB) in the CM3.
5	The OPB performs optical to electrical conversion.
6	The data is sent over the backplane to the TMSF.
7	The data is checked and reformatted before being switched through the TMSF fabric and sent to the QLPS functionality of the TMSF.
8	The QLPS functionality examines the message destination and forwards the message over a QGL to the QGP functionality within the MSGS.
9	The QGP functionality examines and reformats the message before sending it to the MSCU functionality within the MSGS.
10	The MSCU functionality determines the message destination, performs additional formatting before sending the data over the DSCH to the AM.
11	In this example the data being sent is Automatic Message Accounting (AMA), therefore the AM will store the data on disk drive.

4.1.7.5 SM to AM Message Path Through The CM3

Figure 4-23 depicts the operation of an SM to AM message path through the CM3.

Figure 4-23 SM to AM Message Path Diagram

Table 4-10 steps provide a high-level example of the message flow between the SM and AM. The path can be used to send billing data, retrieve diagnostics, and other read/write operations to disk.

Table 4-10 SM to AM Message Path

Stage	Description
1	The protocol circuitry on the Application (APPL) Pack in the SM assembles a message that will be sent to the AM using an assigned Control Time Slot (CTS).
2	After the message is formatted and assembled, it is sent over the Link Interface Bus (LIB) to the Dual Link Interface (DLI).
3	The DLI inserts the message into the CTS and on to the transceiver which will perform the electrical to optical conversion.
4	The transceiver sent the CTS over the NCT link to the corresponding Optical Paddle Board (OPB) in the CM3.

5	The OPB performs the required optical to electrical conversion.
6	The data is sent over the backplane to the TMSF.
7	The data is checked and reformatted before being switched through the TMSF fabric and sent over the Control Time Slot Pump Link (CTPL) to the Module Message Processor (MMP).
8	The MMP functionality examines and reformats the message before sending it to the Message Switch Control Unit (MSCU) functionality within the Message Switch (MSGS).
9	The MSCU functionality determines the message destination, performs additional formatting before sending the data over Dual Serial Channel (DSCH) to the AM.
10	In this example the data being sent is Automatic Message Accounting (AMA), therefore the AM will store the data on disk drive.

4.1.7.6 CM3 to SM-2000 Normal Pump Operation

The Figure 4-24 depicts the operation of a normal pump of the CM3 to an SM-2000.

Figure 4-24 CM3 to SM-2000 Normal Pump Flow Diagram

Table 4-11 details the operation of a normal pump flow of the CM3 to an SM-2000. In the event that the SM-2000 memory becomes corrupt, a normal pump mechanism will be used to restore the memory.

Table 4-11 CM3 to SM-2000 Normal Pump Flow

Stage	Description
1	The AM accesses the proper SM-2000 files from the disk drive.
2	The AM then routes the data through the DMA.
3	The data is sent over the DSCH to the MSGS in the CM3.
4	The MSCU - IP functionality within the MSGS examines the data to determine the destination.
5	The MSCU - IP functionality formats and sends pump data to the PPC functionality within the MSGS.
6	The PPC functionality sent the data (32 odd network time slots) to the TMSF.
7	The TMSF routes the data through the fabric to the proper SM-2000.
8	The TMSF fabric sends the data to the OPB that terminates the "primary" odd NCT2 Link for an SM-2000.
9	The OPB performs the electrical to optical conversion and sends the data through a "primary" odd NCT2 link to

	the proper destination SM-2000.
10	The data is received by the NLI in the SM-2000.
11	The NLI converts the data from optical to electrical.
12	The data is sent through the TSI to the SMP and loaded into memory.

4.1.7.7 CM3 to SM Normal Pump Operation

The Figure 4-25 depicts the operation of a normal pump of the CM3 to an SM.

Figure 4-25 CM3 Normal Pump Flow Diagram

Table 4-12 details the operation of a normal pump flow of the CM3 to an SM. In the event that the SM memory becomes corrupt, a normal pump mechanism will be used to restore the memory.

Table 4-12 CM3 to SM Normal Pump Flow

Stage	Description
1	The AM accesses the proper SM files from the disk drive.
2	The AM then routes the data through the DMA.
3	The data is sent over the DSCH to the MSGS in the CM3.
4	The MSCU - IP functionality within the MSGS examines the data to determine the destination.
5	The MSCU - IP functionality formats and sends pump data to the PPC functionality within the MSGS.
6	The PPC functionality sent the data (32 odd network time slots) to the TMSF.
7	The TMSF routes the data through the fabric to the proper SM.
8	The TMSF fabric sends the data to the OPB that terminates the odd NCT Link for an SM.
9	The OPB performs the electrical to optical conversion and sends the data through a odd NCT link to the proper destination SM.
10	The data is received by the transceiver where it converts the data from optical to electrical, before being sent to the DLI.
11	The data is sent through the DLI to the TSI.
12	From the TSI the pump data is routed to the Data Interface 1 (DI 1) where the data is inserted onto a Peripheral Interface Data Bus (PIDB).
13	The PIDB carries the pump data to the APPL pack where the boot-strapper function formats the data to be

	loaded into the SMP memory.
14	After the pump data is prepared, it is loaded into dynamic memory.

4.1.7.8 CM3 to SM-2000 Backup Pump Operation

Figure 4-26 depicts the operation of a backup pump flow of the CM3.

Figure 4-26 CM3 to SM-2000 Backup Pump Flow Diagram

Table 4-13 details the operation of a backup pump flow of the CM3 to an SM-2000. When a normal pump can not be performed, then the *5ESS*® switch reverts to a backup pump.

Table 4-13 CM3 Backup Pump Flow

Stage	Description
1	The AM accesses the proper SM-2000 files from the disk drive.
2	The AM then routes the data through the DMA.
3	The data is sent over the DSCH to the MSGS in the CM3.
4	The MSCU - AP functionality within the MSGS examines the data to determine the destination.
5	The MSCU - AP functionality formats and sends pump data to the MMPs functionality within the MSGS.
6	The MMPs functionality sends the data (1 odd and 1 even CTS) to the TMSF.
7	The TMSF routes the data through the fabric to the proper SM-2000.
8	The TMSF fabric sends the data to the OPB that terminates the "primary" odd NCT2 Link for an SM-2000.
9	The OPB performs the electrical to optical conversion and sends the data through the "primary" NCT2 link to the proper destination SM-2000.
10	The data is received by the NLI in the SM-2000.
11	The NLI converts the data from optical to electrical.
12	The data is sent through the TSI to the SMP and loaded into memory.

When a backup pump is performed for an SM, the CM3 performs the same functions. However the CTS's are sent over the NCT links to the DLI in the SM. From the DLI, the CTS's are sent over the LIB to the APPL pack where the pump data is formatted and loaded into the dynamic memory.

4.1.8 Timing, CM3

Figure 4-27 details the timing of the CM3 between the Network Clock and Control (NCC) pack and Oscillator (OSC) packs.

Figure 4-27 CM3 Timing Operation

The NCC pack provides high stability clock synchronization (stratum 2) with the digital phone network. The NCC pack in the CM3 can terminate up to 8 external reference sources. (For information regarding reference terminations, refer to the CM3 cabling 4.1.14 .) The CM3 supports external references of stratum 2 or stratum 3 stability. The external references are monitored by the NCC pack which is capable of detecting lost or bad signals. In addition to the external references, the NCC monitors cross-coupled signals, and the input from both OSC packs.

The Network clocks operate in the "major-minor" mode. The AM selects which external reference (active) to use for synchronization. The NCC major filters and locks in to the requested reference, while the minor locks onto the cross-coupled signal generated by the major.

The NCC supports several modes of operation:

- **Normal**: Used when the clock is synchronized to the network.
- **Fast**: Used when attempting to quickly synchronize the primary reference.
- **Holdover**: Used when a reference is not available, the references become corrupt or by a request from the AM. When references are unavailable, one of the oscillators will provide the timing source that is used to maintain synchronization until a stable external source is available.

The Network Clock circuits main function is to generate a clock and sync pulse that is synchronized with one of its input reference clocks. The clocks are sent to even and odd TMSF circuit packs. Timing and synchronization is ultimately sent to the SMs over the NCT and NCT2 links.

The Oscillator Circuit Pack interfaces with both NCC boards. The Oscillator board contains an oven controlled oscillator that outputs a high stability Stratum 2, clock and a number of status indication signals to the NCC packs. The oven must reach its proper operating temperature before the oscillator can maintain a stratum 2 quality signal. The time required for the oscillator to obtain a stable stratum 2 signal is dependent on the length of time that the OSC pack has not had power applied and its starting temperature.

NOTE: Because it could take hours or even days to arrive at an acceptable frequency, care should be taken before removing power from the OSC pack.

4.1.9 Configuration, CM3

The CM3 architecture is duplex, with both Side 0 and Side 1 residing within the same cabinet.

In the CM3, MSGS Side 0 and Side 1 normally run active/active with one Control Time Slot (CTS) from each SM/SM-2000 routed through MSGS 0 and the other CTS routed through MSGS 1.

The NCC circuit packs are part of the ONTC failure group and as such are normally run active major/active minor, with messaging being directed at both ONTCs.

The QLPS architecture is divided into an even and an odd packet switch on Sides 0 and 1. The QLPS is normally run in an active/standby mode. The active/standby selection for the even QLPS is independent of the active/standby selection for the odd QLPS, (for example, the even QLPS may be active on Side 0, and the odd QLPS may be active on Side 1).

The MSGS selects which gateway time slots to monitor depending on which QLPS is active. The QLPS supports simultaneous gateway links to both sides of the MSGS since QGPs run active/active.

Table 4-14 lists the detailed duplex status in the major fault groups.

Table 4-14 CM3 Duplex Status

Unit	Status on Side 0		Status on Side 1	
MSGS	□		□	
□ MSCU	Active		Active	
□ CMP	Active/Standby		Standby/Active	
□ FPC	Active/Standby		Standby/Active	
□ PPC	Active/Standby		Standby/Active	
□ QGP	Active		Active	
□ MMP	Active (even)	Active (odd)	Active (even)	Active (odd)
ONTC	Active Major/Active Minor		Active Minor/Active Major	
□ ONTCCOM	Active Major/Active Minor		Active Minor/Active Major	
- NCLK	Active Major/Active Minor		Active Minor/Active Major	
□ QLPS	Active/Standby (even)	Active/Standby (odd)	Standby/Active (even)	Standby/Active (odd)
OSC	Active		Active	
□ TMSFP*****	Active		Active	
NOTE: *****For 5E16.2 and later.				

Under normal operating conditions the Office Network Timing Complex (ONTC) operates in an Active Major/Active Minor configuration. The Active Major ONTC carries calls and fifty percent of the control messages. The Active Minor ONTC is available to carry calls if the Active Major ONTC detects an abnormal condition. In addition, the Active Minor ONTC carries the remaining control messages. For 5E16.2 and later, all in-service TMSFPs on the major ONTCCOM side carry calls and all in-service TMSFPs on the minor ONTCCOM side are available to carry calls if problems occur on the major side.

When both ONTCs and both OSC are in-service, each network clock side utilizes the OSC on it's own side and both OSC are therefore considered "active". If one ONTC and both OSC are in-service, the ONTC selects one of the OSCs to be "active" and the other is considered "standby". If both ONTCs and

only one OSC are in-service, both network clocks utilize the only in-service ("active") OSC.

When a fault is detected on the ONTC, depending on it's severity, the ONTC will either be degraded or removed from service. A non-critical fault (for example a link out-of-frame condition) will cause the ONTC status to change to Active Major/Degraded Minor. When a more severe fault is detected, the ONTC status will change to Active Major/OOS.

Several of the functions in the message switch (MMPs, QGP and MSCU) operate in a load-shared configuration (Active/Active). Load sharing allows each side of the message switch to process control messages. The system splits the control messages evenly across the ONTCs which delivers them to each message switch. When engineered properly, under a fault condition, one side of the message switch will handle the entire load (all messages).

For 5E16.2 and later, TMSFPs are children of the ONTCCOM and parents of QLPSs/NLIs/DLIs. ONTC complex configuration requests include TMSFPs while ONTCCOM configuration requests do not. For example, manually removing an ONTC will also manually remove TMSFPs, whereas manually removing an ONTCCOM will instead put TMSFPs into an OOS family-of-equipment state. TMSFPs can also be configured (removed, restored, and diagnosed) individually. A TMSFP can only be diagnosed if the parent ONTCCOM is in-service.

Figure 4-28 depicts a high-level duplexed messaging architecture of the CM3 hardware fault groups, the MSGS, OSC, and ONTCCOM which are cross-coupled.

Figure 4-28 Duplex Messaging Architecture Diagram

The following signals within the CM3 are cross-coupled:

- The Control Time Slot and Pump Links (CTPL), QGLs between the MSGS and the TMS.
- The CDALs between the MSGS and the NCC.
- The OSC output between the OSC and the NCC.

- The timing reference between the NCCs.

In addition, the DSCH links between the CM3 and the AM are cross-coupled.

4.1.10 Service Impacts, CM3

Table 4-15 details the service impacts of the CM3.

Table 4-15 CM3 Service Impacts

Unit	Simplex Failure	Duplex Failure
MSGS	May lose some transient calls.	AM will start a transient clear initialization of the CM until it establishes a working configuration. The transient calls are lost but stable calls are preserved.
ONTCCOM	May lose some transient calls.	AM will start a stable clear initialization of the CM until it establishes a working configuration. All stable inter-SM calls will be lost, but stable intra-SM calls are not impacted.
QLPS	May lose some transient calls.	During periods of heavy traffic a significant reduction in capacity to set up new Inter SM calls. Stable Inter SM calls not impacted.
MSCU	May lose some transient calls.	AM will start a transient clear initialization of the CM until it establishes a working configuration. The transient calls are lost but stable calls are preserved.
CMP	Soft switch from active side no impact. Hard switch from active side transient calls may be impacted.	AM will start a transient clear initialization of the CM until it establishes a working configuration. The transient calls are lost but stable calls are preserved.
FPC	Soft switch from active side no impact. Hard switch from active side transient calls may be impacted.	AM will start a transient clear initialization of the CM until it establishes a working configuration. The transient calls are lost but stable calls are preserved.
QGP	May lose some transient calls.	During periods of heavy traffic a significant reduction in capacity to set up new Inter SM calls. Stable Inter SM calls not impacted.
MMP	May lose some transient calls.	Loss of normal pump and CTS pump.
PPC	No subscriber impact.	Loss of normal pump.
TMSFP	No subscriber impact if failure occurs on the minor ONTCCOM side. May lose some transient calls for failures on the major side and, if an ONTC switch cannot occur (e.g. due to other OOS units), some inter-SM stable calls may be lost and TMS capacity will be reduced.	All inter-SM stable calls carried by the affected TMSFP will be lost and TMS capacity will be reduced. If the primary TMSFP is impacted, the AM can no longer communicate with the SMs/SM-2000s, and will therefore start a stable clear initialization of the CM until it establishes a working configuration. All stable inter-SM calls will be lost. Stable intra-SM calls are not impacted.

4.1.11 Remove Electrical Power, CM3

The circuit packs used in the CM3 are automatically powered down as they are removed from the shelf. Circuits must be removed from service before any pack changing can be done.

4.1.12 MCC Pages and Pokes, CM3

This section shows the CM3-related MCC pages for all supported software releases. In cases where significant changes have been made for some software releases, multiple versions are shown.

MCC Page	Title
Prior to 5E16.2 and 5E16.2 and later	
1005	CM PAGE INDEX
115	COMMUNICATION MODULE SUMMARY
1201	SM X - DLI/NLI/TMSLNK SET Y
1209	ONTC 0 AND 1

1210	NETWORK CLOCK
1211	NETWORK CLOCK REFERENCES
1212	TMS FABRIC PAIR STATUS
1214	QLPS SUMMARY
1220	TMS 0/1 SUMMARY
1221-1228/1231-1238	TMS LINKS 0/1
1240	MSGS 0 STATUS
1250	MSGS 1 STATUS
1380/1381	QLPS NETWORK 0/1 STATUS
1850	CMP PRIM INH & RCVRY CNTL
1851	CMP MATE INH & RCVRY CNTL
1900,X	SM X CLNK STATUS AND CONTROL

The CM Page Index MCC page (1005) is an index to the primary CM subunit pages that have status reflected on the MCC 115 page. Figure 4-29 shows the 1005 page 5E16.2 and later figure 4-30 shows the 1005 page prior to 5E16.2.

Figure 4-29 1005 - CM Page Index MCC Page (5E16.2 and later)

Figure 4-30 1005 - CM Page Index MCC Page (Prior to 5E16.2)

The Communication Module Summary MCC Page (115) provides a summary of the CM status. Figures 4-31 show this MCC page (prior to 5E16.2 and later) and figure 4-32 (5E16.2 and later), has been modified to show the new MCC screens 1212 and 1214. The 1221-1228 and 1231-1238 boxes are removed. Those pages are now accessed from the 1220,Y (Y=TMSFP) pages off of the 1212 page.

Figure 4-31 115 - Communication Module Summary MCC Page (Prior to 5E16.2)

Figure 4-32 115 - Communication Module Summary MCC Page (5E16.2 and Later)

The DLI/NLI/TMSLNK Set MCC pages (1201,Y), show status for the DLIs, NLIs, and the TMSLNKs that are connected to each ONTCCOM on a per-SM basis and provide maintenance commands for the DLIs/NLIs. Figure 4-33 shows SM/SM-2000 versions for MCC pages prior to 5E16.2 and figure 4-34 , was modified to add the TMSFP number in the ONTCCOM box to display the state of the TMSFP associated with the NLIs/DLIs for SM/SM-2000 versions for MCC pages 5E16.2 and later.

Figure 4-33 1201 - DLI/NLI/TMSLNK Set MCC Page (Prior to 5E16.2)

Figure 4-34 1201 - DLI/NLI/TMSLNK Set MCC Page (5E16.2 and Later)

The ONTC 0 and 1 MCC page (1209), displays maintenance states for ONTC 0 and 1 and provides maintenance commands for the ONTCs, ONTCCOMs and QLPS and hardware check status for ONTC 0 and 1. Figure 4-35 show the MCC page 1209 prior to 5E16.2 and figure 4-36 , was modified to remove the QLPS indicators (which moved to page 1214) which is the version for MCC pages 5E16.2 and later.

Figure 4-35 1209 - ONTC 0 and 1 MCC Page (Prior to 5E16.2)

Figure 4-36 1209 - ONTC 0 and 1 MCC Page (5E16.2 and Later)

Figure 4-37 shows MCC page 1210 for Network Clock and the Network Clock Oscillator (NCOSC).

Figure 4-37 Network Clock MCC Page (1210)

Figure 4-38 shows the MCC page 1211 for the Network Clock References.

Figure 4-38 Network Clock References MCC Page (1211)

The TMS Fabric Pair Status MCC page (1212), shown in figure 4-39 displays the state of the ONTCCOMs and all TMSFPs equipped in the office. Off-normal conditions related to QLPS and NLI/DLI/TMSLNK units will cause indicators on the 1212 page to backlight.

Figure 4-39 1212 - TMS Fabric (N=4) Pair Status MCC Page (5E16.2 and Later) The QLPS Summary MCC page (1214), shown in figure 4-40 displays the state of the ONTCCOMs, primary TMSFPs, and QLPSs. It provides an overall view of the status of both QLPS networks on a single page. Prior to 5E16.2, this information was found on MCC page 1209.

Figure 4-40 1214 - QLPS Summary MCC Page (5E16.2 and Later)

The TMSLNK Summary page (1220,Y where Y = TMSFP number), displays status for the TMS or TMSFP and to provide an index to the TMS LINK pages. Figure 4-41 shows the version prior to 5E16.2 and figure 4-42 shows the 5E16.2 and later version which now includes the state of the TMSFP as well as the ONTCCOM. If NLIs/DLIs/TMSLNKs are out-of-service, the indicators associated with the affected TMSLNK set will backlight.

Figure 4-41 1220 - TMS 0 and 1 Summary MCC Page (Prior to 5E16.2)

Figure 4-42 1220 - TMS 0 and 1 Summary MCC Page (5E16.2 and Later)

The TMS Links MCC pages 1221-1228 (Side 0) and 1231-1238 (Side 1) shows the status and maintenance commands for the TMS links. Figure 4-43 shows the version prior to 5E16.2 and figure 4-44 shows the version for 5E16.2 and later which was modified to show the TMSFP links are assigned to.

Figure 4-43 1221-1228 - TMS Links (Side 0) and 1231-1238 - TMS Links (Side 1) Example MCC Page (Prior to 5E16.2)

Figure 4-44 1221-1228 - TMS Links (Side 0) Example MCC Page (5E16.2 and Later)

The 1240 Page is for MSGS 0, and the 1250 Page is for MSGS 1 show status and provide maintenance commands for the message switches (MSGS). The MCC pages 1240 (figure 4-45) and 1250 (figure 4-46) detail the MSGS 0 and 1 status.

Figure 4-45 1240 - MSGS 0 Status MCC Page

Figure 4-46 1250 - MSGS 1 Status MCC Page

The QLPS Network 0 Status (1380) and QLPS Network 1 Status (1381) pages show status and provide maintenance commands for the Quad Link Packet Switch (QLPS) network 0 and network 1, figure 4-47 shows the version prior to 5E16.2 and figure 4-48 shows the version for 5E16.2 and later which were modified to indicate that the QLPS units are always associated with TMSFP 0.

Figure 4-47 1380 and 1381 - QLPS Network 0 and 1 Status MCC Page (Prior to 5E16.2)

Figure 4-48 1380 and 1381 - QLPS Network 0 and 1 Status MCC Page (5E16.2 and Later)

The CMP PRIM INH & RCVRY CNTL page 1850 provides status displays for both the primary and mate CMPs of the pair. Also provided are menu commands to inhibit or allow hardware and software checks, routine audits, automatic pump, brevity control, and set and clear for recent change backout as shown in figure 4-49 . The CMP Mate Inhibit and Recovery Control page 1851 is similar to the 1850 page except that 600 and 700 level pokes cannot be entered from the 1851 page. Also, the 1851 page has the 930 and 931 commands that the 1850 does not have as shown in figure 4-50 .

Figure 4-49 1850 - CMP PRIM INH & RCVRY CNTL MCC Page (5E15.2 and Later)

Figure 4-50 1851 - CMP MATE INH & RCVRY CNTL MCC Page (5E15.2 and Later)

The LSM CLNK Status & Control page (1900,X where X = SM/SM-2000 number), shows the status of each CLNK to SM X and the status of the supporting hardware. Figure 4-51 shows version prior to 5E16.2 and figure 4-52 shows version 5E16.2 and later which includes the state of the TMSFP as well as the ONTCCOM.

Figure 4-51 1900,X - SM X CLNK Status and Control MCC Page (Prior to 5E16.2)

Figure 4-52 1900,X - SM X CLNK Status and Control MCC Page (5E16.2 and Later)

The *5ESS*® switch provides two methods of testing hardware components:

- They can be tested with a restore command, which will run the associated diagnostic or operational tests and if all tests pass this command will place the unit back in service.
- They can also be tested with a diagnose command, which will run the associated diagnostic test and whether all tests pass or not this command will leave the unit out of service.

For CM3, the MSGS units (MSCU, FPC, MMP, PPC, QGP, and CMP) are combined into a single circuit pack. As such there is only one MSGS diagnostic and only one circuit pack to replace. The MSCU, FPC, MMP, PPC, QGP, and CMP units do not have diagnostic tests directly associated with them. These units are tested when the MSGS is tested.

For CM3, the FPC, MMP, PPC, QGP, and CMP conditional restore command (MML or poke) has been changed to execute operational tests instead of diagnostic tests. If these tests pass the unit is then placed into service, if the tests fail the unit is placed out of service and a MSGS restore or diagnostic must be performed to determine the cause of the failure.

For CM3, the MSCU conditional restore command (MML or poke) is not allowed. The reason for this is because there is no MSCU diagnostics, only MSGS diagnostics. Since the MSCU is the central controlling function of the MSGS, no operational tests could be performed to insure that faulty MSGS hardware would

not interfere with operation of the AM, ONTCs, or SMs. If an MSCU conditional restore must be performed, the MSGS conditional restore command should be used.

It is highly recommended that if these units are out of service, for any reason other than a manual remove, that the MSGS diagnostic or restore command be used to ensure all functionality is tested.

In the following table, the MSGS is the only unit that is diagnosable. All functionality of the MSCU, CMP, FPC, PPC, QGP, and the MMP will be tested when the MSGS is tested.

CM3 MSGS Functionality

Unit	Diagnosable?	Restores	Removes	Inhibits	Switch
MSGS	Yes	Yes	Yes	Yes	NA
MSCU	No*	No*	Yes	Yes	NA
CMP	No*	Yes**	Yes	Yes	Yes
FPC	No*	Yes**	Yes	Yes	Yes
PPC	No*	Yes**	Yes	Yes	Yes
QGP	No*	Yes**	Yes	Yes	NA
MMP	No*	Yes**	Yes	Yes	NA

NOTE: *******In order to run diagnostic test on any of these units you must use the MSGS diagnostic/restore using the poke/MML command. The MML message for restoring the MSCU has been changed in CM3. *RST:MSCU=n* is no longer a valid message.

******Operational tests are performed before restores on these units.

The following table describes the configuration actions that can be performed on the ONTC complex and its sub-components.

ONTC and ONTCCOM

Unit	Diagnosable?	Restores	Removes	Inhibits	Switch
ONTC	No*	Yes**	Yes	Yes	Yes
ONTCCOM	Yes***	Yes	Yes	No	No
DLI	Yes	Yes	Yes	No	No
NLI	Yes	Yes	Yes	No	No
QLPS	Yes****	Yes	Yes	No	Yes
TMSFP	Yes*****	Yes	Yes	No	No
NCLK	No	No	No	No	Yes****

NOTE: *******The MML message DGN:ONTC=n will return an NG (No Good).

******The MML message or poke command to restore the ONTC will run all diagnostics on the ONTCCOM and it's subtending units.

*******Prior to 5E16.2, the ONTCCOM diagnostic tests the MLI, NCLK, and TMS functionality. In 5E16.2 and later, most TMS functionality (with the exception of the TMS controller on the NCC board) is tested as part of the TMSFP diagnostic.

********To run diagnostics, the TMSFP (5E16.2 and Later) must be in service.

*********The NCLK switch changes which NCLK (ONTC) side is the master source of timing, whereas an ONTC switch changes which TMS (ONTC) side is normally used for call processing.

4.1.13 Diagnostic Phases, CM3

The following tables detail each diagnostic phases and descriptions of the Message Switch (MSGS) 4-16 , [ONTCCOM (Prior to 5E16.2)] 4-17 , [ONTCCOM (5E16.2 and later)] 4-18 , (TMSFP) 4-19 , and (QLPS) 4-20 of the CM3.

Table 4-16 MSGS Diagnostic Phases

MSGS	
Phase	**Description**
PH 1	Interfaces between DSCH and DDSBS, DDSBS and BIC
PH 2	MSGS power/BIST/Boundary-Scan; MSGS-IP PowerQuicc bus access; DSCH controller; Asset IP power/BIST/Boundary-Scan; Critical MSGS reset; MSGS/Asset Loop 6 Boundary-Scan; IP DRAM March test; AP DRAM BIST
PH 3	IP Register Access, Interrupts, Reset, PCI
PH 4	IP Timers, IP Sanity Maze

PH 5	IP DRAM/ECC,Cache, MMU
PH 6	AP Register Access, Interrupts, Reset,PCI
PH 7	AP Timers, AP Sanity Maze
PH 8	AP Caches, MMU
PH 9 (demand)	IP and AP PFI
PH 10	IP and AP Interface
PH 11	PACMAN static functional operation; PCI bus for application; Ethernet controller reset; ACT MSGS/NCC presence/power status; MSGS IP/AP interrupts/error tree; PFI registers with disabled PFI strap; DMA/control strobe points interface update; MSGS clock
PH 12	MSGS SPYDER-256 platform static tests: PCI/device resets; SRAM BIST; PCI/message errors; Standby and key registers; SRAM access/scrub; Serial loop; Multi-channel
PH 13	Connectivity between OOST MSGS and ACT ONTC over CTS links
PH 14	Connectivity between OOST MSGS and ACT ONTC over pump link
PH 15	Ability of OOST MSGS to establish and utilize the CDAL link to each ONTCCOM
PH 16 (demand)	PFI registers with enabled PFI strap

Table 4-17 ONTCCOM Diagnostic Phases (Prior to 5E16.2)

ONTCCOM	
Phase	**Description**
PH 1	NCC power/presence
PH 2	ONTC processor reset; AM and ONTC-IP communication; Asset IP power/BIST/Boundary-Scan; NCC/Asset Loop 6 Boundary-Scan; IP DRAM March test; AP DRAM BIST
PH 3	IP Register Access, Interrupts, Reset, PCI
PH 4	IP Timers, IP Sanity Maze
PH 5	IP DRAM/ECC,Cache, MMU
PH 6	AP Register Access, Interrupts, Reset,PCI
PH 7	AP Timers, AP Sanity Maze
PH 8	AP Caches, MMU
PH 9 (demand)	IP and AP PFI
PH 10	IP and AP Interface
NCC	
PH 11	SPYDER-256 platform
PH 12	Register exercises; TMSF ESRs in NCC_CSI; STARS/CSI/SPYDER to IRR error propagation; SPYDER/CSI to IP SIPEND error propagation; DMA state machine and phase counters operation on STARS; STARS input mux control register; Line framer T7630 capability; Operation of HWPLLEN in PLL/frequency control registers
PH 13	Far/Near side oscillator power and board presence; STARS equipped digital/analog and unequipped analog references; Cross couple references
PH 14	Operation of digital/analog references and oscillator; CDAL link synchronization; CDAL bits A/E/F/G; CDAL bits B/C/D
PH 15 (demand)	PFI registers with enabled PFI strap
TMS	
PH 16	AM and ONTC-AP communication; TMSF reset; Primary CSI; Fuse alarm; Fan alarm
PH 17	FMI reset; FMI BIST; FMI secondary CSI; FMI test function; FMI CPI; FMI CPTL/CTS
PH 18	(on all TMSF/Xs) LIT48 reset; LIT48 BIST; LIT48 secondary CSI; FMI - LIT48 FDI links; PFI registers with disabled PFI strap
PH 19	(on all TMSF/Xs) FMI - LIT48 - FMI TMS link to link internal loop back; FMI fabric
PH 20	TRCU (NAR only)
PH 21 (demand)	External TMS link loop back
PH 22 (demand)	TMSF/X PFI registers with enabled PFI strap

Table 4-18 ONTCCOM Diagnostic Phases (5E16.2 and later)

ONTCCOM	
Phase	**Description**
PH 1	NCC power/presence
PH 2	ONTC processor reset; AM and ONTC-IP communication; Asset IP power/BIST/Boundary-Scan; NCC/Asset Loop 6 Boundary-Scan; IP DRAM March test; AP DRAM BIST
PH 3	IP Register Access, Interrupts, Reset, PCI
PH 4	IP Timers, IP Sanity Maze
PH 5	IP DRAM/ECC,Cache, MMU
PH 6	AP Register Access, Interrupts, Reset,PCI
PH 7	AP Timers, AP Sanity Maze
PH 8	AP Caches, MMU
PH 9 (demand)	IP and AP PFI
PH 10	IP and AP Interface
NCC	
PH 11	SPYDER-256 platform
PH 12	Register exercises; TMSF ESRs in NCC_CSI; STARS/CSI/SPYDER to IRR error propagation;

	SPYDER/CSI to IP SIPEND error propagation; DMA state machine and phase counters operation on STARS; STARS input mux control register; Line framer T7630 capability; Operation of HWPLLEN in PLL/frequency control registers
PH 13	Far/Near side oscillator power and board presence; STARS equipped digital/analog and unequipped analog references; Cross couple references
PH 14	Operation of digital/analog references and oscillator; CDAL link synchronization; CDAL bits A/E/F/G; CDAL bits B/C/D
PH 15 (demand)	PFI registers with enabled PFI strap

Table 4-19 TMSFP Diagnostic Phases (5E16.2 and later)

TMSFP	
Phase	**Description**
PH 1	AM and ONTC-AP communication; TMSF reset; Primary CSI; Fuse alarm; Fan alarm
PH 2	FMI reset; FMI BIST; FMI secondary CSI; FMI test function; FMI CPI; FMI CPTL/CTS
PH 3	(on all TMSF/Xs) LIT48 reset; LIT48 BIST; LIT48 secondary CSI; FMI - LIT48 FDI links; PFI registers with disabled PFI strap
PH 4	Internal loop around of LIT48 - FMI
PH 5	(on all TMSF/Xs) FMI - LIT48 - FMI TMS link to link internal loop back; FMI fabric
PH 6	TRCU3 (NAR only)
PH 7 (demand)	TMS link loop back

Table 4-20 QLPS Diagnostic Phases

QLPS	
Phase	**Description**
PH 1	AM and ONTC-AP communication; PRISM reset; PRISM device/PRAM BIST; PRISM secondary CSI
PH 2	PRISM QTMSLNK; PRISM pointer monitor; PRISM packet reception
PH 3	PRISM single broadcast; PRISM multiple broadcast; PRISM QGL

4.1.14 Cables, CM3

The following sections depict a fully configured backplane and cabling information for the CMU2 and TMSU4 of a CM3.

4.1.14.1 CMU2 Cable Description

Figure 4-53 depicts the CMU2 backplane and cabling locations.

Figure 4-53 CMU2 OPBs and Pin Field Cabling Diagram

The Communication Module Unit Model 2 (CMU2) is located in the CM3. Figure 4-53 details the pin field cable terminal and cabling for each side of the CMU2. Also 40 slots for optical paddleboards (OPBs) (20 OPBs is the limit if populating with NCT2 and 40 OPBs for NCT link connections). The OPBs are the same for both base and growth cabinets.

Figure 4-54 shows how to read figure 4-53 and table 4-21 .

Figure 4-54 How to Read Optical Paddle Boards and Pin Field Cables

Table 4-21 depicts the port assignments for CMU2 TMS link optical paddleboards connections to the SMs/SM-2000s as shown in Figure 4-53 .

Table 4-21 CMU2 Port Assignments

Port Assignment for CMU2 TMS Links								
CMU2 Front - Side 0					CMU2 Rear - Side 1			
SM Number	EQL	PB	TMS LNK	Port	EQL	PB	TMS LNK	Port
SM( )	18F-093-TX/RX	Even	004	001-Top	18R-093-TX/RX	Even	004	001-Top
SM( )	18F-093-TX/RX	Odd	005	001-Bot	18R-093-TX/RX	Odd	005	001-Bot
SM( )	18F-113-TX/RX	Even	006	002-Top	18R-113-TX/RX	Even	006	002-Top

SM( )	18F-113-TX/RX	Odd	007	002-Bot	18R-113-TX/RX	Odd	007	002-Bot
SM( )	18F-133-TX/RX	Even	008	003-Top	18R-133-TX/RX	Even	008	003-Top
SM( )	18F-133-TX/RX	Odd	009	003-Bot	18R-133-TX/RX	Odd	009	003-Bot
SM( )	18F-153-TX/RX	Even	010	004-Top	18R-153-TX/RX	Even	010	004-Top
SM( )	18F-153-TX/RX	Odd	011	004-Bot	18R-153-TX/RX	Odd	011	004-Bot
SM( )	18F-173-TX/RX	Even	012	005-Top	18R-173-TX/RX	Even	012	005-Top
SM( )	18F-173-TX/RX	Odd	013	005-Bot	18R-173-TX/RX	Odd	013	005-Bot
SM( )	18F-193-TX/RX	Even	014	006-Top	18R-193-TX/RX	Even	014	006-Top
SM( )	18F-193-TX/RX	Odd	015	006-Bot	18R-193-TX/RX	Odd	015	006-Bot
SM( )	18F-213-TX/RX	Even	016	007-Top	18R-213-TX/RX	Even	016	007-Top
SM( )	18F-213-TX/RX	Odd	017	007-Bot	18R-213-TX/RX	Odd	017	007-Bot
SM( )	18F-233-TX/RX	Even	018	008-Top	18R-233-TX/RX	Even	018	008-Top
SM( )	18F-233-TX/RX	Odd	019	008-Bot	18R-233-TX/RX	Odd	019	008-Bot
SM( )	18F-253-TX/RX	Even	020	009-Top	18R-253-TX/RX	Even	020	009-Top
SM( )	18F-253-TX/RX	Odd	021	009-Bot	18R-253-TX/RX	Odd	021	009-Bot
SM( )	18F-273-TX/RX	Even	022	010-Top	18R-273-TX/RX	Even	022	010-Top
SM( )	18F-273-TX/RX	Odd	023	010-Bot	18R-273-TX/RX	Odd	023	010-Bot
SM( )	21F-093-TX/RX	Even	024	011-Top	21R-093-TX/RX	Even	024	011-Top
SM( )	21F-093-TX/RX	Odd	025	011-Bot	21R-093-TX/RX	Odd	025	011-Bot
SM( )	21F-113-TX/RX	Even	026	012-Top	21R-113-TX/RX	Even	026	012-Top
SM( )	21F-113-TX/RX	Odd	027	012-Bot	21R-113-TX/RX	Odd	027	012-Bot
SM( )	21F-133-TX/RX	Even	028	013-Top	21R-133-TX/RX	Even	028	013-Top
SM( )	21F-133-TX/RX	Odd	029	013-Bot	21R-133-TX/RX	Odd	029	013-Bot
SM( )	21F-153-TX/RX	Even	030	014-Top	21R-153-TX/RX	Even	030	014-Top
SM( )	21F-153-TX/RX	Odd	031	014-Bot	21R-153-TX/RX	Odd	031	014-Bot
SM( )	21F-173-TX/RX	Even	032	015-Top	21R-173-TX/RX	Even	032	015-Top
SM( )	21F-173-TX/RX	Odd	033	015-Bot	21R-173-TX/RX	Odd	033	015-Bot
SM( )	21F-193-TX/RX	Even	034	016-Top	21R-193-TX/RX	Even	034	016-Top
SM( )	21F-193-TX/RX	Odd	035	016-Bot	21R-193-TX/RX	Odd	035	016-Bot
SM( )	21F-213-TX/RX	Even	036	017-Top	21R-213-TX/RX	Even	036	017-Top
SM( )	21F-213-TX/RX	Odd	037	017-Bot	21R-213-TX/RX	Odd	037	017-Bot
SM( )	21F-233-TX/RX	Even	038	018-Top	21R-233-TX/RX	Even	038	018-Top
SM( )	21F-233-TX/RX	Odd	039	018-Bot	21R-233-TX/RX	Odd	039	018-Bot
SM( )	21F-253-TX/RX	Even	040	019-Top	21R-253-TX/RX	Even	040	019-Top
SM( )	21F-253-TX/RX	Odd	041	019-Bot	21R-253-TX/RX	Odd	041	019-Bot
SM( )	21F-273-TX/RX	Even	042	020-Top	21R-273-TX/RX	Even	042	020-Top
SM( )	21F-273-TX/RX	Odd	043	020-Bot	21R-273-TX/RX	Odd	043	020-Bot
SM( )	25F-093-TX/RX	Even	044	021-Top	25R-093-TX/RX	Even	044	021-Top
SM( )	25F-093-TX/RX	Odd	045	021-Bot	25R-093-TX/RX	Odd	045	021-Bot
SM( )	25F-113-TX/RX	Even	046	022-Top	25R-113-TX/RX	Even	046	022-Top
SM( )	25F-113-TX/RX	Odd	047	022-Bot	25R-113-TX/RX	Odd	047	022-Bot
SM( )	25F-133-TX/RX	Even	048	023-Top	25R-133-TX/RX	Even	048	023-Top
SM( )	25F-133-TX/RX	Odd	049	023-Bot	25R-133-TX/RX	Odd	049	023-Bot
SM( )	25F-153-TX/RX	Even	050	024-Top	25R-153-TX/RX	Even	050	024-Top
SM( )	25F-153-TX/RX	Odd	051	024-Bot	25R-153-TX/RX	Odd	051	024-Bot

SM( )	25F-173-TX/RX	Even	052	025-Top	25R-173-TX/RX	Even	052	025-Top
SM( )	25F-173-TX/RX	Odd	053	025-Bot	25R-173-TX/RX	Odd	053	025-Bot
SM( )	25F-193-TX/RX	Even	054	026-Top	25R-193-TX/RX	Even	054	026-Top
SM( )	25F-193-TX/RX	Odd	055	026-Bot	25R-193-TX/RX	Odd	055	026-Bot
SM( )	25F-213-TX/RX	Even	056	027-Top	25R-213-TX/RX	Even	056	027-Top
SM( )	25F-213-TX/RX	Odd	057	027-Bot	25R-213-TX/RX	Odd	057	027-Bot
SM( )	25F-233-TX/RX	Even	058	028-Top	25R-233-TX/RX	Even	058	028-Top
SM( )	25F-233-TX/RX	Odd	059	028-Bot	25R-233-TX/RX	Odd	059	028-Bot
SM( )	25F-253-TX/RX	Even	060	029-Top	25R-253-TX/RX	Even	060	029-Top
SM( )	25F-253-TX/RX	Odd	061	029-Bot	25R-253-TX/RX	Odd	061	029-Bot
SM( )	25F-273-TX/RX	Even	062	030-Top	25R-273-TX/RX	Even	062	030-Top
SM( )	25F-273-TX/RX	Odd	063	030-Bot	25R-273-TX/RX	Odd	063	030-Bot
SM( )	29F-093-TX/RX	Even	064	031-Top	29R-093-TX/RX	Even	064	031-Top
SM( )	29F-093-TX/RX	Odd	065	031-Bot	29R-093-TX/RX	Odd	065	031-Bot
SM( )	29F-113-TX/RX	Even	066	032-Top	29R-113-TX/RX	Even	066	032-Top
SM( )	29F-113-TX/RX	Odd	067	032-Bot	29R-113-TX/RX	Odd	067	032-Bot
SM( )	29F-133-TX/RX	Even	068	033-Top	29R-133-TX/RX	Even	068	033-Top
SM( )	29F-133-TX/RX	Odd	069	033-Bot	29R-133-TX/RX	Odd	069	033-Bot
SM( )	29F-153-TX/RX	Even	070	034-Top	29R-153-TX/RX	Even	070	034-Top
SM( )	29F-153-TX/RX	Odd	071	034-Bot	29R-153-TX/RX	Odd	071	034-Bot
SM( )	29F-173-TX/RX	Even	072	035-Top	29R-173-TX/RX	Even	072	035-Top
SM( )	29F-173-TX/RX	Odd	073	035-Bot	29R-173-TX/RX	Odd	073	035-Bot
SM( )	29F-193-TX/RX	Even	074	036-Top	29R-193-TX/RX	Even	074	036-Top
SM( )	29F-193-TX/RX	Odd	075	036-Bot	29R-193-TX/RX	Odd	075	036-Bot
SM( )	29F-213-TX/RX	Even	076	037-Top	29R-213-TX/RX	Even	076	037-Top
SM( )	29F-213-TX/RX	Odd	077	037-Bot	29R-213-TX/RX	Odd	077	037-Bot
SM( )	29F-233-TX/RX	Even	078	038-Top	29R-233-TX/RX	Even	078	038-Top
SM( )	29F-233-TX/RX	Odd	079	038-Bot	29R-233-TX/RX	Odd	079	038-Bot
SM( )	29F-253-TX/RX	Even	080	039-Top	29R-253-TX/RX	Even	080	039-Top
SM( )	29F-253-TX/RX	Odd	081	039-Bot	29R-253-TX/RX	Odd	081	039-Bot
SM( )	29F-273-TX/RX	Even	082	040-Top	29R-273-TX/RX	Even	082	040-Top
SM( )	29F-273-TX/RX	Odd	083	040-Bot	29R-273-TX/RX	Odd	083	040-Bot

The following cables are common between the base and growth CM3 cabinets:

- Control Synchronization Interface (CSI) and Expansion Cables between the CMU2 and each TMSU4.
- CMU2 Cross Coupling cables between CMU2 side 0 and 1.
- CMU2 ports: NCT, primary NCT2 (base only) and secondary NCT2 links (base and growth)
- TMSU4 ports NCT, primary NCT2 (base only) and secondary NCT2 links (base and growth) .

The following base cabinet cables are terminated at the CM3:

- Dual Serial Channel.
- Scan and Signal Distribute.

- Network Clock Reference Cables.
- Control and Synchronization Interface (CSI) cables from the NCC to the Growth Cabinets.

The CM3 NxTMS adds a control and timing synchronization (CSI) fan-out from the base cabinet out to each growth cabinet, as shown in figure 4-55 .

Figure 4-55 CM3 NxTMS CSI Cable Fan-Out

Table 4-22 depicts the intra-cabinet cabling termination between the CMU2 to the TMSU4 as shown in figure 4-56 . The intra-cabinet cabling is the same in the base and growth cabinets.

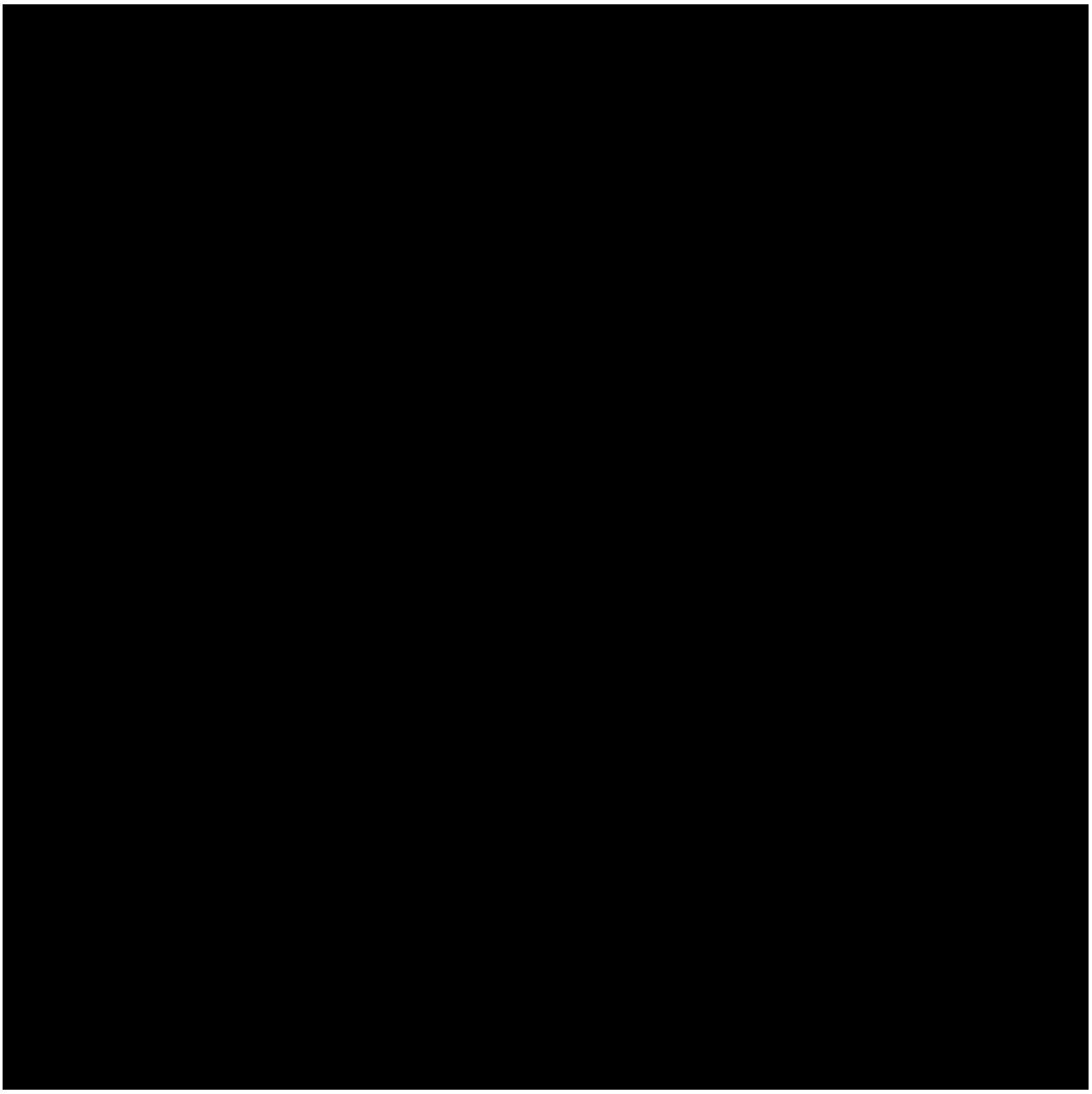

Figure 4-56 CMU2 Cable Field of the Base and Growth Cabinets

Table 4-22 CMU2 to TMSU4 Pin Field Cables

TMSU 4 Shelf	CMU2 EQL Cables	TMSU4 EQL Cables
Control and Synchronization Interface (CSI)		
1	24F-309-157	35F-324-007
	24R-309-151	35R-324-001
2	24F-329-157	45F-324-007
	24R-329-151	45R-324-001
3	24F-349-157	55F-324-007
	24R-349-151	55R-324-001
(expansion)		
1	24F-309-145	35F-324-019
	24R-309-139	35R-324-013
2	24F-329-145	45F-324-019
	24R-329-139	45R-324-013
3	24F-349-145	55F-324-019
	24R-349-139	55R-324-013

Table 4-23 depicts the intra-cabinet cabling between the CMU2 and Fan Fuse Alarm cables as shown in

figure 4-56 . The intra-cabinet cabling is the same in the base and growth cabinets.

Table 4-23 CMU2 to Fan Fuse Alarm Pin Field Cables

Fan Fuse Alarm	CMU2	Fan Fuse Alarm Cables
11F-300	24F-349-121	68-098-106
		68-098-103
11F-200	24R-349-121	68-098-003
		68-098-006

Table 4-24 depicts the inter-cabling terminations of the CM3 to the AM as shown in figure 4-56 . The intra-cabling is the same in the base and growth cabinets.

Table 4-24 CM3 to AM Pin Field Cables

CM3		AM	
Side	EQL	Unit	EQL
CM 0 DSCH	024F-309-121	CU 0 DMA 0	028-075-151
CM 1 DSCH	024R-309-121	CU 0 DMA 1	028-075-119
CM 0 DSCH	024F-329-121	CU 1 DMA 0	053-075-151
CM 1 DSCH	024R-329-121	CU 1 DMA 1	053-075-119
CM 0 SCAN	024F-309-109	IOP 0 SCAN 0	019-110-541
CM 1 SCAN	024R-309-109	IOP 0 SCAN 1	019-110-741
CM 0 SCAN	024F-329-109	IOP 1 SCAN 1	045-110-154
CM 1 SCAN	024R-329-109	IOP 1 SCAN 0	045-110-341

Table 4-25 depicts the CMU2 Network Clock pin cabling fields. The source for Network timing varies in each Central Office. Because of this, figure 4-56 will only depict where the external reference cables will be terminated on CM3. The cabling is the same in the base and growth cabinets.

Table 4-25 Network Clock Pin Field Cables

Network Clock Reference Location	
Cable	CMU2
64K - 1	24F-309-103
	24R-309-103
64K - 2	24F-329-103
	24R-329-103
Analog 2.048 MHz - 1	24F-309-097
	24R-309-097
Analog 2.048 MHz - 2	24F-329-097
	24F-329-097
Analog 10 MHz - 1	24R-309-091
	24F-309-091
Analog 10 MHz - 2	24R-329-091
	24R-329-091
T1 or E1 - 1	24F-309-079
	24R-309-079
T1 or E1 - 5	24F-329-079
	24R-329-079
T1 or E1 - 2	24F-309-073
	24R-309-073
T1 or E1 - 6	24F-329-073
	24R-329-073
T1 or E1 - 3	24F-309-067
	24R-309-067
T1 or E1 - 7	24F-329-067
	24R-329-067
T1 or E1 - 4	24F-309-061
	24R-309-061
T1 or E1 - 8	24F-329-061
	24R-329-061

Table 4-26 depicts the cross-coupling cables between the CMU2 side 0 and 1 as shown in figure 4-56 .

Table 4-26 CMU2 Cross-Couple Pin Field Cables

Cable	CMU2 0	CMU2 1
MSGS Update	24F-309-055	24R-329-055
	24F-329-055	24R-309-055

MSGS to TMS	24F-309-049	24R-329-049
	24F-309-043	24R-329-043
TMS to MSGS	24F-329-049	24R-309-049
	24F-329-043	24R-309-043
NCC to MSGS	24F-309-037	24R-329-037
	24F-309-031	24R-329-031
MSGS to NCC	24F-329-037	24R-309-037
	24F-329-031	24R-309-031
8K NCC to MSGS	24F-309-019	24R-329-019
8K MSGS to NCC	24F-329-019	24R-309-019

For 5E16.2 and later, table 4-27 shows the CMU2 cable field of the base and growth cabinets. The TMSU4 cable field stays the same.

Table 4-27 CMU2 Cable Field of the Base and Growth Cabinets

EQL	Base CMU2	EQL	Growth CMU2
025-349	NXTMS Out	019-349	NXTMS Base of Cabinet 0
031-349	NXTMS 01	019-349	NXTMS Base of Cabinet 1
037-349	NXTMS 02	019-349	NXTMS Base of Cabinet 2
043-349	NXTMS 03	019-349	NXTMS Base of Cabinet 3

4.1.14.1.1 CMU2 Cable Reference

Figure 4-57 depicts the actual CMU2 panel label.

Figure 4-57 CMU2 Shelf Panel Label

4.1.14.2 TMSU4 Cable Description

Each TMSU4 has a total of 48 ports for CM3 optical paddleboards. Figure 4-58 shows the TMS link optical paddleboard connections to the SMs/SM-2000s.

Figure 4-58 TMSU4 Layout

Table 4-28 depicts the port assignments for TMSU4, shelf 1 TMS link optical paddleboard connections to the SMs/SM-2000s.

Table 4-28 TMSU4 Shelf 1 Port Assignments

PORT Assignment for TMSU4 Shelf 1 TMS Links								
TMSU4 Front - Side 0					TMSU4 Rear - Side 1			
SM Number	EQL	PB	TMS LNK	Port	EQL	PB	TMS LNK	Port
SM( )	33F-093-TX/RX	Even	84	001-Top	33R-093-TX/RX	Even	84	001-Top
SM( )	33F-093-TX/RX	Odd	85	001-Bot	33R-093-TX/RX	Odd	85	001-Bot
SM( )	33F-113-TX/RX	Even	86	002-Top	33R-113-TX/RX	Even	86	002-Top
SM( )	33F-113-TX/RX	Odd	87	002-Bot	33R-113-TX/RX	Odd	87	002-Bot
SM( )	33F-133-TX/RX	Even	88	003-Top	33R-133-TX/RX	Even	88	003-Top
SM( )	33F-133-TX/RX	Odd	89	003-Bot	33R-133-TX/RX	Odd	89	003-Bot
SM( )	33F-153-TX/RX	Even	90	004-Top	33R-153-TX/RX	Even	90	004-Top
SM( )	33F-153-TX/RX	Odd	91	004-Bot	33R-153-TX/RX	Odd	91	004-Bot
SM( )	33F-173-TX/RX	Even	92	005-Top	33R-173-TX/RX	Even	92	005-Top
SM( )	33F-173-TX/RX	Odd	93	005-Bot	33R-173-TX/RX	Odd	93	005-Bot
SM( )	33F-193-TX/RX	Even	94	006-Top	33R-193-TX/RX	Even	94	006-Top
SM( )	33F-193-TX/RX	Odd	95	006-Bot	33R-193-TX/RX	Odd	95	006-Bot

SM( )	36F-093-TX/RX	Even	96	007-Top	36R-093-TX/RX	Even	96	007-Top
SM( )	36F-093-TX/RX	Odd	97	007-Bot	36R-093-TX/RX	Odd	97	007-Bot
SM( )	36F-113-TX/RX	Even	98	008-Top	36R-113-TX/RX	Even	98	008-Top
SM( )	36F-113-TX/RX	Odd	99	008-Bot	36R-113-TX/RX	Odd	99	008-Bot
SM( )	36F-133-TX/RX	Even	100	009-Top	36R-133-TX/RX	Even	100	009-Top
SM( )	36F-133-TX/RX	Odd	101	009-Bot	36R-133-TX/RX	Odd	101	009-Bot
SM( )	36F-153-TX/RX	Even	102	010-Top	36R-153-TX/RX	Even	102	010-Top
SM( )	36F-153-TX/RX	Odd	103	010-Bot	36R-153-TX/RX	Odd	103	010-Bot
SM( )	36F-173-TX/RX	Even	104	011-Top	36R-173-TX/RX	Even	104	011-Top
SM( )	36F-173-TX/RX	Odd	105	011-Bot	36R-173-TX/RX	Odd	105	011-Bot
SM( )	36F-193-TX/RX	Even	106	012-Top	36R-193-TX/RX	Even	106	012-Top
SM( )	36F-193-TX/RX	Odd	107	012-Bot	36R-193-TX/RX	Odd	107	012-Bot
SM( )	39F-093-TX/RX	Even	108	013-Top	39R-093-TX/RX	Even	108	013-Top
SM( )	39F-093-TX/RX	Odd	109	013-Bot	39R-093-TX/RX	Odd	109	013-Bot
SM( )	39F-113-TX/RX	Even	110	014-Top	39R-113-TX/RX	Even	110	014-Top
SM( )	39F-113-TX/RX	Odd	111	014-Bot	39R-113-TX/RX	Odd	111	014-Bot
SM( )	39F-133-TX/RX	Even	112	015-Top	39R-133-TX/RX	Even	112	015-Top
SM( )	39F-133-TX/RX	Odd	113	015-Bot	39R-133-TX/RX	Odd	113	015-Bot
SM( )	39F-153-TX/RX	Even	114	016-Top	39R-153-TX/RX	Even	114	016-Top
SM( )	39F-153-TX/RX	Odd	115	016-Bot	39R-153-TX/RX	Odd	115	016-Bot
SM( )	39F-173-TX/RX	Even	116	017-Top	39R-173-TX/RX	Even	116	017-Top
SM( )	39F-173-TX/RX	Odd	117	017-Bot	39R-173-TX/RX	Odd	117	017-Bot
SM( )	39F-193-TX/RX	Even	118	018-Top	39R-193-TX/RX	Even	118	018-Top
SM( )	39F-193-TX/RX	Odd	119	018-Bot	39R-193-TX/RX	Odd	119	018-Bot
SM( )	33F-365-TX/RX	Even	120	019-Top	33R-365-TX/RX	Even	120	019-Top
SM( )	33F-365-TX/RX	Odd	121	019-Bot	33R-365-TX/RX	Odd	121	019-Bot
SM( )	33F-385-TX/RX	Even	122	020-Top	33R-385-TX/RX	Even	122	020-Top
SM( )	33F-385-TX/RX	Odd	123	020-Bot	33R-385-TX/RX	Odd	123	020-Bot
SM( )	33F-405-TX/RX	Even	124	021-Top	33R-405-TX/RX	Even	124	021-Top
SM( )	33F-405-TX/RX	Odd	125	021-Bot	33R-405-TX/RX	Odd	125	021-Bot
SM( )	33F-425-TX/RX	Even	126	022-Top	33R-425-TX/RX	Even	126	022-Top
SM( )	33F-425-TX/RX	Odd	127	022-Bot	33R-425-TX/RX	Odd	127	022-Bot

SM( )	33F-445-TX/RX	Even	128	023-Top	33R-445-TX/RX	Even	128	023-Top
SM( )	33F-445-TX/RX	Odd	129	023-Bot	33R-445-TX/RX	Odd	129	023-Bot
SM( )	33F-465-TX/RX	Even	130	024-Top	33R-465-TX/RX	Even	130	024-Top
SM( )	33F-465-TX/RX	Odd	131	024-Bot	33R-465-TX/RX	Odd	131	024-Bot
SM( )	33F-485-TX/RX	Even	132	025-Top	33R-485-TX/RX	Even	132	025-Top
SM( )	33F-485-TX/RX	Odd	133	025-Bot	33R-485-TX/RX	Odd	133	025-Bot
SM( )	33F-505-TX/RX	Even	134	026-Top	33R-505-TX/RX	Even	134	026-Top
SM( )	33F-505-TX/RX	Odd	135	026-Bot	33R-505-TX/RX	Odd	135	026-Bot
SM( )	33F-525-TX/RX	Even	136	027-Top	33R-525-TX/RX	Even	136	027-Top
SM( )	33F-525-TX/RX	Odd	137	027-Bot	33R-525-TX/RX	Odd	137	027-Bot
SM( )	33F-545-TX/RX	Even	138	028-Top	33R-545-TX/RX	Even	138	028-Top
SM( )	33F-545-TX/RX	Odd	139	028-Bot	33R-545-TX/RX	Odd	139	028-Bot
SM( )	36F-365-TX/RX	Even	140	029-Top	36R-365-TX/RX	Even	140	029-Top
SM( )	36F-365-TX/RX	Odd	141	029-Bot	36R-365-TX/RX	Odd	141	029-Bot
SM( )	36F-385-TX/RX	Even	142	030-Top	36R-385-TX/RX	Even	142	030-Top
SM( )	36F-385-TX/RX	Odd	143	030-Bot	36R-385-TX/RX	Odd	143	030-Bot
SM( )	36F-405-TX/RX	Even	144	031-Top	36R-405-TX/RX	Even	144	031-Top
SM( )	36F-405-TX/RX	Odd	145	031-Bot	36R-405-TX/RX	Odd	145	031-Bot
SM( )	36F-425-TX/RX	Even	146	032-Top	36R-425-TX/RX	Even	146	032-Top
SM( )	36F-425-TX/RX	Odd	147	032-Bot	36R-425-TX/RX	Odd	147	032-Bot
SM( )	36F-445-TX/RX	Even	148	033-Top	36R-445-TX/RX	Even	148	033-Top
SM( )	36F-445-TX/RX	Odd	149	033-Bot	36R-445-TX/RX	Odd	149	033-Bot
SM( )	36F-465-TX/RX	Even	150	034-Top	36R-465-TX/RX	Even	150	034-Top
SM( )	36F-465-TX/RX	Odd	151	034-Bot	36R-465-TX/RX	Odd	151	034-Bot
SM( )	36F-485-TX/RX	Even	152	035-Top	36R-485-TX/RX	Even	152	035-Top
SM( )	36F-485-TX/RX	Odd	153	035-Bot	36R-485-TX/RX	Odd	153	035-Bot
SM( )	36F-505-TX/RX	Even	154	036-Top	36R-505-TX/RX	Even	154	036-Top
SM( )	36F-505-TX/RX	Odd	155	036-Bot	36R-505-TX/RX	Odd	155	036-Bot
SM( )	36F-525-TX/RX	Even	156	037-Top	36R-525-TX/RX	Even	156	037-Top
SM( )	36F-525-TX/RX	Odd	157	037-Bot	36R-525-TX/RX	Odd	157	037-Bot
SM( )	36F-545-TX/RX	Even	158	038-Top	36R-545-TX/RX	Even	158	038-Top
SM( )	36F-545-TX/RX	Odd	159	038-Bot	36R-545-TX/RX	Odd	159	038-Bot

SM( )	39F-365-TX/RX	Even	160	039-Top	39R-365-TX/RX	Even	160	039-Top
SM( )	39F-365-TX/RX	Odd	161	039-Bot	39R-365-TX/RX	Odd	161	039-Bot
SM( )	39F-385-TX/RX	Even	162	040-Top	39R-385-TX/RX	Even	162	040-Top
SM( )	39F-385-TX/RX	Odd	163	040-Bot	39R-385-TX/RX	Odd	163	040-Bot
SM( )	39F-405-TX/RX	Even	164	041-Top	39R-405-TX/RX	Even	164	041-Top
SM( )	39F-405-TX/RX	Odd	165	041-Bot	39R-405-TX/RX	Odd	165	041-Bot
SM( )	39F-425-TX/RX	Even	166	042-Top	39R-425-TX/RX	Even	166	042-Top
SM( )	39F-425-TX/RX	Odd	167	042-Bot	39R-425-TX/RX	Odd	167	042-Bot
SM( )	39F-445-TX/RX	Even	168	043-Top	39R-445-TX/RX	Even	168	043-Top
SM( )	39F-445-TX/RX	Odd	169	043-Bot	39R-445-TX/RX	Odd	169	043-Bot
SM( )	39F-465-TX/RX	Even	170	044-Top	39R-465-TX/RX	Even	170	044-Top
SM( )	39F-465-TX/RX	Odd	171	044-Bot	39R-465-TX/RX	Odd	171	044-Bot
SM( )	39F-485-TX/RX	Even	172	045-Top	39R-485-TX/RX	Even	172	045-Top
SM( )	39F-485-TX/RX	Odd	173	045-Bot	39R-485-TX/RX	Odd	173	045-Bot
SM( )	39F-505-TX/RX	Even	174	046-Top	39R-505-TX/RX	Even	174	046-Top
SM( )	39F-505-TX/RX	Odd	175	046-Bot	39R-505-TX/RX	Odd	175	046-Bot
SM( )	39F-525-TX/RX	Even	176	047-Top	39R-525-TX/RX	Even	176	047-Top
SM( )	39F-525-TX/RX	Odd	177	047-Bot	39R-525-TX/RX	Odd	177	047-Bot
SM( )	39F-545-TX/RX	Even	178	048-Top	39R-545-TX/RX	Even	178	048-Top
SM( )	39F-545-TX/RX	Odd	179	048-Bot	39R-545-TX/RX	Odd	179	048-Bot

Table 4-29 depicts the port assignments for TMSU4, shelf 2 TMS link optical paddleboard connections to the SMs/SM-2000s.

Table 4-29 TMSU4 Shelf 2 Port Assignments

Port Assignment for TMSU4 Shelf 2 TMS Links								
TMSU4 Front - Side 0					TMSU4 Rear - Side 1			
SM Number	**EQL**	**PB**	**TMS LNK**	**Port**	**EQL**	**PB**	**TMS LNK**	**Port**
SM( )	43F-093-TX/RX	Even	180	001-Top	43R-093-TX/RX	Even	180	001-Top
SM( )	43F-093-TX/RX	Odd	181	001-Bot	43R-093-TX/RX	Odd	181	001-Bot
SM( )	43F-113-TX/RX	Even	182	002-Top	43R-113-TX/RX	Even	182	002-Top
SM( )	43F-113-TX/RX	Odd	183	002-Bot	43R-113-TX/RX	Odd	183	002-Bot
SM( )	43F-133-TX/RX	Even	184	003-Top	43R-133-TX/RX	Even	184	003-Top
SM( )	43F-133-TX/RX	Odd	185	003-Bot	43R-133-TX/RX	Odd	185	003-Bot
SM( )	43F-153-TX/RX	Even	186	004-Top	43R-153-TX/RX	Even	186	004-Top

SM( )	43F-153-TX/RX	Odd	187	004-Bot	43R-153-TX/RX	Odd	187	004-Bot
SM( )	43F-173-TX/RX	Even	188	005-Top	43R-173-TX/RX	Even	188	005-Top
SM( )	43F-173-TX/RX	Odd	189	005-Bot	43R-173-TX/RX	Odd	189	005-Bot
SM( )	43F-193-TX/RX	Even	190	006-Top	43R-193-TX/RX	Even	190	006-Top
SM( )	43F-193-TX/RX	Odd	191	006-Bot	43R-193-TX/RX	Odd	191	006-Bot
SM( )	46F-093-TX/RX	Even	192	007-Top	46R-093-TX/RX	Even	192	007-Top
SM( )	46F-093-TX/RX	Odd	193	007-Bot	46R-093-TX/RX	Odd	193	007-Bot
SM( )	46F-113-TX/RX	Even	194	008-Top	46R-113-TX/RX	Even	194	008-Top
SM( )	46F-113-TX/RX	Odd	195	008-Bot	46R-113-TX/RX	Odd	195	008-Bot
SM( )	46F-133-TX/RX	Even	196	009-Top	46R-133-TX/RX	Even	196	009-Top
SM( )	46F-133-TX/RX	Odd	197	009-Bot	46R-133-TX/RX	Odd	197	009-Bot
SM( )	46F-153-TX/RX	Even	198	010-Top	46R-153-TX/RX	Even	198	010-Top
SM( )	46F-153-TX/RX	Odd	199	010-Bot	46R-153-TX/RX	Odd	199	010-Bot
SM( )	46F-173-TX/RX	Even	200	011-Top	46R-173-TX/RX	Even	200	011-Top
SM( )	46F-173-TX/RX	Odd	201	011-Bot	46R-173-TX/RX	Odd	201	011-Bot
SM( )	46F-193-TX/RX	Even	202	012-Top	46R-193-TX/RX	Even	202	012-Top
SM( )	46F-193-TX/RX	Odd	203	012-Bot	46R-193-TX/RX	Odd	203	012-Bot
SM( )	49F-093-TX/RX	Even	204	013-Top	49R-093-TX/RX	Even	204	013-Top
SM( )	49F-093-TX/RX	Odd	205	013-Bot	49R-093-TX/RX	Odd	205	013-Bot
SM( )	49F-113-TX/RX	Even	206	014-Top	49R-113-TX/RX	Even	206	014-Top
SM( )	49F-113-TX/RX	Odd	207	014-Bot	49R-113-TX/RX	Odd	207	014-Bot
SM( )	49F-133-TX/RX	Even	208	015-Top	49R-133-TX/RX	Even	208	015-Top
SM( )	49F-133-TX/RX	Odd	209	015-Bot	49R-133-TX/RX	Odd	209	015-Bot
SM( )	49F-153-TX/RX	Even	210	016-Top	49R-153-TX/RX	Even	210	016-Top
SM( )	49F-153-TX/RX	Odd	211	016-Bot	49R-153-TX/RX	Odd	211	016-Bot
SM( )	49F-173-TX/RX	Even	212	017-Top	49R-173-TX/RX	Even	212	017-Top
SM( )	49F-173-TX/RX	Odd	213	017-Bot	49R-173-TX/RX	Odd	213	017-Bot
SM( )	49F-193-TX/RX	Even	214	018-Top	49R-193-TX/RX	Even	214	018-Top
SM( )	49F-193-TX/RX	Odd	215	018-Bot	49R-193-TX/RX	Odd	215	018-Bot
SM( )	43F-365-TX/RX	Even	216	019-Top	43R-365-TX/RX	Even	216	019-Top
SM( )	43F-365-TX/RX	Odd	217	019-Bot	43R-365-TX/RX	Odd	217	019-Bot
SM( )	43F-385-TX/RX	Even	218	020-Top	43R-385-TX/RX	Even	218	020-Top

SM( )	43F-385-TX/RX	Odd	219	020-Bot	43R-385-TX/RX	Odd	219	020-Bot
SM( )	43F-405-TX/RX	Even	220	021-Top	43R-405-TX/RX	Even	220	021-Top
SM( )	43F-405-TX/RX	Odd	221	021-Bot	43R-405-TX/RX	Odd	221	021-Bot
SM( )	43F-425-TX/RX	Even	222	022-Top	43R-425-TX/RX	Even	222	022-Top
SM( )	43F-425-TX/RX	Odd	223	022-Bot	43R-425-TX/RX	Odd	223	022-Bot
SM( )	43F-445-TX/RX	Even	224	023-Top	43R-445-TX/RX	Even	224	023-Top
SM( )	43F-445-TX/RX	Odd	225	023-Bot	43R-445-TX/RX	Odd	225	023-Bot
SM( )	43F-465-TX/RX	Even	226	024-Top	43R-465-TX/RX	Even	226	024-Top
SM( )	43F-465-TX/RX	Odd	227	024-Bot	43R-465-TX/RX	Odd	227	024-Bot
SM( )	43F-485-TX/RX	Even	228	025-Top	43R-485-TX/RX	Even	228	025-Top
SM( )	43F-485-TX/RX	Odd	229	025-Bot	43R-485-TX/RX	Odd	229	025-Bot
SM( )	43F-505-TX/RX	Even	230	026-Top	43R-505-TX/RX	Even	230	026-Top
SM( )	43F-505-TX/RX	Odd	231	026-Bot	43R-505-TX/RX	Odd	231	026-Bot
SM( )	43F-525-TX/RX	Even	232	027-Top	43R-525-TX/RX	Even	232	027-Top
SM( )	43F-525-TX/RX	Odd	233	027-Bot	43R-525-TX/RX	Odd	233	027-Bot
SM( )	43F-545-TX/RX	Even	234	028-Top	43R-525-TX/RX	Even	234	028-Top
SM( )	43F-545-TX/RX	Odd	235	028-Bot	43R-525-TX/RX	Odd	235	028-Bot
SM( )	46F-365-TX/RX	Even	236	029-Top	46R-365-TX/RX	Even	236	029-Top
SM( )	46F-365-TX/RX	Odd	237	029-Bot	46R-365-TX/RX	Odd	237	029-Bot
SM( )	46F-385-TX/RX	Even	238	030-Top	46R-385-TX/RX	Even	238	030-Top
SM( )	46F-385-TX/RX	Odd	239	030-Bot	46R-385-TX/RX	Odd	239	030-Bot
SM( )	46F-405-TX/RX	Even	240	031-Top	46R-405-TX/RX	Even	240	031-Top
SM( )	46F-405-TX/RX	Odd	241	031-Bot	46R-405-TX/RX	Odd	241	031-Bot
SM( )	46F-425-TX/RX	Even	242	032-Top	46R-425-TX/RX	Even	242	032-Top
SM( )	46F-425-TX/RX	Odd	243	032-Bot	46R-425-TX/RX	Odd	243	032-Bot
SM( )	46F-445-TX/RX	Even	244	033-Top	46R-445-TX/RX	Even	244	033-Top
SM( )	46F-445-TX/RX	Odd	245	033-Bot	46R-445-TX/RX	Odd	245	033-Bot
SM( )	46F-465-TX/RX	Even	246	034-Top	46R-465-TX/RX	Even	246	034-Top
SM( )	46F-465-TX/RX	Odd	247	034-Bot	46R-465-TX/RX	Odd	247	034-Bot
SM( )	46F-485-TX/RX	Even	248	035-Top	46R-485-TX/RX	Even	248	035-Top
SM( )	46F-485-TX/RX	Odd	249	035-Bot	46R-485-TX/RX	Odd	249	035-Bot
SM( )	46F-505-TX/RX	Even	250	036-Top	46R-505-TX/RX	Even	250	036-Top

SM( )	46F-505-TX/RX	Odd	251	036-Bot	46R-505-TX/RX	Odd	251	036-Bot
SM( )	46F-525-TX/RX	Even	252	037-Top	46R-525-TX/RX	Even	252	037-Top
SM( )	46F-525-TX/RX	Odd	253	037-Bot	46R-525-TX/RX	Odd	253	037-Bot
SM( )	46F-545-TX/RX	Even	254	038-Top	46R-545-TX/RX	Even	254	038-Top
SM( )	46F-545-TX/RX	Odd	255	038-Bot	46R-545-TX/RX	Odd	255	038-Bot
SM( )	49F-365-TX/RX	Even	256	039-Top	49R-365-TX/RX	Even	256	039-Top
SM( )	49F-365-TX/RX	Odd	257	039-Bot	49R-365-TX/RX	Odd	257	039-Bot
SM( )	49F-385-TX/RX	Even	258	040-Top	49R-385-TX/RX	Even	258	040-Top
SM( )	49F-385-TX/RX	Odd	259	040-Bot	49R-385-TX/RX	Odd	259	040-Bot
SM( )	49F-405-TX/RX	Even	260	041-Top	49R-405-TX/RX	Even	260	041-Top
SM( )	49F-405-TX/RX	Odd	261	041-Bot	49R-405-TX/RX	Odd	261	041-Bot
SM( )	49F-425-TX/RX	Even	262	042-Top	49R-425-TX/RX	Even	262	042-Top
SM( )	49F-425-TX/RX	Odd	263	042-Bot	49R-425-TX/RX	Odd	263	042-Bot
SM( )	49F-445-TX/RX	Even	264	043-Top	49R-445-TX/RX	Even	264	043-Top
SM( )	49F-445-TX/RX	Odd	265	043-Bot	49R-445-TX/RX	Odd	265	043-Bot
SM( )	49F-465-TX/RX	Even	266	044-Top	49R-465-TX/RX	Even	266	044-Top
SM( )	49F-465-TX/RX	Odd	267	044-Bot	49R-465-TX/RX	Odd	267	044-Bot
SM( )	49F-485-TX/RX	Even	268	045-Top	49R-485-TX/RX	Even	268	045-Top
SM( )	49F-485-TX/RX	Odd	269	045-Bot	49R-485-TX/RX	Odd	269	045-Bot
SM( )	49F-505-TX/RX	Even	270	046-Top	49R-505-TX/RX	Even	270	046-Top
SM( )	49F-505-TX/RX	Odd	271	046-Bot	49R-505-TX/RX	Odd	271	046-Bot
SM( )	49F-525-TX/RX	Even	272	047-Top	49R-525-TX/RX	Even	272	047-Top
SM( )	49F-525-TX/RX	Odd	273	047-Bot	49R-525-TX/RX	Odd	273	047-Bot
SM( )	49F-545-TX/RX	Even	274	048-Top	49R-545-TX/RX	Even	274	048-Top
SM( )	49F-545-TX/RX	Odd	275	048-Bot	49R-545-TX/RX	Odd	275	048-Bot

Table 4-30 depicts the port assignments for TMSU4, shelf 3 TMS links optical paddleboard connections to the SMs/SM-2000s.

Table 4-30 TMSU4 Shelf 3 Port Assignments

Port Assignment for TMSU4 Shelf 3 TMS Links								
TMSU4 Front - Side 0					TMSU4 Rear - Side 1			
SM Number	**EQL**	**PB**	**TMS LNK**	**Port**	**EQL**	**PB**	**TMS LNK**	**Port**
SM( )	53F-093-TX/RX	Even	276	001-Top	53R-093-TX/RX	Even	276	001-Top
SM( )	53F-093-TX/RX	Odd	277	001-Bot	53R-093-TX/RX	Odd	277	001-Bot

SM( )	53F-113-TX/RX	Even	278	002-Top	53R-113-TX/RX	Even	278	002-Top
SM( )	53F-113-TX/RX	Odd	279	002-Bot	53R-113-TX/RX	Odd	279	002-Bot
SM( )	53F-133-TX/RX	Even	280	003-Top	53R-133-TX/RX	Even	280	003-Top
SM( )	53F-133-TX/RX	Odd	281	003-Bot	53R-133-TX/RX	Odd	281	003-Bot
SM( )	53F-153-TX/RX	Even	282	004-Top	53R-153-TX/RX	Even	282	004-Top
SM( )	53F-153-TX/RX	Odd	283	004-Bot	53R-153-TX/RX	Odd	283	004-Bot
SM( )	53F-173-TX/RX	Even	284	005-Top	53R-173-TX/RX	Even	284	005-Top
SM( )	53F-173-TX/RX	Odd	285	005-Bot	53R-173-TX/RX	Odd	285	005-Bot
SM( )	53F-193-TX/RX	Even	286	006-Top	53R-193-TX/RX	Even	286	006-Top
SM( )	53F-193-TX/RX	Odd	287	006-Bot	53R-193-TX/RX	Odd	287	006-Bot
SM( )	56F-093-TX/RX	Even	288	007-Top	56R-093-TX/RX	Even	288	007-Top
SM( )	56F-093-TX/RX	Odd	289	007-Bot	56R-093-TX/RX	Odd	289	007-Bot
SM( )	56F-113-TX/RX	Even	290	008-Top	56R-113-TX/RX	Even	290	008-Top
SM( )	56F-113-TX/RX	Odd	291	008-Bot	56R-113-TX/RX	Odd	291	008-Bot
SM( )	56F-133-TX/RX	Even	292	009-Top	56R-133-TX/RX	Even	292	009-Top
SM( )	56F-133-TX/RX	Odd	293	009-Bot	56R-133-TX/RX	Odd	293	009-Bot
SM( )	56F-153-TX/RX	Even	294	010-Top	56R-153-TX/RX	Even	294	010-Top
SM( )	56F-153-TX/RX	Odd	295	010-Bot	56R-153-TX/RX	Odd	295	010-Bot
SM( )	56F-173-TX/RX	Even	296	011-Top	56R-173-TX/RX	Even	296	011-Top
SM( )	56F-173-TX/RX	Odd	297	011-Bot	56R-173-TX/RX	Odd	297	011-Bot
SM( )	56F-193-TX/RX	Even	298	012-Top	56R-193-TX/RX	Even	298	012-Top
SM( )	56F-193-TX/RX	Odd	299	012-Bot	56R-193-TX/RX	Odd	299	012-Bot
SM( )	59F-093-TX/RX	Even	300	013-Top	59R-093-TX/RX	Even	300	013-Top
SM( )	59F-093-TX/RX	Odd	301	013-Bot	59R-093-TX/RX	Odd	301	013-Bot
SM( )	59F-113-TX/RX	Even	302	014-Top	59R-113-TX/RX	Even	302	014-Top
SM( )	59F-113-TX/RX	Odd	303	014-Bot	59R-113-TX/RX	Odd	303	014-Bot
SM( )	59F-133-TX/RX	Even	304	015-Top	59R-133-TX/RX	Even	304	015-Top
SM( )	59F-133-TX/RX	Odd	305	015-Bot	59R-133-TX/RX	Odd	305	015-Bot
SM( )	59F-153-TX/RX	Even	306	016-Top	59R-153-TX/RX	Even	306	016-Top
SM( )	59F-153-TX/RX	Odd	307	016-Bot	59R-153-TX/RX	Odd	307	016-Bot
SM( )	59F-173-TX/RX	Even	308	017-Top	59R-173-TX/RX	Even	308	017-Top
SM( )	59F-173-TX/RX	Odd	309	017-Bot	59R-173-TX/RX	Odd	309	017-Bot

SM( )	59F-193-TX/RX	Even	310	018-Top	59R-193-TX/RX	Even	310	018-Top
SM( )	59F-193-TX/RX	Odd	311	018-Bot	59R-193-TX/RX	Odd	311	018-Bot
SM( )	53F-365-TX/RX	Even	312	019-Top	53R-365-TX/RX	Even	312	019-Top
SM( )	53F-365-TX/RX	Odd	313	019-Bot	53R-365-TX/RX	Odd	313	019-Bot
SM( )	53F-385-TX/RX	Even	314	020-Top	53R-385-TX/RX	Even	314	020-Top
SM( )	53F-385-TX/RX	Odd	315	020-Bot	53R-385-TX/RX	Odd	315	020-Bot
SM( )	53F-405-TX/RX	Even	316	021-Top	53R-405-TX/RX	Even	316	021-Top
SM( )	53F-405-TX/RX	Odd	317	021-Bot	53R-405-TX/RX	Odd	317	021-Bot
SM( )	53F-425-TX/RX	Even	318	022-Top	53R-425-TX/RX	Even	318	022-Top
SM( )	53F-425-TX/RX	Odd	319	022-Bot	53R-425-TX/RX	Odd	319	022-Bot
SM( )	53F-445-TX/RX	Even	320	023-Top	53R-445-TX/RX	Even	320	023-Top
SM( )	53F-445-TX/RX	Odd	321	023-Bot	53R-445-TX/RX	Odd	321	023-Bot
SM( )	53F-465-TX/RX	Even	322	024-Top	53R-465-TX/RX	Even	322	024-Top
SM( )	53F-465-TX/RX	Odd	323	024-Bot	53R-465-TX/RX	Odd	323	024-Bot
SM( )	53F-485-TX/RX	Even	324	025-Top	53R-485-TX/RX	Even	324	025-Top
SM( )	53F-485-TX/RX	Odd	325	025-Bot	53R-485-TX/RX	Odd	325	025-Bot
SM( )	53F-505-TX/RX	Even	326	026-Top	53R-505-TX/RX	Even	326	026-Top
SM( )	53F-505-TX/RX	Odd	327	026-Bot	53R-505-TX/RX	Odd	327	026-Bot
SM( )	53F-525-TX/RX	Even	328	027-Top	53R-525-TX/RX	Even	328	027-Top
SM( )	53F-525-TX/RX	Odd	329	027-Bot	53R-525-TX/RX	Odd	329	027-Bot
SM( )	53F-545-TX/RX	Even	330	028-Top	53R-545-TX/RX	Even	330	028-Top
SM( )	53F-545-TX/RX	Odd	331	028-Bot	53R-545-TX/RX	Odd	331	028-Bot
SM( )	56F-365-TX/RX	Even	332	029-Top	56R-365-TX/RX	Even	332	029-Top
SM( )	56F-365-TX/RX	Odd	333	029-Bot	56R-365-TX/RX	Odd	333	029-Bot
SM( )	56F-385-TX/RX	Even	334	030-Top	56R-385-TX/RX	Even	334	030-Top
SM( )	56F-385-TX/RX	Odd	335	030-Bot	56R-385-TX/RX	Odd	335	030-Bot
SM( )	56F-405-TX/RX	Even	336	031-Top	56R-405-TX/RX	Even	336	031-Top
SM( )	56F-405-TX/RX	Odd	337	031-Bot	56R-405-TX/RX	Odd	337	031-Bot
SM( )	56F-425-TX/RX	Even	338	032-Top	56R-425-TX/RX	Even	338	032-Top
SM( )	56F-425-TX/RX	Odd	339	032-Bot	56R-425-TX/RX	Odd	339	032-Bot
SM( )	56F-445-TX/RX	Even	340	033-Top	56R-445-TX/RX	Even	340	033-Top
SM( )	56F-445-TX/RX	Odd	341	033-Bot	56R-445-TX/RX	Odd	341	033-Bot

SM( )	56F-465-TX/RX	Even	342	034-Top	56R-465-TX/RX	Even	342	034-Top
SM( )	56F-465-TX/RX	Odd	343	034-Bot	56R-465-TX/RX	Odd	343	034-Bot
SM( )	56F-485-TX/RX	Even	344	035-Top	56R-485-TX/RX	Even	344	035-Top
SM( )	56F-485-TX/RX	Odd	345	035-Bot	56R-485-TX/RX	Odd	345	035-Bot
SM( )	56F-505-TX/RX	Even	346	036-Top	56R-505-TX/RX	Even	346	036-Top
SM( )	56F-505-TX/RX	Odd	347	036-Bot	56R-505-TX/RX	Odd	347	036-Bot
SM( )	56F-525-TX/RX	Even	348	037-Top	56R-525-TX/RX	Even	348	037-Top
SM( )	56F-525-TX/RX	Odd	349	037-Bot	56R-525-TX/RX	Odd	349	037-Bot
SM( )	56F-545-TX/RX	Even	350	038-Top	56R-545-TX/RX	Even	350	038-Top
SM( )	56F-545-TX/RX	Odd	351	038-Bot	56R-545-TX/RX	Odd	351	038-Bot
SM( )	59F-365-TX/RX	Even	352	039-Top	59R-365-TX/RX	Even	352	039-Top
SM( )	59F-365-TX/RX	Odd	353	039-Bot	59R-365-TX/RX	Odd	353	039-Bot
SM( )	59F-385-TX/RX	Even	354	040-Top	59R-385-TX/RX	Even	354	040-Top
SM( )	59F-385-TX/RX	Odd	355	040-Bot	59R-385-TX/RX	Odd	355	040-Bot
SM( )	59F-405-TX/RX	Even	356	041-Top	59R-405-TX/RX	Even	356	041-Top
SM( )	59F-405-TX/RX	Odd	357	041-Bot	59R-405-TX/RX	Odd	357	041-Bot
SM( )	59F-425-TX/RX	Even	358	042-Top	59R-425-TX/RX	Even	358	042-Top
SM( )	59F-425-TX/RX	Odd	359	042-Bot	59R-425-TX/RX	Odd	359	042-Bot
SM( )	59F-445-TX/RX	Even	360	043-Top	59R-445-TX/RX	Even	360	043-Top
SM( )	59F-445-TX/RX	Odd	361	043-Bot	59R-445-TX/RX	Odd	361	043-Bot
SM( )	59F-465-TX/RX	Even	362	044-Top	59R-465-TX/RX	Even	362	044-Top
SM( )	59F-465-TX/RX	Odd	363	044-Bot	59R-465-TX/RX	Odd	363	044-Bot
SM( )	59F-485-TX/RX	Even	364	045-Top	59R-485-TX/RX	Even	364	045-Top
SM( )	59F-485-TX/RX	Odd	365	045-Bot	59R-485-TX/RX	Odd	365	045-Bot
SM( )	59F-505-TX/RX	Even	366	046-Top	59R-505-TX/RX	Even	366	046-Top
SM( )	59F-505-TX/RX	Odd	367	046-Bot	59R-505-TX/RX	Odd	367	046-Bot
SM( )	59F-525-TX/RX	Even	368	047-Top	59R-525-TX/RX	Even	368	047-Top
SM( )	59F-525-TX/RX	Odd	369	047-Bot	59R-525-TX/RX	Odd	369	047-Bot
SM( )	59F-545-TX/RX	Even	370	048-Top	59R-545-TX/RX	Even	370	048-Top
SM( )	59F-545-TX/RX	Odd	371	048-Bot	59R-545-TX/RX	Odd	371	048-Bot

Figure 4-59 depicts the pin field cabling of the TMSU4.

Figure 4-59 TMSU4 Pin Field Diagram

Table 4-31 depicts the TMSU4 Expansion and Control and Synchronization Interface (CSI) intra-cabling terminations to the CMU2 as shown in figure 4-60 .

Figure 4-60 TMSU4 Pin Field Cabling Shelves

Table 4-31 TMSU4 Expansion and Control and Synchronization Interface (CSI) to CMU2 Pin Field Cables

TMSU 4 Shelf	TMSU4 EQL Cables	CMU2 EQL Cables
(expansion)		
1	35F-324-013	24F-309-145

	35R-324-019	24R-309-139
2	45F-324-013	24F-329-145
	45R-324-019	24R-329-139
3	55F-324-013	24F-349-145
	55R-324-019	24R-349-139
(CSI)		
1	35F-324-001	24F-309-157
	35R-324-007	24R-309-151
2	45F-324-001	24F-329-157
	45R-324-007	24R-329-151
3	55F-324-001	24F-349-157
	55R-324-007	24R-349-151

4.1.14.2.1 TMSU4 Cable Reference

The following figures depicts the actual panel door label of shelves 1, 2, and 3 of TMSU4.

Each TMSU 4 shelf has two panel doors. Figures 4-61 and 4-62 depicts the panel door labels of TMSU4 Shelf 1.

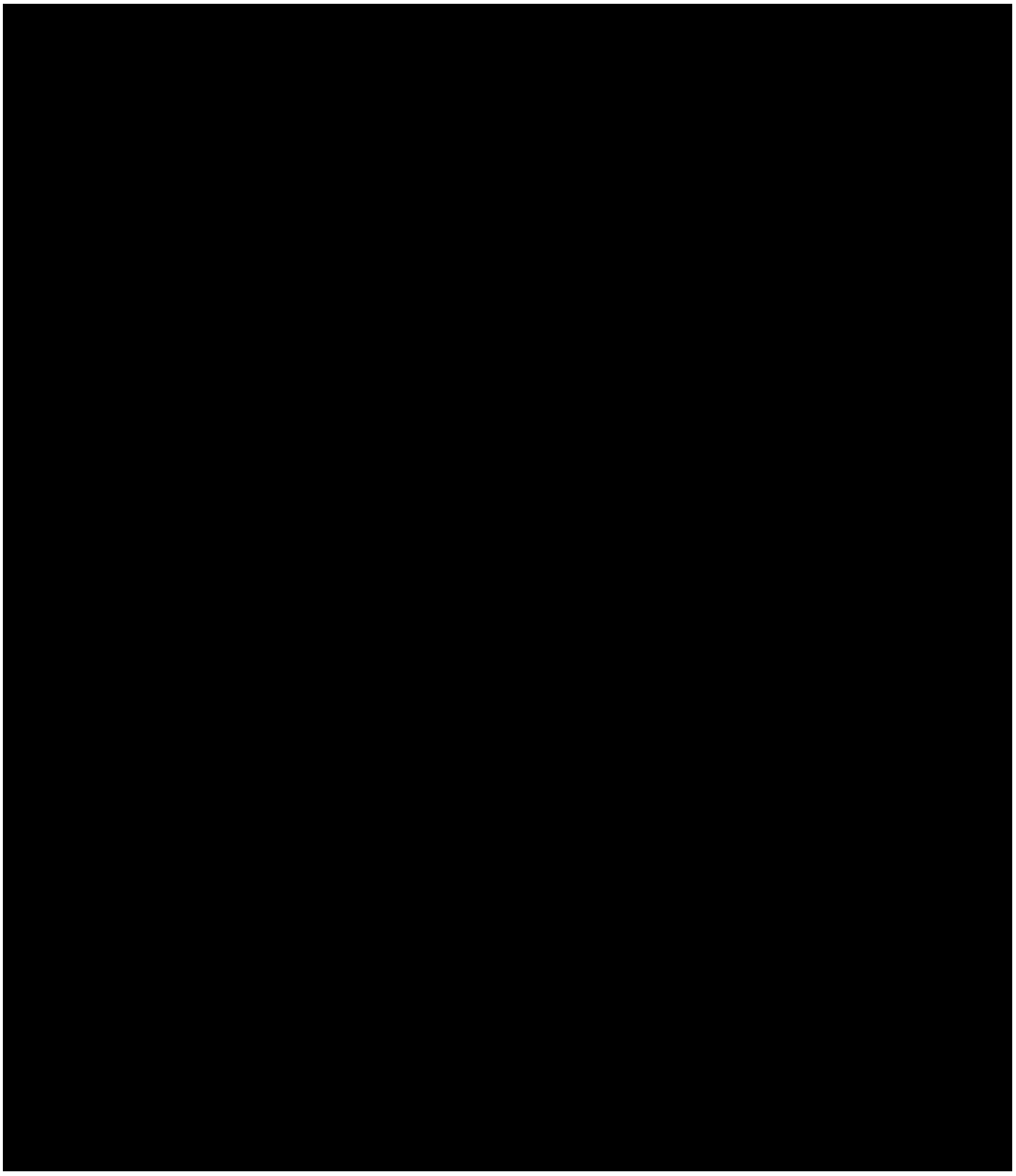

Figure 4-61 TMSU4 Panel Label 1 of Shelf 1

Figure 4-62 TMSU4 Panel Label 2 of Shelf 1

Figures 4-63 and 4-64 depicts the panel door labels of TMSU4 Shelf 2.

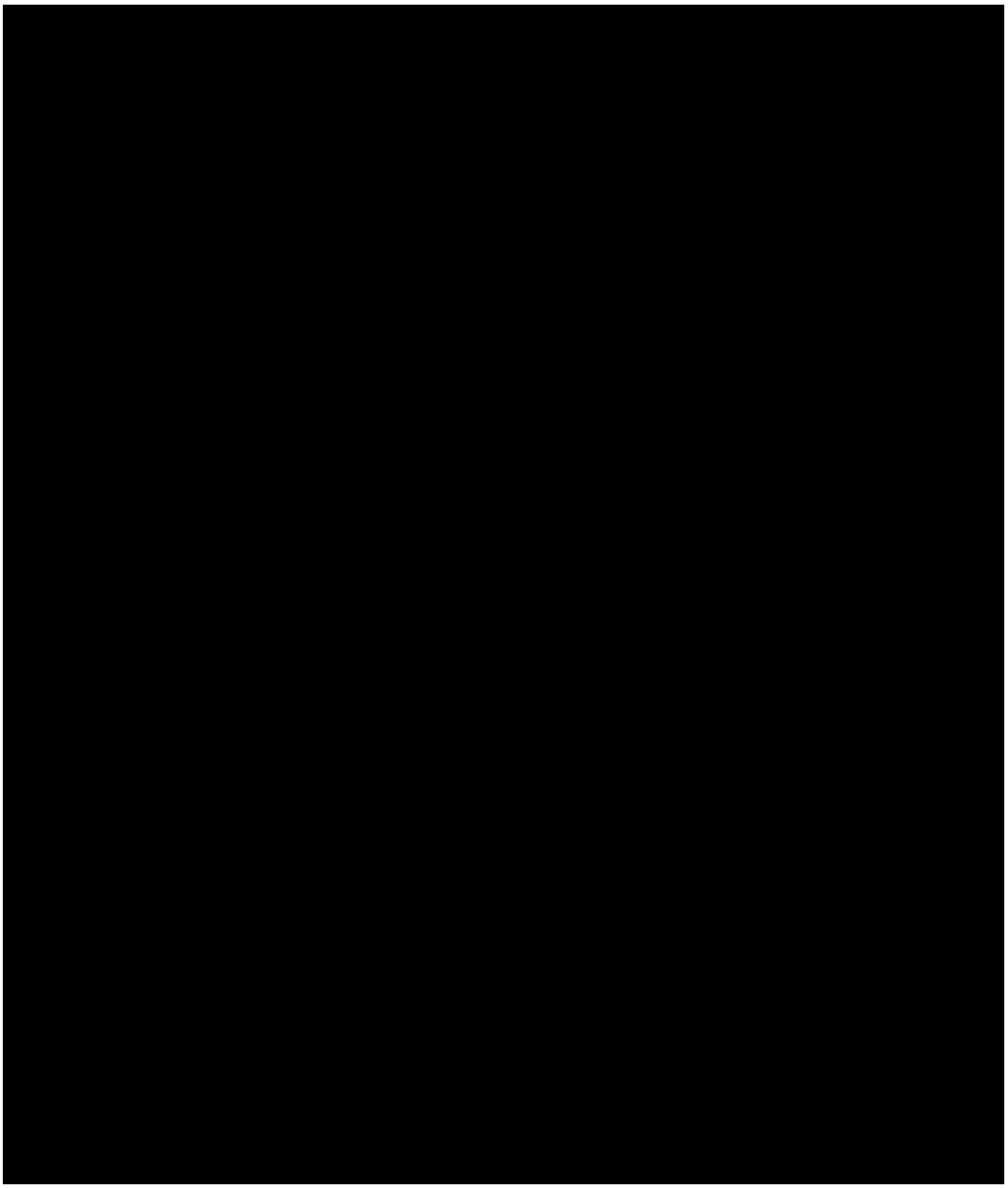

Figure 4-63 TMSU4 Panel Label 1 of Shelf 2

Figure 4-64 TMSU4 Panel Label 2 of Shelf 2

Figures 4-65 and 4-66 depicts the panel door labels of TMSU4 Shelf 3.

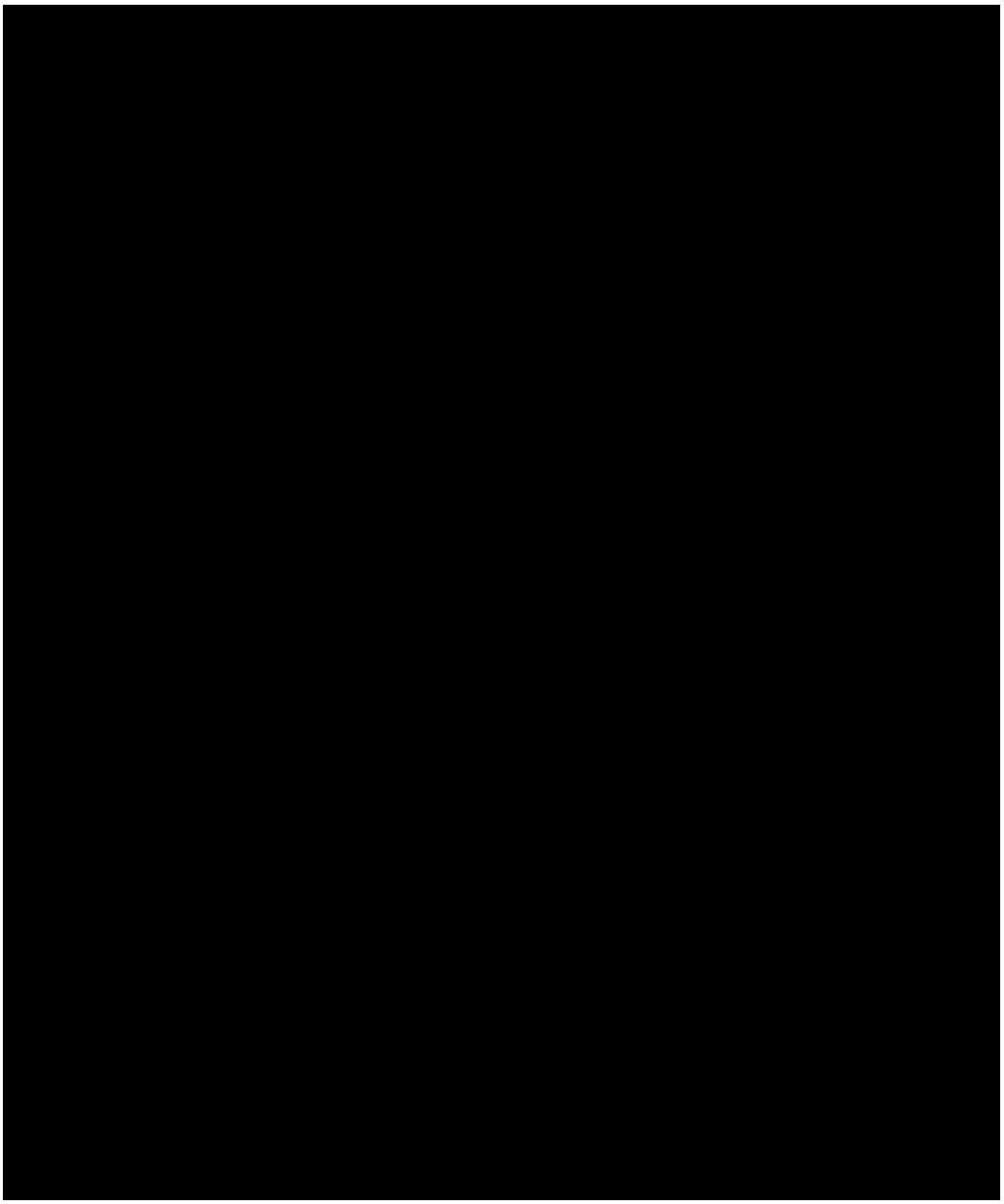

Figure 4-65 TMSU4 Panel Label 1 of Shelf 3

Figure 4-66 TMSU4 Panel Label 2 of Shelf 3

4.1.15 Capacity, CM3

The full base CM3 or NxTMS, N = 1 consists of an odd and an even TMS fabric each supporting 184 NCT links which is 94,208 (2*184*256) network timeslots. In a large gateway switch application with square TSI engineering (Square/Non-Square), the number of network timeslots equals the available trunk terminations on the switch, and therefore the full base CM3 or NxTMS, N = 1 can support 94,208 trunk terminations.

The table 4-32 shows the number of NCT Equivalent ports and the number of available trunk terminations (network timeslots) of the switch when various size CM3 configurations are used. The CM3 meets a 256K trunk objective by utilizing the NxTMS architecture with N>=3.

Table 4-32 Base and Growth CM3 Cabinet Capacity

NxTMS Configuration	Equivalent NCT Ports (Even + Odd)	Trunk Terminations
Base CM3 (1xTMS)	184 Even + 184 Odd	94,208
2xTMS	368 Even + 368 Odd	188,416
3xTMS	552 Even + 552 Odd	282,624
4xTMS	736 Even + 736 Odd	376,832

4.1.16 Procedure Reference, CM3

Table 4-33 provides reference for the CM3 procedures.

Table 4-33 CM3 Procedural References

Document	Procedure Title
235-105-210	PERFORM CM/TMS FAN ALARM TESTS
	REPLACE FAN UNIT AIR FILTER
	ROUTINE EXERCISE DESCRIPTION as follows: □ PURPOSE OF REX

	□ REX SCHEDULING □ REX SCHEDULING ALGORITHMS □ REX SCHEDULING RECOMMENDATIONS □ DIAGNOSTIC FAILURES
235-105-220	CLEAR DIAGNOSTIC FAILURE IN HARDWARE UNITS/CIRCUITS
	DIAGNOSTIC PHASE DESCRIPTIONS as follows: □ Diagnostic Phase Descriptions for DLI □ Diagnostic Phase Descriptions for MSGS □ Diagnostic Phase Descriptions for NC □ Diagnostic Phase Descriptions for NLI □ Diagnostic Phase Descriptions for ONTCCOM - Prior to 5E16.2 □ Diagnostic Phase Descriptions for ONTCCOM - 5E16.2 and Later □ Diagnostic Phase Descriptions for QLPS (CM3) □ Diagnostic Phase Descriptions for TMS (CM2)
	RESPOND TO FUSE/POWER ALARM FAILURE
	FAN MAINTENANCE
	ANALYZE CM PROBLEMS
	CLEAR MESSAGE SWITCH PROBLEMS
	CLEAR ONTC PROBLEMS
	CLEAR NETWORK CLOCK PROBLEMS
	CLEAR DLI/TMSLNK PROBLEMS
	CLEAR NLI/TMSLNK PROBLEMS
	CLEAR QGP PROBLEMS
	CLEAR QLPS PROBLEMS
	CLEAR QGL AND QGP QPIPE PROBLEMS
	CLEAR QTMSLNK PROBLEMS
	CLEAR MH QPIPE PROBLEMS
	CLEAR TRCU3 PROBLEMS as follows: □ NCTIU REPAIR PROCEDURE (RED FAULT LED LIGHTED) □ NLI/DLI FAULT PROCEDURE
	CLEAR TROUBLE IN TMSFP
	REPLACE OPTICAL DATA TRANSCEIVER as follows: □ REPLACE CM2/CM2C/CM3 ODT □ CLEAN OPTICAL FIBER
	POWER UP/DOWN EQUIPMENT as follows: □ RESPOND TO FUSE/POWER ALARM FAILURE □ POWER-DOWN AND POWER-UP ONTCCOM (CM2/CM3) AND MSGS (CM3) UNITS
235-105-231	SECONDARY NETWORK LINK INTERFACE GROWTH WITH SM-2000/GMS-CM3 - 5E15 SOFTWARE RELEASE ONLY
	TIME MULTIPLEXED SWITCH SHELF GROWTH WITH GMS-CM3 - 5E15 SOFTWARE RELEASE ONLY
	SECONDARY NETWORK LINK INTERFACE GROWTH WITH TRCU3/GMS-CM3 - 5E15 SOFTWARE RELEASE ONLY
	LOCAL SM-2000 GROWTH WITH GMS-CM3 - 5E15 SOFTWARE RELEASE ONLY
	RSM VIA DNU-S GROWTH WITH GMS-CM3 - 5E15 AND LATER SOFTWARE RELEASES
	EXM-2000 GROWTH WITH TRCU/GMS-CM3 - 5E15 SOFTWARE RELEASE ONLY
	NETWORK CLOCK REFERENCE GROWTH WITH GMS-CM3 - 5E15 AND LATER SOFTWARE RELEASES
	LOCAL SM GROWTH WITH GMS-CM3 - 5E15 SOFTWARE RELEASE ONLY
	EXM-2000 GROWTH WITH TRCU2/GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
	SECONDARY NETWORK LINK INTERFACE GROWTH WITH SM-2000/GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
	ORM GROWTH WITH TRCU3/GMS-CM3 - 5E15 SOFTWARE RELEASE ONLY
	RSM VIA DLTU2 GROWTH WITH GMS-CM3 - 5E15 SOFTWARE RELEASE ONLY
	TIME MULTIPLEXED SWITCH FABRIC PAIR SHELF GROWTH WITH GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
	SECONDARY NETWORK LINK INTERFACE GROWTH WITH TRCU3/GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
	EXM-2000 GROWTH WITH TRCU3/GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES

	LOCAL SM-2000 GROWTH WITH GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
	ORM GROWTH WITH TRCU3/GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
235-105-331	LOCAL SM-2000 DEGROWTH WITH GMS-CM3 - 5E15 AND LATER SOFTWARE RELEASES
	SECONDARY NETWORK LINK INTERFACE DEGROWTH WITH SM-2000/GMS-CM3 - 5E15 SOFTWARE RELEASE ONLY
	SECONDARY NETWORK LINK INTERFACE DEGROWTH WITH SM-2000/GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
	RSM VIA DNU-S DEGROWTH WITH GMS-CM3 - 5E15 AND LATER SOFTWARE RELEASES
	EXM-2000 DEGROWTH WITH TRCU/GMS-CM3 - 5E15 AND LATER SOFTWARE RELEASES
	SECONDARY NETWORK LINK INTERFACE DEGROWTH WITH TRCU3/GMS-CM3 - 5E15 SOFTWARE RELEASE ONLY
	SECONDARY NETWORK LINK INTERFACE DEGROWTH WITH TRCU3/GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
	TIME MULTIPLEXED SWITCH SHELF DEGROWTH WITH GMS-CM3 - 5E15 AND LATER SOFTWARE RELEASES
	TIME MULTIPLEXED SWITCH SHELF DEGROWTH WITH GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
	NETWORK CLOCK REFERENCE DEGROWTH WITH GMS-CM3 - 5E15 AND LATER SOFTWARE RELEASES
	LOCAL SM DEGROWTH WITH GMS-CM3 - 5E15 SOFTWARE RELEASE ONLY
	LOCAL SM-2000 DEGROWTH WITH GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
	EXM-2000 DEGROWTH WITH TRCU/GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
	EXM-2000 DEGROWTH WITH TRCU3/GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
	ORM DEGROWTH WITH TRCU1-2/GMS-CM3 - 5E15 AND LATER SOFTWARE RELEASES
	ORM DEGROWTH WITH TRCU3/GMS-CM3 - 5E15 SOFTWARE RELEASE ONLY
	ORM DEGROWTH WITH TRCU3/GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
	RSM VIA DLTU2 DEGROWTH WITH GMS-CM3 - 5E15 AND LATER SOFTWARE RELEASES
	SECONDARY NETWORK LINK INTERFACE DEGROWTH WITH TRCU3/GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
	SECONDARY NETWORK LINK INTERFACE MIGRATION WITH SM-2000/GMS-CM3 - 5E16.2 AND LATER SOFTWARE RELEASES
235-105-250	POWER-RELATED SYSTEM RECOVERY DECISIONS as follows: □ REMOTE SITE (RSM/ORM/EXM) IS WITHOUT POWER
	POWER-UP 5ESS ® SWITCH APPLICATION HARDWARE UNITS as follows: □ POWER-UP APPLICATION HARDWARE UNITS FOR ALL UNITS EXCEPT LUs, ISLUs/RISLUs, AND PSUs □ POWER-DOWN AND POWER-UP ONTCCOM (CM2/CM3) AND MSGS (CM3) UNITS
	POWER DOWN 5ESS ® SWITCH as follows: □ DECREASE THE RATE OF BATTERY PLANT DISCHARGE
	REPLACE BLOWN FFU OR MFFU FUSES
	DECREASE THE RATE OF BATTERY PLANT DISCHARGE
	HARDWARE CONDITIONING, APR-COMPLIANT UNITS, AND POWER DISTRIBUTION
	ANALYZE UNIX ® RTR OPERATING SYSTEM FAULT
	ANALYZE ADMINISTRATIVE MODULE (AM) SOFTWARE FAULT
	AM INITIALIZATION PROCEDURE AND APPLICATION PARAMETERS as follows: □ PERFORM A MANUAL AM INITIALIZATION
	USE EAI APPLICATION COMMANDS 4-9 TO RAISE THE LEVEL OF INITIALIZATION as follows: □ DETERMINE WHAT EAI POKE(S) IS NEEDED TO ACHIEVE THE DESIRED LEVEL OF INITIALIZATION
	ANALYZE AND CONTROL THE REPAIR OF CM DUPLEX HARDWARE FAILURE
	REPAIR FAILURES IN A CM UNIT
	ANALYZE/RESOLVE CM HARDWARE PROBLEMS as follows: □ MESSAGE SWITCH ANALYSIS □ OFFICE NETWORK TIMING COMPLEX COMMON (ONTCCOM) ANALYSIS □ NETWORK CLOCK ANALYSIS □ TIME MULTIPLEXED SWITCH/DUAL LINK INTERFACE ANALYSIS □ TIME MULTIPLEXED SWITCH LINKS/NETWORK LINK INTERFACE ANALYSIS □ QUAD-LINK PACKET SWITCH GATEWAY PROCESSOR ANALYSIS □ TIME-MULTIPLEXED SWITCH FABRIC PAIR ANALYSIS

ESTABLISH COMMUNICATION WITH ISOLATED SM/SM-2000
ESTABLISH COMMUNICATION WITH ISOLATED RSM
ESTABLISH QLPS COMMUNICATION WITH SM-2000
EQUIPMENT RECOVERY LEVELS
SYSTEM RECOVERY INITIALIZATION LEVELS

4.1.17 Recent Change View References, CM3

Table 4-34 details the Recent Change View (RC/V) references for the CM3.

Table 4-34 CM3 RC/V References

CM3 RC/V References		
View	**Component Name**	**ODA Form**
17.11	TMS SHELF	5708
17.12	TMS LINK	5851
17.16	ONTC HARDWARE	5725
17.17	MSGS HARDWARE	5726
17.18	TRCU SHELF	5812
17.19	QLPS HARDWARE	5854
17.20	MH PIPE ASSIGNMENT	5544
17.23	TRCU PATH	5814
17.24	QPH PIPE ASSIGNMENT	5828
18.1	SWITCHING MODULE	57001
18.16	NLI GROWTH	5853

5. SWITCHING MODULE (SM) and SWITCHING MODULE 2000 (SM-2000)

5.1 Configuration

SM-2000:

- Each SM-2000 contains a duplicated MCTSI, duplicated NLIs, and LDSF DSCs. All other hardware components are configured according to office requirements.

SM:

- Each SM contains a duplicated MCTSI, duplicated DLIs, and two LDSU DSCs. All other hardware components are configured according to office requirements.

The following tables detail the hardware that is contained in the switching modules.

The following table details the control units that are contained in the switching modules.

Control Shelf Units	Diagnosable Components	SM	SM-2000
MCTU3	MCTSI LDSU DLI (Also diagnosed as part of RLI in an RSM)	X	
MCTU2	MCTSI LDSU DLI (Also diagnosed as part of RLI)	X	
SMPU4	MCTSI LDSF		X
SMPU5	MCTSI LDSF		X
TSIU4	MCTSI NLI		X
TSIU4-2	MCTSI NLI		X
FIU	RLI	RSM only	

RCU	□ RCLK	RSM only	

The following table details the line peripheral units that are contained in the switching modules.

Line Peripheral Shelf Units	Diagnosable Components	SM	SM-2000
AIU	□ COMDAC □ LP □ RG	X	X
BAIU	□ COMDAC □ RG □ POTS AP		X
EAIU	□ COMDAC □ LP □ RG		X
ISLU2	□ CC □ CD □ HLSC □ MAN □ LBD □ LCKT	X	X
LU3	□ COMC □ HLSC □ GDXACC □ CHBD □ BD	X	X
PSU2	□ PSUCOM □ PSUPH	X	X
RISLU2	□ CC	X	X

	□ CD □ HLSC □ MAN □ RLGI □ DFI-R □ RRCLK □ LG □ LBD □ LCKT		

The following table details the trunk peripheral units that are contained in the switching modules.

Trunk Peripheral Shelf Units	Diagnosable Components	SM	SM-2000
DNU-S	□ SFI □ TMUX □ CD □ CC		X
OIU	□ OFI		X
ECSU			X
DLTU	□ DFI	X	X
TU	□ CDI □ CHBD □ CKT □ TAC	X	X

The following table details the service peripheral units that are contained in the switching modules.

Service Peripheral Shelf Units	Diagnosable Components	SM	SM-2000
DSU2	□ SAS □ RAF (SM only) □ ISTF (SM only)	X	X

DSU3	□ LDSF □ GDSF □ ISTF □ TTF2		X
GDSU	□ Three-Port Conference □ Six-Port Conference □ TTF	X	
SMPU5	□ GDSF		X
SMPU4	□ LDSF		X
MCTU2	□ LDSU	X	
MCTU3	□ LDSU	X	
CSU	□ ISTF □ GDSF □ TTF2	X	

The following table details the test peripheral units that are contained in the switching modules.

Test Peripheral Shelf Units	Diagnosable Components	SM	SM-2000
MMSU	□ MSUCOM □ ALIT □ SCAN □ SC □ SD □ DFTAC □ MA □ GDXC □ SLIM2 □ PROTO	X	X

DCTU	□ DCTUCOM □ EAN □ PMU □ DCTU Port	X	

The following table details the links and buses that are contained in the switching modules.

Wires	Connects to...		SM	SM-2000	CM	AM	CNI	ASM
	Unit	Unit						
PICB/PIDB	All peripherals	MCTSI	X	X				
NCT Link	SM	TMS	X					
PCT Link	OIU	TSIU		X				
NCT2 Link	SM-2000	TMS		X				
Foundation Link	FLI in the TMSU3	DMI in the CMCU2			X			
MIB	DMI	MMPs PPC			X			
CDAL	DMI NCLK (Backplane) TMS Controller (Backplane)	FPC			X			
IOMI	MMPs FPC (Backplane) PPC (Backplane)	MSCU			X			
DSCH	IOP DFC	DMA				X		
	MSCU	DMA			X	X		
	RPCN DLN	DMA				X	X	
	ASM CDI	DMA				X		X
Umbilical	RSM	HSM	X	X				
ICL	RSM	RSM	RSM only					

5.2 Detailed Description

The following tables detail the functions of the components in the SM-2000 or SM.

The following tables details the functions of the diagnosable components in control units of the SM-2000 or SM.

Part	Function
DLI	Connects the MCTSI to the NCT Link.
NLI	Connects the MCTSI to the NCT2 Link.
MCTSI	Routes switching module control messages and subscriber data. Switches time slots.
RLI	Transmits subscriber data and control messages between an SM at a host site and an SM at an RSM

	site.
RCLK	Stabilizes clock signals for the RSM when the RSM is disconnected from the switch.
LDSF	Refer to the following service peripheral unit table.
LDSU	Refer to the following service peripheral unit table.

The following table details the functions of the line peripheral units of the SM-2000 or SM.

Part	Function
AIU	□ Connects subscriber lines to the SM-2000 □ Converts information from the subscriber lines to a format that is compatible with the *5ESS*® switch
BAIU	□ Connects digital subscriber lines to the *5ESS*® switch and the ATM network for POTS and internet access
ISLU2	□ Connects subscriber lines to the *5ESS*® switch □ Converts information from the subscriber lines to a format that is compatible with the *5ESS*® switch
LU3	□ Connects local subscriber analog lines to the switching module □ Converts analog information from local subscriber lines to a digital format
PSU2	□ Routes packets of control messages and data messages for ISDN lines and C7 signaling trunks
RISLU2	□ Connects subscriber lines to the *5ESS*® switch from a remote site □ Converts information from subscriber lines to a format that is compatible with the *5ESS*® switch.

The following table details the functions of the trunk peripheral units in the SM-2000 or SM.

Part	Function
ECSU	□ Removes echo from long-distance or wireless calls
OIU	□ Converts OC-3/OC-3c format to PCT format and vice versa. □ Interfaces up to three PCT links and one OC-3/OC-3c facility. □ Provides 1+1 (working and protection) Automatic Protection Switching (APS) capability.
DNU-S	□ Terminate Synchronous Optical NETwork (SONET) facilities. □ Convert data/signaling to the Peripheral Control and Timing (PCT) link format for the SM-2000.

DLTU	□ Connects a digital carrier facility to a switching module
TU	□ Connects the local test desk to the Metallic Service Unit to test metallic lines □ Connects analog trunks to a switching module □ Converts analog trunks to a digital format

The following table details the functions of the diagnosable components of the line peripheral units in the SM-2000 or SM.

Part	Function
GDSF	□ Performs three or six user conferencing □ Performs transmission tests □ Performs integrated services test
GDSU	□ Performs three or six user conferencing, and/or □ Performs transmission tests on trunks and subscriber loops
ISTF	□ Tests digital subscriber lines and trunks for maintenance problems
LDSU	□ Generates and decodes all tones that are needed to perform call processing in an SM
LDSF	□ Generates and decodes all tones that are needed to perform call processing in an SM-2000
SAS	□ Provides recorded announcements

The following table details the functions of the test peripheral units in the SM-2000 or SM.

Part	Function
DCTU	□ Measures DC voltages, resistance, and capacitance for analog subscriber lines and trunks
MMSU	□ Tests subscriber lines and trunks □ Monitors and controls various scan and distribute points in the *5ESS*® switch □ Measures DC voltages, resistance, and capacitance for analog subscriber lines and trunks

The following table details the functions of the links and buses in the SM-2000 or SM.

Part	Function
ICL	□ Carries subscriber data between switching modules in an RSM
PICB	□ Carries control messages between the module controller and the peripheral and service units
PIDB	□ Carries data messages between the TSI and the peripheral and service units
PCT Link	□ Carries control, data, and maintenance messages between the TSIU and the DNU-S, PSU2 or OIU.
NCT Link	□ Carries time slots between the CM and the SM
NCT2 Link	□ Carries time slots between the CM and the SM-2000

6. SWITCHING MODULE APPLICATIONS

6.1 Local Switching Module (LSM)

6.1.1 Basic Description

The Local Switching Module (LSM) is an SM or SM-2000.

The LSM is one of five types of switching modules. The acronym, LSM, refers to a switching module that:

- Is located at the host office.
- Connects subscriber lines and trunks to the *5ESS*® switch through the switching module peripheral units.
- Connects to the CM by the NCT links.

For more information about the LSM, go to the hardware description of the switching module.

6.2 Host Switching Module (HSM)

6.2.1 Basic Description

The Host Switching Module (HSM) is an SM or SM-2000.

The HSM is one of five types of switching modules. The acronym, HSM, refers to a switching module that:

- Is located at the host office.
- Connects subscriber lines and trunks to the *5ESS*® switch through the switching module peripheral units.
- Connects subscriber lines and trunks to one or more RSMs to the *5ESS*® switch at the host office by the umbilicals.

The primary job of the HSM is to connect subscriber lines, trunks and one or more RSMs to the CM in the host office.

6.2.2 Functional Description

6.2.2.1 Functions

The HSM connects lines, trunks and one or more RSMs to the CM at the host *5ESS*® switch by the umbilicals, peripherals and NCT or NCT2 links.

6.2.2.2 Operation

In addition to the operations that the switching module performs, the HSM is the only type of switching module that connects one or more RSMs to the *5ESS*® switch.

6.3 Remote Switching Module (RSM)

6.3.1 Basic Description

The Remote Switching Module (RSM) is an SM.

The RSM is one of five types of switching modules. The acronym RSM refers to a switching module that:

- Is located at a remote site up to 150 miles from the *5ESS*® switch at a host site.
- Connects to a switching module at the host site.
- Contains an FIU, RCLK and ASU.

The primary job of the RSM is to switch subscriber lines and trunks from a remote site.

6.3.2 Detailed Description

The following table details the function of the components that are unique to the RSM.

Part	Function
FIU	Connects the DFI to the DLI by the umbilical
RCLK	Maintains processor timing in the RSM when the RSM loses contact with the SM at the host office
ASU	Displays alarms for the RSM

6.3.3 Functional Description

6.3.3.1 Functions

The RSM connects lines and trunks, which are located up to 150 miles from the host site, to the HSM at the host *5ESS*® switch by the umbilicals.

6.3.3.2 Operation

The RSM performs switch operations at a remote location.

The Figure 6-1 depicts the operation of the RSM.

Figure 6-1 RSM Block Diagram

The following table details the operation of the RSM.

The RSM routes subscriber data and control messages to the HSM at the host office.

Stage	Description
1	The MCTSI in the RSM sends subscriber data and control messages to the FIU by the PICB and NCT links.
2	The FIU receives and sends the subscriber data and control messages from the MCTSI to the RDFIs in the DLTU by the FIDB.
3	The RDFIs receive and send the subscriber data and control messages to the HDFI in the DLTU at the host site by the DS1 umbilical.

NOTE: In addition to the functions detailed previously, the RSM performs the same functions as the SM. For general information about the switching modules, refer to the hardware description of the switching modules.

6.4 Optically Integrated Remote Switching Module (ORM)

6.4.1 Basic Description

The Optically Integrated Remote Module (ORM) is an SM or SM-2000.

The ORM is one of five types of switching modules. The acronym ORM refers to a switching module that:

- Is located at a remote site up to 1000 miles from the CM at a host site.
- Connects to the CM at the host office.
- Contains the TRCU.

The primary job of the ORM is to connect lines and trunks, which are located up to 1000 miles from the host office, to the CM at the host office by a DS3 or OC3 transmission system.

NOTE: When the ORM is an SM-2000, some information products refer to the ORM as the EXM-2000.

6.4.2 Configuration

The following table details the configuration of the ORM components that are not contained in the switching module hardware description.

Component	Link/Bus	Connects to ...	Method of Operation	State of Operation
TRCU	NCT	MCTSI	Duplex	ACT/ACT
	DS3 or OC3 transmission system	TRCU at the host site		

6.4.3 Detailed Description

The following table details the function of the ORM components that are not contained in the hardware description of the switching module.

Part	Function
TRCU	Maintains signal clarity for up to 1000 miles between the host site and remote site

6.4.4 Functional Description

6.4.4.1 Functions

The ORM connects lines and trunks, which are located up to 1000 miles from the host office, to the CM at the host *5ESS*® switch by a DS3 or OC3 transmission system.

6.4.4.2 Operation

The ORM interacts with other components to operate the switch.

Figure 6-2 depicts the operation of the ORM.

Figure 6-2 ORM Block Diagram

The ORM routes subscriber data and control messages to the CM that is located at the host site.

Stage	Description
1	The TSI receives subscriber data and control messages from the MCTSI by the NCT links.
2	The TRCU sends the subscriber data and control messages to the TRCU at the host site by the DS3 or OC3 transmission system.

6.5 Transmissionless Remote Switching Module (TRM)

6.5.1 Basic Description

The Transmissionless Remote Module (TRM) is an SM.

The TRM is one of five types of switching modules. The acronym TRM refers to a switching module that:

- Is located at a remote site up to two miles from the CM.
- Connects to the CM at the host office.
- Contains a 982TH circuit pack.

The primary job of the TRM is to connect lines and trunks, which are located up to two miles from the host office, to the CM at the host *5ESS*® switch by a multi-mode optical fiber.

NOTE: Some information products refer to the TRM as the Two-Mile Remote Module.

6.5.2 Detailed Description

The following table details the function of the TRM component that is not contained in the hardware description of the switching module.

Part	Function
982TH	Transmits signals at a distance further than the circuit pack that is used in the LSM

6.5.3 Functional Description

6.5.3.1 Functions

The TRM connects lines and trunks, which are located up to two miles from the host office, to the CM at the host *5ESS*® switch by a multi-mode optical fiber.

6.5.3.2 Operation

The TRM interacts with other components to operate the switch.

Figure 6-3 depicts the operation of the TRM.

Figure 6-3 TRM Block Diagram

The following table details the operation of the TRM.

The TRM routes subscriber data and control messages to the host CM.

Stage	Description
1	The 982TH receives subscriber data and control messages from the MCTSI by the backplane.
2	The 982TH sends the subscriber data and control messages to the 982TH at the host site by a multi-mode fiber.

7. SWITCHING MODULE CONTROL UNITS

7.1 Module Controller and Time Slot Interchanger Unit, Model 3 (MCTU3)

7.1.1 Basic Description

The Module Controller/Time Slot Interchanger Unit Model 3 (MCTU3) is one shelf. The MCTU3 is located in the SMC cabinet of an SM.

The MCTU3 contains the diagnosable components:

- MCTSI
- DLI
- LDSU

7.1.2 Shelf and Circuit Pack Arrangement

The Module Controller/Time Slot Interchanger Unit Model 3 (MCTU3) is located in the SMC cabinet of an SM.

The following table details the shelf and circuit pack arrangement of the MCTU3 hardware components.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
128	014 and 106	**Power Converter**	TN1424
128	021 and 113	**CORE**	KBN20, KBN21, or KBN22
128	032, 040, 124, and 132	**CI**	UN71B or UN71C
128	048 and 140	**PI**	TN1042 or UN395
128	056 or 148	**TSI/SP**	TN1086
128	066, 074, 158, and 166	**DI**	TN1377 or TN1524
128	084 or 176	**DLI**	TN1077F
128	094 or 186	**LDSU (DSC*)**	TN833 or TN1890
NOTE: *******The LDSU circuit pack also is named the DSC. When LDSU-related software programs are installed, the DSC circuit pack is named the LDSU.			

7.2 Module Controller and Time Slot Interchanger Unit, Model 2 (MCTU2)

7.2.1 Basic Description

The Module Controller/Time Slot Interchanger Unit, Model 2 (MCTU2) is two shelves. The MCTU2 is located in the SMC cabinet of an SM.

The MCTU2 contains the diagnosable components:

- MCTSI
- DLI
- LDSU

7.2.2 Shelf and Circuit Pack Arrangement

The Module Controller/Time Slot Interchanger Unit Model 2 (MCTU2) is located in an SMC cabinet of an SM.

The following table details the shelf and circuit pack arrangement of the MCTU2 hardware components.

EQL		Component Name	Component Number
Vertical	Horizontal		
19 and 28	012	**Power Converter**	414AA
19 and 28	018	Empty	UN516
19 and 28	028	**Control and Display and CORE Support 1**	
19 and 28	034	**CORE Support 2**	UN517
19 and 28	042	**CORE**	UN520
19 and 28	050, 058, 064, 070, 076, and 082	**MEM**	TN1376 and TN1661
19 and 28	088	**APP**	UN518
19 and 28	096 and 104	**CI**	UN71
19 and 28	112	**PI**	TN1042
19 and 28	122	Empty	
19 and 28	130 and 138	**DI**	TN1377
19 and 28	144	**TSI/SP**	TN1086
19 and 28	156	**DLI**	TN1077F
19 and 28	166	**LDSU (DSC*)**	TN833 or TN1890
19 and 28	178	Empty	
NOTE: *******The LDSU circuit pack also is named the DSC. When LDSU - related software programs are installed, the DSC circuit pack is named the LDSU.			

7.3 Module Controller and Time Slot Interchanger (MCTSI)

7.3.1 Basic Description

The Module Controller/Time Slot Interchanger (MCTSI) is a multi-circuit pack component. The MCTSI is located in the SMC cabinet of each switching module.

The primary jobs of the MCTSI are to:

- Route switching module control messages and subscriber data.
- Switch time slots.

7.3.2 Electrical Power

The following details the power control packs of the MCTSI:

- **MCTU3**: The TN1424 supplies power for the MCTSI circuit packs in the MCTU3.
- **MCTU2**: The UN516 controls power for the MCTSI circuit packs in the MCTU2.
- **SMPU5**: The UN589 controls power for the MCTSI circuit packs in the SMPU5. The SMPU5 uses one power pack per service group.
- **SMPU4**: The 410AA and SN516B power circuit packs control power for the MCTSI circuit packs in the SMPU4. The SMPU4 uses one power pack per service group.
- **TSIU4**: The 486AA power pack controls power for the MCTSI circuit packs and other circuit packs in the TSIU4 shelf. The TSIU4 uses one power pack per service group.
- **TSIU4-2**: The 486AA and 410AA power packs supply power for each service group of the TSIU4-2. The 486AA supplies power to the TSICOM and TSIS. The 410AA supplies power to the XDX.

7.3.3 Shelf and Circuit Pack Arrangement

The Module Controller/Time Slot Interchanger (MCTSI) is located in an SM or SM-2000 cabinet.

In an SM, the MCTSI circuit packs are contained in the MCTU2 or MCTU3 shelf. In an SM-2000, the

MCTSI circuit packs are contained in the SMPU4 or SMPU5 and TSIU4 or TSIU4-2 shelves.

The following tables detail the shelf and circuit pack arrangement of the MCTSI.

The following table details the shelf and circuit pack arrangement of the MCTSI circuit packs that are contained in the MCTU3 shelf.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
128	014 and 106	**Power Converter**	TN1424
128	021 and 113	**CORE**	KBN20, or KBN21, or KBN22
128	032, 040, 124, and 132	**CI**	UN71B or UN71C
128	048 and 140	**PI**	TN1042 or UN395
128	056 or 148	**TSI/SP**	TN1086
128	066, 074, 158, and 166	**DI**	TN1377 or TN1524

The following table details the shelf and circuit pack arrangement of the MCTSI circuit packs that are contained in the MCTU2 shelf.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
19 and 28	012	**Power Converter**	414AA
19 and 28	018	Empty	
19 and 28	028	**Control and Display and CORE Support 1**	UN516
19 and 28	034	**CORE Support 2**	UN517
19 and 28	042	**CORE**	UN520
19 and 28	050, 058, 064, 070, 076, 082	**MEM**	TN1376, TN1661
19 and 28	088	**APP**	UN518
19 and 28	096, 104	**CI**	UN71
19 and 28	112	**PI**	TN1042
19 and 28	122	Empty	
19 and 28	130, 138	**DI**	TN1377
19 and 28	144	**TSI/SP**	TN1086
19 and 28	178	Empty	

The following table details the shelf and circuit pack arrangement of the MCTSI circuit packs that are contained in the SMPU5 shelf.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
19 and 28	014	**Power Control and Display**	UN589
19 and 28	022	Empty	
19 and 28	032	**CORE**	UN560
19 and 28	042, 052	**MEM**	TN1685 or TN1806
19 and 28	061	**BSN**	KBN8B
19 and 28	072	Empty	
19 and 28	080	**MH**	UN538 or UN584
19 and 28	088, 096	**MH**	UN538
19 and 28	106	**APC**	UN539
19 and 28	114	**PI2**	TN1042B or 395B
19 and 28	122, 130, 138, 146	**CI2**	UN71C

The following table details the shelf and circuit pack arrangement of the MCTSI circuit packs that are contained in the SMPU4 shelf.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
19 and 28	018 and 178	**Power**	410AA
19 and 28	028	**Control and Display**	SN516C
19 and 28	036	**CORE**	UN540
19 and 28	044, 052, 060, and 068	**Memory**	TN1685 or TN1806
19 and 28	077	**BSN**	KBN8
19 and 28	086	Empty	
19 and 28	096*, 104, and 112	**MH**	UN538
19 and 28	122	**APC**	UN539

19 and 28	130	**PI**	TN1042B or 395B
19 and 28	138, 146, 154, and 162	**CI**	UN71B
NOTE: EQL 096 may be equipped with either a UN538 or UN584.			

The following table details the shelf and circuit pack arrangement of the MCTSI circuit packs that are contained in the TSIU4 shelf.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
62	012, 088, 108, and 184	**Power Supply**	486AA
62	020 and 116	**TSICOM**	UM74
62	028, 036, 044, 052, 060, 068, 124, 132, 140, 148, 156, and 164	**DX**	UM73
53	018, 026, 034, 042, 050, 060, 068, 076, 084, 092, 106, 114, 122, 130, 138, 148, 156, 164, 172, and 180	**TSIS**	KLU1

The following table details the shelf and circuit pack arrangement of the MCTSI circuit packs that are contained in the TSIU4-2 shelf.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
62	020, 106, 108, and 184	**Power Supply**	410AA
62	038, 032, 052, 060, 068, 076, 084, 124, 138, 146, 154, 162, and 170	**XDX**	UN553
53	011(LOWER)	**POWER 0**	486AA
53	011(UPPER)	**POWER 1**	486AA
53	017(LOWER)	**TSICOM 0**	UM74C
53	017 (UPPER)	**TSICOM 1**	UM74C
53	029, 037, 045, 053, 061, 069, 077, 085, 093, 101, 111, 119, 127, 135, 143, 151, 159, 167, 175, and 183	**TSIS**	KLU1

7.3.4 Configuration

The following tables detail the configuration of the MCTSI.

The following table details the configuration of the MCTSI circuit packs in the SMPU5 and SMPU4 shelves.

Circuit packs	Link/Bus	Connects to...	Method of Operation	State of Operation
CORE	LS bus	MEM	Duplex	ACT/STBY
		BSN		
BSN	LS bus	CORE		
	System update bus	Mate BSN		
	RS Bus	APC		
MEM	LS Bus	CORE		
MH	RS Bus	BSN		
		APC		
	Backplane	APC		
	Update bus	Mate MH		
APC	RS bus	MH		
		BSN		
	Backplane	MH		
	SUIB	PI		
		CI		
	STCL	TSICOM		
	MCP link	TSIS		
PI	SUIB	APC		
		CI		
	Packet bus	PSIUCOM		

CI	SUIB	APC		
		PI		
	PICB	Peripheral units		

The following table details the configuration of the MCTSI circuit packs in the TSIU4-2 and TSIU4 shelves.

Circuit Packs	Link/Bus	Connects to...	Method of Operation	State of Operation
DX (TSIU4) or XDX (TSIU4-2)	PIDB	Peripheral units	Duplex	ACT/STBY
	TSI Link	TSIS		
	TSICNTL	TSICOM		
TSIS	TSI Link	DX or XDX	Duplex	ACT/STBY
	MCP Link	SMP (TSIS 0 only)		
	PCT Link	DNU-S		
		OIU		
	TSICNTL	TSICOM		
	Backplane	NLI		
TSICOM	STCL	SMP	Duplex	ACT/STBY
	TSICNTL	TSIS DX		

The following table details the configuration of the MCTSI circuit pack in the MCTU3 shelf.

Circuit Packs	Link/Bus	Connects to...	Method of Operation	State of Operation
CORE	Backplane	CI	Duplex	ACT/STBY
		PI		
		TSI		
	LIB	DLI		
	Backplane	Mate SMP	Simplex	ACT
CI	Backplane	CORE	Duplex	ACT/STBY
	PICBs	Peripheral units		
PI	Backplane	CORE	Duplex	ACT/STBY
	Packet Bus	PSU		
TSI/SP	Backplane	DLI	Duplex	ACT/STBY
		SMP		
		DI		
		DSC		
DI	PIDBs	Peripheral units	Duplex	ACT/STBY

The following table details the configuration of the MCTSI circuit packs in the MCTU2 shelf.

Sub-Modules	Link/Bus	Connects to...	Method of Operation	State of Operation
CORE	Backplane	CI	Simplex	ACT
		PI		
		TSI		
	LIB	DLI		
	PICB	Peripheral units		
	Backplane	Mate SMP		
		CORE Support	Duplex	ACT/STBY
		MEM		
		CI		
		APPL		
CORE Support	Backplane	CORE	Duplex	ACT/STBY
APPL	Backplane	CORE	Duplex	ACT/STBY
MEM	Backplane	CORE	Duplex	ACT/STBY
CI	Backplane	CORE	Duplex	ACT/STBY
		TSI/SP		
	PICBs	Peripheral units		
PI	Backplane	TSIU/SP	Duplex	ACT/STBY
		CORE		
	Packet Bus	PSU		
TSI/SP	Backplane	DLI	Duplex	ACT/STBY
		SMP		
		CI		
		PI		
		DI		
		DSC		
DI	PIDBs	Peripheral units	Duplex	ACT/STBY
	Backplane	TSI/SP		
	PIDB	SMP		

7.3.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the MCTSI components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
MCTSI	One side	Major	No impact	No impact
	Both sides	Critical	Stops all call processing for subscriber lines and trunks Stops all service functions to the SM	Reduces call processing capacity
NOTE: The SM-2000 has more capacity than the SM. Therefore, the service impact on the *5ESS*® switch is greater for the SM-2000 than the SM.				

7.3.6 Detailed Description

The following tables detail the function of the circuit packs in the MCTSI.

The following table details the MCTSI circuit packs that are contained in the MCTU3 and MCTU2 shelves.

Part	Function
CORE	Executes call processing control messages and maintenance control messages for all of the switching module components
CORE SUPPORT (MCTU2 only)*	Stores micro-code program instructions for an initialization of the SM
APP (MCTU2 only)*	Routes program instructions and ODD between the MEM and TSI
MEM (MCTU2 only)*	Stores program instructions and ODD
CI	Sends control messages between the CORE and SM peripherals by the PICB
PI2	Sends subscriber data and control messages between the SMP and the PSU by the PB
TSI	Switches time slots between the SM peripheral units and the TMS Monitors the time slot signaling bits and reports changes in state of the bits to the SMP
DI	Sends subscriber data between the SM peripheral units and the MCTSI by the PIDB
NOTE: *******In the MCTU2, the CORE, CORE SUPPORT, APP, and MEM circuit packs are used to perform the functions that the CORE circuit pack performs in the MCTU3.	

The following table details the MCTSI circuit packs that are contained in the SMPU shelf.

Part	Function
APC	Routes control messages and clock pulses between: □ the CORE and TSI, and □ the MHs.
MEM	Stores program instructions and Office Dependent Data (ODD).
BSN	Routes control messages between the APC, CORE, MH, and mate SMPU. Generates and sends internal clock pulses for the SMP.
MH	Sends control messages between the CORE and QLPS by the virtual Q-pipe.
CORE	Executes call processing control messages and maintenance control messages for all of the switching module components.
PI	Sends control messages between the PSU and the CORE by a PB.
CI	Sends control messages between the MCTSI and the peripherals by the PICB.

The following table details the MCTSI circuit packs that are contained in the TSIU shelf.

Part	Function
DX (TSIU4) or XDX (TSIU4-2)	Sends subscriber data between the TSI and peripheral units by the PIDBs.
TSIS	Switches time slots for the SM-2000.

TSICOM	Distributes control messages from the SMP and clock pulses to the TSISs and DX circuits.

7.3.7 Functional Description

7.3.7.1 Functions

The MCTSI does the following:

- Controls call processing activities for the peripheral units in the switching module.
- Handles maintenance activities for the switching module.
- Monitors and reports all switching module activities to the AM to generate hardware status reports.
- Handles subscriber data and control messages from the switching module peripherals and CM.
- Performs a "bootstrapper function" which enables the *5ESS*® switch to rapidly reload memory in the SMP.

7.3.7.2 Operation

The MCTSI interacts with other components to operate the switch. Figure 7-1 depicts the operation of the MCTSI in an SM-2000.

Figure 7-1 MCTSI Block Diagram for an SM-2000

Figure 7-2 depicts the operation of the MCTSI in an SM.

Figure 7-2 MCTSI Block Diagram for an SM

The following tables detail the operation of the MCTSI.

The MCTSI controls call processing.

Stage	Description
1	The MCTSI receives call processing control messages and subscriber data from a peripheral unit.
2	The MCTSI sets up and routes the call to the appropriate destination that include the following: □ The same switching module. □ Two other switching modules through the CM.

The MCTSI handles maintenance control messages that request diagnostic information from the AM.

Stage	Description
1	The MCTSI receives a control message for diagnostic information from the AM through the CM by the NCT links.
2	The MCTSI executes the message for the target unit.
3	The MCTSI generates and sends a message with the diagnostic result through the CM to the AM by the NCT links.

The MCTSI collects and sends information about call processing activities to the AM.

Stage	Description
1	The MCTSI monitors call processing activities for all *5ESS*® switch calls.
2	The MCTSI compiles a record of various call processing activities as defined by software, which include the number of calls that are processed.
3	The MCTSI periodically sends messages that contain the entire record of call processing activities to the AM. (The frequency of these intervals is determined by software.)

The MCTSI handles subscriber data and control messages between the peripherals in the switching module and the CM.

Stage	Description
1	The MCTSI receives a message from either a peripheral unit in the switching module, inter-SM trunk, or CM.
2	The MCTSI accesses its ODD that is stored in memory and determines the destination of the message.
3	The MCTSI routes the message to the appropriate destination: □ When the message is addressed to the CM, then the MCTSI routes the message to the CM by the NCT links. □ When the message is addressed to the peripherals in the switching module, then the MCTSI routes the message to the peripherals by the PICBs, PCT link, or PB.

7.4 Switching Module Processor Unit (SMPU)

7.4.1 Basic Description

The Switching Module Processor Unit (SMPU) is a two shelf unit. The SMPU is located in the SM-2000 cabinet (SMC). There are two models of the SMPU: SMPU4 and SMPU5.

The SMPU contains the diagnosable components:

- LDSF.
- module controller part of the MCTSI.

7.4.2 Shelf and Circuit Pack Arrangement

The Switching Module Processor Unit (SMPU) is located in the SMC cabinet of an SM-2000.

The following table details the shelf and circuit pack arrangement of the SMPU5.

EQL		Component Name	Component Number
Vertical	Horizontal		
19 and 28	014	**Power Control and Display**	UN589
19 and 28	019	Empty	
19 and 28	032	**CORE**	UN560
19 and 28	042 and 052	**MEM**	TN1685 or TN1806
19 and 28	061	**BSN**	KBN8B
19 and 28	072	Empty	
19 and 28	080	**MH**	UN538 or UN584
19 and 28	088 and 096	**MH**	UN538
19 and 28	106	**APC**	UN539
19 and 28	114	**PI2**	TN1042B or 395B
19 and 28	122, 130, 138, and 146	**CI2**	UN71C

The following table details the shelf and circuit pack arrangement of the SMPU4.

EQL		Component Name	Component Number
Vertical	Horizontal		
19 and 28	018 and 178	**Power**	410AA
19 and 28	028	**Control and Display**	SN516C
19 and 28	036	**CORE**	UN540
19 and 28	044, 052, 060, and 068	**Memory**	TN1685 or TN1806
19 and 28	077	**BSN**	KBN8
19 and 28	086	Empty	
19 and 28	096*****, 104, and 112	**MH**	UN538
19 and 28	122	**APC**	UN539
19 and 28	130	**PI**	TN1042B or 395B
19 and 28	138, 146, 154, and 162	**CI**	UN71B
NOTE: *****EQL 096 may be equipped with either a UN538 or UN584.			

7.5 Time Slot Interchanger Unit, Model 4 (TSIU4)

7.5.1 Basic Description

The Time Slot Interchanger Unit (TSIU) is two shelves. The TSIU is located in the SMC cabinet of the SM-2000 cabinet. There are two models of the TSIU: the TSIU4-2 and TSIU4.

The TSIU contains the diagnosable components:

- time slot interchanger portion of the MCTSI
- NLI

7.5.2 Shelf and Circuit Pack Arrangement

The Time Slot Interchanger Unit (TSIU) is located in the SMC cabinet of an SM-2000. Each SM-2000 contains either one TSIU4 or one TSIU4-2.

- The table below details the shelf and circuit pack arrangement of the TSIU4 hardware components.

EQL		Component Name	Component Number
Vertical	Horizontal		
62	012, 088, 108, 184	**Power Supply**	486AA
62	020, 116	**TSICOM**	UM74
62	028, 036, 044, 052, 060, 068, 124, 132, 140, 148, 156, 164	**DX**	UM73
53	018, 026, 034, 042, 050, 060, 068, 076, 084, 092, 106, 114, 122, 130, 138, 148, 156, 164, 172, 180	**TSIS**	KLU1

The table below details the shelf and circuit pack arrangement of the TSIU4-2 hardware components.

EQL		Component Name	Component Number
Vertical	Horizontal		
62	020, 106, 108, 184	**Power Supply**	410AA
62	038, 032, 052, 060, 068, 076, 084, 124, 138, 146, 154, 162, 170	**XDX**	UN553
53	011(LOWER)	**POWER 0**	486AA
53	011(UPPER)	**POWER 1**	486AA
53	017(LOWER)	**TSICOM 0**	UM74C
53	017 (UPPER)	**TSICOM 1**	UM74C
53	029, 037, 045, 053, 061, 069, 077, 085, 093, 101, 111, 119, 127, 135, 143, 151, 159, 167, 175, 183	**TSIS**	KLU1

7.6 Network Link Interface (NLI)

7.6.1 Basic Description

The Network Link Interface (NLI) is a one paddle board component. The NLI is located in the backplane of the TSIU4 or TSIU4-2 shelf in an SMC cabinet of an SM-2000.

The primary job of the NLI is to connect the MCTSI to the TMS.

7.6.2 Electrical Power

The power pack controls power for the Network Link Interface (NLI). The power pack is located on the

TSIU4 or TSIU4-2 shelf.

7.6.3 Shelf and Circuit Pack Arrangement

The Network Link Interface (NLI) is located in the backplane of the TSIU4 or TSIU4-2 shelf in an SMC cabinet of an SM-2000.

The table below details the shelf and circuit pack arrangement of the NLI hardware components.

EQL		Component Name	Component Number
Vertical	Horizontal		
49	018, 106*	**NLI**	BKD7
49	029, 111**		

NOTE: Additional NLI boards may be connected at the backplane of any TSIS circuit pack.

*TSIU4 only

**TSIU4-2 only

7.6.4 Configuration

The table below details the configuration of the Network Link Interface (NLI).

Circuit Packs	Link/Bus	Connects to...	Method of Operation	State of Operation
NLI	NCT2	QLI2	Duplex	ACT MAJ/ ACT MIN
	Backplane	TSIS		

7.6.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the Network Link Interface (NLI) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
NLI	One side	Major	No impact	No impact
	Both sides	Critical	Reduces call processing between switching modules	□ When the first four NLIs go out-of-service, then the SM is isolated from the *5ESS*® switch □ When additional NLIs go out-of-service, then call processing capacity of the SM is reduced

7.6.6 Detailed Description

The table below details the function of the Network Link Interface (NLI).

Part	Function
NLI	□ Connects the MCTSI to the TMS □ Converts subscriber data and control messages

7.6.7 Functional Description

7.6.7.1 Functions

The Network Link Interface (NLI):

- Connects the MCTSI to the TMS.
- Converts subscriber data and control messages.

7.6.7.2 Operation

- The Figure 7-3 depicts the operation of the NLI.

Figure 7-3 NLI Block Diagram

- The table below details the operation of the NLI.

  The NLI handles subscriber data and control messages between the MCTSI and the TMS.

Stage	Description
1	The NLI receives subscriber data and control messages from the TSIS via the backplane.
2	The NLI converts and sends the messages to the QLI2 in the TMS via the NCT2.

7.7 Dual Link Interface (DLI)

7.7.1 Basic Description

The Dual Link Interface (DLI) is a one circuit pack component. The DLI is located in the MCTU2 or MCTU3 shelf of the SMC cabinet of an SM.

The primary job of the DLI is to connect the MCTSI to the TMS.

7.7.2 Electrical Power

A power converter circuit in the Dual Link Interface (DLI) circuit pack controls power for the circuit pack. The power converter circuit is located on the faceplate of the DLI circuit pack.

7.7.3 Shelf and Circuit Pack Arrangement

The Dual Link Interface (DLI) is located in the MCTU2 or MCTU3 shelf in the SMC cabinet of an SM.

The following table details the shelf and circuit pack arrangement of the DLI hardware components.

EQL		Component Name	Component Number
Vertical	Horizontal		
19 and 28	156*	DLI	TN1077F
28	084 and 176**		
NOTE: ******* MCTU2 only. ******** MCTU3 only.			

7.7.4 Configuration

The following table details the configuration of the Dual Link Interface (DLI).

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
DLI	NCT Link	QLI	Duplex	ACT/ACT or ACT/STBY*
	Backplane	TSI		
NOTE: ******* RSM only				

7.7.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Dual Link Interface (DLI) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
DLI	One side	Major	No impact.	No impact.
	Both sides	Critical	Reduces call processing between the SMs.	Isolates one SM from the *5ESS*® switch.

7.7.6 Detailed Description

The following table details the functions of the Dual Link Interface (DLI).

Part	Function
DLI	Connects the MCTSI to the TMS. Converts subscriber data and control messages.

7.7.7 Functional Description

7.7.7.1 Functions

The Dual Link Interface (DLI) provides the following:

- Connects the MCTSI to the TMS.
- Converts subscriber data and control messages.

7.7.7.2 Operation

Figure 7-4 depicts the operation of the DLI.

Figure 7-4 DLI Block Diagram

The following table details the operation of the DLI.

The DLI handles subscriber data and control messages between the MCTSI and TMS.

Stage	Description
1	The DLI receives subscriber data and control messages from the MCTSI by the backplane.
2	The DLI converts and sends the messages to the QLI by the NCT link.

7.8 Facilities Interface Unit (FIU)

7.8.1 Basic Description

The Facility Interface Unit (FIU) is one shelf. The FIU is located in an LTP cabinet of an RSM.

The FIU contains part of the diagnosable component, the RLI.

7.8.2 Shelf and Circuit Pack Arrangement

The Facility Interface Unit (FIU) is located in an LTP cabinet of an RSM.

The following table details the shelf and circuit pack arrangement of the FIU3 hardware components.

Horizontal	Component Name	Component Number
026	**PWR**	495KA
036, 086, 126, and 176	**MUX**	TN619 and TN1039
046,056 076, 136, 146 and 166	**LI**	TN834
056 and 156	**CLK CTRL**	TN618

The following table details the shelf and circuit pack arrangement of the FIU3 hardware components.

Horizontal	Component Name	Component Number
016	**PWR**	494LA
026, 076, 116, and 166	**MUX**	TN619 and TN1039
036 and 126	**MUX LI**	TN1510
056 and 146	**CLK CTRL**	TN618

7.9 Remote Link Interface (RLI)

7.9.1 Basic Description

The Remote Link Interface (RLI) is a multi-circuit pack component.

The RLI consists of the following:

- Circuit packs that are located in the FIU shelf of an LTP cabinet of an RSM, and
- Circuit pack, the DLI, that is located in the MCTU2 or MCTU3 shelf of an SMC cabinet of an RSM.

The primary job of the RLI is to transmit subscriber data and control messages between an switching module at a host site and an SM at a remote site.

7.9.2 Electrical Power

FIU shelf. The 495KA power circuit pack controls power for the Remote Link Interface (RLI) packs.

MCTU shelf. A power circuit in the RLI circuit pack, the DLI, controls power for the circuit pack.

7.9.3 Shelf and Circuit Pack Arrangement

The Remote Link Interface (RLI) is located in:

- FIU shelf of an RSM cabinet (LTP), and
- MCTU2 or MCTU3 shelf of an SM cabinet (SMC).

- The table below details the shelf and circuit pack arrangement of the RLI hardware components.

  The table below details the shelf and circuit pack arrangement of the RLI circuit packs that the FIU shelf contains.

EQL		Component Name	Component Number
Vertical	Horizontal		
	026	**PWR**	495KA
	036, 086, 126, and 176	**MUX**	TN619
	046, 076, 136, and 166	**LI**	TN834
	056	**CLK**	TN835
	066	**CLK CTRL**	TN618

The table below details the shelf and circuit pack arrangement of the RLI circuit packs that the MCTU shelf contains.

EQL		Component Name	Component Number
Vertical	Horizontal		
19, 28	156*	**DLI**	TN1077
28	084, 176**		
*MCTU2 only **MCTU3 only			

7.9.4 Configuration

The following tables detail the configuration of the Remote Link Interface (RLI).

The following table details the RLI circuit packs that are contained in the FIU shelf.

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
MUX	FIDB	RDFI	Duplex	ACT/STBY
	Backplane	LI		
LI	NCT	DLI	Duplex	ACT/STBY
	MUX	Backplane		
CLK	Backplane	CLK CTRL	Duplex	ACT/STBY
CLK CTRL	PICB	MCTSI	Duplex	ACT/STBY
	Backplane	CLK		
		MUX		
		LI		

The following table details the RLI circuit packs that are contained in the MCTU2 or MCTU3 shelf.

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
DLI	NCT Link	LI	Duplex	ACT/STBY
	Backplane	TSI		

7.9.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the Remote Link Interface (RLI) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
RLI	One side	Major	No impact	No impact
	Both sides	Critical	May restrict long-distance calls because the Host SM and RSM are disconnected	May increase call failures between the Host SM and RSM are disconnected
NOTE: When the RSM is disconnected from the host SM, then the RLI uses the clock pulses that are generated by the RCLK.				

7.9.6 Detailed Description

The following tables detail the functions of the circuit packs in the Remote Link Interface (RLI).

The following table details the functions of the RLI circuit packs that are contained in the FIU shelf.

Part	Function
MUX	The MUX performs the following: □ Splits and combines call processing control messages and subscriber data. □ Connects the LI to the RDFIs.
LI	Connects the DLI to the MUX.
CLK	Generates clock pulses for the RSM.
CLK CTRL	The CLK CTRL performs the following: □ Routes control messages to the FIU components. □ Sends clock pulses to the MCTSI.

The following table details the functions of the RLI circuit pack that are contained in the MCTU2 or MCTU3 shelf.

Part	Function
DLI	The DLI performs the following: □ Connects the MCTSI and FIU in the RSM. □ Converts subscriber data and control messages.

7.9.7 Functional Description

7.9.7.1 Functions

The Remote Link Interface (RLI) performs the following:

- Transmits subscriber data and control messages between an switching module at a host site and an SM at an RSM site.
- Generates clock pulses for the RSM when the RSM is operating in a stand-alone mode.

7.9.7.2 Operation

- The Figure 7-5 depicts the operation of the RLI.

Figure 7-5 RLI Block Diagram

- The tables below detail the operation of the RLI.

The RLI handles control messages and subscriber data between the MCTSI and the RDFIs.

Stage	Description
1	The DLI receives control messages and subscriber data from the MCTSI via the backplane.
2	The DLI sends the messages to the LI via the NCT link.
3	The LI receives and sends the messages to the MUX via the backplane.
4	The MUX combines and sends the messages to the RDFIs via FIDB.

The RLI handles control messages and subscriber data between the RDFIs in the DLTU.

Stage	Description
1	The MUX receives control messages and subscriber data from the RDFIs via the FIDB.
2	The MUX splits and sends the messages to the LI via the backplane.
3	The LI receives and sends the messages to the DLI via the NCT link.
4	The DLI receives and sends the messages to the MCTSI via the backplane.

The RLI generates and handles clock pluses.

Stage	Description
1	□ When the RSM is operating in the System Normal mode, then the MUX receives clock pulses from the RDFI via the FIDB and sends the pulses to the CLK CTRL via the backplane. □ When the RSM is operating in Stand-Alone mode, then the CLK generates and sends clock pulses to the CLK CTRL via the backplane.
2	The CLK CTRL receives and sends the clock pulses to the MCTSI via the NCT links.

7.10 Remote Clock Unit (RCLKU)

7.10.1 Basic Description

The Remote Clock Unit (RCLKU) is a one shelf, multi-circuit pack component. The RCLKU is located in the common resource RSM at an MMRSM site.

The primary job of the RCLKU is to stabilize clock signals for the RSM during stand-alone operation.

NOTE: Some documents refer to the RCLKU as the RCU.

7.10.2 Electrical Power

The SN516 Control and Display pack controls power for all Remote Clock Unit (RCLKU) packs, except the oscillator pack.

The 494LA Power Converter circuit pack controls power for the oscillator pack.

The SN516 Control and Display circuit pack and 494LA Power Converter circuit pack are located in the RCLKU shelf.

7.10.3 Shelf and Circuit Pack Arrangement

The Remote Clock Unit (RCLKU) is located in the Remote Switching Module (RSM).

The table below details the shelf and circuit pack arrangement of the RCLKU hardware components.

EQL		Component Name	Component Number
Vertical	Horizontal		
	008 and 098	**Power Control and Display**	SN516
	016 and 106	**Power Converter**	494LA
	026 and 116	**RCLK Synchronizer (1)**	TN1274B
	038 and 128	**RCLK Controller**	TN1276
	048 and 138	**RCLK Synchronizer (0)**	TN1274B
	072 and 162	**RCLK Oscillator***	TN1286B, TN1285B, and TN1283B

7.10.4 Configuration

The table below details the configuration of the Remote Clock Unit (RCLKU).

Circuit Pack	Link/Bus	Connects to...	Method of Operation	State of Operation
RCLK Synchronizer	Backplane	RCLK Controller	ACT/ACT	Duplex
		DFI		
RCLK Controller	PICB	RSM Module Controller	ACT MAJ/ ACT MIN	Duplex
	Backplane	FIU		
		Other RCLKUs		
		RCLK Synchronizer		
RCLK Oscillator	Backplane	RCLK Controller	ACT/ACT	Duplex

		Other RCLKUs RMMSU		

7.10.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the Remote Clock Unit (RCLKU) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
RCLK	One side	Major	No impact	No impact
	Both sides	Critical	No impact	No impact *
* When the RSM is operating in the stand-alone mode, timing errors may occur in the digital carrier systems that connect to the RSM.				

7.10.6 Detailed Description

The table below details the function of the circuit packs in the Remote Clock Unit (RCLKU).

Part	Function
RCLK Oscillator	□ During a normal operation state, the RCLK Oscillator provides the synchronizer with a source to remove jitter from the clock pulses that are received from the SM at the host site. □ During isolation from the host office, the RCLK Oscillator generates clock pulses for the RSM.
RCLK Synchronizer	During a normal operation state, the RCLK Synchronizer removes jitter from the clock pulses. (This action maintains timing in the RSM.)
RCLK Controller	Synchronizes the oscillator clock pulses with the synchronizer clock pulses

7.10.7 Functional Description

7.10.7.1 Functions

The Remote Clock Unit (RCLKU) maintains RSM processor timing when the RSM loses contact with the switching module at the host office.

7.10.7.2 Operation

The RCLKU interacts with other components to operate the switch.

□ The Figure depicts the operation of the RCLKU.

□ The table below details the operation of the RCLKU.

The RCLKU provides clock signals for the RSM.

Stage	Description
1	The oscillator packs generate clock pulses.
2	The oscillator packs send the pulses to the controller packs via the backplane.
3	The synchronizer packs receive clock pulses from the RDFI Type1 that is connected to the HDFI at the host office.
4	The synchronizer packs temporarily store each clock pulse.
5	The synchronizer packs send the pulse to the controller packs via the backplane.
6	The controller packs receive the pulses from the oscillator and synchronizer packs.
7	The controller packs compare the oscillator pulse with the synchronizer pulse and calculate the average difference.
8	The controller packs send the pulse to the FIU.
9	When the RDFI does not receive clock pulses from the HDFI, the synchronizer packs do not send clock

	pulses to the controller.
10	When the controller does not receive clock pulses from the synchronizer packs, the controller sends the clock pulse that the oscillator generates to the FIU.

8. SWITCHING MODULE LINE PERIPHERALS

8.1 Access Interface Unit (AIU)

8.1.1 Basic Description

The Access Interface Unit (AIU) is a one shelf unit. The AIU is located in an LTP or FAC cabinet of an SM or SM-2000 cabinet.

The primary job of the AIU is to connect subscriber lines to the switching modules.

8.1.2 Electrical Power

A power converter circuit in each Access Interface Unit (AIU) circuit pack controls power for the circuit pack.

8.1.3 Shelf and Circuit Pack Arrangement

The Access Interface Unit (AIU) is located in an LTP or FAC cabinet of a switching module cabinet. A standard LTP cabinet contains one to three AIU shelves. The FAC cabinet contains one to six AIU shelves.

The table below details the shelf and circuit pack arrangement of the AIU hardware components.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
Various	083 and 108	**COMDAC**	DAC100
Various	133, 158, 183, 208, 233, 258, 283, 308, 333, 363, 388, 413, 438, 463, 488, 513, 538, 563, 588, and 613	**LP (0 - 19)**	LPZ100, LPP100, LPM100, LPU100, LPT100
Various	563 and 613	**RG**	RPG100

8.1.4 Configuration

The table below details the configuration of the Access Interface Unit (AIU).

Circuit Pack	Link/Bus	Connects to...	Method of Operation	State of Operation
COMDAC	PICB	SMP	ACT	Simplex
	PIDB	TSI		
	DPIDB	PSU		
	MTB	MMSU		
LP	32-bit bus	COMDAC	ACT	Simplex
	RGB	RG		
RG	RGB	LP	ACT	Simplex

8.1.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the diagnosable components in the Access Interface Unit (AIU) are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
AIU (Service Groups), COMDAC	One side	Major	Reduces the possibility to complete a call by 50 percent	Reduces the capacity of the AIU by 50 percent
	Both sides	Critical	Removes service to the subscriber lines that connect to the out-of-service AIU	Reduces call processing capacity
LP	One circuit pack	Major	**LP**: Removes up to 32 subscriber lines from	**LP**: Reduces call processing capacity

			service **LC**: Removes one subscriber line from service	**LC**: No impact
	Multiple circuit packs	Critical	**LP**: Removes up to 32 additional subscriber lines per circuit pack	**LP**: Further reduces call processing capability
RG	One circuit pack	Major	No impact	Increases the time necessary to complete the call
	Multiple circuit packs	Critical	Stops termination of calls in up to three AIUs	Reduces call processing capacity

8.1.6 Detailed Description

The table below details the functions of the diagnosable components in the Access Interface Unit (AIU).

Circuit Pack	Function
COMDAC	Routes control messages and subscriber data between the application packs and MCTSI
LP	**LP** □ Connects between 16 and 32 subscriber lines **LC (Diagnosable circuit in the LP)** □ Connects one subscriber line
RG	Provides power ring for analog lines

8.1.7 Functional Description

8.1.7.1 Functions

The Access Interface Unit (AIU):

□ Connects up to 640 subscriber lines to the SM or SM-2000.

8.1.7.2 Operation

The AIU interacts with other components to operate the switch.

□ The Figure 8-1 depicts the operation of the AIU.

Figure 8-1 AIU Block Diagram

- The table below details the operation of the AIU.

The AIU handles analog and digital subscriber signals from the MDF.

Stage	Description
1	The LP receives a signal from the MDF via a cable pair.
2	The LP sends the signal to the COMDAC via the backplane.
3	The COMDAC receives and sends a control message from the LP to: - the SMP via the PICB (analog), or - the PSU via the DPIDB (digital)
4	The PSU receives and sends the message to the SMP via the PB.
5	The SMP receives and sends the message to the COMDAC via the PICB.
6	The COMDAC receives and sends the message to the LP via the backplane.
7	The LP tests the line and sends the message to the COMDAC via the backplane.
8	The COMDAC receives and sends the message from the LP to the MCTSI via the PICB.

The AIU handles analog and digital subscriber signals from the MCTSI.

Stage	Description
1	The COMDAC receives a control message from the MCTSI via the PICB.
2	The COMDAC sends the message to the LP via the backplane.
3	The LP receives the message from the COMDAC. - When the message is handled by a digital LP, then the LP sends the message to ring the phone via a cable pair. - When the message is handled by an analog LP, then the LP closes a gate to the RG via the RGBs.
4	The RG passes ringing current through the LP to the phone via a cable pair.

8.2 Broadband Access Interface Unit

8.2.1 Basic Description

The Broadband Access Interface Unit (BAIU) is a one to six shelf unit. The BAIU is located in an LTP or FAC cabinet of an SM-2000.

The primary job of the BAIU is to connect digital subscriber lines to the *5ESS*® switch and the ATM network for POTS and internet access.

8.2.2 Electrical Power

A power converter circuit in each Broadband Access Interface Unit (BAIU) circuit pack controls power for the circuit pack.

8.2.3 Shelf and Circuit Pack Arrangement

The Broadband Access Interface Unit (BAIU) is located in an LTP or FAC cabinet of an SM-2000.

The tables below detail the shelf and circuit pack arrangement of the BAIU hardware components.

The table below details the shelf and circuit pack arrangement for the BAIU that is located in shelves 0 and 3.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
Various	001 and 002	**COMDAC**	DAC100
Various	003	**AFM**	LPA900
Various	004	**AFM (reserved)**	LPA900, LPA910
Various	005	**POTS LP**	LPZ100B, LPZ100C
Various	006, 007, 008, 009, 010, 011, 012 and 013	**DSL LP**	LPA400, LPA408, LPA800
Various	014, 015, 016, 017, and 018	**POTS LP***	LPZ100B (Analog), LPC100B,
Various	014, 015, 016, 017, and 018	**ISDN LP***	LPU100, LPU116
Various	019, 020, 021, and 022	**RG****	RGP100
*Shelf 0 and 3 only. In shelves 1,2, 4 and 5, the LPZ100 is located in EQL 014. DSL LP circuit packs occupy the remaining slots.			
**Shelf 0 and 3 only.			

The table below details the shelf and circuit pack arrangement for the BAIU that is located in shelves 1,2, 4 and 5.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
Various	001 and 002	**COMDAC**	DAC100
Various	003	**AFM**	LPA900
Various	004	**AFM (reserved)**	LPA900
Various	005, 014	**POTS LP**	LPZ100B
Various	006, 007, 008, 009, 010, 011, 012, 013, 015, 016, 017, 018, 019, 020, 021, and 022	**DSL LP**	LPA400

8.2.4 Configuration

The table below details the configuration of the Broadband Access Interface Unit (BAIU).

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
COMDAC	PICB	SMP	ACT	Simplex
	PIDB	TSI		
	DPIDB	PSU		
	MTB	MMSU		

POTS LP	32-BIT BUS	COMDAC	ACT	Simplex
	MTB	MMSU		
	Backplane	DSL AP		
	Cable pair	MDF		
	RGB	RG		
DSL LP	32-BIT BUS	COMDAC	ACT	Simplex
	MTB	MMSU		
	Backplane	POTS AP		
	Backplane	AFM		
	Cable pair	MDF		
ISDN LP	32-BIT BUS	COMDAC	ACT	Simplex
	MTB	MMSU		
	Cable pair	MDF		
RG	RGB	POTS AP	ACT	Simplex
	Backplane	COMDAC		
AFM	Backplane	ADSL AP	ACT	Simplex
	DS3	Packet Network*		
	MTNCE Port	PCGSI		
*The AFM packs are linked sequentially. Only the first circuit pack in the chain is connected to the packet network.				

8.2.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the Broadband Access Interface Unit (BAIU) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
COMDAC	One side	Major	Reduces the possibility to complete a POTS call by 50 percent	Reduces the POTS capacity of the BAIU by 50 percent
	Both sides	Critical	Removes the subscriber POTS lines that connect to the out-of-service AIU	Reduces POTS call processing capacity
POTS or ISDN AP	One circuit pack	Major	**LP:** Removes 32 or 16 subscriber lines from service **LC:** Removes one subscriber line from service	**LP:** Reduces call processing capacity **LC:** No impact
	Multiple circuit packs	Critical	**LP:** Removes up to 32 or 16 additional subscriber lines per circuit pack	**LP:** Further reduces call processing capability
DSL AP	One circuit pack	*	**LP:** Removes up to four subscriber lines from service **LC:** Removes one subscriber line from service	**LP:** Reduces call processing capacity **LC:** No impact
	Multiple circuit packs	*	**LP:** Removes up to four additional subscriber lines per circuit pack	**LP:** Further reduces call processing capability
RG	One circuit pack	Major	No impact	Increases the time necessary to complete the call
	Multiple circuit packs.	Critical	Stops call termination in up to three BAIUs	Reduces call processing capacity
AFM	One pack	*	Stops DSL service for subscribers that are connected to the BAIU**	No impact

* Go to the element manager terminal for alarm status.

** The AFM packs are sequentially linked. Only the first circuit pack in the chain is connected to the packet network. An out-of-service circuit pack impacts each pack that follows the out-of-service circuit pack in the chain. The closer the circuit pack is to the connection with the packet network the more subscribers that are impacted.

8.2.6 Detailed Description

The table below details the function of the diagnosable components in the Broadband Access Interface Unit (BAIU).

Part	Function
COMDAC	Routes control messages and subscriber data between the LPs and the MCTSI
POTS LP	□ **LP**

	Connects subscriber lines □ **LC (Diagnosable circuit in the LP)** Connects one subscriber line
DSL LP	Connects DSL subscribers to: □ the POTS LP for POTS calls, and □ the ATM network for internet access
ISDN AP	Connects 16 subscriber lines
RG	Provides power ring for the DSL and analog lines
AFM	□ Splits and combines DSL signals □ Connects the DSL LPs to the ATM

8.2.7 Functional Description

8.2.7.1 Functions

The Broadband Access Interface Unit (BAIU):

□ Connects digital subscriber lines to the *5ESS*® switch and the ATM network for POTS and internet access.

8.2.7.2 Operation

□ The Figure 8-2 depicts the operation of the BAIU.

Figure 8-2 BAIU Block Diagram

- The table below details the operation of the BAIU.

The BAIU handles call processing data for DSL, ISDN, and POTS subscriber signals from the MDF.

Stage	Description
1	The DSL, POTS, and ISDN LPs receive a signal from the MDF via a metallic wire.
2	- When the signal is DSL-specific, then the DSL LP splits and sends a DSL-specific message and control packet message to the AFM and the POTS-specific call processing and control signal to the POTS LP. - When the signal is ISDN-specific, then the ISDN LP sends a call processing data message to the COMDAC. - When the signal is analog-specific, then the POTS LP converts and sends the call processing data message to the COMDAC.
3	- The AFM receives and routes the DSL packet-specific message from the DSL LP to the ATM via the DS3. - The POTS LP receives and sends the messages from the DSL LP to the COMDAC via the backplane. - The COMDAC receives the ISDN signal and analog signal from the POTS or ISDN LP via the backplane. A. When the COMDAC receives the ISDN signal, then the COMDAC splits and sends the control and packet message to the PSU via the DPIDB. B. When the COMDAC receives the analog signal and DSL POTS-specific signal, then the COMDAC

	splits and sends a control message to the MCTSI via the PICB.

The BAIU handles call processing data DSL, ISDN, and POTS subscriber messages from the PSU and the MCTSI.

Stage	Description
1	The COMDAC receives a message from the PSU and MCTSI.
2	□ When the COMDAC receives an ISDN-specific control message and packet message from the PSU via the DPIDB and an ISDN-specific call processing message from the MCTSI via the PIDB, then the COMDAC combines and sends the messages to the LP via the backplane. □ When the COMDAC receives the POTS-specific control message from the MCTSI via the PICB and the DSL or POTS-specific call processing message from the MCTSI via the PIDB, then the COMDAC combines and sends the messages to the LP via the backplane.
3	□ When the ISDN LP receives an ISDN and packet-specific message from the COMDAC, then the LP sends the message to the MDF via a metallic wire. □ When the POTS LP receives a DSL-specific message and POTS-specific message from the COMDAC, then the POTS LP converts and sends: A. the POTS call processing data message to the MDF via a metallic wire. B. the DSL-specific message to the DSL LP via the backplane.
4	The DSL AP receives a DSL-specific message from the POTS LP. The DSL LP converts and sends the message to the MDF via a metallic wire.

The BAIU handles packet-specific messages from the packet network.

Stage	Description
1	The AFM receives a packet-specific message from the packet network via the DS3.
2	The AFM routes the message to the DSL LP via the backplane.
3	The DSL LP routes the message to the MDF via a metallic wire.

8.3 Expansion Access Interface Unit (EAIU)

8.3.1 Basic Description

The Expansion Access Interface Unit (EAIU) is a one shelf unit. At the host site, the EAIU is located in an SM-2000 cabinet (FAC). At the remote site, the EAIU is located in a cabinet up to 300 miles from the host SM-2000. The cabinet is dedicated for EAIU use.

The EAIU contains individually diagnosable components that include the following:

- RCOMDAC
- RG
- LP.

The primary job of the EAIU is to connect subscriber lines to the SM-2000 through a DNUS by the PCT links.

The EAIU support Emergency Standalone (ESA) operations when all primary communication access to the host switch is severed for any reason.

8.3.2 Electrical Power

A power converter circuit in each EAIU circuit pack controls power for the circuit pack.

8.3.3 Shelf and Circuit Pack Arrangement

At a host site, the Expansion Access Interface Unit (EAIU) is located in a SM-2000 cabinet (LTP or FAC). A standard FAC cabinet contains three or six EAIU shelves.

At a remote site, the EAIU may be located in a cabinet up to 300 miles from the host SM-2000. The cabinet is dedicated for EAIU use.

The following table details the shelf and circuit pack arrangement of the EAIU hardware components.

EQL	Component Name	Component Number
083 and 108	**RCOMDAC**	DAC624B
133, 158, 183, 208, 233, 258, 283, 308, 333, 363, 388, 413, 438, 463, 488, 513, 538, 563, 588, and 613	**LP (0 - 19)**	LPZ100B, LPC100B, LPU116, LPU112 LPU100, TAP100, LPA400, and LPA900
563 and 613	**RG**	RGP100

8.3.4 Configuration

The EAIU connects the remote site to the host site by a transmission system. The transmission system consists of the DS1 carrier facilities, SONET MUX, STS1 facilities, and DNUS. When supporting the ESA operation, the EAIU is connected remotely to the host site by a BZ-RS module.

The following table details the configuration of the EAIU.

Circuit Pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
RCOMDAC	DS1	SONET MUX	ACT	Simplex
	BITS bus	External timing reference		
	T1/E1	BZ-RS		
LP U, Z, C	32-bit bus	RCOMDAC	ACT	Simplex
	RGB	RG		
LP TAP	Backplane	LP U, Z, or C	ACT	Simplex
RG	RGB	LP	ACT	Simplex
BZ-RS	T1/E1	RCOMDAC	ACT	Simplex
		Host Switch		

8.3.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the EAIU components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
EAIU (Service Groups), COMDAC	One side	Major	Reduces the possibility for call completion by 50 percent.	Reduces the capacity of the EAIU by 50 percent.
	Both sides	Critical	Removes the subscriber lines that connect to the out-of-service EAIU.	Reduces call processing capacity.
LP	One-circuit pack	Major	**LP**: Removes up to 32 subscriber lines from service. **LC**: Removes one	**LP**: Reduces call processing capacity. **LC**: No impact.

			subscriber line from service. **TP**: No impact.	**TP**: Reduces testing capability.
	Multiple-circuit packs	Critical	**LP**: Removes up to 32 additional subscriber lines per circuit pack. **TP**: No impact.	**LP**: Further reduces call processing capability. **TP**: Further reduces testing capability.
RG	One-circuit pack	Major	No impact.	Increases the time necessary to complete calls.
	Multiple-circuit packs	Critical	Stops call termination in up to three EAIUs.	Reduces call processing capacity.

In normal operation, the relays of the EAIU with ESA shall be set such that the primary facilities simply pass through the ESA distribution panel, as shown in Figure 8-3 .

Figure 8-3 EAIU with ESA Configured In Normal Operation

The following table details the impact on subscriber service and switch performance when the EAIU components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
EAIU (Service Groups), COMDAC	One side	Major	Reduces the possibility for call completion by 50 percent.	Reduces the capacity of the EAIU by 50 percent.
	Both sides	Critical	Removes the subscriber lines that connect to the out-of-service EAIU.	Reduces call processing capacity.
LP	One-circuit pack	Major	**LP**: Removes up to 32 subscriber lines from service.	**LP**: Reduces call processing capacity.

			LC: Removes one subscriber line from service. **TP**: No impact.	**LC**: No impact. **TP**: Reduces testing capability.
	Multiple-circuit packs	Critical	**LP**: Removes up to 32 additional subscriber lines per circuit pack. **TP**: No impact.	**LP**: Further reduces call processing capability. **TP**: Further reduces testing capability.
RG	One-circuit pack	Major	No impact.	Increases the time necessary to complete calls.
	Multiple-circuit packs	Critical	Stops call termination in up to three EAIUs.	Reduces call processing capacity.

In emergency mode of operation, the switches (relays) are activated in the manner depicted in Figure 8-4 .

Figure 8-4 ESA Operation The BZ-RS will use two T1/E1 port in order to connect a primary facility one per RCOMDAC and another pair of T1/E1 port in order to monitor the Host side of the affected links. The connection of the BZ-RS module to the corresponding host side links allows the BZ-RS to detect when stable transmission from the host switch is reestablished. On taking over the primary facilities, the BZ-RS must match the facilities impedance since the BZ-RS now terminates them. Only primary transmission facilities from any EAIU shelf are connected to the detachable distribution panel associated with the BZ-RS. Secondary facilities shall not be connected to the BZ-RS at all. The secondary links are only available when the system is operating in normal mode, or used during emergency standalone operations, to maintain existing stable calls.

8.3.6 Detailed Description

The following table details the functions of the circuit packs in the EAIU with ESA operation.

Circuit Pack	Function
RCOMDAC	Routes control messages and subscriber data between application packs and the MCTSI that contains the T1 interface.
LP	Connects between 16 and 32 subscriber lines. **LC (Diagnosable circuit in the LP)**: Connects one subscriber line. **Test Pack** : Provides metallic test access to test subscriber lines.
RG	Provides power ring for analog lines in up to three EAIUs.
BZ-RS	Provides the emergency standalone mode capability for the EAIU when all primary communication access to the host switch is severed for any reason.

8.3.7 Functional Description

8.3.7.1 Functions

The EAIU connects subscriber lines to the SM-2000 through a DNUS by the PCT links.

The EAIU in ESA mode connects subscriber lines to the BZ-RS by T1/E1 then to the Host switch by T1/E1.

8.3.7.2 Operation

Figure 8-5 depicts the operation of the EAIU.

Figure 8-5 EAIU Block Diagram

The following table details the operation of the EAIU.

The EAIU handles analog and digital subscriber signals from the distribution frame.

Stage	Description
1	The LP (LPZ100-analog) or (LPU100-digital) receives a signal from the distribution frame by a cable pair.
2	The LP sends a control message to the RCOMDAC by the backplane.
3	The RCOMDAC receives the message from the LP by the backplane.

4	The RCOMDAC sends the message to the TSI, SMP, or PSU through the DNUS by the transmission system.

The EAIU handles analog and digital subscriber signals from the MCTSI.

Stage	Description
1	The RCOMDAC receives control messages from the DNUS by the transmission system.
2	The RCOMDAC sends the messages to the LP by the backplane.
3	The LP receives the message from the RCOMDAC by the backplane.
4	The LP tests the line and sends the messages to the RCOMDAC by the backplane.
5	The RCOMDAC receives and sends the messages from the LP to the TSI, SMP, or PSU through the DNUS by the transmission system.

Figure 8-6 depicts the operation of the EAIU with Emergency Stand Alone (ESA) mode.

Figure 8-6 ESA System Operation

The ESA system is a physically separate entity not located within the EAIU. When the RCOMDACs detect the loss of **BOTH** primary facilities to an EAIU, the RCOMDACs will switch the primary facilities to the ESA system. The ESA system then takes over control of the EAIU. The ESA system will monitor the integrity of the primary *5ESS*® facilities and when ONE facility to the EAIU becomes active the ESA system notifies the RCOMDAC. At this time the RCOMDAC will start direct communication with the host switch and transition back to normal operation.

Stable calls in the secondary facilities will be maintained during ESA, but new calls using secondary facilities will not be supported

8.4 Integrated Digital Carrier Unit (IDCU)

8.4.1 Basic Description

The Integrated Digital Carrier Unit (IDCU) is a five-circuit pack component that is located in the Line Trunk Peripheral (LTP) Cabinet or the Switching Module Control (SMC) Cabinet of the Switching Module (SM).

The primary job of the IDCU is to provide a direct interface for digital lines, ISDN lines, and DS1s terminating on the *5ESS*® Switch.

8.4.2 Electrical Power

The 429AA Control and Display pack controls the DC power for the Integrated Digital Carrier Unit (IDCU) shelf.

8.4.3 Shelf and Circuit Pack Arrangement

The Integrated Digital Carrier Unit (IDCU) occupies one equipment shelf and is located in the Line Trunk Peripheral (LTP) Cabinet or the Switching Module Control (SMC) Cabinet of the Switching Module (SM).

The table below details the shelf and circuit pack arrangement of the IDCU hardware components.

EQL	Component Name	Component Number
SG0: 037 SG1:145	**PTI**	KBN6
SG0: 056 SG1:136	**CCP**	UN359
SG0: 068,078 SG1:112, 122	**LSI**	TN1670
SG0: 085 SG1:097	**ELI**	KBN7
SG0: 014 SG1:176	**PCDC**	429AA

8.4.4 Configuration

The table below details the configuration of the Integrated Digital Carrier Unit (IDCU).

Circuit Packs	Link/Bus	Connected to ...	Method of Operation	State of Operation	Service Groups
LSI	IDB ICB	PTI	Dual Duplex	ACT/STBY	0,1
	Tip and Ring	ELI			
PTI	PIDB	MCTSI	Duplex	ACT/ STBY	
	DPIDB	PSU			
	ICB IDB	LSI			
ELI	Tip and Ring	LSI	Dual Simplex	ACT/ ACT	
CCP	PICB	MCTSI	Duplex	ACT/ STBY	
	Common Control Bus	PTI			
	Update Bus	CCP		ACT	
PCDC	Backplane	IDCU	Duplex	ACT/ ACT	

8.4.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the Integrated Digital Carrier Unit (IDCU) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
IDCU	One side	Minor	No impact	No impact
	Both sides	Major	Loss of service to all subscribers on SLCs connected to IDCU unit	Switch call processing reduced
LSI	One side	Minor	No impact	No impact
	Both sides	Major	Loss of service to all subscribers on SLCs connected to IDCU unit	Switch call processing reduced
ELI	One side	Minor	Loss of service to all subscribers on SLCs connected to OOS ELI	Switch call processing reduced
	Both sides	Major	Loss of service to all subscribers on SLCs connected to IDCU unit	Switch call processing reduced

8.4.6 Detailed Description

The table below details the functions of the circuit packs in the Integrated Digital Carrier Unit (IDCU):

Part	Function
IDCU	Interface on the SM that provides integrated access to digital loop carrier (DLC) systems.
LSI	Collects DS1 performance-monitoring data and detects DS1 failures and alarms.
ELI	Splits the received DS1 signals to active/standby LSIs and combines the transmitted DS1 signals.
PTI	Monitors incoming signaling to detect originations and transmits idle signaling.
CCP	Controls the PTI, and controls the LSI through the PTI.

8.4.7 Functional Description

8.4.7.1 Functions

The Integrated Digital Carrier Unit (IDCU):

- Terminates digital lines using a TR008 interface.
- Terminates ISDN lines using a TR303 interface.
- Terminates non-switched DS1s using the PUB43801 format.

8.4.7.2 Operation

The IDCU converts different data protocol signals to the data protocol used in the *5ESS*® Switch.

- The Figure 8-7 depicts the operation of the IDCU.

Figure 8-7 IDCU Block Diagram

- The table below details the operation of the IDCU.

Stage	Description
1	Incoming digital signals (T1) from DS1s received from TR 008, TR303, or PUB43801 at ELI.
2	Digital signals are sent to active and standby LSIs.
3	LSI converts DS1 Time Slots to Interface Data Bus format (IDB) and sends the time slots on to the PTI.
4	PTI further converts IDB format signals to PIDB format used in the *5ESS*® Switch.
5	The PTI switches the signals to the appropriate destinations using its own TSI. - PTI sends control signals through the CCP to the MCTSI - PTI sends data signals to MCTSI via PIDB - PTI sends Data to the PSU2 via DPIDB

	□ PTI may "hairpin" signals, sending them out immediately to another port on the same IDCU without sending them through to the TSI in the SM.

8.5 Integrated Services Line Unit, Model 2 (ISLU2)

8.5.1 Basic Description

The Integrated Services Line Unit, Model 2 (ISLU2) is a multi-shelf unit. The ISLU2 is located in a switching module.

The primary job of the ISLU2 is to connect digital subscriber lines to the *5ESS*® switch.

8.5.2 Electrical Power

The Power Converter circuit packs control power for the Integrated Services Line Unit, Model 2 (ISLU2). The power converter packs are located in the Common shelf.

8.5.3 Shelf and Circuit Pack Arrangement

The Integrated Services Unit Model 2 (ISLU2) is located in the switching module cabinet.

The table below details the shelf and circuit pack arrangement of the ISLU2 hardware components.

EQL		Component Name	Component Number
Horizontal	**Vertical**		
Various	010, 118, 026, 164, 172, and 180	**(E)HLSC**	TN1412
Various	032, 038, 150, and 156	**MAN**	TN1676
Various	054 and 144	**Power Converter**	495NA
Various	060, 068, 118, and 126	**CD**	UN361
Various	084 and 102	**CCP**	UN359
Various	076 and 104	**CCI**	UN360
Various	Various	**LBD**	MPT/MPU

8.5.4 Configuration

The Integrated Services Line Unit, Model 2 (ISLU2) consists of four to six shelves that include a common shelf, fan unit shelf, and two to four line shelves.

The table below details the configuration of the ISLU2.

Circuit packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
HLSC	PCADB	CCP	ACT	Simplex
MAN	PCADB	CCP		
	Backplane	HLSC		
CCI	PICB	MCTSI	ACT or ACT/STBY	Simplex or Duplex
	PCADB	CCP		
	Backplane	HLSC		
CCP	PCADB	MAN	ACT or ACT/STBY	Simplex or Duplex
		HLSC		
	Backplane	CCI		
	CIDB	CD		
CD	PIDB	TSI	ACT	Simplex
	CIDB	CCP		
	LIDB	LBD		
	DPIDB	PSU		
LBD	LIDB	CD	ACT	Simplex
	Backplane	HLSC		
	SPARE	MAN		
	TEST			
	Metallic wire	MDF		

8.5.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the diagnosable components of the Integrated Services Line Unit, Model 2 (ISLU2) are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
ISLUCC	One side	Major	May reduce the possibility for call completion by 50 percent*	May reduce the call processing capacity of the ISLU2 by 50 percent*
	Both sides	Critical	Removes the subscriber lines from service	Reduces call processing capacity
ISLUCD	One side	Major	Reduces the possibility for call completion by 50 percent	Reduces the call processing capacity of the ISLU2 by 50 percent
	Both sides	Critical	Removes the subscriber lines from service	Reduces call processing capacity
ISLUMAN	One side	Major	No impact	No impact
	Both sides	Critical	No impact	Reduces ability of the *5ESS*® switch to test subscriber lines and provide a spare line board
ISLUHLSC	One pack	Major	Reduces call processing capacity	Increases the time necessary to respond to call requests
	Multiple	Critical	As the number of faulty circuit packs increases, then call processing decreases	Decreases call processing capacity
LBD	One pack	Major	Removes eight subscribers from service	Reduces call processing capacity
	Multiple packs	Major	Removes the eight additional subscribers per circuit pack that is connected to the out-of-service LBD	Further reduces call processing capacity
* When the ISLU operates in the ACT/STBY mode, then the loss of one side does not impact capacity or service.				

8.5.6 Detailed Description

The table below details the functions of the diagnosable components in the Integrated Services Line Unit, Model 2 (ISLU2).

Part	Function
HLSC	Tests 2-wire subscriber lines
MAN	□ Provides the Metallic Access Network for testing subscriber lines □ Enables technicians to use the poke commands to remotely substitute a spare line-card pack
CC	Routes control messages between MCTSI and ISLU2 circuit packs □ **CCI (circuit pack)** Connects the CCP to the MCTSI □ **CCP (circuit pack)** Generates and handles call processing control messages and maintenance control messages
CD	

	□ Routes subscriber data between the MCTSI and ISLU2 □ Routes call processing control messages between the ISLU2 and PSU
LBD	Connects subscriber lines to the ISLU2 □ U-Card: Connects subscriber lines via a 2-wire BRI □ T-Card: Connects subscriber lines via a 4-wire BRI **LCKT (diagnosable circuit in the LBD)** Connects one subscriber line to the ISLU2

8.5.7 Functional Description

8.5.7.1 Functions

The Integrated Services Line Unit Model 2 (ISLU2) connects digital subscriber lines to the *5ESS*® switch.

8.5.7.2 Operation

The ISLU2 interacts with other components to operate the switch.

□ The Figure 8-8 depicts the operation of the ISLU2.

Figure 8-8 ISLU2 Block Diagram

□ The tables below details the operation of the ISLU2.

The ISLU2 handles subscriber signals from the MDF for an originating call.

Stage	Description
1	The LBD receives a signal from the MDF via a cable pair.
2	The LBD sends the signal to the CD via the LIDB.
3	The CD receives and sends a control message to:

	□ the CC via the CIDB, and □ the PSU via the DPIDB.
4	The CC receives the control message from the MCTSI through the PSU via the PICB.
5	□ When the message relates to the T-card, then the CC sends the message to the CD via the PCADB. □ When the message relates to the U-card, then the CC sends the message to the HLSC via the PCADB.
6	The HLSC tests the line and sends the message to the CC via the PCADB.
7	The CC sends the message to the CD via the PCADB.
8	The CD receives the message to connect the subscriber lines via the LIDB from the CC.
9	The CC sends the message to the MCTSI via the PIDB.

The ISLU2 handles subscriber data and control messages from the MCTSI for a call connecting to another customer.

Stage	Description
1	The CC receives a control message from the MCTSI via the PICB.
2	□ When the message relates to the T-card, then the CC sends the message to CD via the CIDB. □ When the message relates to the U-card, then the CC sends the message to the HLSC via the PCADB.
3	The HLSC: □ Receives the message, □ Tests the line, and □ Sends a message to the CC via the PCADB.
4	The CC sends the message to the CD via the CIDB.
5	The CD sends the message to the LBD via the LIDB.
6	The LCKT in the LBD sends the message to the MDF via a metallic wire.
7	When the subscriber answers, then the LCKT receives data from the MDF via a metallic wire.
8	The LBD sends the message to the CD via the LIDB.
9	The CD sends the message to: □ the CC via the PCADB, and □ the PSU via the DPIDB.

8.6 Line Unit, Model 3 (LU3)

8.6.1 Basic Description

The Line Unit Model 3 (LU3) is a two shelf unit. The LU3 is located in an LTP cabinet of an SM or SM-2000.

The primary job of the LU3 is to connect local analog subscriber lines to the *5ESS*® switch.

8.6.2 Electrical Power

The power converter circuit packs supply power to the Line Unit Model 3 (LU3). The circuit packs are located in the LU3 shelf of SG 0 and SG 1.

8.6.3 Shelf and Circuit Pack Arrangement

Each Line Unit Model 3 (LU3) is located in an LTP cabinet of an SM or SM-2000. Each cabinet may contain one to three LU3 shelves.

The table below details the shelf and circuit pack arrangement of the LU3 hardware components.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
Various	008	**Power Converter**	494GB
Various	016, 024, and 032	**HLSC**	TN844 and TN844B
Various	042, 050, 058, and 066	**CHBD**	335C
Various	074	**COMC**	UN322 and UN322B
Various	084	**GDXACC**	TN831 and TN831B
Various	092	**GDX Access & Power Circuit**	TN832 and TN832B
Various	100, 108, 116, 124, 132, 140, 148, 156, 164, and 172	**BD**	TN1048, TN1058, and TN1058B

8.6.4 Configuration

The table below details the configuration of the Line Unit Model 3 (LU3).

Circuit pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
HLSC	Backplane	GDXACC	Simplex	ACT
	Backplane	COMC		
BD	B-Link	GDXACC	Simplex	ACT
	House cable	MDF		
GDXACC	C-Link	CHBD	Simplex	ACT
	MTB	MMSU		
	Backplane	BD		
	Backplane	HLSC		
CHBD	Backplane	COMC	Simplex	ACT
	C-link	GDXACC		
COMC	PIDB/ PICB	MCTSI	Simplex	ACT
	Backplane	CHBD		

8.6.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the diagnosable components of the Line Unit Model 3 (LU3) are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
HLSC, CHBD, COMC, and GDXACC	One Circuit pack	Major	No impact	Increases the time necessary to return dial tone
	Multiple Circuit packs	Critical	As the number of faulty circuit packs increases, call processing decreases	Decreases call processing capacity of the SM
BD	One circuit pack	Major	Removes 32 subscriber lines from service	Reduces call processing capacity of the SM
	Multiple circuit packs	Major	Removes 32 additional subscribers per circuit pack that is impacted	Further reduces call processing capacity of the SM

8.6.6 Detailed Description

The table below details the functions of the individually diagnosable components in the Line Unit Model 3 (LU3).

Part	Function
COMC	Routes control messages and subscriber data between the LU3 circuit packs and the MCTSI
GDX ACC	Connects the BD to the CHDB and/or HLSC in the LU3 or the MMSU
CHBD	□ Converts analog signals from the BD to digital signals □ Converts digital signals from the COMC to analog signals
HLSC	□ Tests subscriber lines □ Generates ringing current
BD	□ Connects subscriber cable pairs to the GDXACC □ Scans the subscriber line for a change of state from idle to busy

8.6.7 Functional Description

8.6.7.1 Functions

The Line Unit Model 3 (LU3):

□ Connects up to 640 analog subscriber lines to the *5ESS*® switch.

8.6.7.2 Operation

The LU3 interacts with other components to operate the switch.

□ The Figure 8-9 depicts the operation of the LU3.

Figure 8-9 LU3 Block Diagram

- The table below details the operation of the LU3.

The LU3 handles subscriber signals from the MDF.

Stage	Description	
1	The BD receives signals from the MDF via a cable pair.	
2	The BD sends the signals to the COMC via the backplane.	
3	The COMC receives and sends the messages from the BD to the MCTSI via the PICB.	
4	The COMC receives the messages from the MCTSI via the PICB.	
5	The COMC sends the messages to the BD, GDX ACC, and HLSC via the backplane.	
6	The BD, GDX ACC, and HLSC receive messages from the COMC via the backplane.	
7	**When**	**Then**
	The BD receives the message,	The BD closes the A-link and B-link gates.
	The GDX ACC receives the message,	The GDX ACC closes the HLSC and B-link gates.
	The HLSC receives the message,	The HLSC tests the line and sends a message to the COMC via the backplane.
8	The COMC receives and sends the message from the HLSC to the GDXACC via the backplane.	
9	The GDXACC receives the message from the COMC, opens the HLSC gate, closes the CHBD gate, and sends the message to the CHBD via the backplane.	
10	The CHBD receives and sends the message from the GDXACC to the COMC via the backplane.	
11	The COMC receives and sends the message from the CHBD to the MCTSI via the PIDB.	

The LU3 handles subscriber data and control messages from the SMP.

Stage	Description	
1	The COMC receives control messages from the MCTSI via the PICB and subscriber data from the MCTSI via the PIDB.	
2	The COMC sends the messages to BD, GDX ACC, and HLSC.	
	When	**Then**
	The BD receives the message,	The BD closes the A-link and B-link gates, and sends the message to the GDXACC, CHBD and HLSC via the backplane.
	The GDXACC receives the message,	The GDXACC closes the B-link to the HLSC gates

		and B-link to the CHBD gates.
	The HLSC receives the message,	The HLSC tests the line, and sends a message to the COMC via the backplane.
3	The COMC receives and sends the message from the HLSC to the MCTSI via the PICB.	

8.7 Packet Switching Unit, Model 2 (PSU2)

8.7.1 Basic Description

The Packet Switch Unit Model 2 (PSU2) is a one to five shelf unit. The PSU2 is located in an LTP cabinet of a switching module.

The PSU2 contains individually diagnosable components that include, the PSUCOM and PSUPH.

The PSU2 supports the following:

- routing packets of control messages and subscriber data to ISDN lines,
- wireless 2G/3G call routing and packet processing,
- Signaling System 7 (SS7) signaling for circuit trunks, and
- Session Initiation Protocol (SIP) signaling for Internet Protocol (IP) packet trunks.

8.7.2 Electrical Power

A power converter circuit in each Packet Switch Unit Model 2 (PSU2) circuit pack controls power for the circuit pack.

8.7.3 Shelf and Circuit Pack Arrangement

The Packet Switch Unit Model 2 (PSU2) is located in an LTP or SMC cabinet of a switching module.

The following table details the shelf and circuit pack arrangement of the PSU2 hardware components.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
Various	006, 014, 022, 030, 038, 046, 054, 062, 128, 136, 144, 152, 160, 168, 176, and 184	**PH3**	TN1367C
		PH4	TN1846
		PHV1	TN1844
		PHV2	TN1856
		PHV3	TN1862
		PHV4	TN1863
		PHV5	TN1891
		PHA1	TN1845
		PHA2*	TN113
		PH22**	TN1873
		PH31	TN13
		PHE2***	
		PH33	TN113
Various	070 and 120	**CF2******	TN1843
Various	078 and 110	**PF2**	UN396
Various	088 and 100	**DF-FLEX**	UN192B
		DFMP-FLEX	UN399
		DF2	UN592

NOTE: *******The PHA2 definition includes the TN113 and LLE1 OC3 Paddleboard which is located on the backplane.

********A 10 power feeder MFFU (J5D003FJ-1, List 161) configuration is required when the LTP cabinet is equipped with five PSU2 shelves and one or more of the PSU2 shelves are equipped with PH22 packs.

*********The PHE2 definition includes the TN13 and LLE2 100BaseT Ethernet Paddleboard which is located on the backplane.

********Located in the Basic shelf only.

8.7.4 Configuration

The following table details the configuration of the Packet Switch Unit Model 2 (PSU2).

Circuit Pack*	Link/ Bus	Connects to...	Method of Operation	State of Operation
CF2	PICB	MCTSI	ACT/STBY	Duplex
	PB			
	PIB	PF2		
	CIB	PF2		
		DF-FLEX		
		DFMP-FLEX		
		DF2		
DF-FLEX	PHDB	PH	ACT/STBY	Duplex
	DPIDB	ISLU2		
		AIU		
		IDCU		
	PIDB	MCTSI		
	CIB	CF2		
DFMP-FLEX	PHDB	PH	ACT/STBY	Duplex
	PIDB	MCTSI		
	CIB	CF2		
DF2	PHDB	PH	ACT/STBY	Duplex
	CIB	CF2		
	PCT Link	MCTSI		
PF2	CIB	CF2	ACT/STBY	Duplex
	PIB			
	PB	PH		
	CB			
PH	PHDB	DF-FLEX	ACT**	N+K
		DFMP-FLEX		
		DF2		
	PB	PF2		
	CB			

NOTE: *****For a detailed functions of the diagnosable components in the PSU2, go to the PSU Detailed Description section 8.7.6 .

******PH hardware with a logical channel group assigned is ACT. In-service spare PH hardware, if it exists, with no logical channel group assigned, is STBY. Sparing strategy differs in different applications.

8.7.5 Service Impacts

The following tables detail the impact on subscriber service and switch performance when the Packet Switch Unit Model 2 (PSU2), or packs within the PSU2, are not available.

Unit Unavailable		Service Impact	Switch Impact
PSUCOM	One side	No impact. System operates in Simplex mode.	No impact. PSUCOM side OOS.
	Both sides	Removes all ISDN subscriber lines connected to the impacted PSU2 from service, and/or Reduces call processing for trunks that are connected to the out-of-service PSU2, and/or Removes wireless calls associated with the impacted PSU2.	Reduces ISDN call processing capacity, and/or Reduces SS7 trunk signaling/SIP signaling capacity. In the impacted GSM it removes: all SS7 signaling links from service, CCSQPH pipes, GQPH (general QLPS protocol handler) pipes, SIP processor groups, SCTP endpoints and their associations, and/or Reduces wireless call capacity.

To understand the impacts of PHs being out-of-service (OOS), the PH sparing scheme must be understood. Depending on the PH type, N+K sparing is used, or a mated pair operation is used. N+K means there are "N" logical channels groups on a PSU2 shelf that can be assigned to a PH hardware type

and "K" spare PHs of that hardware type on that shelf, for a total of N+K physical PHs of that hardware type on the shelf. The following table details impacts caused due to PH(s) being OOS.

Unit Unavailable		Service Impact	Switch Impact
PSUPH	N+K sparing with at least one PH, spare available*****	No impact.	Physical PH OOS.
	N+K sparing - no spare available	The impact depends on the channel group type(s) OOS. Reduces ISDN call processing capacity, and/or Reduces call processing for trunks that are connected to the out-of-service circuit pack(s), and/or Reduces SS7/SIP signaling capacity, and/or Removes wireless calls associated with the impacted PH(s).	Channel group type(s) OOS. Reduces ISDN call processing capacity, and/or Reduces SS7/SIP call capacity, and/or Reduces wireless call capacity.
	Mated pair - one PH unavailable	No service impact.	Logical channel group OOS, simplex operation.
	Mated pair - both PHs unavailable******	The impact depends on the channel group type(s) OOS. Logical channel group OOS.SIP processor group(s) unavailable. SCTP endpoints and associations removed/closed.	Reduces SIP signaling capacity. Reduces SIP call processing.

NOTE: *****For the SIP-T application, N+K sparing does not apply to the PHE2.

******For wireless impacts, refer to the 235-200-100, *Flexent®/AUTOPLEX® Wireless Networks Applications OA& M Manual.*

8.7.6 Detailed Description

The following table details the functions of the diagnosable components in the Packet Switch Unit 2 (PSU2).

Diagnosable component	Function
PSUCOM	**CF2** - Routes control messages between the MCTSI and the PF2.
	DF-FLEX/DFMP-FLEX/DF2 - Switches packets of control messages and subscriber data between the PHs and MCTSI.
	PF2 - Routes packets of control messages and subscriber data between the PHs and CF2.
PSUPH	Routes packets of control messages and subscriber data between the AIU, IDCU, and ISLU2. Transports/routes SS7 signaling messages, internal SIP signaling messages, and internal maintenance packets. Processes SS7 signaling messages, SIP signaling messages and supports wireless applications.

8.7.7 Functional Description

8.7.7.1 Functions

The Packet Switch Unit Model 2 (PSU2) performs the following functions:

- routing packets of control messages and subscriber data to ISDN lines,
- wireless 2G/3G call routing and packet processing,
- Signaling System 7 (SS7) signaling for circuit trunks, and
- Session Initiation Protocol (SIP) signaling for Internet Protocol (IP) packet trunks.

NOTE: For additional information regarding PH functions when used in wireless applications, refer to the 235-200-100, *Flexent ®/AUTOPLEX® Wireless Networks Applications OA&M Manual*. For more information regarding SIP PHs, refer to the 235-200-118, *SIP for Packet Trunking OA&M Manual*. For more information regarding the SS7 PHs, refer to the 235-200-116, *Signaling Gateway Common Channel Signaling* document.

8.7.7.2 Operation

The PSU2 interacts with other components to operate the switch.

The Figure 8-10 depicts the operation of the PSU2.

Figure 8-10 PSU2 Block Diagram

The following tables detail the operation of the PSU2.

The PSU2 handles data packets for SS7 signaling from the PI2 in the SMP. The following stages describe an "Island" SS7 GSM. (The SS7 signals are used to provide a path to set up and tear down trunk calls.)

Stage	Description

1	The CF2 receives a data packet from the PI2 in the SMP over the PB.
2	The CF2 sends the packet to the PF2 by the backplane.
3	The PF2 receives and sends the packet from the CF2 to the MDPH by the backplane.
4	The MDPH receives and sends the packet to the STPH by the backplane.
5	The STPH receives and sends the packet to the DF***** by the backplane.
6	The DF***** receives and sends the packet from the STPH to the TSIS by the PIDB.
NOTE: *****The DF type can vary.	

The PSU2 handles the data packets for SS7 signaling from the TSIS. The following stages describe an "Island" SS7 GSM. (The SS7 signals are used to provide a path to set up and tear down trunk calls.)

Stage	Description
1	The DF***** receives a data packet from the TSIS by the PIDB.
2	The DF***** sends the packet to the STPH by the backplane.
3	The STPH receives and sends the packet to the PF2 by the backplane.
4	The PF2 receives and sends the packet to the CF2 by the backplane.
5	The CF2 receives and sends the packet to the PI2 in the SMP by the PB.
NOTE: *****The DF type can vary.	

The PSU2 handles the control signaling messages from the AIU, IDCU, and/or ISLU2 for B-Channel signaling.

Stage	Description
1	The DF***** receives a control signaling message from the AIU, IDCU, and/or ISLU2 by the DPIDB.
2	The DF***** sends the message to the PH by the backplane.
3	The PH receives and sends the message from the DF***** to the PF2 by the backplane.
4	The PF2 receives and sends the message from the PH to the CF2 by the PIB.
5	The CF2 receives and sends the message from the PF2 to the PI2 in the SMP by the PB.
NOTE: *****The DF type can vary.	

The PSU2 handles the data packets from the AIU, IDCU, and/or ISLU2 for B-Channel signaling.

Stage	Description
1	The DF***** receives a data packet from the AIU, IDCU, and/or ISLU2 by the DPIDB.
2	The DF***** sends the packet to the PH by the backplane.
3	The PH receives and sends the packet from the DF***** to the PF2 by the backplane.
4	The PF2 receives and sends the packet from the PH to the CF2 by the PIB.
5	The CF2 receives the packet from the PF2 and routes the packet to the appropriate destination.
NOTE: *****The DF type can vary.	

The PSU2 handles the data packets from the AIU, IDCU, and/or ISLU2 for D-Channel signaling.

Stage	Description
1	The DF***** receives a data packet from the AIU, IDCU, and/or ISLU2 by the DPIDB.
2	The DF***** sends the packet to the PH by the backplane.
3	The PH receives and sends the packet from the DF***** to the PF2 by the backplane.
4	The PF2 receives and sends the packet from the PH to the CF2 by the PIB.
5	The CF2 receives the packet from the PF2 and routes the packet to the appropriate destination.
NOTE: *****The DF type can vary.	

The PSU2 handles SIP signaling packets from the Router or Layer 2 Switch for IP packet trunk calls. This description assumes incoming messages that will be sent to an SMP.

Stage	Description
1	The (serving) SIP PH receives SIP signaling packets from the router/layer 2 switch. The packets travel over Category 5 cable to the Ethernet 100BaseT LLE2 paddle board which is located on the backplane of the SIP PH.
2	The messages are passed through the paddle board to the SIP PH.
3	The SIP PH receives and processes the SIP messages, updates the (non-serving) SIP PH with stable call information, and sends messages to the GQPH. The message transfer between PHs is over the packet bus (PB) to the Packet Fanout 2 (PF2) board. The PF2 determines the message destination and sends the message to the proper GQPH.
4	The GQPH performs additional processing of the message, and prepares the message to be sent to its' destination through the QLPS network. Once the message is formatted correctly, the GQPH inserts the message on to the protocol handler data bus (PHDB) where it is sent to the Data Fanout 2 (DF2) board.
5	The DF2 switches the message from the PHDB to a PCT link which terminates at the backplane of a TSI Slice board. The messages are switched through the TSI and sent to the QLPS network.
NOTE: For additional information regarding the SIP for Packet Trunking - NAR feature, refer to the 235-200-118, *SIP for Packet*	

Trunking - OA&M Manual.

NOTE: For operational information concerning wireless application, refer to the 235-200-100, *Flexent® AUTOPLEX® Wireless Networks Applications OA&M Manual*.

8.7.8 MCC Pages and Pokes

MCC pages 1186,Y,X and 118X,Y display poke commands for the Packet Switch Unit Model 2 (PSU2) as follows:

- MCC page 1186,Y,X
  - Y=PSU number (0 or 1 - for wireline applications 0), and
  - X=SM number (1 - 192).
- MCC page 118X,Y
  - Y=PSU number (0 or 1 - for wireline applications 0), and
  - X=Shelf number (0 - 4).

NOTE: To view the complete list of PSU2 MCC pages, refer to the 235-105-110, *5ESS® Switch System Maintenance Requirements and Tools* document.

The following table details the MCC poke commands for the PSU2.

PSU2 Poke Commands	
Poke	**Description**
PSUCOM pokes are on page 1186.	
200	Remove PSUCOM 0
201	Remove PSUCOM 1
300	Restore PSUCOM 0
301	Restore PSUCOM 1
400	Switch PSUCOM
500	Diagnose PSUCOM 0
501	Diagnose PSUCOM 1
PSUPH pokes are on pages 1180 - 1184.	
2XX	Remove PSUPH
3XX	Restore PSUPH
4XX	Switch PSUPH
5XX	Diagnose PSUPH

8.7.9 Diagnostic Phases

The following tables detail each diagnostic phase of the Packet Switch Unit Model 2 (PSU2).

NOTE: The diagnosable component, the PSUCOM, consists of the CF2, DF***** and PF2. The PSUCOM is displayed as the PSUCOM on the poke command screen.

The following table details each diagnostic phase of the PSUCOM.

Diagnose PSUCOM	
Phase	**Description**
1	Tests the PICB communication between CI and UCI chip on CF.
2	Tests UCI chip on CF.
3	Tests LP of CFs UCI chip. SMP sends messages for LP that sees messages and performs required reads and writes (to verify interrupts to LP).
4	Tests CFs LP error source registers and CRC in ROM.
5	Tests CIB between CF, PF, and DF.
6	Tests PB between CF, PF, and PI.
7	Demand phase for factory and growth testing only: Tests all DUARTS in CF for unequipped shelves.

8	Demand phase for factory and growth testing only: Tests internal CF interfaces to all unequipped PFs.
9	Demand phase for factory and growth testing only: Tests OOS lamps on equipped and growth CFs, PFs, and DFs. Diagnostic cycles through five times, starting by turning all lamps off.
10	Tests the CF2 polling ram, arbiter, and packet bus between the active and mate PIs via the CF2. (Only executed with PSU2/CF2 pack.).
11	Tests communication between CI and PF.
12	Tests LPs ROM and ability of PF to be reset.
13	Tests communication between PF and each of equipped and growth PHs.
14	Tests PB arbiter and PB connections through PF to each equipped PH.
15	Demand phase for factory and growth testing only: Tests internal communication path on PF for each unequipped PH.
16	Demand phase for factory and growth testing only: Tests internal communication path on PF for each unequipped PH.
21	Tests communication path between CI and DF, by CF.
22	Tests LPs ROM for ability of DF to be reset.
23	Performs reads and writes on DFs 8751 bus.
24	Provides a memory test for DFs parity error buffer.
25	Performs a test on DFs TSI chip.
26	Tests data paths on DF (UN192 or UN348).
27	Demand phase for factory and growth testing only: Tests data paths between DF and STBY CD board by DPIDBs.
28	Tests the PLI associated with any DF2 equipped in the PSUCM under test.
29	Tests the DFTS and PCTLI devices resident on the DF2 circuit pack.
30	Tests interdevice connections, timing circuitry and PHDB connections from a DF2 to equipped PH's.

The following tables detail each diagnostic phase of the PSUPH.

Diagnose PSUPH	
Phase	**Description**
1	Tests interface between ACT PF and PH under test. This includes CB and PB leads.
2	Tests PP side of PH board.
3	Tests DMA processor side of PH board.
4	Tests PHDB interfaces from each RA chip to ACT DF.
5	Tests interfaces between STBY PF and PH under test.
90	Demand phase only: Tests full range of memory using a high-coverage memory algorithm.
91	Demand phase only: Runs stress tests on SPORT chip (for TN1371).
92	Demand phase only: Reruns Phase 2 for better fault resolution (for TN1371).
93	Demand phase only: Reruns Phase 3 for better fault resolution (for TN1371).

Diagnose PSUPH (PH31)	
Phase	**Description**
1	Used to verify the interface between the active PF2, active CF2, standby PF2, standby CF2 and the protocol handler powerPC (PHPPC) under test. This includes the control signal leads, the packet bus signal leads, interrupt signal leads, and side select signal leads. This phase also tests the PHPPC reset capability and the protocol handler data bus (PHDB) between the PHPPC and the DF2.
2	Used to verify circuitry on the PHPPC that is common to all PowerPC-based protocol handlers. This includes tests for the PHPPC SDRAM, MPC755 processor, Exception Handling, MPC107 and CUB, PCI, PBMAX, memory management unit (MMU), and the Data and Instruction Caches.
3	Used to verify circuitry on the PHPPC that is common to all PH30-based PowerPC protocol handlers. This includes tests for the PH30 PCI interfaces, the Network Processor-to-PBMAX Interface, the Network Processor FPGA, the Network Processor's 8 Mb of SRAM, and the Network Processor's 128 Mb of SDRAM.
4	Used to verify circuitry on the PHPPC that is specific to the PH31 application. This includes tests for the PH31 Application Network Processor and to verify that a paddle board is not connected to the PH31.
5	(DEMAND ONLY PHASE) Used as a demand phase for all PHPPC circuit packs and is used to verify circuitry on the PHPPC that is common with all PowerPC-based protocol handlers that cannot run in an automatic phase but are able to run in a demand phase. This phase will do a memory test of the entire SDRAM on the PHPPC under test and takes up to 20 minutes to run.
6	(DEMAND ONLY PHASE) Used as a demand phase for PH31 and tests PH31 circuitry that could ***not*** be tested during an automatic phase.

Diagnose PSUPH (PH33 - GQPH)	
Phase	**Description**
1	Verifies the interface between the active PF2, active CF2, standby PF2, standby CF2 and the Protocol Handler PowerPC (PHPPC) under test. This includes the control signal leads, the packet bus signal leads, interrupt signal leads, and side select signal leads. This phase also tests the

	PHPPC reset capability and the Protocol Handler Data Bus (PHDB) between the PHPPC and the DF2.
2	Verifies circuitry on the Protocol Handler PowerPC (PHPPC) that is common with all PowerPC based Protocol Handlers. This includes tests for the PHPPC SDRAM, MPC755 processor, Exception Handling, MPC107 and CUB, PCI, PBMAX, Memory Management Unit (MMU), and Data and Instruction Caches.
3	Verifies circuitry on the Protocol Handler PowerPC (PHPPC) that is common with all PH30 based PowerPC Protocol Handlers. This includes tests for the PH30 PCI interfaces, the Network Processor to PBMAX Interface, the Network Processor FPGA, the Network Processor's 8MBytes of SRAM, and the Network Processor's 128MBytes of SDRAM.
4	Verifies circuitry on the Protocol Handler PowerPC (PHPPC) that is specific to the PH33 application. This includes tests for the PH33 Application Network Processor and a test to verify that a paddleboard is not connected to PH33.
5	(DEMAND ONLY PHASE) for all Protocol Handler PowerPC (PHPPC) circuit packs. Verifies circuitry on the Protocol Handler PowerPC (PHPPC) that is common with all PowerPC based Protocol Handlers that cannot run in an automatic phase but will be able to run in a demand phase. This phase will do a memory test of the entire SDRAM on the PHPPC under test.
6	(DEMAND ONLY PHASE) for the PH33. Tests the PH33 circuitry that was ***not*** testable during an automatic phase.

Diagnose PSUPH (PHE2 - SIP PH)	
Phase	**Description**
1	Verifies the interface between the active PF2, active CF2, standby PF2, standby CF2 and the Protocol Handler PowerPC (PHPPC) under test. This includes the control signal leads, packet bus signal leads, interrupt signal leads, and side select signal leads. This phase also tests the PHPPC reset capability and the Protocol Handler Data Bus (PHDB) between the PHPPC and the DF2.
2	Verifies circuitry on the Protocol Handler PowerPC (PHPPC) that is common with all PowerPC based Protocol Handlers. This includes tests for the PHPPC SDRAM, MPC755 processor, Exception Handling, MPC107 and CUB, PCI, PBMAX, Memory Management Unit (MMU), and Data and Instruction Caches.
3	Verifies circuitry on the Protocol Handler PowerPC (PHPPC) that is common with all PH30 based PowerPC Protocol Handlers. This includes tests for the PH30 PCI interfaces, the Network Processor to PBMAX Interface, the Network Processor FPGA, the Network Processor's 8MBytes of SRAM, and the Network Processor's 128MBytes of SDRAM.
4	Verifies circuitry on the Protocol Handler PowerPC (PHPPC) that is specific to the PHE2 application. This includes tests for the PHE2 Application Network Processor, the PHE2 Paddle Board, and an Ethernet Ping test.
5	(DEMAND ONLY PHASE) for all Protocol Handler PowerPC (PHPPC) circuit packs. Verifies circuitry on the Protocol Handler PowerPC (PHPPC) that is common with all PowerPC based Protocol Handlers that cannot run in an automatic phase but will be able to run in a demand phase. This phase will do a memory test of the entire SDRAM on the PHPPC under test.
6	(DEMAND ONLY PHASE) for the PHE2. Tests PHE2 circuitry that was ***not*** testable during an automatic phase. This includes Manual Ethernet Loop around tests.

9. SWITCHING MODULE PERIPHERAL TRUNK UNITS

9.1 DIGITAL LINE and TRUNK UNIT, MODEL 2 (DLTU2)

9.1.1 Basic Description

The Digital Line and Trunk Unit, Model 2 (DLTU2) is a one shelf, multi-circuit pack component. The DLTU2 is located in an SM or SM-2000 cabinet (SMC or LTP).

The primary job of the DLTU2 is to connect a switching module to a digital carrier facility.

9.1.2 Electrical Power

The SN346 Manual Power Start or SN730 Automatic Power Start Circuit Pack supplies power to the DFI circuit packs in the Digital Line and Trunk Unit, Model 2 (DLTU2) shelf. The power circuit packs are located at the left end of the DLTU2.

9.1.3 Shelf and Circuit Pack Arrangement

The table below details the shelf and circuit pack arrangement of the Digital Line and Trunk Unit, Model 2 (DLTU2) hardware components.

EQL	Component Name	Component Number
006	**Power Start**	SN346B or SN730
022, 038, 054, 070, 086, 112, 128, 144, 160, 176	**DFI2**	TN1611, TN1611B
		TN1612, TN1612B

9.1.4 Configuration

The table below details the configuration of the Digital Line and Trunk Unit, Model 2 (DLTU2).

Circuit pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
DFI2	PICB	MCTSI	Duplex	ACT/ STBY
	PIDB			
	T1-0-IN and T1-0-OUT	DSX	Simplex	ACT
	T1-1-IN and T1-1-OUT			
	FIDB	FIU*	Duplex	ACT/ STBY
*RSM only				

9.1.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the diagnosable components of the Digital Line and Trunk Unit, Model 2 (DLTU2) are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
DFI2	One T-Carrier	Major	May deny subscriber service.	Reduces call processing capacity.
	Both T-Carriers	Major		
DFI	One T-Carrier	Major	May deny subscriber service.	Reduces call processing capacity.
RRCLK and/or DFI slot 22 and DFI slot 32	One side	Major	No impact.	No impact.
	Both sides	Major	Stops all call processing.	Reduces call processing capacity.
* Go to office records to determine what carrier systems are impacted. **The Host DLTU-R may handle two times more calls than the Remote DLTU-R.				

9.1.6 Detailed Description

The table below details the components of the Digital Line and Trunk Unit, Model 2 (DLTU2).

Circuit Packs	Function
DFI 2	Converts the format of control and data signals between the *5ESS*® switch and the carrier.

The table below details the connections of the DFI circuit packs. Each DFI at the host site connects to a second DFI that is located at a remote site.

Circuit Pack	DFI2 Connection
TN1611	Connects up to 48 inter-office trunks.
TN1612	Connects the RSM to the HSM. Connects up to four switching modules in a RSM.

9.1.7 Functional Description

9.1.7.1 Functions

The Digital Line and Trunk Unit, Model 2 (DLTU2):

- Connects the switching modules to the digital carrier facilities.
- Carries and generates clock pulses.

9.1.7.2 Operation

The DLTU2 interacts with other components to operate the switch.

- The Figure 9-1 depicts the operation of the DLTU2.

Figure 9-1 DLTU2 Block Diagram

- The table below details the operation of the DLTU2.

  The DFI in the DLTU2 shelf handles data signals from the far-end switching office, RSM, or RISLU. The DFI also handles data signals between 2 RSMs.

Stage	Description
1	The DFI receives a data signal from the DSX via the ABAM cable.
2	The DFI converts and splits the signal into a data and control message.
3*	- When the message is a control message, then the DFI sends the message to the MCTSI via the PICB. - When the message is subscriber data, then the DFI sends the message to the MCTSI via the PIDB.
*When the DLTU is located in a, RSM, then the RDFI sends the message through the RLI to the MCTSI.	

The DFI in the DLTU2 shelf handles control messages and subscriber data from the MCTSI.

Stage	Description
1*	The DFI receives both: - a control message from the MCTSI via the PICB, and - subscriber data from the MCTSI via the PIDB.
2	- When the DFI receives a control message, then the DFI either executes or sends the message to the DSX via the ABAM. - When the DFI receives subscriber data, then the DFI converts and sends the message to DSX via the ABAM.
*When the DLTU is located in a RSM, then the RDFI sends the message through the RLI to the MCTSI.	

9.2 Digital Network Unit - SONET (DNU-S)

9.2.1 Basic Description

The Digital Network Unit - SONET (DNU-S) is a shelf unit. The DNU-S is located in an SM-2000 cabinet (LTP).

The DNU-S contains individually diagnosable components that include:

- SFI,
- TMUX,
- CD, and
- CC

The primary jobs of the DNU-S are to:

- Connect the SONET equipment to the *5ESS*® switch for call processing in subscriber lines and trunks, and

- Converts control messages and subscriber data to a format that is compatible with the *5ESS*® switch equipment.

9.2.2 Electrical Power

A power converter circuit in each Digital Network Unit - SONET (DNU-S) circuit pack controls power for the circuit pack.

9.2.3 Shelf and Circuit Pack Arrangement

The Digital Network Unit - SONET (DNU-S) is located in an SM-2000 cabinet (LTP).

The following table details the shelf and circuit pack arrangement of the DNU-S hardware components.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
Various	002, 008, 180, 186	**SFI**	KTU2
Various	016, 024, 032, 040, 048, 056, 132, 140, 148, 156, 164, 172	**TMUX**	KTU1
Various	064, 124	**TMUX (Spare)**	KTU1
Various	072, 080, 106, 114	**CD**	KLU3
Various	088, 098	**CC**	KLU2

9.2.4 Configuration

The following table details the configuration of the Digital Network Unit - SONET (DNU-S).

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
SFI	TIDBs	TMUX	Duplex	ACT/STBY
	SLI/STSX1	SONET equipment		
	ICB	CC		
TMUX	TIDBs	SFI	Simplex	ACT
	BPIDBs	CD		
	ICBs	CC		
CD	BPIDB	TMUX	Duplex	ACT/STBY
	ICBs	CC		
	COT/PCT link	TSIS		
	PCAMB	CC		
	Timing Cross-Couple	Mate CD		
CC	ICB	SFI	Duplex	ACT/STBY
	ICB	TMUX		
	ICB	CD		
	PCAMB			
	Update Bus	Mate CC		

9.2.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the diagnosable Digital Network Unit - SONET (DNU-S) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
CC	One circuit pack	Major	No impact.	No impact.
	Two circuit packs	Major	No impact unless a third failure occurs.	Removes the ability of the *5ESS*® switch to switch to the TMUX spare. Removes the ability of the *5ESS*® switch to switch between the active and standby CD or SFI.
CD, SFI	One circuit pack in a Data Group	Major	No impact.	No impact.
	Two circuit packs in a	Major	Impact depends on the	Reduces call processing

	Data Group		number of calls the data group handles.**	capacity.
TMUX	One TMUX in a Data Group	Major	No impact.	No impact.
	Multiple TMUXs in a Data Group	Major	Impact depends on the number of calls the data group handles.**	Reduces call processing capacity.

NOTE: The DNU-S uses the STXS to handle subscriber data from another site. When the STXS is removed from service, then the DNU-S components that are connected to the STXS lose capacity.

* Removal of more than one TMUX in the same data group degrades customer service for that data group. A data group consists of duplicated CDs, six active TMUXs, one spare TMUX, and duplicated SFIs.

** Go to the office records to determine what carrier systems are impacted.

9.2.6 Detailed Description

The following table details the functions of the diagnosable components in the Digital Network Unit - SONET (DNU-S).

Part	Function
CC	Updates software and routes maintenance messages. The CC does not handle call processing control messages.
CD	Converts and sends control messages and subscriber data between the TMUX and the TSIS.
TMUX	Converts and sends control messages and subscriber data between the CD and the SFI.
SFI	Converts and sends subscriber data between the STSX1 and the TMUX.

9.2.7 Functional Description

9.2.7.1 Functions

The Digital Network Unit - SONET (DNU-S):

- Connects the SONET equipment to the *5ESS*® switch for call processing in subscriber lines and trunks.
- Converts control messages and subscriber data to a format that is compatible with the *5ESS*® equipment.

9.2.7.2 Operation

The DNU-S interacts with other components to operate the switch.

The Figure 9-2 depicts the operation of the DNU-S.

Figure 9-2 DNU-S Block Diagram

The following tables detail the operation of the DNU-S.

The DNU-S handles subscriber data and control signals from the far-end switching office, RSM or EAIU.

Stage	Description
1	The SFI receives subscriber data and control messages from the DSX via the STSX1 Link.
2	The SFI converts and sends the data and messages to the TMUX via the backplane.
3	The TMUX receives, converts and sends the data and messages to the CD via the backplane.
4	The CD receives, converts and sends the data and messages through the COT to the TSIS via the PCT Link.

The DNU-S handles control maintenance messages from the SMP.

Stage	Description
1	The CD receives a control message from the SMP through the TSIS via the PCT link.
2	The CD sends the message to the CC via the PCAMB.
3	The CC receives and executes the message.
4	The CC generates and sends a control message to either the CD, the TMUX, and/or the SFI, via the ICBs.

9.3 Optical Interface Unit (OIU)

9.3.1 Description, OIU

Figure 9-3 depicts a high-level diagram of the Optical Interface Unit (OIU) equipped with both Optical Facility Interface (OFI) Time Division Multiplex (TDM) and Internet Protocol (IP) packs.

Figure 9-3 OIU High Level Diagram

The Optical Interface Unit (OIU) is a peripheral unit that supports both Time Division Multiplex (TDM) and IP Packet trunks. The OIU provides a high-speed interface to the Synchronous Optical Network (SONET) through the use of Optical Carrier - level 3 (OC-3) and Optical Carrier - level 3 Concatenated (OC-3c) links.

The OIU supports the following functionality:

- Terminates point-to-point intra-office OC-3 interfaces from co-located Add/Drop Multiplexers (ADM) for TDM applications.
- Terminates point-to-point intra-office OC-3c interfaces from co-located routers that support Packet Over SONET (POS) for packet applications. The IP application can also be terminated to an ADM that is terminated to a POS router.
- Supports (1+1) Automatic Protection Switching (APS) for both the optical facility and circuit pack.
- Provides integrated *5ESS*® Operation Administration Maintenance and Provisioning (OAM&P).
- Terminates SONET facilities to the SM-2000 and then converts subscriber data and signaling to the PCT format that is compatible with the SM-2000.
- Supports split bus backplane.

9.3.2 Availability, OIU

The availability of the OIU is:

- Base OIU feature Software Release 5E16.2 BMI - TDM only.
- OIU-IP feature Software Release 5E16.2 FR 3

9.3.3 Frame/Cabinet Arrangement, AIP

The OIUs are located in the Line Trunk Peripheral (LTP) cabinets. The OIU is a logical unit that resides within a physical unit or sub-rack referred to as the *AnyMedia*® Interface Platform (AIP). Each AIP is a half-depth shelf which allows units to be mounted in both the front (equipment aisle) and rear (wiring aisle) of the frame. These frames are also called Front Access Cabling (FAC) cabinet. A fully equipped cabinet will support six AIP units.

A single AIP shelf can support from one to ten logical OIUs. Each OIU consists of at least one Protection Group (PG). Each PG is made up of two Optical Facility Interface (OFI) circuit packs.

Figure 9-4 depicts a fully equipped LTP frame with AIP units.

Figure 9-4 FAC Cabinet with 6 AIP Shelves

NOTE: A host SM-2000 can have up to 16 AIPs, numbered 0 - 15.

The power cables and transmissions links are fed in through the top of the cabinet.

Table 9-1 details the shelf arrangement of the AIP.

Table 9-1 AIP Shelf Arrangement

EQL	Shelf Unit	Designation
68	Modular Fuse and Filter Unit (MFFU)	Fuse and Filter Unit

57	*AnyMedia*® Interface Platform (AIP)	AIP 2 (Front) and AIP 5 (Rear)
40	*AnyMedia*® Interface Platform	AIP 1 (Front) and AIP 4 (Rear)
23	*AnyMedia*® Interface Platform	AIP 0 (Front) and AIP 3 (Rear)
11	Fan	Fan Unit

9.3.4 Shelf and Circuit Pack Arrangement, OIU

A fully equipped AIP will accommodate 20 OFI circuit packs. The OFI packs are equipped as pairs in adjacent slots, with each pair being a protection group. Therefore a fully equipped AIP consists of 10 PGs. Each PG can terminate to a separate SM-2000, and be associated with different logical OIU. A mixture of TDM and IP protection groups can be equipped in the same OIU and/or AIP unit.

9.3.4.1 OFI Shelf and Circuit Pack Arrangement

Figure 9-5 depicts the AIP shelf locations and pack arrangement (refer to OFI Basic Description section 9.3.6.2 for a detailed description of the OFI packs).

Figure 9-5 AIP Shelf and Circuit Pack Arrangement

Table 9-2 provides a cross reference between the horizontal equipment locations (EQLs), corresponding slots, protection group, protection group pack number, pack name and pack codes.

Table 9-2 OFI Shelf and Circuit Pack Arrangement

Horizontal EQL	Slot	PG	PG Pack	Component Name	Pack Code
083	001	N/A	N/A	Blank	N/A
108	002				
133	003	0	0	Optical Facility Interface	LPA 931, LPA935, or
158	004		1	(OFI)	LPA936
183	005	1	0		
208	006		1		
233	007	2	0		
258	008		1		
283	009	3	0		
308	010		1		
338	011	4	0		
363	012		1		
388	013	5	0		
413	014		1		
438	015	6	0		
463	016		1		
488	017	7	0		
513	018		1		
538	019	8	0		

563	020		1		
588	021	9	0		
613	022		1		

Table 9-3 provides a cross reference between the supported Optical Facility Interface (OFI) circuit packs, applications, interface, fiber type, transceiver and the maximum number of supported physical ports.

Table 9-3 OFI Circuit Pack Cross Reference

Pack Code	Application	Interface	Fiber Type	Transceiver	Maximum Ports
LPA931	TDM	OC-3	Single-Mode	Laser	3 PCT and 1 OC-3
LPA935	IP	OC-3c	Multi-Mode	LED	3 PCT and 1 OC-3c
LPA936	IP	OC-3c	Single-Mode	Laser	

NOTE: All PCT connections will use multimode fiber with MTRJ connectors.

9.3.5 Power, OIU

The AIP units are located in a front access cable (FAC) line trunk peripheral frame. The LTP cabinets that house the AIPs can terminate up to twelve -48 VDC power feeders from the Global Power Distribution Frame (GPDF). The power feeders are terminated at the rear of the cabinet. Six of the power feeders are terminated to the "A" power bus and six power feeders are terminated to the "B" power bus. The A power bus supplies power to the OFIs designated 0 in each PG and the B power bus supplies power to the OFIs designated 1 in each PG. The power feeders terminate to the locations listed in the following table.

NOTE: The actual operating range is -39.5 VDC to -56 VDC.

Power Bus A	Power Bus B
69-017	69-108
69-032	69-123
69-047	69-139
69-063	69-154
69-078	69-169
69-093	69-184

After the power is filtered and fused, it is cabled to the individual shelf units and fans. Figure 9-6 depicts the fuse assignments. Though the AIPs are mounted in a front access cabinet, the front of the MFFU faces the equipment aisle in the office, therefore the fuses are accessible only through that side of the cabinet.

NOTE: Each OFI board contains a three amp fuse.

Figure 9-6 OFI Fuse Assignments

The following tables provide a cross reference between the fuses, power cables and the AIP units/OFI packs receiving power.

Fuse Position	Fuse Amperage	Power Lug Terminals	Unit Fused	Protects ...
014A	20	23F -48VA 23F -48RTNA	AIP 0	"0" OFI packs in each Protection Group
023A	20	23R -48VA 23R -48RTNA	AIP 3	
041A	20	40F -48VA 40F -48RTNA	AIP 1	
050A	20	40R -48VA 40R -48RTNA	AIP 4	
073A	20	57F -48VA 57F -48RTNA	AIP 2	
082A	20	57R -48VA 57R -48RTNA	AIP 5	
109A	20	23R -48VB 23R -48RTNB	AIP 3	"1" OFI packs in each Protection Group
118A	20	23F -48VB 23F -48RTNB	AIP 0	
141A	20	40R -48VB 40R -48RTNB	AIP 4	
150A	20	40F -48VB 40F -48RTNB	AIP 1	
168A	20	57R -48VB 57R -48RTNB	AIP 5	
177A	20	57F -48VB 57F -48RTNB	AIP 2	

The following tables provide a cross reference between the AIP units, power lugs and the equipment location within the AIP unit.

Unit Fused	Power Lug Terminals	Protects ...
AIP 0	23F -48VA	23F-027-131
	23F -48RTNA	23F-027-118
	23F -48VB	23F-027-157
	23F -48RTNB	23F-027-144
AIP 1	40F -48VA	40F-027-131
	40F -48RTNA	40F-027-118
	40F -48VB	40F-027-157
	40F -48RTNB	40F-027-144
AIP 2	57F -48VA	57F-027-131
	57F -48RTNA	57F-027-118
	57F -48VB	57F-027-157
	57F -48RTNB	57F-027-144
AIP 3	23R -48VA	23R-027-131
	23R -48RTNA	23R-027-118
	23R -48VB	23R-027-157
	23R -48RTNB	23R-027-144
AIP 4	40R -48VA	40R-027-131
	40R -48RTNA	40R-027-118
	40R -48VB	40R-027-157
	40R -48RTNB	40R-027-144
AIP 5	57R -48VA	57R-027-131
	57R -48RTNA	57R-027-118
	57R -48VB	57R-027-157
	57R -48RTNB	57R-027-144

Figure 9-7 depicts the fan units for the LTP containing the AIP units.

Figure 9-7 Fan Unit

The alarm circuit contains 2 push-button switches and eight status LEDs. The following tables provides a cross reference between the buttons and LEDs.

Button Label	Description
R	Reset
T	Test

LED Label	Description
OT	Over Temperature
G	Fan G
F	Fan F

E	Fan E
C	Fan C
B	Fan B
A	Fan A
S	Status

The following table provides a cross reference between the fuses and the fans in the FAC containing the AIP shelves. The fan unit power equipment location is: 11-162.

Fuse Position	Fuse Amperage	Unit Fused	Protects ...
109C	3	FAN	FAN ALARM
023B	3	FAN	FAN A
109B	3	FAN	FAN B
041B	3	FAN	FAN C
118B	3	FAN	FAN E
014B	3	FAN	FAN F
141B	3	FAN	FAN G

Figure 9-8 depicts the power lug locations, power feeder distribution (A and B), working/protection OFI pack slot (W and P). Also shown are the PCT and OC-3/OC-3c facility, the amber out-of-service LEDs.

Figure 9-8 OIU Power

9.3.6 Basic Description, OIU

An OIU consists of at least two Optical Facility Interface (OFI) packs that create a single protection group. The OIU consists of the following:

- Contained within an AIP shelf.
- Supported by an SM-2000.
- Made up of two to twenty OFIs, (one to ten PGs).
- Supports both TDM and IP applications.
- Terminated to a POS router for IP applications or an ADM for TDM applications.
- Provides 1+1 (working and protection) Automatic Protection Switching (APS) capability.

9.3.6.1 Protection Group Basic Description

Each Protection Group (PG) consists of the following:

- Two OFI-TDM or OFI-IP circuit packs.
- PCT links hosted by the same SM-2000.
- Two OC-3/OC-3c links, one designated as Working and one as Protection.

9.3.6.2 OFI-TDM Pack Basic Description

Each Optical Facility Interface - Time Division Multiplex (OFI-TDM) circuit pack:

- Interfaces up to three PCT links and one OC-3 facility.
- Converts OC-3 format to/from PCT format.
- Supports 672 voice time slots per PCT link.
- Utilizes one MH time slot for control and pump.
- Requires at least PCT 0 equipage.

Figure 9-9 OFI-TDM Block Diagram

Figure 9-9 provides a high-level diagram of the OFI-TDM circuit Pack. The following is a brief description of the blocks shown in figure 9-9 :

- **Control complex**:
  - *Microprocessor* - provides OFI control.

- *Flash memory* - provides software boot code.
- *Memory* - instruction storage.

- **PCT Interface** - terminates PCT Links and performs conversions.
- **DS1, V-Path Termination** - provides PCT overhead termination, VT1.5 disassembly, DS1 framing and robbed-bit signaling processing.
- **Field Programmable Gate Array (FPGA)** - processes and manipulates signals between the DS1, V-Path circuits, control complex and the OC-3 Section, Path, Line Block.
- **OC-3, Section, Path, Line block** - termination for SONET Section, Line and STS-1 Path overheads, detects signal degrade and failure conditions.
- **OC-3 Interface** - provides conversions and fiber termination.
- **Power** - provides power conversion and distribution.

9.3.6.3 OFI-IP Pack Basic Description

Each Optical Facility Interface - Internet Protocol (OFI-IP) circuit pack:

- Interfaces up to three PCT links and one OC-3c facility
- Converts OC-3c format to/from PCT format,
- Supports one Point-to-Point Protocol Link (PPPLK),
- Performs all required protocol conversions and error detection,
- Supports a maximum of 2016 PCT time slots depending on provisioned characteristics, number of PCT links equipped,
- Utilizes one MH time slot for control,
- Requires at least PCT 0 equipage,
- Utilizes four MH32 times slots or 16 MHPPC time slots for pump.

NOTE: The MH pump time slots are shared among all OFI-IPs supported by the same MH.

Figure 9-10 OFI-IP Block Diagram

Figure 9-10 provides a high-level diagram of the OFI-IP circuit Pack. The following is a brief description of the blocks shown in figure 9-10 :

- **Control complex**:
  - *Microprocessor*- provides OFI control.
  - *Flash memory*- provides software boot code.
  - *Memory* - instruction storage.
- **PCT Interface**- terminates PCT Links and performs conversions.
- **TDM FPGA** - unscrambles PCT data, searches for framing, locates PCM time slots, performs mapping to DSP.
- **DSP Complex**- formats and adds/validates IPv4 headers, UDP headers, RTP, and voice processing. Provides jitter buffer management, voice coding and echo cancellation.
- **Packet FPGA** - provides PPP protocol layer, IP header validation, detects and counts IP header errors, ICMP protocol support, UDP header validation, detects and counts UDP header error statistics.
- **POS OC-3c Interface** - provides conversions and fiber termination.
- **Power** - provides power conversion and distribution.

Figure 9-11 depicts an OFI circuit pack residing in an AIP shelf. The front of the pack provides a termination for the OC-3/OC-3c fiber, and equipped PCT Links. Notice the PCT Links are number 0 - 2, starting from the bottom.

Figure 9-11 OFI Circuit Pack Diagram

9.3.7 Connecting Circuits, OIU

An OIU consists of at least one protection group, which consists of two OFI circuit packs as shown in figure 9-12 . The following are the OFI external interfaces:

- Module Controller Time Slot Interchange (MCTSI).
- Add Drop Multiplexer (ADM) - TDM and IP applications.
- Packet Over SONET (POS) Router - IP application.
- Cross-couple between the OFIs within a protection group.

Figure 9-12 External Interfaces

9.3.7.1 OFI - MCTSI Interface

The interface between the OFI and the MCTSI is a Peripheral Control and Timing (PCT) link connected to a Peripheral Link Interface (PLI). The OFI provides a PCT link optical connection through the faceplate. Each PLI:

- Terminates one transmit and receive fiber.
- Performs the optical to electrical/electrical to optical conversion.
- Is cross-coupled to the mate TSI through the backplane.

NOTE: The PLI is a BKD10 pack attached to the backplane of the TSI.

9.3.7.2 OFI - ADM Interface

This interface is supported by TDM and IP applications. The interface between the OFI and the ADM is an OC-3 fiber. The OFI provides an OC-3 optical connection through the faceplate. When used for an IP application, the interface is OC-3c and an additional connection from the ADM to the router is required.

9.3.7.3 OFI - Router Interface

This interface is supported by IP applications only. The interface between the OFI and the Router is an OC-3c fiber. The OFI provides an OC-3c optical connection through the faceplate.

9.3.7.4 OFI - OFI PG Interface

This interface is part of the AIP backplane. It is used to provide an exchange of clock and data between the two packs that makeup a protection group.

9.3.8 Functional Description, OIU

The Optical Interface Unit (OIU) provides paths for the following:

- Data path for TDM applications,
- Data path for IP applications,
- Control path for OFI operation.

9.3.8.1 OIU - TDM Functional Operation

The Figure 9-13 depicts the operation of the OIU - TDM.

Figure 9-13 OIU - TDM Block Diagram

Table 9-4 details the flow of data from the TSI to the ADM for a TDM call.

Following an origination, digit analysis and resource allocation a path is established through the OIU for a voice/data call.

Table 9-4 OIU - TDM Functional Operation

Stage	Description
1	Voice/data time slots are switched through the Active TSI and broadcast to both PLI boards.
2	Each PLI inserts the time slots onto the PCT link and sends them to the corresponding OFI-TDM circuit pack.
3	The OFI recovers switch data DS0s from the PCT links and maps them to virtual containers. The virtual containers (VT1.5s) are multiplexed into higher order virtual containers (STS-1) for packaging in an OC-3 optical interface.
4	The electrical signal is converted to an optical signal and inserted onto an OC-3 fiber and sent to an ADM.

9.3.8.2 OIU - IP Functional Operation

The Figure 9-14 depicts the operation of the OIU - IP.

Figure 9-14 OIU - IP Block Diagram

Table 9-5 details the flow of data from the TSI to the Router for an IP call.

Following an origination, digit analysis and resource allocation a path is established through the OIU for a voice/data call.

Table 9-5 OIU - IP Functional Operation

Stage	Description
1	Voice/data time slots are switched through the Active TSI and broadcast to both PLI boards.
2	Each PLI inserts the time slots onto the PCT link and sends them to the corresponding OFI - IP circuit pack.
3	Once the data enters the OFI-IP the following events occur: □ Each DS0 is routed to the appropriate DSP for echo cancellation and RTP processing. □ Each DSP collects enough DS0 voice/data to form RTP samples which are sent towards the network in IP datagrams using UDP transport. □ IP datagrams are inserted into the PPP link towards the router. □ The PPP link is embedded in the STS-3c high-level virtual container carried on OC-3c fiber.
4	The electrical signal is converted to an optical signal and inserted onto an OC-3c fiber and sent to a router.

9.3.8.3 OIU Control Flow Operation

The Figure 9-15 depicts the control flow operation of the OIU.

Figure 9-15 OIU Control Flow Diagram

Table 9-6 details the control flow from the MCTSI to an OFI pack

Table 9-6 OIU Control Flow Operation

Stage	Description
1	A control message is assembled in the SMP complex and sent to the MH.
2	The MH inserts the control into the designated channel.
3	The control time slot is forwarded to the TSI over the MCP link.
4	The control time slot is inserted onto PCT link 0 and sent to the corresponding OFI-IP circuit pack.
5	The control time slot is extracted from the PCT link and routed and processed by a HDLC sequencer before being accessed by the OFI processor complex.

9.3.9 Timing, OIU

The first PCT link (designated PCT 0) is required on every OFI for control and timing purposes. A 65 Mhz clock is recovered for each of the three received scrambled PCT data streams using PLL circuits. These recovered clocks are used in the PCT framer circuits. The recovered PCT 0 clock is used as the transmit clock for all three PCT links.

9.3.10 Configuration, OIU

Tables 9-7 and 9-8 provide configuration information for the OIU when configured with the TDM application or IP application respectively.

Table 9-7 OIU-TDM Configuration

Component	Normal Operation	Operating State
OFI-TDM	Active/Active	Duplex
OC3	Active/Standby	
STS1	Active	Simplex
VT 1.5		
DS1		

Table 9-8 OIU-IP Configuration

Component	Normal Operation	Operating State
OFI-IP	Active/Active	Duplex
OC3c	Active/Standby	
STS3c	Active	Simplex
PPPLK		

NOTE: An OFI PG operates in active/active mode with one side selected and the other non-selected (there is no STBY mode for OFIs).

9.3.11 Service Impacts, OIU

Table 9-9 and 9-10 details the impact on subscriber service and switch performance when the Optical Interface Unit (OIU) components are not available.

Table 9-9 OIU-TDM Service Impacts

Component	Simplex Failure	Duplex Failure
OFI-TDM	No impact.	All calls carried by the PG are lost. All trunks removed from service.
OC3	No impact.	All calls carried by the PG are lost. All trunks removed from service.
STS1	All calls carried by the STS1 are lost. All trunks removed from service.	N/A
VT 1.5	All calls carried by the VT 1.5 are lost. All trunks removed from service.	N/A
DS1	All calls carried by the DS1 are lost. All trunks removed from service.	N/A

Table 9-10 OIU-IP Service Impacts

Component	Simplex Failure	Duplex Failure
OFI-IP	No impact.	All calls carried by the PG are lost. This packet trunking interface is removed from service. Packet trunks will be routed to other OFI-IP protection groups.
OC3c	No impact.	All calls carried by the PG are lost. This packet trunking interface is removed from service. Packet trunks will be routed to other OFI-IP protection groups.
STS3c	All calls carried by the STS3c are lost. This packet trunking interface is removed from service. Packet trunks will be routed to other OFI-IP protection groups.	N/A
PPPLK	All calls carried by the PG are lost. This packet trunking interface is removed from service. Packet trunks will be routed to other OFI-IP protection groups.	N/A

9.3.12 Remove Electrical Power, OIU

Each OFI circuit pack receives -48 VDC power through the back plane and performs its own power conversion. Therefore the circuit packs are powered down by unseating them from the unit. There is no separate power control.

9.3.13 MCC Pages and Pokes, OIU

Table 9-11 details the new or modified MCC pages and their associated poke commands for the OIU. For additional details regarding a specific MCC page, refer to the 235-105-110 *System Maintenance Requirements and Tools* document.

Table 9-11 OIU MCC Poke Table

Poke	Description
100	Page Index
132,1 and 132,2	Call Trace Menu
1000	SM Page Index
1007	Platform Configuration
1410	AIP Equipage
1440	AIP Shelf
1490	OIU Status
1491	OC3 Protection Group OC3/OC3c Status
1492	OIU Protection Group STS-1, VT1.5 and DS1 Status
1493	OIU Protection Group STS-1 Application
1494	OIU Protection Group Packet Status

Figure 9-16 depicts MCC page 1007 (Platform Configuration page) that provides a list of platform pages displaying hardware configuration information.

Figure 9-16 MCC Page 1007 (Platform Configuration Page)

Figure 9-17 depicts MCC page 1410 (AnyMedia interface platform (AIP) Equipage page). This page displays all the AIP shelves equipped on an SM. No status information will be displayed on this page.

Figure 9-17 MCC Page 1410 (AnyMedia Interface Platform (AIP) Equipage Page)

Figure 9-18 depicts MCC page 1440 (AIP Shelf page). This page displays units that occupy slots on an AIP shelf hosted by a given SM. For each slot, the page displays the unit type, unit number, and SM that logically owns the unit. No status information is displayed on this page.

Figure 9-18 MCC Page 1440 (AIP Shelf Page)

Figure 9-19 depicts MCC page 1490 (OIU Status page). This page displays detailed status for all OFIs (optical facility interfaces), as well as a summary status of facilities within each PG (protection group).

Figure 9-19 MCC Page 1490 (OIU Status Page)

Figure 9-20 depicts MCC page 1491 (OIU Protection Group Status page). There are two different formats of this display page. The first format provides a view of the page when OFIs with service type "TDM," are equipped. This version displays detailed status information for each OC-3 link and a summary status of the STS1 and all related VT 1.5/DS1 facilities.

Figure 9-20 MCC Page 1491 (OIU Protection Group Status Page for TDM)

Figure 9-21 depicts MCC page 1491 (OIU Protection Group Status page). The second format provides a view of the page when OFIs with service type "IP," are equipped. This version displays detailed status information for each OC-3c link, status of the STS-3c, and summary status of the PPP Link.

Figure 9-21 MCC Page 1491 (OIU Protection Group Status Page for IP)

NOTE: For uni-directional APS, no remote status is displayed.

Figure 9-22 depicts MCC page 1492 (OIU PG STS1 Status page). The status of the STS1 and related VT 1.5 and DS1 facilities are displayed.

Figure 9-22 MCC Page 1492 (OIU PG STS1 Status Page - TDM Only)

Figure 9-23 depicts MCC page 1493 (OIU PG STS1 Application page). This page displays the application and the far end information for each DS1 in the STS1. The DS1-numbers column serves as a summary status for that DS1.

Figure 9-23 MCC Page 1493 (OIU PG STS1 Application Page - TDM Only)

Figure 9-24 depicts MCC page 1494 (Packet Status page). This display page provides PPP link status and, overload status when needed.

Figure 9-24 MCC Page 1494 (Packet Status Page - IP Only)

9.3.14 Diagnostic Phases, OIU

Table 9-12 provides a diagnostic phase description for the OFI-TDM and Table 9-13 provides a description for each OFI - IP diagnostic phase.

Table 9-12 OIU-TDM Diagnostics Phases

Diagnose OFI-TDM	
Phase	**Description**
1	Tests the PCT link, SM-to-PLI interface, and the PLI pack. Interfaces to both sides of the MCTSI.
2	Tests the PCT interface to the circuit under test. The slot position and the PCT physical connection at the circuit under test are tested.
3	Runs self-tests, pack-to-pack communication tests, and the ROM-based RAM tests.
4	Not used.
5	(Demand phase only) Tests the external facility loopback on the OFI. Installation of an external loopback is required before running this phase.

Table 9-13 OIU-IP Diagnostics Phases

Diagnose OFI-IP	
Phase	**Description**
1	Tests the PCT link, SM-to-PLI interface, and the PLI pack. Interfaces to both sides of the MCTSI.
2	Tests the PCT interface to the circuit under test. The slot position and the PCT physical connection at the circuit under test are tested.
3	Runs self-tests, pack-to-pack communication tests, and the ROM-based RAM tests. OIU-IP hardware tested include the: microprocessor interface, SONET interface, IP interface, Digital Signal Processors, all FPGAs, SRAM memory and the cross-couple link between mate pairs of OFI-IP packs.
4	Not used.
5	(Demand phase only) Tests the external facility loopback on the OFI. Installation of an external loopback is required before running this phase.
6	(Demand phase only) Dumps inventory ROM contents.

9.3.15 Cables, OIU

The AIP unit terminates power cables to the "mid-plane" and all other cables are terminated to the OFI packs. The following sections depict the cabling information for the OFIs of an OIU.

9.3.15.1 AIP Shelf Description

Each AIP shelf can support up to 10 OFI paired circuit packs. Figures 9-25 and 9-26 show the front and rear layout of the AIP shelves.

Figure 9-25 AIP Front Subrack Layout

Figure 9-26 AIP Rear Subrack Layout

Table 9-14 depicts the OC-3/OC-3c port assignments for AIP shelves 0 and 3.

Table 9-14 AIP Shelves 0 and 3 Port Assignments

Port Assignment for OIU OC-3/OC-3c Links					
AIP Front of Paired OFIs - Shelf 0			AIP Rear of Paired OFIs - Shelf 3		
PG	OFI CP	EQL	PG	OFI CP	EQL
0	000	023F-003-TX/RX	0	000	023R-003-TX/RX
	001	023F-004-TX/RX		001	023R-004-TX/RX
1	000	023F-005-TX/RX	1	000	023R-005-TX/RX
	001	023F-006-TX/RX		001	023R-006-TX/RX
2	000	023F-007-TX/RX	2	000	023R-007-TX/RX
	001	023F-008-TX/RX		001	023R-008-TX/RX
3	000	023F-009-TX/RX	3	000	023R-009-TX/RX
	001	023F-010-TX/RX		001	023R-010-TX/RX
4	000	023F-011-TX/RX	4	000	023R-011-TX/RX
	001	023F-012-TX/RX		001	023R-012-TX/RX
5	000	023F-013-TX/RX	5	000	023R-013-TX/RX
	001	023F-014-TX/RX		001	023R-014-TX/RX
6	000	023F-015-TX/RX	6	000	023R-015-TX/RX
	001	023F-016-TX/RX		001	023R-016-TX/RX
7	000	023F-017-TX/RX	7	000	023R-017-TX/RX
	001	023F-018-TX/RX		001	023R-018-TX/RX
8	000	023F-019-TX/RX	8	000	023R-019-TX/RX
	001	023F-020-TX/RX		001	023R-020-TX/RX
9	000	023F-021-TX/RX	9	000	023R-021-TX/RX
	001	023F-022-TX/RX		001	023R-022-TX/RX
NOTE: **Legend**: circuit pack (CP)					

Table 9-15 depicts the OC-3/OC-3c port assignments for AIP shelves 1 and 4.

Table 9-15 AIP Shelves 1 and 4 Port Assignments

Port Assignment for OIU OC-3/OC-3c Links					
AIP Front of Paired OFIs - Shelf 1			AIP Rear of Paired OFIs - Shelf 4		
PG	OFI CP	EQL	PG	OFI CP	EQL
0	000	040F-003-TX/RX	0	000	040R-003-TX/RX
	001	040F-004-TX/RX		001	040R-004-TX/RX
1	000	040F-005-TX/RX	1	000	040R-005-TX/RX
	001	040F-006-TX/RX		001	040R-006-TX/RX
2	000	040F-007-TX/RX	2	000	040R-007-TX/RX
	001	040F-008-TX/RX		001	040R-008-TX/RX
3	000	040F-009-TX/RX	3	000	040R-009-TX/RX
	001	040F-010-TX/RX		001	040R-010-TX/RX
4	000	040F-011-TX/RX	4	000	040R-011-TX/RX
	001	040F-012-TX/RX		001	040R-012-TX/RX
5	000	040F-013-TX/RX	5	000	040R-013-TX/RX
	001	040F-014-TX/RX		001	040R-014-TX/RX
6	000	040F-015-TX/RX	6	000	040R-015-TX/RX
	001	040F-016-TX/RX		001	040R-016-TX/RX
7	000	040F-017-TX/RX	7	000	040R-017-TX/RX
	001	040F-018-TX/RX		001	040R-018-TX/RX
8	000	040F-019-TX/RX	8	000	040R-019-TX/RX
	001	040F-020-TX/RX		001	040R-020-TX/RX
9	000	040F-021-TX/RX	9	000	040R-021-TX/RX
	001	040F-022-TX/RX		001	040R-022-TX/RX
NOTE: **Legend**: circuit pack (CP)					

Table 9-16 depicts the OC-3/OC-3c port assignments for AIP shelves 2 and 5.

Table 9-16 AIP Shelves 2 and 5 Port Assignments

Port Assignment for OIU OC-3/OC-3c Links					
AIP Front of Paired OFIs - Shelf 2			AIP Rear of Paired OFIs - Shelf 5		
PG	OFI CP	EQL	PG	OFI CP	EQL
0	000	057F-003-TX/RX	0	000	057R-003-TX/RX
	001	057F-004-TX/RX		001	057R-004-TX/RX
1	000	057F-005-TX/RX	1	000	057R-005-TX/RX
	001	057F-006-TX/RX		001	057R-006-TX/RX
2	000	057F-007-TX/RX	2	000	057R-007-TX/RX
	001	057F-008-TX/RX		001	057R-008-TX/RX
3	000	057F-009-TX/RX	3	000	057R-009-TX/RX
	001	057F-010-TX/RX		001	057R-010-TX/RX
4	000	057F-011-TX/RX	4	000	057R-011-TX/RX
	001	057F-012-TX/RX		001	057R-012-TX/RX
5	000	057F-013-TX/RX	5	000	057R-013-TX/RX

	001	057F-014-TX/RX		001	057R-014-TX/RX
6	000	057F-015-TX/RX	6	000	057R-015-TX/RX
	001	057F-016-TX/RX		001	057R-016-TX/RX
7	000	057F-017-TX/RX	7	000	057R-017-TX/RX
	001	057F-018-TX/RX		001	057R-018-TX/RX
8	000	057F-019-TX/RX	8	000	057R-019-TX/RX
	001	057F-020-TX/RX		001	057R-020-TX/RX
9	000	057F-021-TX/RX	9	000	057R-021-TX/RX
	001	057F-022-TX/RX		001	057R-022-TX/RX
NOTE: **Legend**: circuit pack (CP)					

9.3.15.1.1 OIU Cable Reference

Figure 9-27 depicts an example of an AIP finger tray label. This label is stenciled to add the appropriate OIU number and SM assignment information.

Figure 9-27 AIP Finger Tray Label Layout

9.3.16 Capacity, OIU

The following section provides some OIU capacity related information. A more detailed description of the capacity and engineering considerations can be found in the 235-070-100 *Administration and Engineering Guidelines* document.

Table 9-17 provides the quantities of OIU components required.

Table 9-17 OIU Operational Equipage Values

Component	MIN SERVE EQUIPMENT	MAX SERVE EQUIPMENT
AIP Units per Frame	1	6
OIUs per AIP	1	10
Protection Groups (PGs) per OIU	1	10
OFIs per PG	2	2
OC-3/OC-3c per OFI	1	1
PCT Links per OFI	1	3

9.3.16.1 Message Handler (MH)

Each SM-2000 supporting an OIU will require MH time slots for control purposes. These time slots are assigned from either MH1 or MH2.

The following table provides the related OIU - MH information.

MH Time Slot Allocation	OFI-TDM	OFI-IP
Control Time Slots (per OFI pair)	2	2
Pump Time Slots (MH32)	0	4
Pump Time Slots (MHPPC)	0	16

NOTE: The OFI-TDM is pumped using the assigned Control Time Slot.

9.3.16.2 PCT Links

Each equipped OFI pack requires a minimum equipage of PCT Link 0. PCT Link 0 provides control, timing

and bearer. PCT Links 1 and 2 are equipped based on traffic needs. The table below provides some PCT Link capacity related information.

PCT Link Number	OFI-TDM Supported DS0s	OFI-IP Supported DS0s
0	672	720
1	672	768
2	672	528

NOTE: Each PLI terminates 1 duplex PCT Link.

9.3.17 Procedure Reference, OIU

Table 9-18 provides reference for the OIU procedures.

Table 9-18 OIU Procedural References

Document	Procedure Title
235-105-220	Clearing Diagnostic Failure in an OFI
	Verify DEN/NEN/OIUEN of a Digital Trunk
	Determine Hardware and Software used during Call Processing
	Test OIU-IP Connections
235-105-231	OIU VT1.5/DS1 Facility Growth - 5E16.2 and Later Software Releases
	Bearer Network Growth - 5E16.2 and Later Software Releases
	Optical Interface Unit (OIU) *AnyMedia* ® Interface Platform (AIP) Unit Growth - 5E16.2 and Later Software Releases
	Optical Interface Unit (OIU) Growth - 5E16.2 and Later Software Releases
	Optical Interface Unit (OIU) Optical Facility Interface (OFI) Protection Group (PG) Growth - 5E16.2 and Later Software Releases
	Optical Interface Unit (OIU) Synchronous Transport Signal-1/Synchronous Transport Signal-Level 3 Concatenated (STS-1/STS-3c) Facility Growth - 5E16.2 and Later Software Releases
	Optical Facility Interface (OFI) - PPP Link Provisioning - 5E16.2 and Later Software Releases
	Optical Interface Unit (OIU) Peripheral Control and Timing (PCT) Links 1 and/or 2 Growth - 5E16.2 and Later Software Releases
235-105-331	Optical Interface Unit (OIU) Peripheral Control and Timing (PCT) Links Degrowth - 5E16.2 and Later Software Releases
	Optical Facility Interface (OFI) - PPP Link Deprovisioning - 5E16.2 and Later Software Releases
	OIU Synchronous Transport Signal-1/ Synchronous Transport Signal -3c (STS-1/STS-3c) Facility Degrowth - 5E16.2 and Later Software Releases
	Optical Interface Unit (OIU) Optical Facility Interface Protection Group Degrowth - 5E16.2 and Later Software Releases
	Optical Interface Unit (OIU) Degrowth - 5E16.2 and Later Software Releases
	AnyMedia® Interface Platform (AIP) Unit Degrowth - 5E16.2 and Later Software Releases
	OIU-IP Facility Bearer Network Degrowth - 5E16.2 and Later Software Releases
	OIU VT1.5/DS1 Facility Degrowth - 5E16.2 and Later Software Releases
235-105-250	OIU Duplex Failure
	OIU-IP Protection Group Duplex Failure

9.3.18 Recent Change View References, OIU

Table 9-19 details the new Recent Change View (RC/V) references for the OIU.

Table 9-19 OIU RC/V References

OIU RC/V References		
View	**Component Name**	**ODA Form**
8.15	Office Options	5509
8.29	Threshold Alarm Levels	5769
19.27	Any Media Interface Platform	5765
19.28	Optical Interface Unit	5760
20.28	Optical Facility Interface Pack	5761
20.29	OIU SONET Terminating Equipment	5762
20.30	High-Level Virtual Container	5763
20.31	Low-Level Virtual Container	5764
20.32	OIU Performance Monitoring Threshold Group	5767
20.33	Carrier Group Alarm Integration Times	5766
33.1	Internet Protocol (IP) Processor Assignment	5987
33.15	Bearer Network Definition	5935

9.4 TRUNK UNIT (TU)

9.4.1 Basic Description

The Trunk Unit (TU) is a one shelf unit that contains individually diagnosable components. The components include:

- CDI,
- CHBD,
- CKT, and
- TAC.

The TU is located in an SM or SM-2000 cabinet.

The primary job of the TU depends on the circuit packs that the TU contains. The TU:

- Connects the LTD to the MMSU for testing metallic lines.
- Connects analog trunks to the MCTSI for routing subscriber data and control messages.

9.4.2 Electrical Power

One power circuit pack controls power for each Trunk Unit (TU) service group in the TU shelf.

9.4.3 Shelf and Circuit Pack Arrangement

The Analog Trunk Unit (TU) is located in an SM or SM-2000 cabinet.

The tables below detail the shelf and circuit pack arrangement of the TU hardware components.

The table below details the shelf and circuit arrangement of the TU.

EQL	Component Name	Component Number
008 and 100	**Power**	494GC
016 and 108	**TAC**	SN100
024 and 116	**CDI**	SN101B
032 - 088 (8 pack slots) and 124 -180 (8 pack slots)	**CHBD***	SN107
* The TUs that were installed prior to 5E8 may contain CHBD circuit packs other than the SN107.		

The table below details the CHBD circuit packs in the TU.

Part	Function
CHBD	The following types of CHBD circuit packs are rated Discontinued Availability (DA) but may be in service in some offices:
	SN102B - Loop Supervision, Outgoing (LSO).
	SN103 - Loop Supervision, Incoming (LSI).
	SN104 - 4-Wire E&M Supervision (4EM).
	SN105 - 2-Wire E&M Supervision (2EM).
	SN107 - Test Access Trunk. (still available as of 5-13-99)
	SN112 - Toll Loop Supervision, Outgoing (TLSO)
	SN113 - Toll Loop Supervision, Incoming (TLSI)
	SN114 - Toll 4-Wire E&M Supervision (T4EM)
	SN115 - Toll 2-Wire E&M Supervision (T2EM)

9.4.4 Configuration

The table below details the configuration of the Trunk Unit (TU).

Component	Link/Bus	Connects to ...	Method of Operation	State of Operation
TAC	TBT0, TBR0	MMSU and Test Access Pack 1	Simplex	ACT
	TBT1, TBR1	MMSU and Test Access Pack 0		
	Backplane	All trunk circuits in service group		
	Backplane	CDI		
	Backplane	CDI		
CDI	PICB	MCTSI		
	PIDB			
	CDIN	Each Trunk Circuit		
	CDOUT	Each Trunk Circuit		
	Backplane	Test access circuit		
CHBD 0 through 7	Metallic Wire	MDF		
	CDIN	CDI		
	CDOUT	CDI		
	Backplane	CDI and the test access circuit		
	TST (0-7)	Test access circuit		

9.4.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the Trunk Unit (TU) components are not available.

Unavailable Component	Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
TAC	Major	No impact.	Prevents test access to all trunks in the service group.
CDI	Major	May deny trunk service.	Prevents access to the PIDB. Removes all trunks in the service group from service.
CHBD	Major	May deny trunk service.	Removes up to four trunks in pack from service.
CKT	Minor	May deny trunk service.	Removes one trunk from service.
NOTE: Depending on the trunk circuit packs that the TU contains, a hardware problem may result in no to severe service impacts. When trunk access is denied for toll calls to some customers or destinations, then the service impact is severe.			

9.4.6 Detailed Description

The table below details the functions of the diagnosable components in the Trunk Unit (TU).

Part	Function
TAC	□ Connects analog trunks to the MMSU.
CDI	□ Controls the operation of the TU circuits. □ Connects the TU circuits to the MCTSI.
CHBDs	□ Connects the analog trunk facility to the CDI. □ Performs trunk supervision and signaling functions.

9.4.7 Functional Description

9.4.7.1 Functions

The Trunk Unit (TU):

- Converts analog signals to digital signals.
- Controls trunk signaling.
- Provides metallic test access and internal trunk testing circuits.

9.4.7.2 Operation

The TU interacts with other components to operate the switch.

- The Figure 9-28 depicts the operation of the TU.

Figure 9-28 TU Block Diagram

- The tables below detail the operation of the TU.

  The TU provides metallic test access for the LTD.

Stage	Description
1	The CHBD receives a signal from the LTD through MDF via a metallic wire.
2	The CHBD sends a control message and subscriber data to the CDI via the backplane.
3	The CDI receives and sends a control message to the MCTSI via a PICB.
4	The CDI receives a control message from the MCTSI via a PICB.
5	The CDI sends a control message to the CHBD via the backplane.
6	The CHBD receives a control message and closes the path between the LTD and the MMSU via the MTB.
7	The CHBD receives and sends tests signals between the LTD and MMSU via the MTB.

10. SWITCHING MODULE SERVICE PERIPHERAL UNITS

10.1 Data Services Unit, Model 3 (DSU3)

10.1.1 Basic Description

The Digital Service Unit - Model 3 (DSU3) is one shelf. The DSU3 may be located in any SM-2000 cabinet.

The DSU3 contains the diagnosable components, the LDSF and GDSF.

10.1.2 Shelf and Circuit Pack Arrangement

The Digital Service Unit - Model 3 (DSU3) is located in any SM-2000 cabinet.

The following table details the shelf and circuit pack arrangement of the DSU3 hardware components in an SM-2000.

EQL		Component Name	Component Number
Vertical	Horizontal		
Service Group 0 through 5 when equipped for LDSF			
	006, 036, 066, 096, 126, 156	**LDSF**	UN363 or UN590
Service Group 0 through 5 when equipped for GDSF			
	006, 036, 066, 096, 126, 156	**GDSF**	UN363 or UN590

10.2 Data Services Unit, Model 2 (DSU2)

10.2.1 Basic Description

The Digital Service Unit - Model 2 (DSU2) is one shelf. The DSU2 may be located in any SM or SM-2000 cabinet.

The DSU2 contains the diagnosable components: ISTF (SM only) and SAS.

10.2.2 Shelf and Circuit Pack Arrangement

The Digital Service Unit - Model 2 (DSU2) may be located in any SM or SM-2000 cabinet.

The table below details the shelf and circuit pack arrangement of the Digital Service Unit - Model 2 (DSU2) hardware components in an SM-2000 cabinet.

EQL		Component Name	Component Number
Vertical	Horizontal		
Service Group 0			
	018	**SAS** (DSC)	TN1841
	028, 038, 048	**SAS** (ASC)	TN1842
Service Group 2			
	058	**SAS** (DSC)	TN1841
	068, 078, 088	**SAS** (ASC)	TN1842
Service Group 1			
	108	**SAS** (DSC)	TN833
	118, 128, 138	**SAS** (ASC)	TN1842
Service Group 3			
	148	**SAS** (DSC)	TN833/TN1841
	158, 168, 178	**SAS** (ASC)	TN1842

The table below details the shelf and circuit arrangement of the DSU2 hardware components in an SM cabinet.

EQL		Component Name	Component Number
Vertical	Horizontal		
Service Group 0			

	018	**ISTF, or**	TN833
		SAS (DSC)	TN1841
	028, 038, 048	**SAS** (ASC)	TN1842
	Service Group 2		
	058	**ISTF, or**	TN833
		SAS (DSC)	TN1841
	068, 078, 088	**SAS** (ASC)	TN1842
	Service Group 1		
	108	**ISTF, or**	TN833
		SAS (DSC)	TN1841
	118, 128, 138	**SAS** (ASC)	TN1842
	Service Group 3		
	148	**ISTF, or**	TN833
		SAS (DSC)	TN1841
	158, 168, 178	**SAS** (ASC)	TN1842

10.3 Directly Connected Test Unit (DCTU)

10.3.1 Basic Description

The Directly Connected Test Unit (DCTU) is a two to four shelf unit. The DCTU is located in an SM cabinet (LTP).

The DCTU contains the individually diagnosable components that include:

- DCTUCOM,
- EAN,
- PMU, and
- DCTU Port

The primary job of the DCTU is to measure DC voltages, resistance, and capacitance for the analog subscriber lines and trunks.

10.3.2 Electrical Power

Separate power converter circuit packs control power for each diagnosable component in the Directly Connected Test Unit (DCTU). The circuit packs are located in an SM cabinet (LTP).

10.3.3 Shelf and Circuit Pack Arrangement

The Directly Connected Test Unit (DCTU) is located in a switching module cabinet (LTP). The DCTU occupies two to four shelves.

The table below details the shelf and circuit pack arrangement of the DCTU hardware components.

EQL		**Component Name**	**Component Number**
Vertical	**Horizontal**		
62	042, 050, 058, 074, 090	**Power Converter**	495FB, 494MA, 495D
62	010, 018	**DCTUCOM**	TN629B, SN422
62	154, 162, 170	**EAN**	SN423
53, 45 and/or 36	010, 018, 026, 030, 034, 042, 050, 058, 070, 078, 086, 094, 102, 110, 118	**PMU**	SM250, SM251, SM274, SM255, SM256, SM260, SM259, SM257, SM253, SM254, SM261, SM262
53, 45 and/or 36	130, 138, 146, 154, 162, 170, 178	**DCTU Port**	SM248B, SM263, SM264

10.3.4 Configuration

The table below details the configuration of the Directly Connected Test Unit (DCTU).

Circuit Packs	Link/Bus	Connects to...	Method of Operation	State of Operation
DCTUCOM	PICB	SMP	Simplex	Act
	Backplane	EAN		
PMU	Backplane	EAN		
EAN	Backplane	Ports		
	Backplane	PMU		
DCTU Port	MTB	MMSU		

10.3.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the diagnosable components in the Directly Connected Test Unit (DCTU) are not available.

Unavailable Component	Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
DCTUCOM, EAN	Major	No impact.	Stops analog line and trunk testing for voltage, resistance and capacitance.
PMU, DCTU Port	Major	No impact.	Reduces analog line and trunk testing capacity.

10.3.6 Detailed Description

The table below details the functions of the diagnosable components in the Directly Connected Test Unit (DCTU).

Part	Function
DCTUCOM	□ Routes control messages between the SMP and the PMUs.
PMU	□ Tests voltage, resistance, and capacitance in the analog subscriber loop.
EAN	□ Receives and sends control messages between the DCTUCOM, PMU, and DCTU ports.
DCTU Ports	□ Connects the MMSU to the EAN.

10.3.7 Functional Description

10.3.7.1 Functions

The Directly Connected Test Unit (DCTU):

□ Measures DC voltages, resistance, and capacitance in the analog subscriber lines and trunks.

10.3.7.2 Operation

The DCTU interacts with other components to operate the switch.

□ The Figure 10-1 depicts the operation of the DCTU.

Figure 10-1 DCTU Block Diagram

- The table below details how the DCTU measures voltage, resistance, and capacitance in analog loops and trunks.

  The DCTU handles control messages from the SMP. The control messages are bi-directional.

Stage	Description
1	The DCTUCOM receives a control message from the SMP via the PICB.
2	The DCTUCOM routes the control message through the EAN to the PMU via the backplane.
3	The EAN receives the control message and connects the MTB to the PMU via the backplane.
4	The DCTU Port closes the gates.
5	The EAN sends the message to the PMU via the backplane.
6	The PMU: - Receives the control message from the EAN, - Tests the voltage, resistance, and/or capacitance on the circuit that is connected, and - Sends the message that contains the test results to the DCTUCOM via the backplane.
7	The DCTUCOM receives and sends the message to the SMP via the PICB.

10.4 Global Digital Service Function (GDSF)

10.4.1 Basic Description

The Global Digital Service Function (GDSF) is a one circuit pack component. The GDSF is located in an SMPU5 or DSU3 shelf of an SM-2000 cabinet, or CSU shelf of an SM cabinet.

The primary jobs of the GDSF are to:

- Perform three and six port conference calling.
- Perform transmission tests.

- Perform integrated system tests.

10.4.2 Electrical Power

A power converter circuit in each Global Digital Service Function (GDSF) circuit pack controls power for the circuit pack.

10.4.3 Shelf and Circuit Pack Arrangement

The Global Digital Service Function (GDSF) is located in the SMPU5 or DSU3 shelf of an SM-2000 cabinet or the CSU shelf of an SM cabinet.

The following tables detail the horizontal and vertical EQLs, Component Name, Circuit Pack Name, and Component Number of the GDSF:

- The following table details the shelf and circuit pack arrangement of the GDSF hardware components in the SMPU5 shelf of an SM-2000 cabinet.

EQL		Component Name	Circuit Pack Name	Component Number
Vertical	Horizontal			
19	166 and/or 176	**GDSF**	DSC3 or DSC4	UN363 or UN590
28				

- The following table details the shelf and circuit pack arrangement of the GDSF hardware components in the DSU3 shelf of an SM-2000 cabinet.

EQL		Component Name	Circuit Pack Name	Component Number
Vertical	Horizontal			
Various	Various	**GDSF**	DSC3 or DSC4	UN363 or UN590

- The following table details the shelf and circuit pack arrangement of the GDSF hardware components in the CSU shelf of an SM cabinet.

EQL		Component Name	Circuit Pack Name	Component Number
Vertical	Horizontal			
Various	Various	**GDSF**	DSC3	UN363

10.4.4 Configuration

The following table details the configuration of the Global Digital Service Function (GDSF).

Circuit pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
GDSF	PICBs	MCTSI	ACT	Simplex
	PIDBs			

10.4.5 Service Impacts

The following table details the impact on subscriber service and switch performance when Global Digital Service Function (GDSF) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
GDSF	One GDSF circuit pack OOS.	Major	Conferncing circuits will be unavailble if this/these is/are the only GDSF/s equipped. If GDSFs equipped in other SMs available conferencing circuits will be reduced.	Line and trunk tests that use GDSF circuits will be unavailable if this/these is/are the only GDSF/s equipped. If GDSFs equipped in other SMs testing circuits will be reduced.
	All GDSFs circuit packs OOS.	Critical		
	50% or less	Minor	Number of conferencing circuits will be reduced.	Line and trunk testing circuits will be reduced.
	50% or more	Major		

10.4.6 Detailed Description

The following table details the function of the Global Digital Service Function (GDSF).

Part	Function
GDSF	Performs three and six port conference calling.
	Generates and measures various tones to test POTS and ISDN subscriber lines and trunks.

10.4.7 Functional Description

10.4.7.1 Functions

The Global Digital Service Function (GDSF):

- Performs three or six port conference calling.
- Generates and measures various tones to test POTS and ISDN subscriber lines and trunks.

10.4.7.2 Operation

Figure 10-2 depicts the operation of the GDSF.

Figure 10-2 GDSF Block Diagram

The following table details the operation of the GDSF.

The GDSF performs subscriber line and trunk tests.

Stage	Description
1	The GDSF receives a control message from the MCTSI by the PICB.
2	The GDSF sends test tones to the MCTSI by the PIDB.
3	The GDSF receives test results from the subscriber line or trunk through the MCTSI by the PIDB.
4	The GDSF performs appropriate tests on the results that are received.
5	The GDSF sends the test results to the MCTSI by the PICB.

The GDSF connects three and six port conference calls.

Stage	Description
1	The GDSF receives a control message from the MCTSI by the PICB.
2	The GDSF connects the appropriate time slots to the appropriate conference circuit.
3	The GDSF combines the subscriber data and sends the data to the MCTSI by the PIDB.

10.5 Global Digital Service Unit (GDSU)

10.5.1 Basic Description

The Global Digital Service Unit (GDSU) is a multi-circuit pack component. The GDSU is located in a cabinet of an SM.

The primary jobs of the GDSU are to:

- Perform three or six user conferencing, and/or
- Perform transmission tests on subscriber loops and trunks.

10.5.2 Electrical Power

The 495FB power circuit pack controls power for the GDSU. The 495FB power circuit pack is located to the left end of each service group in the GDSU shelf.

10.5.3 Shelf and Circuit Pack Arrangement

The Global Digital Service Unit Component (GDSU) is located in an SM cabinet.

The table below details the shelf and circuit pack arrangement of the GDSU hardware components.

EQL	Component Name	Component Number
016 and 106	**Power**	495FB
024 and 114	**GDSUCOM**	TN128
032 and 122	**TTFCOM (Interface)**	TN302
035 and 130	**TTFCOM (Processor)**	TN305
032, 040, 048, 056, 062, 072, 080, 088, 122, 130, 138, 146, 154, 162, 170, and 178*	**TTFT**	TN303
	TTFR	TN304
	UCONF (2 ports, 3-party)	TN324
	UCONF (5 ports, 3-party)	TN841
	UCONF (2 ports, 6-party)	TN1032
*Location depends on engineering		

10.5.4 Configuration

The table below details the configuration of the Global Digital Service Unit (GDSU).

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
GDSUCOM	PIDB/PICB	MCTSI	Simplex	ACT
	Backplane	TTFCOM		
		UCONF		
TTFCOM (Interface)	Backplane	GDSUCOM	Simplex	ACT
		TTFCOM (Processor)		
TTFCOM (Processor)	Backplane	TTFCOM (Interface)	Simplex	ACT
		TTFT		
		TTFR		
TTFT	Backplane	TTFCOM	Simplex	ACT
TTFR				
UCONF	Backplane	COM	Simplex	ACT

10.5.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the Global Digital Service Unit Component (GDSU) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
GDSUCOM	One side	Minor	May prevent conference calling for testing subscriber lines and/or testing trunks	May reduce conference calling capacity for subscriber lines and/or trunks
	Both sides	Minor	Reduces access to the CONF for subscriber lines and/or trunks	May eliminate conference calling capacity if no other GDSU is available
TTFCOM	One or both sides	Minor	Stops testing of tones for trunks	No impact
UCONF	One or both sides	Minor	May prevent conference calling if only one UCONF is equipped	May prevent conference calling, or reduce conference calling capacity

10.5.6 Detailed Description

The table below details the function of the circuit packs in the Global Digital Service Unit Component (GDSU).

Part	Function
GDSUCOM	Routes subscriber data and control messages between: □ the MCTSI and TTF, and/or □ UCONF circuit packs
TTFCOM (Interface)	Connects the GDSUCOM to the TTFCOM
TTFCOM (Processor)	Controls the operations of the TTFT and TTFR
TTFT	Generates various tones to test subscriber lines
TTFR	Receives and measures tones to test subscriber lines
UCONF	Performs three or six-party conference calling

10.5.7 Functional Description

10.5.7.1 Functions

The Global Digital Service Unit Component (GDSU):

- Performs three or six port user conferencing.
- Performs transmission tests on subscriber loops and trunks.

10.5.7.2 Operation

- The Figure 10-3 depicts the operation of the GDSU.

Figure 10-3 GDSU Block Diagram

- The table below details the operation of the GDSU.

The GDSU performs call conferencing.

Stage	Description
1	The GDSUCOM receives a control message and subscriber data from the MCTSI via the PICB and PIDB.
2	The GDSUCOM routes the message to the appropriate UCONF via the backplane.
3	The UCONF: - Receives the control message and subscriber data, - Combines the subscriber data, and - Sends the subscriber data to the MCTSI through the GDSUCOM.

The GDSU performs transmission tests.

Stage	Description
1	The GDSUCOM receives a control message and subscriber data for a test on a specific line from the MCTSI via the PIDB and PICB.
2	The GDSUCOM routes the control message and subscriber data to the TTFCOM (Interface) via the backplane.
3	The TTFCOM (Interface) sends the control message and subscriber data to the TTFCOM (Processor) via the backplane.
4	The TTFCOM (Processor) receives and routes the control message and subscriber data to the TTFT via the backplane.
5	The TTFT: - Receives the control message and subscriber data, - Generates test tones, and - Sends the tones through the TTFCOM (Processor), TTFCOM (Interface), and GDSUCOM to the MCTSI via the PIDB.
6	The GDSUCOM receives the tones from the MCTSI via the PIDB.
7	The GDSUCOM sends the tones to the TTFCOM (Processor) via the TTFCOM (Interface).
8	The TTFT: - Receives the tones from the TTFCOM (Interface),

	□ Generates a control message, and □ Sends the control message and tones to the TTFR via the backplane.
9	The TTFR: □ Receives the control message, □ Measures the tones, and □ Sends the results of the test to the MCTSI through the TTFCOM (Processor), TTFCOM (interface), and GDSUCOM.

10.6 Integrated Services Test Function (ISTF)

10.6.1 Basic Description

The primary job of the ISTF is to test digital subscriber lines and trunks for maintenance problems.

The ISTF is located in the DSU2 shelf of an SM cabinet. The Integrated Services Test Function (ISTF) is a one circuit pack component.*

NOTE: *The ISTF may be equipped in a DSC3 pack in a DSU3 (SM-2000) or CSU shelf (SM). In the DSC3, the ISTF is on of three possible programmed functions. See the GDSF for more details.

10.6.2 Electrical Power

A power converter circuit in the Integrated Services Test Function (ISTF) circuit pack controls power for the circuit pack.

10.6.3 Shelf and Circuit Pack Arrangement

The ISTF is located in the DSU2 shelf of an SM cabinet.

The table below details the shelf and circuit pack arrangement of the ISTF hardware components.

EQL		Component Name	Component Number
Vertical	Horizontal		
Various	048, 088, 138, 178	**ISTF**	TN833C or TN1054

10.6.4 Configuration

The table below details the configuration of the Integrated Services Test Function (ISTF).

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
ISTF	PIDB/ PICB	MCTSI	Simplex	ACT

10.6.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the Integrated Services Test Function (ISTF) is not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
ISTF	One ISTF	Major	No Impact.	Reduces switch capacity for line and trunk testing
	All ISTFs	Major	Prevents digital subscriber line and trunk testing.	Further reduces switch capacity for line and trunk testing

10.6.6 Detailed Description

The table below details the function of the Integrated Services Test Function.

Part	Function
ISTF	□ Generates digital signals to test digital subscriber lines and trunks for maintenance problems. □ Measures the test results from the subscriber lines and trunks.

10.6.7 Functional Description

10.6.7.1 Functions

The Integrated Services Test Function (ISTF):

- Generates digital signals to test digital subscriber lines and trunks for maintenance problems.
- Measures the test results from the subscriber lines and trunks.

10.6.7.2 Operation

- The Figure 10-4 depicts the operation of the ISTF.

Figure 10-4 ISTF Block Diagram

- The table below details the operation of the ISTF.

  The ISTF tests subscriber lines and trunks.

Stage	Description
1	The ISTF receives control messages from the MCTSI via the PICB.

2	The ISTF generates and sends a digital test message to the MCTSI via the PIDB.
3	The ISTF receives test results from the subscriber line or trunk through the MCTSI via the PIDB.
4	The ISTF evaluates the test results, generates a message and sends the message to the MCTSI via the PICB.

10.7 Local Digital Service Function (LDSF)

10.7.1 Basic Description

The Local Digital Service Function (LDSF) is a one circuit pack component. The LDSF is located in an SMPU5 or DSU3 shelf of an SM-2000.

The primary job of the LDSF is to generate and decode all tones that the SM□2000 uses for call processing.

10.7.2 Electrical Power

The power converter circuit in each LDSF circuit pack controls power for the circuit pack.

10.7.3 Shelf and Circuit Pack Arrangement

The Local Digital Service Function (LDSF) circuit packs are located in a SMPU5 or DSU3 shelf of SM-2000 cabinets.

- The table below details the shelf and circuit pack arrangement of the LDSF circuit packs that the SMPU5 shelf contains in an SM-2000 cabinet.

EQL		Component Name	Circuit Pack Name	Component Number
Vertical	Horizontal			
19, 28	156, 166, 176	**LDSF**	DSC3	UN363, or UN590

- The table below details the shelf and circuit pack arrangement of the LDSF circuit packs that the DSU3 shelf contains in an SM-2000 cabinet.

EQL		Component Name	Circuit Pack Name	Component Number
Vertical	Horizontal			
006	006, 036, 066, 096, 126, 156, 176	**LDSF**	DSC3	UN363, or UN590

10.7.4 Configuration

The table below details the configuration of the Local Digital Service Function (LDSF).

Circuit Pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
LDSF	PICB	CI in the SMPU	ACT	Simplex
	PIDB	DX in the TSIU		

10.7.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the Local Digital Service Function (LDSF) component is not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
LDSF	One circuit pack	Major	When the volume of traffic is low, there may be no impact on service.	Reduces the capacity of the SM-2000 to provide dial-tone
	Multiple circuit packs		When the volume of traffic is high, dial-tone may be delayed.	
	All LDSFs in	Critical	Stops call processing in the	Reduces call processing capacity in

	one SM		SM-2000	the switch

10.7.6 Detailed Description

The table below details the function of the Local Digital Service Function (LDSF).

Part	Function
LDSF	□ Generates call processing tones for digits and call progress alerts in the SM-2000 □ Decodes call processing tones for routing calls in the SM-2000

10.7.7 Functional Description

10.7.7.1 Functions

The Local Digital Service Function (LDSF):

- Generates call processing tones for digits and call progress alerts in the SM-2000
- Decodes call processing tones for routing calls in the SM-2000

10.7.7.2 Operation

- The Figure 10-5 depicts the operation of the LDSF.

Figure 10-5 LDSF Block Diagram

- The table below details the operation of the LDSF.

  The LDSF handles subscriber data for call processing.

Stage	Description

1	The LDSF receives tones from the TSI via the PIDB.
2	The LDSF sends a control message to the SMP via the PICB.

The LDSF generates tones for trunks and subscriber lines.

Stage	Description
1	The LDSF receives control messages from the SMP via the PICB.
2	The LDSF generates and sends tones to the TSI via the PIDB.

10.8 Local Digital Service Unit (LDSU)

10.8.1 Basic Description

The Local Digital Service Unit (LDSU) is a two circuit pack component. The LSDU is located in a MCTU2 or MCTU3 shelf of an SM.

The primary job of the LDSU is to generate and decode all tones for call processing in the SM.

10.8.2 Electrical Power

A power converter circuit in each Local Digital Service Unit (LDSU) circuit pack controls power for the circuit pack.

10.8.3 Shelf and Circuit Pack Arrangement

The Local Digital Service Unit (LDSU) is located in an MCTU2 or MCTU3 shelf of an SM cabinet.

- The table below details the shelf and circuit pack arrangement of the LDSU circuit packs that the MCTU3 shelf contains in an SM cabinet.

EQL		Component Name	Circuit Pack Name	Component Number
Vertical	Horizontal			
028	094 and 186	**LDSU**	DSC2	TN833, or TN1890

- The table below details the shelf and circuit pack arrangement of the LDSU circuit packs that the MCTU2 shelf contains in an SM cabinet.

EQL		Component Name	Circuit Pack Name	Component Number
Vertical	Horizontal			
028 and 036	168	**LDSU**	DSC2	TN833, or TN1890

10.8.4 Configuration

The table below details the configuration of the Local Digital Service Unit (LDSU).

Circuit Pack	Link/Bus	Connects to ...	Method of Operation	State of Operation
LDSU	LDSUB	DI in the MCTSI	Simplex	ACT
	PICB	CI in the MCTSI		

10.8.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the Local Digital Service Unit (LDSU) component is not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
LDSU	One side	Major	May result in slow dial tone	Reduces call processing capacity
	Both sides	Critical	Stops dial tone to all subscriber lines that connect to the SM	Further reduces call processing capacity

10.8.6 Detailed Description

The table below details the function of the Local Digital Service Unit (LDSU).

Part	Function
LDSU	□ Generates call processing tones for digit and call progress alerts in an SM □ Decodes call processing tones for routing calls in an SM

10.8.7 Functional Description

10.8.7.1 Functions

The Local Digital Service Unit (LDSU):

- Generates call processing tones for digits and call progress alerts in an SM.
- Decodes call processing tones for routing calls in an SM.

10.8.7.2 Operation

- The Figure 10-6 depicts the operation of the LDSU.

Figure 10-6 LDSU Block Diagram

- The table below details the operation of the LDSU.

The LDSU handles subscriber data for call processing.

Stage	Description
1	The LDSU receives tones from the TSI via the LDSUB.
2	The LDSU sends a control message to the SMP via the PICB.

The LDSU generates tones for trunks and subscriber lines.

Stage	Description

1	The LDSU receives control messages from the SMP via the PICB.
2	The LDSU generates and sends tones to the TSI via the LDSUB.

10.9 Modular Metallic Service Unit (MMSU)

10.9.1 Basic Description

The Modular Metallic Service Unit (MMSU) is a one to four shelf unit. The MMSU is located in an SM or SM-2000.

The primary jobs of the MMSU are to:

- Test subscriber lines and trunks.
- Monitor and control various scan and distribute points in the *5ESS*® switch.

10.9.2 Electrical Power

The 494LA power circuit pack controls power for all of the circuit packs in the MMSU shelf.

10.9.3 Shelf and Circuit Pack Arrangement

The Modular Metallic Service Unit Component (MMSU) is located in the SM or SM-2000 cabinet.

Table 10-1 details the shelf and circuit pack arrangement of the MMSU.

Table 10-1 MMSU Shelf and Circuit Pack Arrangment

EQL		Component Name	Component Number
Vertical	**Horizontal**		
Various	010 and 098	**Power**	494LA
Various	018 and 106*****	**MSUCOM**	TN879
Various	026, 114, 082, and 170******	**MA**	TN138
		DIST	TN221
		DFTAC	TN1040
		GDXC	TN880
		ALIT	TN328B, TN329B, TN330B
		SCAN	TN220B
		SLIM2	TN1422
Various	090 and 178	**MTIBAX**	TN138*******

NOTE: *****In an MMSU growth shelf, EQL numbers 18 and 106 are blank.

******The location of the circuit packs depends on engineering.

*******The function for the TN138 is determined by the EQL in the MMSU shelf.

10.9.4 Configuration

The table below details the configuration of the Modular Metallic Service Unit (MMSU).

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
MSUCOM	PICB	MCTSI	Simplex	ACT
MA	Backplane	MSUCOM	Duplex	ACT
	MTB	TU		
		LU		
		DCTU		
		MDF		
MTIBAX	MTIB	MTIBAX in another MMSU shelf	Duplex	ACT
		PROTO		
DIST	SD leads	MDF	Duplex	ACT
	Backplane	MSUCOM		
DFTAC	Backplane	MSUCOM	Duplex	ACT

	Trunk test line	MDF		
	Trunk access line			
	Sleeve control and ground lead			
GDXC	Backplane	ALIT	Duplex	ACT
ALIT	Backplane	MSUCOM	Duplex	ACT
	Backplane	MTIBAX		
	Backplane	GDX		
SCAN	Backplane	MSUCOM	Duplex	ACT
	Scan wires	MDF		
SLIM2	Backplane	MSUCOM	Duplex or Simplex	ACT
	Backplane	MTIBAX		

10.9.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the Modular Metallic Service Unit Component (MMSU) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
MMSUCOM	One side	Major	No impact	Reduces subscriber line testing and access to alarms
	Both sides	Major	No impact	Prevents all subscriber line testing, and Disables alarms and scans
MA	One side	Minor	No impact	Reduces test access to the assigned peripheral units
	Both sides	Major	No impact	Further reduces test access to the assigned peripheral units
GDXC	One side	Major	No impact	Reduces the accuracy of results from line tests
	Both sides	Major	No impact	Reduces the accuracy of results from line tests
DIST and SCAN	One pack	Major	No impact	Reduces notification of office alarms
	All packs	Major	No impact	Prevents notification of office alarms
DFTAC	One pack	Major	No impact	Reduces access to subscriber lines for testing at the MDF
	All packs	Major	No impact	Further reduces access to subscriber lines for testing at the MDF
ALIT and SLIM2	One pack	Minor	No impact	Reduces line testing of faulty subscriber lines
	all packs	Major	No impact	Prevents line testing of faulty subscriber lines

10.9.6 Detailed Description

The table below details the function of the diagnosable circuit packs in the Modular Metallic Service Unit Component (MMSU).

Part	Function
MSUCOM	Generates control messages. Routes control messages between the MCTSI and test packs.
MA	Sets up a metallic path for testing between the test packs and subscriber line or trunk.
MTIBAX	Sets up a metallic path between additional MMSU shelves and the PROTO.
GDXC	Compensates for normal current leakage and resistance in subscriber lines that are tested by the ALIT.
DIST	Routes control messages from the MSUCOM to the appropriate alarm units.
DFTAC	Connects trunks to the DCTU to test trunk and subscriber lines.
ALIT	Tests for maintenance problems in subscriber lines, which include current leaks and pressurized cable failures.

SCAN	Detects changes of power and state of service in hardware components.
SLIM2	Tests subscriber lines and subscriber premise equipment.

10.9.7 Functional Description

10.9.7.1 Functions

The Modular Metallic Service Unit Component (MMSU):

- Tests subscriber analog lines and trunks, and
- Monitors scan and controls distribute points in the *5ESS*® switch.

10.9.7.2 Operation

The Figure 10-7 depicts the operation of the MMSU.

Figure 10-7 MMSU Block Diagram

The table below details the operation of the MMSU.

The MMSU tests subscriber lines and trunks in the host office.

Stage	Description
1	The MSUCOM receives a control message, requesting a line or trunk test, from the MCTSI by the PICB.
2	The MSUCOM sends the message to the ALIT or SLIM2 by the backplane.
3	The ALIT or SLIM2 receives the message and sends the appropriate test to the MA by the backplane.
4	The MA receives and sends the test to the appropriate peripheral by the MTB.
5	The MA receives the test result from a peripheral by the MTB.
6	The MA sends the test result to the ALIT or SLIM2 by the backplane.
7	The ALIT or SLIM2 receives and reads the test results from the MA.
8	The ALIT or SLIM2 sends the test results to the MSUCOM by the backplane.
9	The MSUCOM sends the test results to the MCTSI by the PICB and PIDB.

NOTE: The GDXC automatically compensates for normal electric current leakage on subscriber lines that are tested by the ALIT.

The MMSU tests subscriber lines and trunks at a remote site.

Stage	Description
1	The MSUCOM receives a control message, requesting a line or trunk test, from the MCTSI by the PICB.
2	The MSUCOM sends the message to the DFTAC by the backplane.
3	The DFTAC receives and sends the message to the MA by the backplane.
4	The MA receives and sends the message to the DCTU by the MTB.
4	The MA receives a test message from the DCTU by the MTB.
5	The MA passes the test message to the DFTAC by the backplane.
6	The DFTAC sends the test message to the appropriate subscriber line or trunk at the MDF by the MDF access pair.
7	The DFTAC receives and sends the test results from the subscriber line or trunk to the MSUCOM by the backplane.
8	The MSUCOM sends the test results to the MCTSI by the PICB and PIDB.

The MMSU monitors and controls scan and distribute points in the *5ESS*® switch.

Stage	Description
1	The SCAN detects changes in the state of the scan point by the scan point loop in the MDF.
2	The SCAN sends a message about the change of state to the MSUCOM by the backplane.
3	The MSUCOM receives and sends the message to the MCTSI by the PICB.

10.10 Service Announcement System (SAS)

10.10.1 Basic Description

The Service Announcement System (SAS) is a two to five circuit pack component. The SAS is located in the DSU2 shelf of an SM or SM-2000 cabinet.

The primary job of the SAS is to provide general recorded announcements.

10.10.2 Electrical Power

A power converter circuit in each SAS circuit pack controls power for the circuit pack.

10.10.3 Shelf and Circuit Pack Arrangement

The Service Announcement System (SAS) is located in the DSU2 shelf of an SM or SM-2000 cabinet.

The table below details the shelf and circuit pack arrangement of the SAS hardware components in the DSU2 shelf of a switching module cabinet.

EQL	Component Name	Component Number
Service Group 0		
018	**DSC**	TN1841
028, 038, 048	**MEM**	TN1842
Service Group 2		
058	**DSC**	TN1841
068, 078, 088	**MEM**	TN1842
Service Group 1		
108	**DSC**	TN1841
118, 128, 138	**MEM**	TN1842
Service Group 3		
148	**DSC**	TN1841
158, 168, 178	**MEM**	TN1842

10.10.4 Configuration

The table below details the configuration of the Service Announcement System (SAS).

Circuit Pack	Link/Bus	Connect to ...	Method of Operation	State of Operation
DSC	PICB &PIDB	MCTSI	Simplex	Active
MEM	Backplane	DSC	Simplex	Active

10.10.5 Service Impacts

The table below details the impact on subscriber service and switch performance when the Service Announcement System (SAS) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
SAS	One or more circuit packs	Major	slows subscriber access to general recorded announcements.	Reduces general recorded announcement capability.

10.10.6 Detailed Description

The table below details the components of the Service Announcement System (SAS).

Part	Function
DSC	Routes control messages and subscriber data between the MCTSI and MEM.
MEM	Stores general recorded announcements.

10.10.7 Functional Description

10.10.7.1 Functions

The Service Announcement System (SAS)

- Provides general recorded announcements.

10.10.7.2 Operation

The SAS interacts with other components to operate the *5ESS*® switch.

- The Figure 10-8 depicts the operation of the SAS.

Figure 10-8 SAS Block Diagram

- The table below details the operation of the SAS.

The SAS provides general recorded announcements.

Stage	Description
1	The DSC receives a control message from the MCTSI via the PICB.
2	The DSC sends the control message to the appropriate MEM via the backplane.
3	The MEM sends the appropriate announcement to the MCTSI through the DSC via the PIDB.

11. LINKS AND BUSES

11.1 C-LINK

11.1.1 Basic Description

The Communication Link (CLNK) is a path that consists of hardware components that are used to route control time slots during call processing.

The primary job of the CLNK is route control time slot messages for call processing.

11.1.2 Electrical Power

Power control information is contained in the sections that relate to the MMP, DMI, TMS, NLI, DLI, and MCTSI.

11.1.3 Shelf and Circuit Pack Arrangement

The hardware that is used for the CLNK is located in the following:

- **NLI**: backplane of a TSIU shelf in the SM-2000 cabinet (SMC).
- **CTSNS**: backplane of the NLI.
- **DLI**: MCTU shelf of the SM cabinet (SMC).
- **DIP switch**: backplane of the DLI.
- **NCT/NCT2 Link**: fiber between the switching module and CM.
- **TMS**: TMSU, EBUS, and CMCU shelves of a CM cabinet.
- **MIB**: cable between the MSPU and CMCU shelves.
- **DMI**: CMCU shelf of a CM cabinet.
- **MMP**: MSPU shelf of a CM cabinet.

The following table details the shelf and circuit pack arrangement of the CLNK hardware components.

EQL		Component Name	Component Number
Vertical	**Horizontal**		
47	00 and 10	**CTSNS**	BKD4
36*****	084 and 098	**DIP Switch (Paddleboard)**	MGI 9558
28 ******	084 and 176		
NOTE: The DLI, NLI, TMS, DMI and MMP are detailed in separate hardware descriptions. *****MCTU2 only. ******MCTU3 only.			

11.1.4 Configuration

The hardware components that the Communications Link (CLNK) consists of include the following:

- CTSNS (SM-2000 only),
- NLI (SM-2000 only),

- DIP switch (SM only),
- DLI (SM only),
- NCT/NCT2 link,
- TMS,
- MIB,
- DMI, and
- MMP.

The following table details the configuration of the Communication Link (CLNK).

Components	Link/Bus	Connects to ...	Method of Operation	State of Operation
CTSNS	Backplane	TSIS0	Duplex	ACT/STBY
DIP switch	Backplane	DLI	Duplex	ACT/STBY
		SMP		
NOTE: The configuration of the DLI, NLI, TMS, DMI and MMP are detailed in separate hardware descriptions.				

11.1.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Communication Link (CLNK) components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
CLNK	One, two, or three CLNKs	Major	No impact.	No impact.
	Four or eight CLNKs	Critical	Stops inter-switching module call processing for the switching module that is isolated from the switch.	Reduces inter-switching module call processing capacity.

11.1.6 Detailed Description

The following table details the function of the components in the Communication Link (CLNK).

Part	Function
CTSNS	Stores control time slot addresses for the SM-2000.
NLI	Receives and sends control messages.
DIP switch	Stores control time slot addresses for the switching modules.
DLI	Receives and sends control messages.
NCT Link	Passes control messages between the switching modules and the CM.
TMS	Switches control messages.
MIB	Passes control messages between the DMI and the MMP.
DMI	Receives and sends control messages.
MMP	Routes control messages.

11.1.7 Functional Description

11.1.7.1 Functions

The Communication Link (CLNK) routes control messages for call processing.

11.1.7.2 Operation

Figure 11-1 depicts the operation of the CLNK.

Figure 11-1 CLNK Block Diagram

The following table details the operation of the CLNK.

The CLNK routes control messages between the switching modules and the CM. The control message path is bi-directional.

Stage	Description
1	□ In an SM, the DLI receives a control message from the SMP by the backplane. □ In an SM-2000, the NLI receives a control message from the TSIS by the backplane.
2	□ In an SM, the DLI sends the message to the TMS by the NCT link. □ In an SM-2000, the NLI sends the message to the TMS by the NCT2 link.
3	The TMS switches and sends the message to the DMI by the FLI bus.
4	The DMI receives and sends the message to the MMP by the MIB.
5	□ When the message is addressed to a switching module to which the MMP is connected, then the MMP routes the message to the DMI by the MIB, or □ When the message is addressed to the CMP, AM or any other switching module, then the MMP routes the message to the IOMI by the IOMI bus.

11.2 Control and Data Access Link (CDAL)

11.2.1 Basic Description

The Control and Data Access Link (CDAL) is a paddle-board and wire. The CDAL is located in the CM cabinets 5 and 6.

The primary job of the CDAL is to connect the FPC to the DMI for control and diagnostic access.

The CDAL provides a cross-connect for MSGS 0 and 1 and ONTC 0 and 1.

11.3 Directly Connected Peripheral Interface Data Bus (DPIDB)

11.3.1 Basic Description

The Directly Connected Peripheral Interface Data Bus (DPIDB) is a cable. DPIDBs are located in switching module cabinets.

The primary job of the DPIDB is to carry data messages between the PSU and the AIU , IDCU, or ISLU2.

11.3.2 Functional Description

11.3.2.1 Functions

The Directly Connected Peripheral Interface Data Bus (DPIDB) carries data messages between the AIU, IDCU, or ISLU and the PSU.

11.4 Dual Serial Channel (DSCH)

11.4.1 Basic Description

The Dual Serial Channel (DSCH) is a cable. The DSCH is located in the backplane between the AM and CM cabinets and the AM and CNI cabinets .

The primary jobs of the DSCH are to:

- Connect the AM and CM for maintenance and routing information,
- Connect the AM and CNI for C7 signaling,
- Connect the DMA and IOP for human machine interface,
- Connect the DMA and DFC for long-term bulk storage, and
- Connect the DMA and ASM-DCI for 5ESS switch administrative and maintenance support.

The DSCH provides cross-connects for:

- AM 0 and 1 and MSGS 0 and 1,
- AM 0 and 1 and CNI 0 and 1,
- DMA 0 and 1 and IOP 0 and 1, and
- DMA 0 and 1 and DFC 0 and 1.
- DMA 0 and 1 and ASM-DCI 0 and 1.

11.5 Ethernet Interface

11.5.1 Basic Description

The Session Initiation Protocol (SIP) for Packet Trunking feature introduces a 100BaseT Ethernet connection between the TN13 in the PSU2 and the layer 2 switch or router. The interface is made up of an LLE2 paddle board located on the backplane of the PSU2 behind the TN13 pack and a Category 5 cable

with RJ-45 connectors. The cable provides the physical connection between the LLE2 paddle board and the layer 2 switch or router.

11.5.2 Functional Description

11.5.2.1 Functions

The Ethernet interface between the PSU2 and the layer 2 switch or router carries SIP signaling messages which are used to setup and tear down the bearer path for IP packet trunk calls.

11.6 Inter - RSM Communication Link (ICL)

11.6.1 Basic Description

The Inter-RSM Communication Link (ICL) is a two circuit pack and two twisted-wire pair component. The ICL is located between two SM cabinet at a multi-module RSM site.

The primary job of the ICL is to carry subscriber data and control messages.

11.6.2 Shelf and Circuit Pack Arrangement

The Inter-RSM Communication Link (ICL) is located between two SM cabinets at a multi-module RSM site.

The following table details the shelf and circuit pack arrangement of the ICL hardware components.

EQL	Component Name	Component Number
Backplane of an RDFI	**ABAM**	Not applicable
Various	**CDFI**	TN1612

11.6.3 Configuration

The following table details the configuration of the Inter-RSM Communication Link (ICL).

Component	Link/Bus	Connects to...		Method of Operation	State of Operation
ABAM (wire)	Not applicable.	CDFI in one SM	CDFI in another SM	Simplex	ACT
CDFI	ABAM	CDFI			
	PICB	MCTSI			
	PIDB				

11.6.4 Functional Description

11.6.4.1 Functions

The Inter-RSM Communication Link (ICL) carries subscriber data and control messages between SMs in an multi-module RSM site.

11.6.4.2 Operation

The ICL interacts with other components to operate the switch.

Figure 11-2 depicts the operation of the ICL.

Figure 11-2 ICL Block Diagram

The following table details the operations of the ICL.

The ICL carries subscriber data and control messages.

Stage	Description
1	The CDFI in one SM at the multi-module RSM site receives subscriber data and control messages from the MCTSI by the PICB and PIDB.
2	The CDFI sends the subscriber data and control messages to a CDFI in another SM at the multi-module RSM site by the ABAM.
3	The CDFI receives the subscriber data and control messages from the CDFI in another SM by the ABAM.
4	The CDFI sends the subscriber data and control messages to the MCTSI by the PICB and PIDB.

11.7 Network Control and Timing (NCT) Link

11.7.1 Basic Description

The Network Control and Timing Link (NCT Link) is an optical cable. The NCT2 is located in the between the CM and SM or SM-2000 cabinets.

The primary job of the NCT is to connect the SM or SM-2000 and CM for switching time slots.

11.8 Peripheral Control and Timing (PCT) Link

11.8.1 Basic Description

The Peripheral Control and Timing (PCT) link is an optical cable and paddle board component. The PCT link is located in the TSIU4 and the peripheral unit backplanes.

The primary job of the PCT link is to carry control, data, and maintenance messages between the TSIU and the DNU-S, OIU, or PSU2.

11.8.2 Electrical Power

Not applicable.

11.8.3 Shelf and Circuit Pack Arrangement

The Peripheral Control and Timing (PCT) link is located in the TSIU4, some peripheral unit backplanes and OFI circuit pack face plates.

The following table details the shelf and circuit pack arrangement of the PCT link hardware components.

Component Name	Component Number
PLI Paddle Board	BKD2
	BKD10*****
COT	982T
NOTE: *****Used for new OIU.	

11.8.4 Configuration

The following table details the configuration of the Peripheral Control and Timing (PCT) link.

Component		Connects...		Method of Operation	State of Operation
PCT Link	PLI Paddle Board	TSIU4	DNU-S, OIU, and PSU2	Duplex	ACT/STBY
	optical cable				
	COT Paddle Board				

11.8.5 Service Impacts

The following table details the impact on subscriber service and switch performance when the Peripheral Control and Timing Link (PCT) link components are not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
PCT link	One side	Major	No impact.	No impact.
	Both sides	Critical	May reduce call processing. The service impact depends on the number of calls the PCT link receives.	Reduces call processing capacity.

11.8.6 Functional Description

11.8.6.1 Functions

The Peripheral Control and Timing Link (PCT Link) performs the following:

- Carries control, data, and maintenance messages between the TSIU4 and the DNU-S, OIU, or PSU2.
- In OIU applications, it is also used to carry pump code to OFI circuit packs.

11.8.6.2 Operation

The PCT link interacts with other components to operate the switch. The following table details the operation of the PCT link.

The PCT link carries data, control, and maintenance messages. These data, control, and maintenance messages are bi-directional. The table below details the messages that the PCT link receives from the TSIU4.

Stage	Description
1	The PLI paddle board receives a message from the TSIU4.
2	The PLI paddle board converts and sends the message to the COT paddle boards or OFI packs over the PCT link cable.
3	The COT paddle boards or OFIs receive and convert the messages.

4	The COT paddle board sends the message to the DNU-S.

11.9 Peripheral Interface Control Bus (PICB)

11.9.1 Basic Description

The Peripheral Interface Control Bus (PICB) is a cable. The PICB is located in a switching module cabinet.

The primary job of the PICB is to carry control messages between the SMP and the peripheral and service units.

11.9.2 Configuration

The following table details the configuration of a Peripheral Interface Control Bus (PICB).

Component	Connects...		Method of Operation	State of Operation
PICB	CI in the SMP to	COMDAC in the AIU	Duplex	ACT / STBY
	CI in the SMP to	DSC in the DSU3/DSU2		
	CI in the SMP to	CF in the PSU		
	CI in the SMP to	DFI in the DLTU		
	CI in the SMP to	CC in the ISLU2		
	CI in the SMP to	COMC in the LU		
	CI in the SMP to	CDI in the TU		
	CI in the SMP to	GDSUCOM in the GDSU		
	CI in the SMP to	COMC in the MMSU		
	CI in the SMP to	COM in the IDCU		
	CI in the SMP to	COM in the DCTU		

11.9.3 Service Impacts

The following table details the impact on subscriber service and switch performance when the Peripheral Interface Control Bus (PICB) is not available.

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
PICB	One PICB	Major	Impact depends on the operational state of the MCTSI.	Impact depends on the operational state of the MCTSI.
	All PICBs	Critical	Stops all call processing for the peripheral unit that is connected.	Remove the entire peripheral unit from service.

11.9.4 Functional Description

11.9.4.1 Functions

The Peripheral Interface Control Bus (PICB) performs the following:

- Carries control messages and clock pulses between the SMP and the switching module peripheral and service units.
- Carries maintenance messages from the peripheral and service units to the SMP.

11.10 Peripheral Interface Data Bus (PIDB)

11.10.1 Basic Description

The Peripheral Interface Data Bus (PIDB) is a twisted-pair cable. PIDBs are located in switching module cabinets.

The primary job of the PIDB is to carry data messages between the TSI and the peripheral and service units.

11.10.2 Configuration

The following table details the configuration of the Peripheral Interface Data Bus (PIDB).

Wires	Connects...		Method of Operation	State of Operation
PIDB	TSI to	COMDAC in the AIU	Duplex	ACT / STBY
	TSI to	DFI in the DLTU		
	TSI to	DF in the PSU		
	TSI to	CD in the ISLU2		
	TSI to	COMC in the LU		
	TSI to	DFI in the DLTU		
	TSI to	CDI in the TU		
	TSI to	CF in the PSU		
	TSI to	All service groups in a DSU3/DSU2.		
	TSI to	GDSUCOM in the GDSU		

11.10.3 Service Impacts

When a PIDB or DPIDB is faulty, then the MCC screen displays the peripheral and/or the MCTSI that is connected to the PIDB or DPIDB as out-of-service. Go to the peripheral or MCTSI for service impact information.

11.10.4 Functional Description

11.10.4.1 Functions

The Peripheral Interface Data Bus (PIDB) performs the following:

- Carries data messages and clock pulses from the TSI to the switching module peripheral and service units.
- Carries data messages between the switching module peripheral and service units and the TSI.

12. MISCELLANEOUS UNITS

12.1 Echo Canceler and Signaling Unit (ECSU)

12.1.1 Basic Description

The Echo Canceller Signaling Unit (ECSU) is a one shelf component. The ECSU is located in an SM-2000 cabinet (LTP) at a long-distance or wireless site.

The primary job of the ECSU is to remove echo from long-distance or wireless calls.

12.1.2 Electrical Power

A power converter circuit in each Echo Canceller Signaling Unit (ECSU) circuit pack controls power for the circuit pack.

12.1.3 Shelf and Circuit Pack Arrangement

The Echo Canceller Signaling Unit (ECSU) is located in an LTP cabinet of an SM-2000.

Table 12-1 details the shelf and circuit pack arrangement of the ECSU hardware components.

Table 12-1 ECSU Shelf and Circuit Pack Arrangement

EQL		Component Name	Component Number
Vertical	**Horizontal**		
Various	006	**Power Start**	SN346B
Various	014, 030, 046, 062, 078, 094, 110, 126, 142, and 158	**EC5**	TN1825
Various	022, 038, 054, 070, 086, 102, 118, 134, 150, and 166	**ECD**	TN1512

12.1.4 Configuration

Table 12-2 details the configuration of the Echo Canceller Signaling Unit (ECSU).

Table 12-2 ECSU Configuration

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
EC5	PICB	SMP	Simplex	ACT
	PIDB	TSI		
		DFI		
	Backplane	EC XTNDR		
ECD	Backplane	EC	Simplex	ACT

12.1.5 Service Impacts

Table 12-3 details the impact on subscriber service and switch performance when the Echo Canceller Signaling Unit (ECSU) components are not available.

Table 12-3 ECSU Service Impact

Unavailable Component		Alarm Level	Impact on Subscriber Service	Impact on Switch Performance
ECSU	One pack	Major*	Reduces call processing capacity for long-distance calls.	Removes up to 24 trunks from service.
	Multiple packs	Major*	Further reduces call processing capacity for long-distance calls.	Removes up to 24 trunks from service for each additional circuit pack that goes out-of-service.
NOTE: *When an EC goes out-of-service, then the DFI that connects to the EC is alarmed.				

12.1.6 Detailed Description

Table 12-4 details the function of the circuit packs in the Echo Canceller Signaling Unit (ECSU).

Table 12-4 ECSU Functional

Part	Function
EC5	Removes echo from long-distance or wireless calls.
ECD	Provides the EC5 with the additional power to remove echo from subscriber calls.

12.1.7 Functional Description

12.1.7.1 Functions

The Echo Canceller Signaling Unit (ECSU) removes echo from long-distance or wireless calls.

12.1.7.2 Operation

The Figure 12-1 depicts the operation of the ECSU.

Figure 12-1 ECSU Block Diagram

Table 12-5 details the operation of the ECSU.

The ECSU handles subscriber data and control messages from C7 signaling trunks.

Table 12-5 ECSU Operation

Stage	Description
1	The EC5 receives: □ Subscriber data from the TSI by the PIDB, and

	□ Control messages from the SMP by the PICB.
2	The EC5 removes echo from the subscriber data. (When the ECD is equipped, then the ECD enables the EC5 to remove additional echo from the message.)
3	The EC5 sends the subscriber data to the DFI by the PIDB.

12.2 Office Alarm Unit (OAU)

12.2.1 Basic Description

The Office Alarm Unit (OAU) is shelf unit. The OAU is located in a miscellaneous cabinet of the *5ESS*® switch.

The primary job of the OAU is to convert signals from the scan points into visual and audible office alarms in the central office of the *5ESS*® switch.

12.2.2 Electrical Power

The 131N1A Control and Display circuit pack controls power for the Office Alarm Unit (OAU).

12.2.3 Shelf and Circuit Pack Arrangement

The Office Alarm Unit (OAU) is located in a miscellaneous cabinet in the *5ESS*® switch.

Table 12-6 details the shelf and circuit pack arrangement of the OAU hardware components.

Table 12-6 OAU Shelf and Circuit Pack Arrangement

EQL		Component Name	Component Number
Vertical	**Horizontal**		
04	128	**Audible Alarm Circuit**	TN137B
04	52,72,86, and 118	**Applique Circuit**	TN867

12.2.4 Configuration

Table 12-7 details the configuration of the Office Alarm Unit (OAU).

Table 12-7 OAU Configuration

Sub-Modules	Link/Bus	Connected to ...	Method of Operation	State of Operation	Service Groups
Applique Circuit	Wire	MDF	Simplex	ACT	No
		IOP			
Audible Alarm Circuit	Wire	IOP			
		Pilot Lamps			
		Audible Alarm Panel			
		Scan Applique Circuit			

12.2.5 Service Impacts

When the Office Alarm Unit (OAU) loses service, subscriber service or switch performance is not impacted. However, no audible and/or visual alarms are displayed for other faulty *5ESS*® switch components or central office equipment.

12.2.6 Detailed Description

Table 12-8 details the function of the circuit packs in the Office Alarm Unit (OAU).

Table 12-8 OAU Circuit Functions

Part	Function
Audible Alarm	Activates audible and visual alarms in the *5ESS*® switch.
Scan Applique	Monitors various scan points in the *5ESS*® switch.

12.2.7 Functional Description

12.2.7.1 Functions

The Office Alarm Unit (OAU) converts signals from the scan points into visual and audible office alarms in the central office of the *5ESS*® switch.

12.2.7.2 Operation

The Figure 12-2 depicts the operation of the OAU.

Figure 12-2 OAU Block Diagram

Table 12-9 details the operation of the OAU. The OAU activates office alarms.

Table 12-9 OAU Functional

Stage	Description
1	The Applique Circuit receives a signal from the scan point via the scan leads.
2	The Applique Circuit sends the signal to the Audible Alarm Circuit via the backplane.
3	The Audible Alarm Circuit: □ Activates an alarm in the *5ESS*® central office via alarm wires. □ Changes state of scan lead to IOP.

13. CABINET POWER

The primary job of the power distribution frames is to distribute -48VDC to the *5ESS*® switch cabinets. There are three different kinds of power distribution frames currently in use:

- Power Control and Fuse Distribution (PCFD)
- Global Power Distribution Frame (GPDF)
- Local Power Distribution Cabinet (LPDC)

All three contain up to 24 fuses per bus. Before any fuse can be installed in a PCFD, a charge probe must be used so that the fuse is not subjected to charging currents and become cleared. This can significantly increase system downtime. The GPDF and LPDC eliminate the charge probe. The GPDF accommodates 25A fuses. The LPDC accommodates fuses ranging in size from 25 to 70 amps.

13.1 Power Control and Fuse Distribution (PCFD)

13.1.1 Basic Description, PCFD

The Power Control and Fuse Distribution (PCFD) cabinet is located in the *5ESS*® switch.

The primary job of the PCFD is to distribute -48VDC to the *5ESS*® switch cabinets.

NOTE: Some documents and drawings refer to the PCFD to as the PCDF.

13.1.2 Electrical Power, PCFD

One or more PCFDs supply power to the *5ESS*® switch as follows:

Unit	Number of Buses	Fuses Per Bus	Blown Fuse Indication	Charging Panel Required?	Output Fuse Size
PCFD	2	24	Indicating Fuse	Yes	20

13.1.3 Configuration, PCFD

The following table details the configuration of the PCFD.

Component	Link/Bus	Connects to ...	Method of Operation	State of Operation
Fuse Panel	A and B involt power feeders	Office or building batteries	Duplex	N/A
	Metallic wires	*5ESS*® switch cabinets		
Control Panel	Metallic wire	OAU	Simplex	N/A
		Office or building batteries		

13.1.4 Service Impacts, PCFD

The following table details the impact on subscriber service and switch performance when the PCFD components are not available.

Unavailable Component		Alarm Level	Impact on Switch Performance
PCFD	One Bus (A or B)	Major	Reduces call processing capacity.
	Both Buses (A & B)	Critical	Reduces call processing capacity.
Individual fuse or circuit breaker		Major	Depends on the component that connects to the faulty fuse, refer to the hardware

		description for the component that is connected to the faulty fuse.

13.1.5 Detailed Description, PCFD

The following table details the components of the PCFD.

Part	Function
Fuse Panel	The Alarm Filter Fuse Panel performs the following: □ Distributes -48VDC to the *5ESS*® switch cabinets. □ Monitors fuse and circuit breaker status. □ Reports blown fuses to the Control Panel.
Control Panel	The Control Panel reports blown fuses to the Office Alarm Unit (OAU).

13.1.6 Functional Description, PCFD

13.1.6.1 Functions

The Power Control and Fuse Distribution (PCFD) distributes -48VDC to the *5ESS*® switch cabinets.

13.1.6.2 Operation

Figure 13-1 depicts the operation of the PCFD.

Figure 13-1 PCFD Block Diagram

The following table details the operation of the PCFD.

Stage	Description
1	The fuse panels receive -48VDC from the office battery plant by the A and B power bus bars.
2	The fuse panels distribute -48VDC to the *5ESS*® switch cabinets by the A and B power bus wires.

13.2 Global Power Distribution Frame (GPDF)

13.2.1 Basic Description, GPDF

The Global Power Distribution Frame (GPDF) is a cabinet. The GPDF is located in the *5ESS*® switch.

The primary job of the GPDF is to distribute -48VDC to the *5ESS*® switch cabinets.

13.2.2 Electrical Power, GPDF

One or more GPDFs supply power to the *5ESS*® switch as follows:

Unit	Number of Buses	Fuses Per Bus	Blown Fuse Indication	Charging Panel Required?	Output Fuse Size
GPDF	2	24	Luminated LED	No	25

13.2.3 Configuration, GPDF

The following table details the configuration of the GPDF.

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
Fuse Panel	A and B involt power feeders	Office or building batteries	Duplex	N/A
	Metallic wires	*5ESS*® switch cabinets		
		Alarm Panel Circuit Module 1		
Alarm Panel	Metallic wires	Fuse panel	Simplex	N/A
		Office Alarm Circuit		

13.2.4 Service Impacts, GPDF

The following table details the impact on subscriber service and switch performance when the GPDF components are not available.

Unavailable Component		Alarm Level	Impact on Switch Performance
GPDF	One bus (A or B)	Major	Reduces call processing capacity.
	Both buses (A and B)	Critical	Reduces call processing capacity.
Individual fuse or circuit breaker		Major	Depends on the component that is impacted - refer to the section that is associated with the specific component.

13.2.5 Detailed Description, GPDF

The following table details the functions of the components in the Global Power Distribution Frame (GPDF).

Part	Function
Fuse Panel	Distributes -48VDC power to the *5ESS*® switch cabinets.
Alarm Panel	The Alarm Panel performs the following: □ Monitors fuse status. □ Reports faulty fuses to the OAU.

13.2.6 Functional Description, GPDF

13.2.6.1 Functions

The Global Power Distribution Frame (GPDF) distributes -48VDC to the *5ESS*® switch cabinets.

13.2.6.2 Operation

Figure 13-2 depicts the operation of the GPDF.

Figure 13-2 GPDF Block Diagram

The following table details the operation of the GPDF.

Stage	Description
1	The fuse panels receive -48VDC from the office battery plant by the A and B power bus bars.
2	The fuse panels receive and distribute -48VDC to the *5ESS*® switch cabinets by the A and B power bus wires.

13.3 Local Power Distribution Cabinet (LPDC)

13.3.1 Basic Description, LPDC

The Local Power Distribution Cabinet (LPDC) is a cabinet. The LPDC is located in the *5ESS*® switch.

The primary job of the LPDC is to distribute -48VDC to the *5ESS*® switch cabinets.

13.3.2 Availability, LPDC

The availability of the LPDC is the 5E16.2 Software Release.

13.3.3 Electrical Power, LPDC

One or more LPDCs supply power to the *5ESS*® switch as follows:

Unit	Number of Buses	Fuses Per Bus	Blown Fuse Indication	Charging Panel Required?	Output Fuse Size
LPDC	2	24	Indicating Fuse	No	25 - 70

13.3.4 Configuration, LPDC

The following table details the configuration of the LPDC.

Circuit Packs	Link/Bus	Connects to ...	Method of Operation	State of Operation
Fuse Panel	A and B involt power feeders	Office or building batteries	Duplex	N/A
	Metallic wires	*5ESS*® switch cabinets		
		Alarm Panel Circuit Module 1		
Alarm Panel	Metallic wires	Fuse panel	Simplex	N/A
		Office Alarm Circuit		

13.3.5 Service Impacts, LPDC

The following table details the impact on switch performance when the LPDC components are not available.

Unavailable Component		Alarm Level	Impact on Switch Performance
LPDC	One bus (A or B)	Major	Reduces call processing capacity.
	Both buses (A and B)	Critical	Reduces call processing capacity.
Individual fuse or circuit breaker		Major	Depends on the component that is impacted - refer to the section that is associated with the specific component.

13.3.6 Detailed Description, LPDC

Table 13-1 details the functions of the components in the LPDC.

Table 13-1 LPDC Functions

Part	Function
Fuse Panel	There are four distribution panels that are numbered from top to bottom as shown in figure 13-3 that distributes -48VDC power to the *5ESS*® switch cabinets. Each distribution panel has 48 fuses divided into two buses A and B, see Figure 13-4 for the front fuse panel layout and Figure 13-5 for the rear fuse panel layout. The fuse and ground lug orientation for Bus A and Bus B, mount the lugs in the right position.
Alarm Panel	Monitors fuse and circuit breaker status. Reports faulty fuses to the OAU.

Figure 13-3 shows the LPDC cabinet front and back layout.

Figure 13-3 LPDC Cabinet Front and Back Layout

Figure 13-4 for the front layout and Figure 13-5 for the rear layout.

Figure 13-4 LPDC Front Panel Layout

Figure 13-5 LPDC Rear Panel Layout

13.3.7 Functional Description, LPDC

13.3.7.1 Functions

The LPDC distributes -48VDC to the *5ESS*® switch cabinets.

13.3.7.2 Operation

Figure 13-6 depicts the operation of the LPDC.

Figure 13-6 LPDC Block Diagram

The following table details the operation of the LPDC.

Stage	Description
1	The fuse panels receive -48VDC from the office battery plant by the A and B power bus bars.
2	The fuse panels receive and distribute -48VDC to the *5ESS*® switch cabinets by the A and B power bus wires.

14. Hardware Acronym Expansions

Table 14-1 provides a list of *5ESS*® Switch hardware acronyms and their expansions.

Table 14-1 Hardware Acronym Expansions

Component Acronym	Component Name
ABAM	Digital carrier cross-connect cabling
ACT	Active
ADM	Add/Drop Multiplexers
ADSL	Asynchronous Digital Subscriber Line
AFM	ATM (Asynchronous Transfer Mode) Feeder Multiplexer
AIP	*AnyMedia*® Interface Platform
AIU	Access Interface Unit
ALIT	Automatic Line Insulation Test
AM	Administrative Module
AMA	Automatic Message Accounting
AP	Application Processor
APPL	Application Pack
APC	Application Controller
APP	Application
APS	Automatic Protection Switching
AP TAP	Application Test Access Pack
ASM	Administrative Services Module
ASU	Alarm Services Unit
BAIU	Broadband Access Interface Unit
BD	Board
B-Link	Second internal bus in an analog line unit
BSN	Bus Service Node
C7	Common Channel Signalling - UTI Mode 7
CB	Control Bus
CC	Central Control
CCI	Common Control Interface
CCIO	Central Control Input/Output
CCP	Common Control Processor
CCS	Common Channel Signalling
CD	Common Data
CDAL	Control and Diagnostic Access Link
CDFI	Communication Link Digital Facility Interface
CDI	Control and Data Interface
CDOUT	Common Data Out
CF2	Control Fanout, Model 2
CHBD	Channel Board
CI2	Control Interface, Model 2
CIB	Control Interface Bus
CIDB	Control Interface Data Bus
C-Link	Cross Communication Link
CLK	Clock
CLK CTRL	Clock Control
CM	Communications Module
CM2	Communications Module, Model 2
CM3	Communications Module, Model 3
CMCU	Communications Module Control Unit
CMP	Communications Module Processor
CMPU	Communications Module Processor Unit
CMU2	Communications Module, Unit 2
CNI	Common Network Interface
COMC	Common Control
COMDAC	Common Data and Control
CORE	Core
CSI	Control and Synchronization Interface
CSU	Cache Store Unit
CSU	Combined Services Unit
CTPL	Control Time Slot and Pump Link
CTS	Control Time Slot
CTSNS	Control Time Slot Number Selector
CU	Control Unit
CUPS	Control Unit Power Switch
DCTU	Directly Connected Test Unit
DCTUCOM	Directly Connected Test Unit-Common Circuit
DDSBS	Duplex Dual Serial Bus Selector
DF	Data Fanout
DF2	Data Fanout 2

DFC	Disk File Controller
DFI2	Digital Facility Interface, Model 2
DFI-H	DFI - Host
DFI-R	DFI - Remote
DFTAC	Distribution Frame Test Access Controller
DI	Data Interface
DIP Switch	Dual Inline Package Switch
DLI	Dual Link Interface
DLN	Direct Link Node
DLTU	Digital Line and Trunk Unit
DLTU-R	Digital Line and Trunk Unit - Remote
DMA	Direct Memory Access
DMI	Dual Message Interface
DNU-S	Digital Network Unit - Synchronous Optical Network (SONET)
DPIDB	Directly Connected Peripheral Interface Data Bus
DS1	Digital Signal Rate 1
DS3	Digital Signal Rate 3
DSC	Digital Service Circuit
DSCH	Dual Serial Channel Bus
DSCP	Digital Service Port
DSL	Digital Subscriber Line
DSL AP	Digital Subscriber Loop Application Pack
DSU2	Digital Service Unit, Model 2
DSU3	Digital Service Unit, Model 3
DSX	Digital Signal Cross-Connect
DX	Data Expansion
EAI	Emergency Action Interface
EAIU	Expansion Access Interface Unit
EAN	Equipment Access Network
EBUS	Emitter-Coupled Logic Bus
EC XTNDR	Echo Canceller Extender
ECD	Equipment Configuration Database
ECS	Echo Canceller Signaling circuit pack
ECSU	Echo Canceller and Signaling Unit
ELI	Electric Line Interface
EX	Expansion Slot
FAB	Fabric
FAC	Front Access Cabling
FIDB	Facility Interface Data Bus
FIU	Facility Interface Unit
FLI	Foundation Link Interface
FPC	Foundation Peripheral Controller
FPGA	Field Programmable Gate Array
GDSF	Global Digital Service Function
GDSU	Global Digital Service Unit
GDSUCOM	Global Digital Service Unit Controller
GDXACC	Gated-Diode Access Cross-Connect
GPDF	Global Power Distribution Frame
GQPH	General QLPS Protocol Handler
GWI	Gateway Interface
HLSC	High-level Service Circuit
HSM	Host Switching Module
ICB	Internal Control Bus
ICL	Inter-RSM Communications Link
IDB	Internal Data Bus
IDCU	Integrated Digital Carrier Unit
IOMI	Input/Output Microprocessor Interface
IOP	Input/Output Processor
IOPC	Input/Output Controller
IOPPS	Input/Output Power Switch
IP	Initiation Protocol
ISDN	Integrated Services Digital Network
ISDN AP	Integrated Services Digital Network Application Pack
ISLU2	Integrated Services Line Unit, Model 2
ISLUCD	ISLU Common Data
ISLUMAN	ISLU Metallic Access Network
ISLUHLSC	ISLU High Level Service Circuit
ISTF	Integrated Services Test Function
IUN	Interprocess Message Switch User Node
LBD	Line Board
LDSF	Local Digital Service Function
LDSU	Local Digital Service Unit
LDSUB	Local Digital Service Unit Bus
LI	Line Interface
LIDB	Line Interface Data Bus

LIB	Link Interface Bus
LN	Link Node
LP	Line Pack
LP C	Line Pack, Coin
LP TAP	Line Pack, Test Application Pack
LP U	Line Pack, U-Interface
LP Z	Line Pack, Z-Interface
LS	Local System
LSI	Loop Side Interface
LSM	Local Switching Module
LTP	Logical Test Port
LU 3	Line Unit, Model 3
MA	Metallic Access
MAN	Metallic Access Network
MAS	Main Store
MASB	Main Store Bus
MASC	Main Store Controller
MASU	Main Store Update
MCHL	Main Channel Link
MCC	Master Control Center
MCP	Messaging Control and Pump
MCTSI	Module Controller and Time Slot Interchanger
MCTU	Module Controller and Time Slot Interchanger Unit
MDF	Main Distribution Frame
MEM	Memory
MFFU	Modular Fuse and Filter Unit
MH	Message Handler
MIB	Message Interface Bus
MIBC	Message Interface Bus Controller
MM	Main Memory
MMP	Module Message Processor
MMSU	Modular Metallic Service Unit
MMU	Memory Management Unit
MSC	Message Switch Controller
MSCU	Message Switch Control Unit
MSGS	Message Switch
MSPP	Message Switch Peripheral Processor
MSPU	Message Switch Peripheral Unit
MSUCOM	Metallic Service Unit Common Board
MTB	Metallic Test Bus
MTIB	Metallic Test Interface Bus
MTIBAX	Metallic Test Interconnect Bus Access
MTTY	Maintenance Teletype
MTTYC	Maintenance Teletype Controller
MUX	Multiplexer
NCC	Network Clock and Control
NCLK	Network Clock
NCOSC	Network Clock Oscillator
NCT	Network Control and Timing
NCT2	Network Control and Timing, Model 2
NLI	Network Link Interface
NTS	Network Time Slot
OA&M	Operations, Administration and Maintenance
OC-3	Optical Carrier Level-3
OC-3c	Optical Carrier - Level 3 Concatenated
ODD	Office Dependent Data
ODF	Optical Distribution Frame
OFI	Optical Facility Interface
OFI - IP	Optical Facility Interface - Internet Protocol
OFI PGs	Optical Facility Interface Protection Groups
OFI - TDM	Optical Facility Interface - Time Division Multiplex
OHCTL	Overhead Controller
OIU	Optical Interface Unit
OIU-IP	Optical Interface Unit - Initiation Protocol
ONTC	Office Network and Timing Complex
ONTCCOM	Office Network and Timing Complex Common
OOS	Out-of-Service
OPB	Optical Paddle Board
ORM	Optically Integrated Remote Switching Module
OSC	Oscillator
PB	Packet Bus
PC	Peripheral Community
PCADB	Peripheral Control And Data Bus
PCAMB	Peripheral Control and Maintenance Bus
PCFD	Power Control Frame Distribution

PCGSI	Personal Computer Graphic Services Interface
PCDC	Power Converter with Display and Control
PCT	Peripheral Control and Timing
PCTLI	Peripheral Control and Timing Link Interface
PF	Packet Fanout
PF2	Packet Fanout, Model 2
PG	Protection Group
PH	Protocol Handler
PHDB	Protocol Handler Data Bus
PHPPC	Protocol Handler PowerPC
PI	Packet Interface
PI2	Packet Interface, Model 2
PICB	Peripheral Interface Control Bus
PIDB	Peripheral Interface Data Bus
PLI	Peripheral Link Interface
PMU	Precision Measuring Unit
POS	Packet Over SONET
POTS	Plain Old Telephone Service
POTS AP	Plain Old Telephone Service Application Pack
PPC	Pump Peripheral Controller
PPP Link	Point to Point Protocol Link
PSIUCOM	Packet Switch Interface Unit Common Control
PSSDB	Port Switch and Scanner-Distribution
PSU	Packet Switch Unit
PSU2	Packet Switch Unit, Model 2
PSUCOM	Packet Switch Unit Common
PSUPH	Packet Switch Unit Protocol Handler
PTI	PIDB Transmission Interface
PTSB	PIDB (Peripheral Interface Data Bus)Time Slot
PWR	Power
QGL	Quad-Link Packet Switch - QLPS Gateway Processor Link
QGP	QLPS Gateway Processor
QLI	Quad Link Interface
QLI2	Quad Link Interface, Model 2
QLPS	Quad-Link Packet Switch
RCLK	Remote Clock
RCLKU	Remote Clock Unit
RCOSC	Remote Clock Oscillator
RCOXC	Remote Clock Oscillator Cross-Couple
RCREF	Remote Clock Reference
RCXC	Remote Clock Cross-Couple
RDFI	Remote Digital Facility Interface
REF	Reference
RG	Ring Generator
RGB	Ring Generator Bus
RISLU2	Remote Integrated Services Line Unit, Model 2
RLI	Remote Link Interface
RMMSU	Remote Modular Metallic Service Unit
ROP	Read Only Printer
RPCN	Ring Peripheral Controller Node
RRCLK	RISLU Remote Clock
RS	Remote System
RSM	Remote Switching Module
SAS	Service Announcement System
SC	Scan
SCAN	Scan pack
SCCS	Switching Control Center System
SCSDC	Scanner and Signal Distributor Controller
SCSI	Small Computer System Interface
SD	Signal Distributor
SDLC	Synchronous Data Link Controller
SFI	STSX-1 Facility Interface
SIP	Session Initiation Protocol
SIP PH	SIP Protocol Handler
SLIM2	Subscriber Loop Instrument Measurement Model 2
SLI	STSX-1 Link Interface
SM/SM-2000	Switching Module
SM-2000	Switching Module-2000
SMP	Switching Module Processor
SMPU	Switching Module Processor Unit
SONET	Synchronous Optical Network
SONET MUX	SONET Multiplexer
SS7	Signaling System 7
STBY	Standby
STCL	Serial Time Slot Interchanger (TSI) Control Link

STPH	Signal Transfer Point Protocol Handler
STM-0	Synchronous Transport Module Level - 0
STM-1	Synchronous Transport Module Level - 1
STS-1	Synchronous Transport Signal Level-1
STS-3	Synchronous Transport Signal Level-3
STS-3c	Synchronous Transport Signal Level-3 Concatenated
STSX-1	Synchronous Transport Signal Electrical - 1
SUB	Shelf Utility Board
SUIB	Subunit Interface Bus
SYSCTL	System Controller
TAC	Test Access Controller
TAU	Test Access Unit
TBCU	Test Bus Control Unit
TDM	Time Division Muliplex
TGS	Synchronous Timing Generator
TIDB	Transmission Interface Data Bus
TLWS	Trunk and Line Work Station
TMS	Time Multiplexed Switch
TMSF	Time Multiplexed Switching Fabric
TMSFP	Time Multiplexed Switch Fabric Pair
TMSU	Time Multiplexed Switch Unit
TMSU4	Time Multiplexed Switching Unit, Model 4
TMSX	Time Multiplexed Switching Expansion
TMUX	T-Carrier Multiplexer
TRCU	Transmission Rate Converter Unit
TRM	Transmissionless Remote SM
TSI	Time Slot Interchanger
TSICNTL	Time Slot Interchanger Controller Bus
TSICOM	TSI Common Control
TSIS	Time Slot Interchanger Slice
TSIU4	Time Slot Interchanger Unit Model 4
TSIU4-2	Time Slot Interchanger Unit Model 4-2
TST	Test
TTF	Transmission Test Facility
TTFCOM	Transmission Test Facility Common Circuit
TTFR	Transmission Test Function Receive
TTFT	Transmission Test Function Tone
TTYC	Teletype Controller
TU	Trunk Unit
UART	Universal Asynchronous Receiver Transmitter
UC	Utility Circuit
UCONF	Universal Conference Circuit
XDX	Extended Data Expansion
XAIU	Extended Access Interface Unit

List of Figures

Figure 13-6 : LPDC Block Diagram

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