CHAPTER 9

NO. 1 ELECTRONIC SWITCHING SYSTEM

9.1 INTRODUCTION

The No. 1 ESS is an automatic telephone switching system that has

(a) The capacity for serving up to 65,000 customer lines

(b) Features which are expected to permit minimum maintenance

(c) The ability to complete connections between subscribers in a fraction of the time required by electromechanical type switching systems.

(d) The versatility to provide new features and services economically

The No. 1 ESS is a common control type system. It differs radically from electromechanical switching systems in the devices that it uses as well as in the techniques that it employs. Throughout the system, solid-state electronic devices are used extensively. Their high operating speeds permit a relatively small amount of equipment to perform all the control functions. A major feature is the greatly reduced time required to complete connections between customers.

Some of the basic techniques employed in this system are:

(a) Stored program control: The functions to be performed by the system are specified by programs consisting of appropriate combinations of precisely defined instructions. Examples of such instructions are: "Observe the supervisory state of a specified group of lines," "Add two specified quantities," and "Observe the sign of a specified quantity and decide accordingly which of two alternatives to follow." The program instructions, suitably encoded, are stored in a memory unit from which they are transmitted one at a time to the control circuitry for execution. Thus, the operation of the system can be altered considerably by program changes.

(b) <u>Functional concentration</u>: The system equipment is concentrated in a small number of highly efficient units, each specialized in some broad system function such as control, input, output, memory, etc. The result is an overall system organization that is conceptually very simple.

(c) <u>Time shared control</u>: A single control unit directs the operation of all other system units in accordance with the program instructions. Using electronic devices, this control unit can operate at speeds much higher than the rate at which events associated with a single call occur. Consequently, the control equipment is time-shared by all the calls handled by the system. This is accomplished by subdividing the work required to process a call into small segments and by interleaving these segments with those associated with other calls. In addition, certain operations can be performed concurrently on behalf of a number of calls.

(d) <u>Modular design</u>: Traffic-dependent units are provided in modular blocks so that growth in a given office, or differences in traffic among offices, can be accommodated economically and conveniently.

(e) <u>Plug-in equipment units</u>: In major portion of the equipment, circuit components such as transistors, resistors, etc., are mounted on circuit packs, which are plug-in units with printed wiring. Faulty circuit packs can be quickly replaced.

(f) <u>Duplication and automatic maintenance</u>: To insure continuity of service, duplication of equipment is provided for a system unit (or portion thereof) whose failure would affect a large number of customers. This is true of most system units because of the functional concentration previously mentioned. Under normal conditions, both units of a duplicate pair operate side-by-side in response to the same input information but only one of the two is given active status. By continuously compairing the outputs of duplicate units and by other means, it is possible to detect the existence of a malfunction within the system. The unit at fault is automatically identified by appropriate programs and is taken out of service. While the system continues to provide telephone service, an appropriate diagnostic program submits the faulty unit to a thorough sequence of tests aimed at pinpointing the trouble within one or a few plug-in units. The results of the tests are printed out by the system via a teletypewriter. A "dictionary" is used by the

maintenance man to translate the diagnostic printout into the identity of the plug-in unit(s) at fault. Additional ease of maintenance results from the use of 7-foot, single-sided frames which eliminate the need for ladders.

Included among the features to be provided by this system are: 2- and 4-wire switching, local switching with connections to all types of systems, toll and tandem, switching, and special services such as CENTREX, wide area telephone service (WATS), and wide area data service (WADS).

Some of the new customer services which may be provided are:

(a) Abbreviated or Speed Dialing: A customer can place calls to one of a group of frequently called numbers by dialing an abbreviated code instead of the seven or more digits that would normally be required.

(b) Dial Conference: A customer can establish a conference call, involving up to four parties, without operator assistance.

(c) Add-On: A customer can add a third party to an established connection.

(d) Call Waiting Service: A customer whose line is busy is informed that an incoming call is waiting. The customer is allowed to hold the present connection while answering the new call.

(e) Variable Transfer: A customer activates this service by dialing a special code followed by the directory number of the station to which his incoming calls are to be transferred. The customer deactivates this service by dialing an appropriate code.

(f) Preset Transfer: A customer activates this service by dialing a special code followed by a digit that specifies to which of eight stations all his incoming calls are to be transferred. The customer deactivates this service by dialing an appropriate code.

Floor space requirements are considerably less than equivalent installations of electromechanical systems.

This system is compatible with existing station equipment and existing local and toll switching machines. It may be used as a growth or dial replacement unit without the necessity of station modifications and with a minimum of trunking changes at the distant offices.

A. PRINCIPLES OF OPERATION

The major No. 1 ESS equipments and their corresponding functions are briefly described below (see Figure 9-1).

1. Program Store

The program store (PS) stores the instructions that guide the system step-by-step in the performance of its operations. The PS also contains translation information regarding lines and trunks. This information is used to convert a directory number into an equipment location or vice versa. Translations are also used to derive routing and charging information, class of service, type of ringing, special services, and other items of fixed information pertaining to individual lines or trunks.

The PS is said to be a semipermanent memory because its contents can be altered only by external means.

2. Call Store

The call store (CS) provides the means for recording various types of information that later can be read, altered, or erased. Since the CS can write as well as read information, it is said to be a temporary or erasable memory.

The CS derives its name from the fact that it is mainly used to store information relating to calls in progress. The stored information includes:

(a) Busy-idle status of network links,
(b) Digits being received,
(c) Digits to be outpulsed,
(d) Billing information to be recorded on an AMA magnetic tape, or
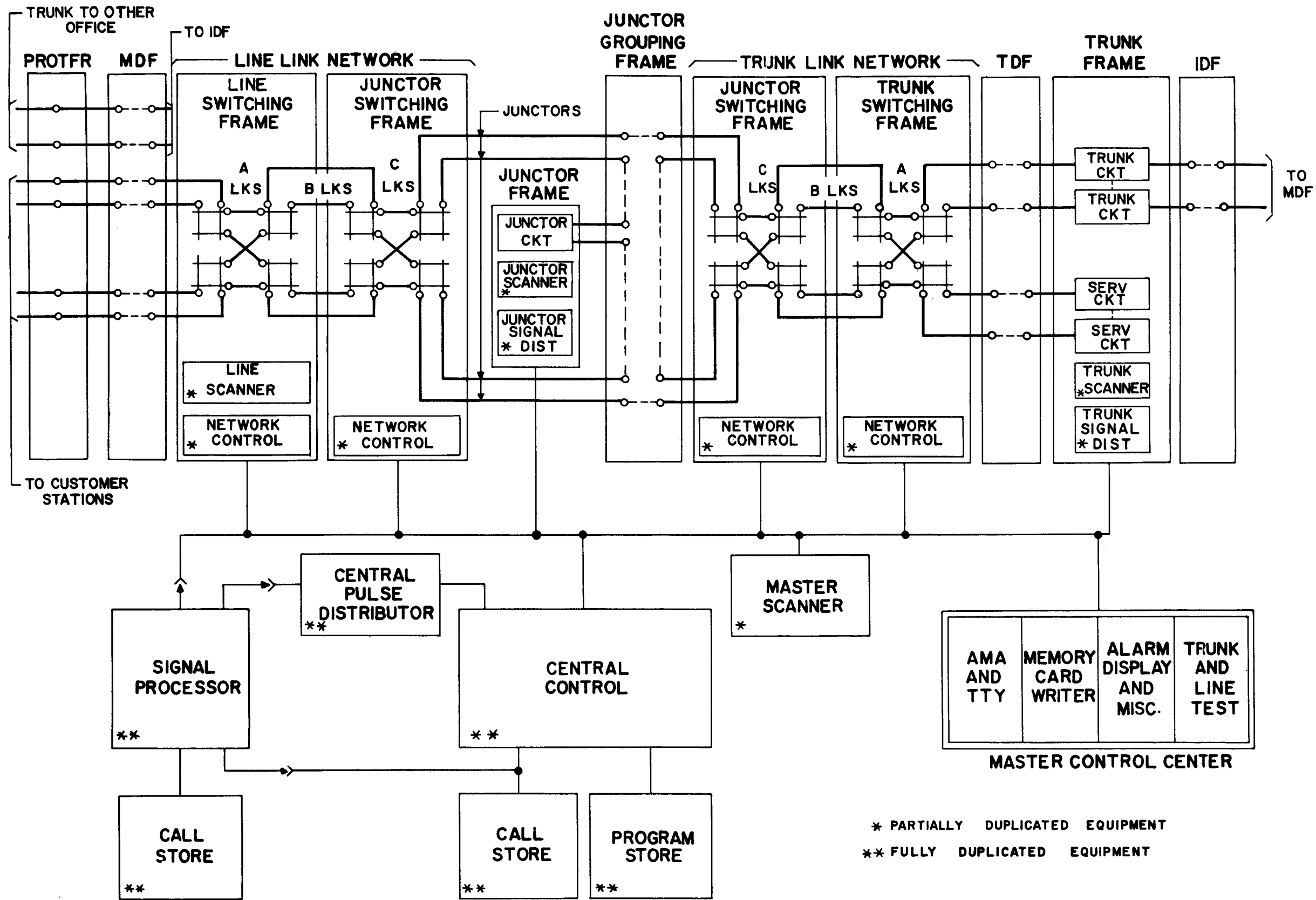(e) Results of diagnostic tests.

Figure 9-1 Block Diagram - No. 1
Electronic Switching System

Another important use of the CS is associated with recent changes of translation information. The superseding information is stored in the temporary memory until it is incorporated in the translation information of the PS. This means that the system must always consult the recent change information of the CS before referring to the translation information in the PS.

3. Central Control

The central control (CC) is a high-speed data-processing unit that controls the actions of all other system units. It interprets and executes instructions received from the program store, normally, at the rate of one instruction every 5.5 usec. The execution of an instruction may involve:

(a) An operation to be carried out within the CC itself, such as the addition or comparison of two quantities, or

(b) A request to some other unit for action or information.

In all cases, the CC determines the location (or address) of the next instruction to be obtained from the program store (PS).

4. Bus System

A group of leads, referred to as a bus, provides a common highway that serves a multiplicity of units. A gating scheme allows the bus to be time-shared by the different units it serves.

5. Central Pulse Distributor

The central pulse distributor (CPD) is used to transmit pulse signals for high-speed control actions. The signals are used to control:

(a) Relays in trunk and service circuits such as dial pulse transmitters or digit receivers,

(b) Various maintenance and test points, or

(c) Lamps and relays in the master control center (MCC).

The CPD is also used to send enable pulses that
activate scanners, signal distributors, network
controllers, teletypewriters, and AMA recorders.
These units are referred to as peripheral units.
The transmission of information to peripheral
units takes place over a common group of wires, or
bus. An enable pulse from a CPD singles out the
particular peripheral unit that must respond to
the information on the common bus.

A CPD selects and pulses the particular output
lead specified by information received from CC.

6. Scanners

The scanners are current sensing devices. The
interrogate and readout wires of a scanner are
similar to the primary-secondary windings of a
transformer.

Line scanners and junctor scanners are used to
supervise lines and junctor circuits, respectively.
Trunk scanners supervise trunk circuits and service
circuits. Via the master scanner, the system can
observe various points within the individual units.
This may be done for one of several reasons:

(a) To perform a diagnostic test,

(b) To verify the proper execution of an action
    previously requested, or

(c) To recognize existing conditions in order to
    take appropriate steps.

The conditions observed are transmitted back to CC.

7. Signal Distributors

The signal distributors (SD) serve to operate or
release magnetically latching relays in various
junctor, trunk, or service circuits. Since they
are mainly relay controlled, they are used only
in applications with limited speed requirements.

An SD receives from CC information specifying
a particular relay to be operated or released.
The SD selects the appropriate lead and sends a
signal to operate or release the relay.

8. Switching Network

The switching network provides the means to connect lines, trunks, and various service circuits such as pulse receivers or transmitters. For any connection between two network terminations, the path required is determined by CC which then sends the appropriate information to the switching network.

The switching network is made up of line link networks (LLN) and trunk link networks (TLN) interconnected by junctors. An LLN connects customer lines or PBX trunks to junctors. A TLN connects interoffice trunks or service circuits to junctors.

Each LLN or TLN involves four stages of switching, that is, a path through it involves three links connected by four pairs of metallic contacts or crosspoints (ferreeds).

9. Trunk and Service Circuits

The trunk circuits of the No. 1 ESS are considerably simpler than those of electromechanical systems. Their functions are limited mainly to supervision and transmission. All other functions of conventional trunks such as pulsing, charging, timing, etc., are delegated either directly to the program control or to the service circuits, which in turn are under program control. Service circuits include customer dial pulse and TOUCH-TONE receivers, tone circuits, ringing circuits, circuits for transmitting or receiving information, coin control circuits and other similar circuits.

The detection of conditions within these circuits is done by CC via the trunk scanner. The control of relays and other devices within the trunk and service circuits is also done by CC using the trunk SD or the CPD. There are very few instances of autonomous control within trunk and service circuits.

10. Master Control Center

The master control center (MCC) is made up of five independent parts:

(a) Teletypewriter system (TTY)

(b) Automatic message accounting (AMA) recorder

(c) Memory card writer

(d) Alarms, displays and miscellaneous controls

(e) Trunk and line test panel.

A teletypewriter provides the means for obtaining information from the system in the form of a page printout and, conversely, for typing information into the system. Examples of inputs to the system are changes in translation information to be recorded temporarily in the recent change area of the CC CS and requests for various maintenance checks under program control. Examples of outputs from the system are results of routine maintenance checks and of diagnostic tests when errors or faults occur. Traffic records are collected and summarized in the CS. Periodically they are printed out via a teletypewriter. Requests for certain traffic records may be made by typing appropriate messages into the system via teletypewriter.

Automatic message accounting in the No. 1 ESS will be compatible with Bell System electronic data processing (EDP) centers. While a call is in progress, the billing information is accumulated in temporary memory. Later, it is transferred to a magnetic tape as a single assembled entry for the call. The entire process is under control of the program.

The memory card writer is used to update periodically the translation information in the program store in order to incorporate recent changes recorded in the CS. By means of the memory card writer, the appropriate information is written on a spare set of memory cards by magnetizing or demagnetizing their magnetic spots, as required. These cards are then used to replace corresponding cards of the program store.

Lamp displays at the MCC show the status of major equipment units. When trouble occurs, audible and visible alarms are given and the general location of the trouble is indicated. Associated with the displays are keys and switches used in emergencies to assign active status to selected units. Keys for line load control and emergency manual service are also provided.

The trunk and line test panel contains facilities to remove from service any outgoing trunk, service circuit, or customer line and to test it. It is also used to dispose of permanent signals.

9.2 SWITCHING LOGIC IN SOLID STATE DEVICES

Unlike the stepper switches in the Step-by-Step System and the motor-driven shafts, clutches and cams of the Panel System or the relays and the relay-like crossbar switches and the "electrical circuits" which operated them, the No. 1 ESS uses "logic circuits" to achieve connecting patterns in its switching process. To establish a talking path between telephones could be viewed as the stage-by-stage progression of simple logical relations AND and OR. For example, consider a lamp plugged into a wall socket controlled by a wall switch. The lamp will not light unless both the lamp switch AND the wall switch are turned on. On the other hand, take the action of the dome light of an automobile which lights if one of the front doors OR the other is opened. Relays can be wired to open or close contacts in the same fashion and these simple logical relations can be repeated as often as necessary to form a highly complex system that decides complicated logical questions.

A. LOGIC CIRCUITS

In switching systems, for every set of "inputs" there is a corresponding set of "outputs." The internal circuitry that connects inputs to outputs consists of paths interconnecting discrete-valued (digital) devices such as relays, diodes, transistors, etc. The function of these devices is to "switch" (open or close) the interconnecting paths in predetermined patterns as required by the input information. The simplest control conditions are two valued, that is, they are in an "on" or "off," "open" or "closed," condition. For this reason, switching circuits are based primarily on "two-valued devices." Another fundamental characteristic of switching systems is their ability to "remember," that is, remain in a certain state until changed by some means. "Memory" makes it possible to combine present inputs with past history so that the processing of information can take into account the time involved relationships.

B. BINARY AND OCTAL NUMBERING SYSTEMS

The No. 1 ESS uses both a binary and octal numbering system. The binary system employes only two digits - a "0" and a "1", and is readily adapted to two-condition type electronic switching components that operate in "on" and "off" modes. Programs in the form of binary digits are stored in the memory portions of the electronic switching system while equipment and circuit numbering arrangements are arranged in the octal system which uses a radix of eight. Both numbering systems, however, can readily be converted to either base and also to the decimal system.

C. SEMICONDUCTOR DEVICES

Semiconductor diodes and resistors are used for the No. 1 ESS AND and OR gate circuits. However, diodes do not provide either gain or inversion, consequently, other switching devices must be employed for these two purposes.

A diode behaves like a low resistance when forward-biased and a high resistance, when back-biased. The low and high resistance states of a diode are often referred to as the "conducting" and the "nonconducting" states respectively. The change from one state to the other occurs in a few hundreds of a microsecond. Figure 9-2 shows the usual circuit symbol for a diode. The arrow points in the direction of the conventional current flow with a forward bias on the diode terminal. Diodes act as good conductors with

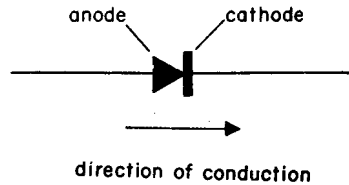anode   cathode

direction of conduction

Figure 9-2 Diode Symbol

forward bias voltage applied and perform as insulators with reverse potentials. A typical No. 1 ESS 10,000 line telephone office contains over 200,000 diodes of eight different types which are used for logic switching, energy storage, voltage level shifting, memory access isolation, voltage regulation and numerous other applications.

The transistor has a number of advantages over that of a tube; for example, it can operate at greater speeds, is more reliable and has a low power requirement. Like the semiconductor diode, the transistor is also used as a two-state device. It is, however, a much more versatile device than the diode because of its gain characteristics. But, whether it is used in an amplifier, an inverter, a flip-flop or a gate circuit, the transistor may be viewed as a switch. Furthermore, the impedance of this switch can be made to vary from tens of megohms to a fraction of an ohm, which at this low value, can be considered as approaching the ohmic value of a metallic contact. Switching times are in the order of 50 nanoseconds (a nanosecond is one billionth of a second).

There are two basic types of transistors: N-P-N and P-N-P. The symbols for these two types are given in Figure 9-3.

NPN   PNP

E —   — C   E —   — C

B   B

Figure 9-3 Transistor Symbols

The No. 1 ESS makes exclusive use of the N-P-N transistor. However, except for a reversal in the direction of currents and in the polarity of voltages, the P-N-P transistor functions in the same manner.

9.13

The transistor has three terminals; the emitter (E), the collector (C), and the base (B). A very rough analogy can be drawn between a transistor and a vacuum tube triode. In this analogy, the emitter corresponds to the cathode, the collector to the plate and the base to the grid. In the vacuum tube, the flow of electrons from the cathode to the plate is controlled by signal conditions applied to the grid; in the transistor, the flow of electrons from the emitter to the collector is controlled by signal conditions applied to the base.

D. BASIC CIRCUIT CONFIGURATIONS

The basic building block for the circuitry of the No. 1 ESS is the AND-NOT (NAND) gate shown in Figure 9-4; it is generally known as low-level logic (LLL) circuit.
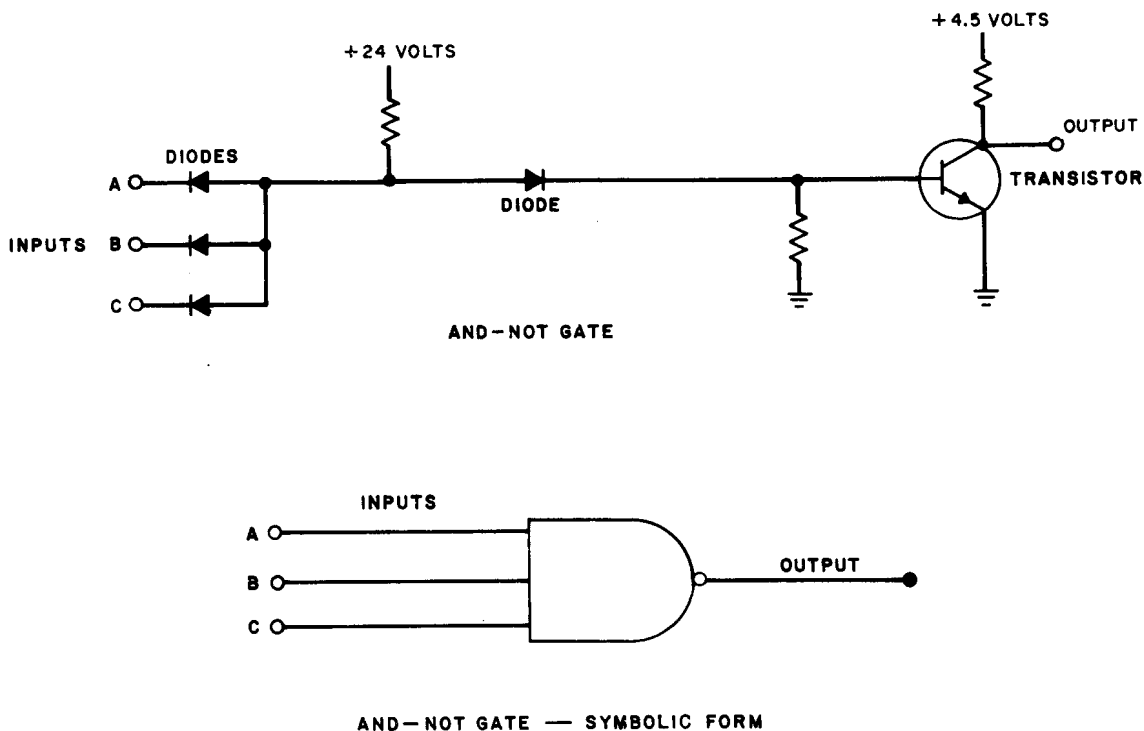

Figure 9-4 AND-NOT Gate Circuit

Its output is considered low (0 volts) when the inputs are high (+4.5 volts) and the output is high (+4.5 volts) whenever at least one of the inputs is low (0 volts). This building block is used in many circuit configurations classified as logic circuits and memory circuits. Consequently, the logic presented is referred to as the positive logic approach in circuit design.

Positive logic can be specified as the relatively more positive potential level of a two-state (binary) signal and is defined as being in the "1" state.

Figure 9-5 shows a typical 2-input NAND gate widely used in the No. 1 ESS. In this gate circuit resistance R2 provides a source of current which can be directed into the base of transistor Q or through either diode CR1 or CR3, depending upon the levels of the input signals.
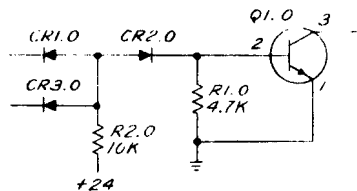

Figure 9-5 2-Input NAND Gate

If both inputs are at a potential above +4V, the current will flow into Q1 and cause it to conduct (ON) and keep the output below +0.5V. If either input is below +0.5V, the current will NOT flow into Q1 due to the voltage threshold provided by CR2 and the base emitter diode of Q1. In this condition Q1 is not conducting and the output is at a potential determined by the external load.

Diode CR1 also provides the turn-off time of Q1 by causing a large reverse base drive current when switching Q1 from its conducting to nonconducting state. Resistor R1 improves the noise and voltage threshold margins by reducing the dc impedance at the base of Q1 during its nonconducting state.

Physically these circuit elements are mounted on printed wiring boards to form plug-in units; collectively they are called circuit packs. Also, they are abbreviated CPS which indicates Circuit Pack Schematic.

The AND-NOT gate can be used as a universal gate for logic and memory applications and is capable of realizing any switching function. For example, when two gates are connected as shown in Figure 9-6 a bistable or flip-flop condition is created. For instance, assume that inputs S and R are both high and that the circuit is in the reset state (output 0 high, output 1 low). Since both inputs of the S gate are high, its output is low; this in turn keeps one of the inputs of the R gate low and insures that its output is high. Thus, the flip-flop is stable in the reset state.
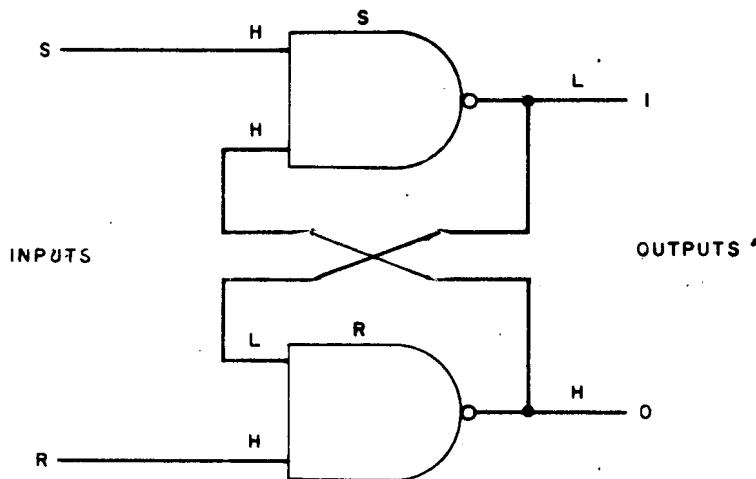
Figure 9-6   LLL Flip-Flop Gates

If the S input goes momentarily low, the output of the S gate goes high. This causes the output of the R gate to go low because both of its inputs are now high. Since the low output of the R gate is fed back to the input of the S gate, it insures that the output of the latter stays high even when the S input goes high again. The flip-flop is now stable in the set state. It will remain in this state until the R input goes low.

E. MAGNETIC CORES

In recent years magnetic cores have been used extensively in memory systems. They have also been employed to a lesser extent in logic circuits.

The cores generally used are ferromagnetic toroids and consist either of ceramic ferrite material or of ultra thin metallic tape wound on a nonferromagnetic spool. The distinguishing feature of these cores is a nearly rectangular or "square" hysteresis loop as shown in Figure 9-7.
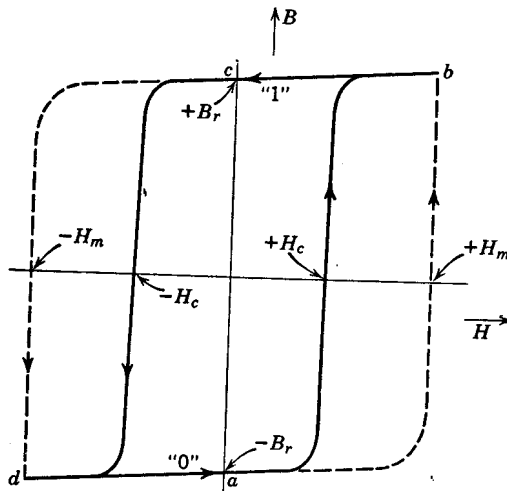

Figure 9-7   Hysteresis Loop of a Switching Core

In order to switch a core, that is, change its position on the hysteresis loop, it is necessary to exceed a certain threshold of applied magnetizing force. Referring to Figure 9-7, if a magnetizing force is slowly varied between $+Hm$ and $-Hm$ and back again, the flux density variation is that indicated by the solid line. It is possible to operate the core in this manner when inputs to the core are changes of voltage levels. In practice, however, inputs to the core are almost always in the form of pulses. The positive value of the remanent flux $+Br$ corresponds to the 1 state and the 0 state corresponds to the negative value of the remanent state $-Br$. The 0 state is marked by a and the 1 state is marked by c.

If the core is in 0 state and receives a pulse of short duration having a maximum magnetizing force of $+Hm$ the core will be driven to a positive value of flux density indicated by point b. The path taken between points a, b depend upon the shape of the pulse.

If the variation of the magnetizing force is slow the path is that indicated by the solid line; if the variation of the magnetizing force is fast the path taken is that of the dotted line. Under practical conditions the path will lie somewhere between the two limits.

Magnetic cores can perform functions of memory and logic. That the core has "memory" is indicated by its inherent characteristic to remain magnetized to saturation in either the positive or negative direction in the absence of a magnetizing force.

9.3 PROGRAM STORE

The program store (PS) is a random access semipermanent memory used in the No. 1 ESS. The capacity of the store is 131.072 readout words of 44 bits each. Cycle time to reach any word is 5.5 usec. The information in the store consists of programs and other data which are used to process calls, translate line and trunk information and carry out maintenance procedures and diagnostic tests in the system. The number of PS's required varies from 2 to 6.

The program store uses twistor modules as the basic storage block. Stored information is in the form of magnetized or demagnetized small bar magnets on removable aluminum cards. The information is semipermanent in that it cannot be changed by any operations in the store including power shut off. To change the information the cards must be removed from the store and the new pattern recorded by means of a card writer.

A. APPARATUS ELEMENTS

1. Memory Cards

Information is stored in the form of bits (0's or 1's) by magnetizing or demagnetizing small bar magnets mounted on aluminum memory cards. A memory card is shown in Figure 9-8; its dimensions are 6-5/8 by 11-1/4 inches.

Each card stores 64 words, each consisting of 44 bits. A 45th bit in each word location is not used for data storage. The 1A memory module holds 128 memory cards. The entire PS includes 16 memory modules. The distribution of words in the program store is summarized below:

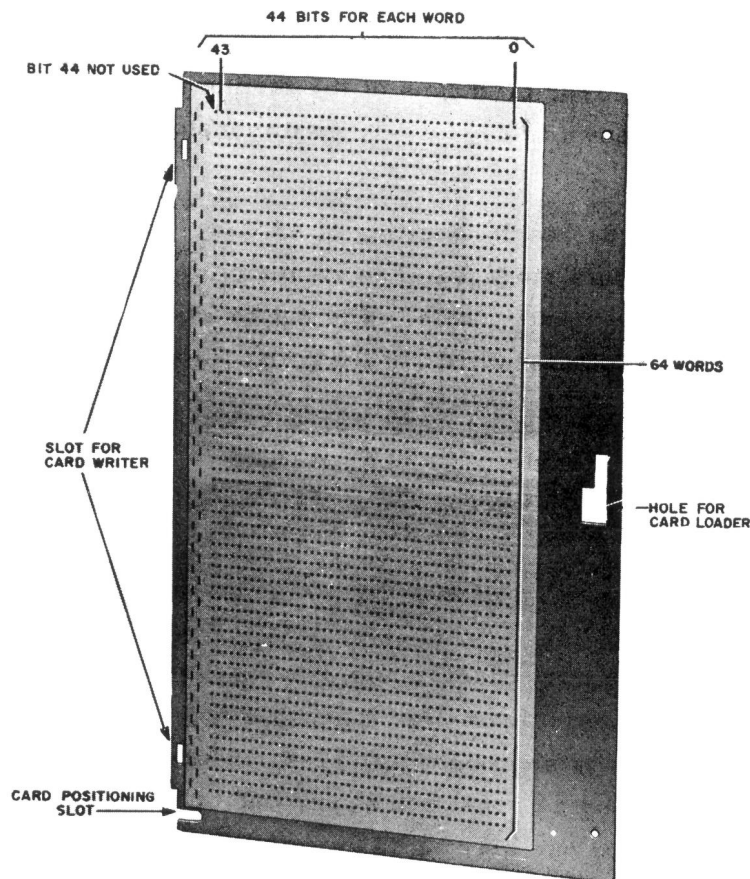| 1 memory card	64 words (44 bits each)
1 memory module (128 cards)	8,192 words
1 program store (16 modules)	131,072 words

Figure 9-8   Memory Card Containing 64 Words

2. Memory Modules

A basic element of the memory module is a 3-mil copper wire that is spiral-wrapped with a thin magnetic permalloy tape; this combination is known as a twistor wire. An enlarged view is shown in Figure 9-9. A plain wire parallels the twistor wire and is paired to it by a connection at one end of both wires. This pair forms the "sensing" or readout loop for one bit of a 44-bit word. The unshorted end of the pair is connected to readout circuitry outside the memory module unit. As shown in Figure 9-10A, the readout pair is perpendicular to a single-turn copper strip solenoid which is driven by a ferrite core. A
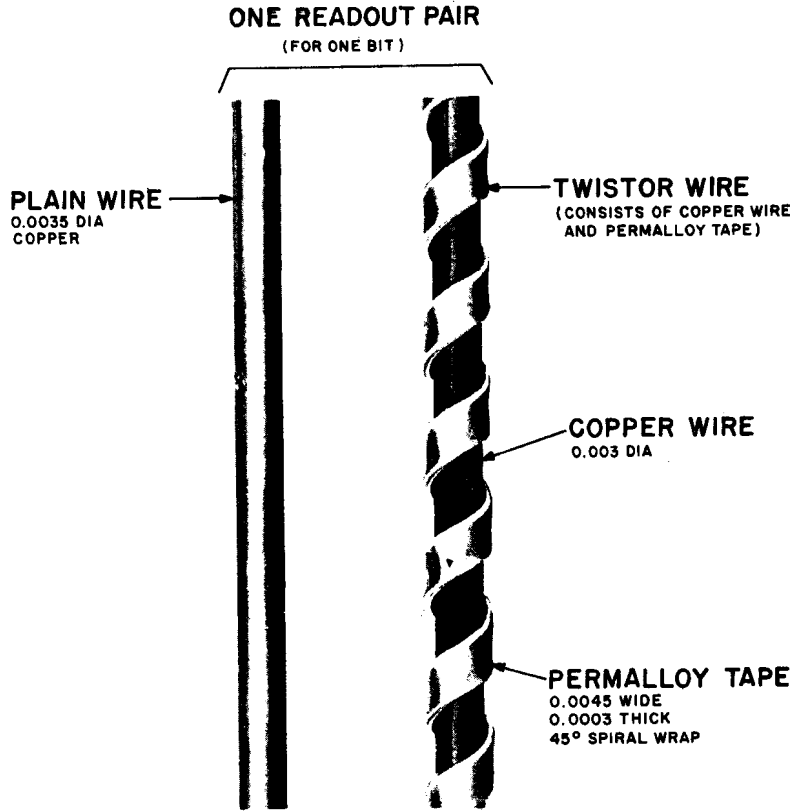
ONE READOUT PAIR
(FOR ONE BIT)

PLAIN WIRE
0.0035 DIA
COPPER

TWISTOR WIRE
(CONSISTS OF COPPER WIRE
AND PERMALLOY TAPE)

COPPER WIRE
0.003 DIA

PERMALLOY TAPE
0.0045 WIDE
0.0003 THICK
45° SPIRAL WRAP

Figure 9-9   Twistor Wire Readout Pair

LOOP CLOSED AT
TERMINAL STRIP

BIAS WIRE
X SELECTION

COPPER STRIP
SOLENOID LOOP

Y SELECTION

BAR MAGNET
ON CARD

FERRITE
ACCESS CORE

PLAIN WIRE

TWISTOR WIRE

READOUT
PAIR

A COUPLING OF ONE READOUT PAIR

B

H

I_{BIAS} ----- I_{INT}
I_X ----- I_Y
2.6 AMP TURNS — 2.6 AMP TURNS
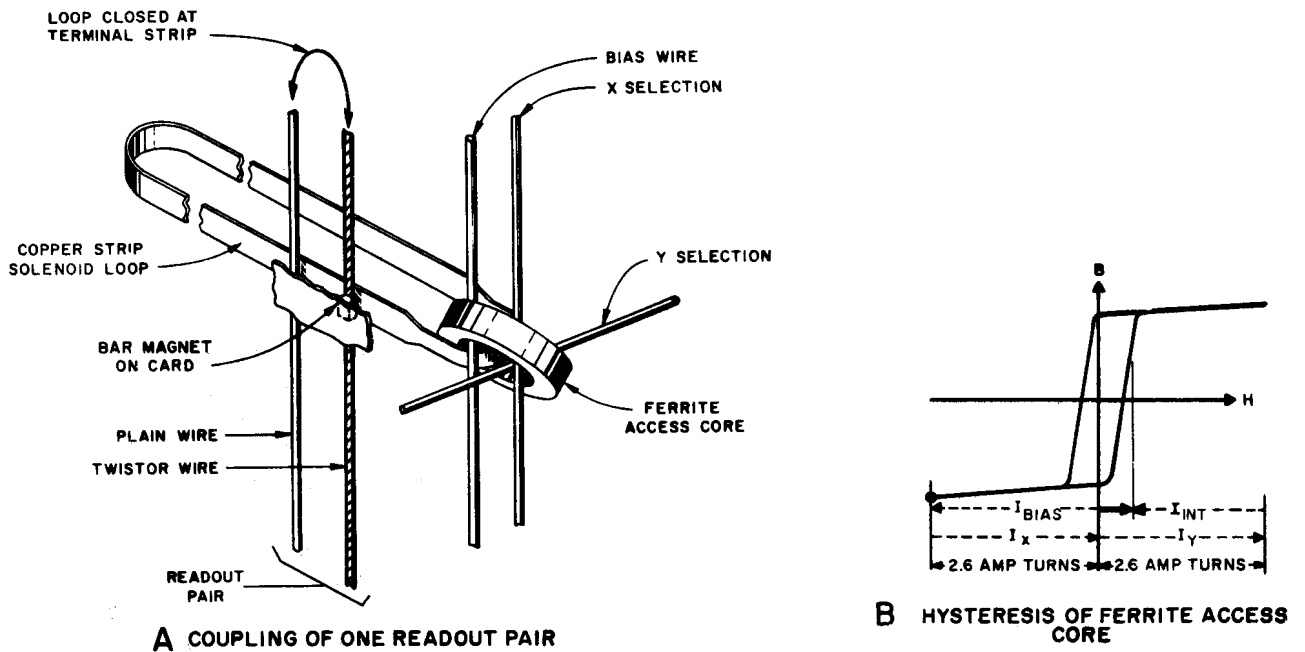
B HYSTERESIS OF FERRITE ACCESS
CORE

Figure 9-10   A Relationship of Currents and Magnetic Field In
A Ferrite Access Core and Solenoid Loop

bar magnet (mounted on the metal card previously described) is placed at the intersection of the solenoid loop and the twistor wire. Both the permalloy tape and the ferrite core have square-loop magnetic characteristics shown in Figure 9-10B.

When the X and Y leads through the ferrite core are pulsed simultaneously, the combined X and Y drives exceed the continuous dc current through the bias wire. A change of flux takes place in the ferrite core and a pulse is induced in the solenoid loop. The current in the solenoid loop is used to interrogate the bit of information stored in the bar magnet. As explained in more detail in the following paragraphs, a 0 or a 1 output is obtained from the readout pair depending on whether the bar magnet has been magnetized or not.

If the magnet has not been magnetized, the readout is a 1. The permalloy tape provides a magnetic coupling between the solenoid loop and the twistor wire. The interrogating pulse in the solenoid loop induces a pulse in the twistor wire by switching the magnetic flux in the portion of the permalloy tape at the intersection of the twistor wire and the solenoid strip.

When current is removed from the X and Y leads, the ferrite core is restored to its initial magnetic condition by the dc current through the bias wire. The pulse induced in the solenoid loop is opposite in direction to the previous interrogate pulse. Consequently, the portion of permalloy tape at the intersection of the twistor wire and the solenoid strip is switched back to its initial magnetic polarity.

If the memory card magnet has been permanently magnetized, the readout from the twistor pair is a 0. The magnetic field due to the interrogate current in the solenoid loop merely aids the stronger field due to the magnetized bar magnet. Consequently, at the intersection of the twistor wire and the solenoid loop, the permalloy tape retains its initial magnetic polarity, and no voltage is induced in the twistor wire. When the ferrite core returns to its original condition, the pulse induced in the solenoid loop

generates a magnetic field which is opposite to, but weaker than, the field due to the magnet. The permalloy tape retains its initial magnetic polarity.

The solenoid current is approximately 1.8 amperes for a duration of 2 usec. A 1 readout in the twistor wire is about 0.6 millivolts.

When a memory card is in place in a module, there are 64 solenoid loops associated with it, one for each row of 45 bar magnets. A pulse in a solenoid loop interrogates simultaneously the corresponding row of 45 magnets on the card.

A preassembled view of a plane of 64 solenoid loops is shown in Figure 9-11. The 64 solenoid loops are encapsulated in an insulated tape which is cemented over a permalloy sheet mounted on each side of the solenoid plane. The permalloy material improves the magnetic coupling between the solenoid loops and the twistor wires. Each solenoid loop parallels a word row of 45 memory magnets when the cards are in place.

There is a separate readout pair for each magnet position in a word row. Each readout pair crosses the same bit position in each of the sixty-four words on the card. The 45 readout pairs (one for each bit) are embedded in a flexible insulated tape. The readout pairs and the interrogating solenoid loops are arranged in a cross-gridded pattern. A miniature bar magnet is located at the intersection of a solenoid loop and a twistor wire when a memory card is properly inserted and positioned.

There are 65 "initializing" permanent magnets in two rows at one edge of the card. These permanent magnets are poled opposite to the memory magnets and are located between memory magnet rows. They are used to give an initial magnetization to the twistor wire permalloy wraps between the magnet rows. This magnetization occurs as the initializing magnets pass over each twistor wire when the cards are inserted in the memory module. Setting up this magnetization results in improved readouts. The initializing magnets are also used in the external card writing operation to control the timing of the row-by-row magnetization of each memory card.
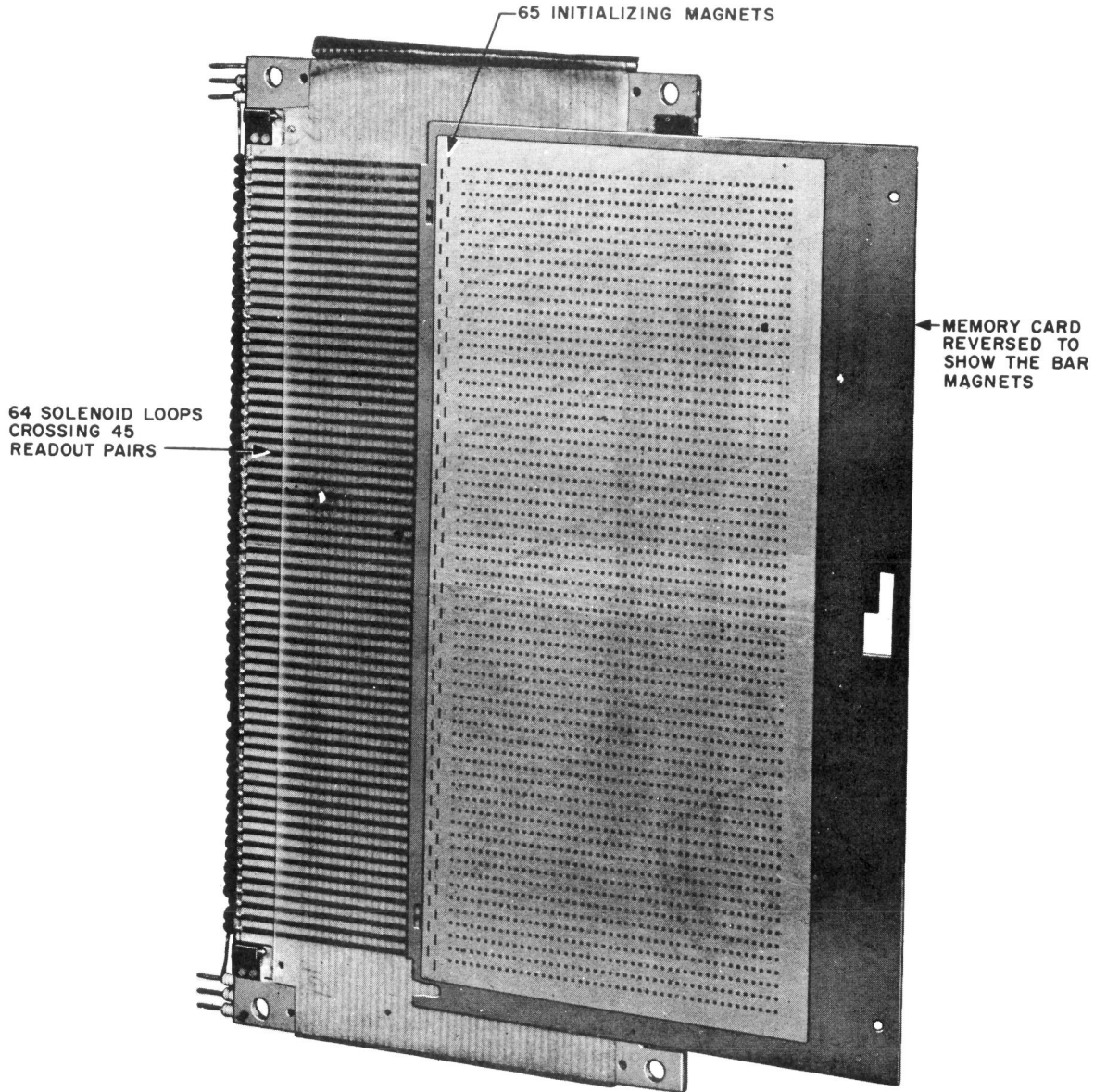
Figure 9-11   Relationship of Bar Magnets, Readout Pairs,
and Solenoid Loops (Preassembled View)

When the cards are in place in the module, there are two memory cards associated with each solenoid plane. There is one memory card on each side of a solenoid plane; therefore, 64 solenoid planes are used to read 128 cards in each module.

There are also two separate 45-pair readout tapes, A and B, one on each side of a solenoid plane. The pulsing of one solenoid loop results in the interrogation of two 44-bit words at the same time. One 44-bit word is located on the right card; the other word is on the same row in the left card. However, only one word is sent to central control as specified by the address received by the program store.

B. MEMORY DUPLICATION

The 16 twistor modules of a program store are divided into two halves of 8 modules each. When viewed from the card inserting side of the program store frame the 8 modules on the left are called the H half and the 8 modules on the right, the G half. Each half of each program store is assigned a unique binary "name" containing two 1's and two 0's, such as 0110. This name is established by means of appropriate cross-wiring at the time of installation. A word to be read out is uniquely identified by the following information from central control:

(a) A 4-bit name code which specifies the store half that contains the word

(b) A 16-bit address which identifies the desired word among the 65,536 contained in the specified half-store.

Identical names are assigned to the duplicate information blocks in the G half of one store and the H half of another store as shown in Figure 9-12B.

Normal nonmaintenance programs are written without considering duplication. In a 4-store office, although there are actually four pairs of duplicate information blocks (0_H, 0_G; 1_H, 1_G; 2_H, 2_G; and 3_H, 3_G), the programs "see" only the four unduplicated blocks shown in Figure 9-12A. Assume that a program wants to read the word A in block 1. As shown in Figure 9-12B, there are actually two copies of this word available, one copy a_G in PS 0, and the other copy

a_H in PS 2.   CC identifies word a by means of a 20-bit
address which is divided into a 4-bit name code K to specify
information block 1 and a 16-bit address A to specify the
word within information block 1.   The name code K and the
address A are transmitted by CC on both buses to all the PS's.
However, only PS 0 and PS 2 will detect a match between the
name code and a name internally assigned.   As a result, only
these two stores will use the address A.   Within each of the
two stores, the 16-bit address A received from the buses is
supplemented by a seventeenth bit A_{16} to select the appro-
priate half store.   In the example considered, PS 0 generates
an $A_{16} = 1$ in order to locate the word a_G; PS 2 generates an
$A_{16} = 0$ to locate the word a_H.

The basic 44-bit program store word in always organized
into 7 checking bits and 37 information bits as shown in
Figure 9-13A.
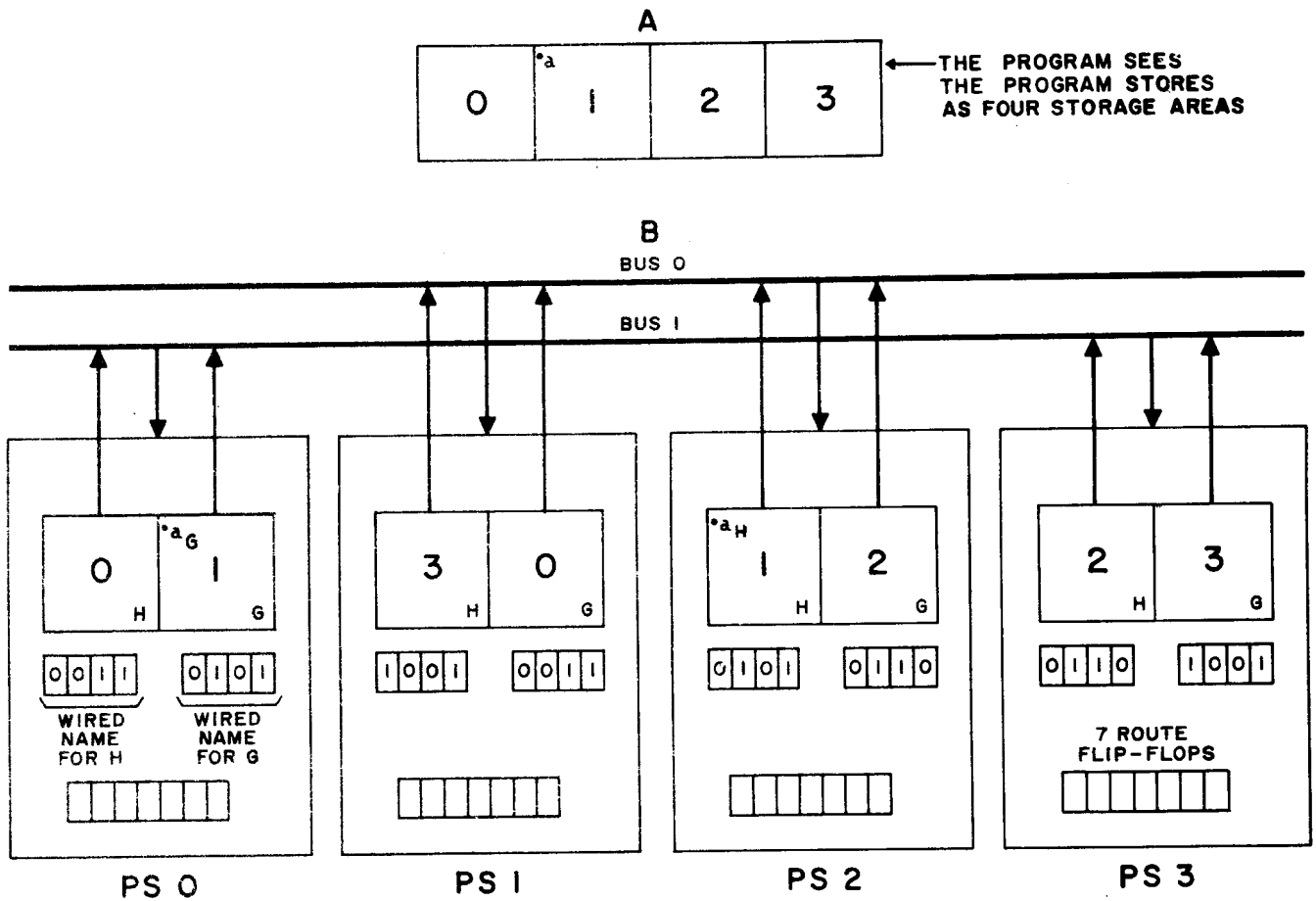
Figure 9-12   Program Store Names and Route Flip-Flops

```
43              37 36                                    0
 ┌──────────────┬──────┐   ┌──────────────────────────┐
 │    CHECK     │      │   │      INFORMATION         │
 └──────────────┴──────┘   └──────────────────────────┘
```
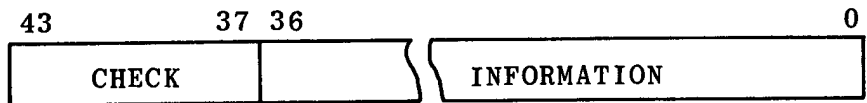
Figure 9-13A Basic Program Store Word

PROGRAM STORE ADDRESS STRUCTURE										
Ø. DIGIT										
BINARY CODE										
BIT POS ON BUS.	E21	E20	E19	E16	A15	A13	A12	A11	A6	A5 ... A0
FUNCTION				MOD IN 1/2 STORE		0=R 1=L	CARD IN A 1/2 MODULE		WORD ON A CARD	
		PROGRAM STORE		0=H 1=G						

Figure 9-13B Locating a Word in Program Store

C. ADDRESS STRUCTURE

The program store address structure is shown in
Figure 9-13B. The addressing scheme used to select a single
program store word uses twenty bits. These twenty bits
originate from the central control program address register
(PAR) and are pulsed out to a program store over the central
control to the program store bus system. A component trans-
lating circuit of the PAR alters the four most significant
bits of an address into a two out of four code called the
K code. The resultant four bits appear on bus lead pairs
E19 to E16 and must match the corresponding K code name
wired into the program store half that contains the word to
be selected. The PAR can be arranged for six bit selection
of program stores in which case the K code would become a
two out of six code and would be displayed as bits E21 to
E16 in the PAR. If the K code derived from the address has
a 0 bit in position E16 and H half will be selected, a 1 bit
selects the G half. The next three bits (A15 to A13) are
used to select the module location (all 0 bits equal module 0
while all 1 bits equal module 7) within the Program Store
half. The following bit (A12) is used to determine which
readout tape will be used the A side (Left) or the B side
(Right). If this bit is 0 the B tape reads the right hand
memory cards and if the bit is a 1 the A tape will read the
left hand cards. Each module has 128 memory cards with the
cards numbered 0 to 63 on the right and 64 to 127 on the
left. The following six bits (A11 to A6) will select one of
the 64 cards and the last six bits (A5 to A0) will select
one of the 64 Program Store words on a card. Word 0 is
located at the bottom of the card while word 63 is located
at the top.

D. BUS INPUT AND OUTPUT CONTROL

Seven flip-flops within each PS control the inputs and
outputs to and from the buses. These flip-flops operate as
follows. A flip-flop R0 allows the store to receive only
from bus 0, if set; from bus 1, if reset. Two flip-flops,
HS0 and HS1, determine whether the normal readouts from the
H half shall be sent on bus 0 and/or bus 1. These readouts
can be sent on bus 0 if HS0 is set; on bus 1 if HS1 is set.
Similarly, two flip-flops GS0 and GS1 determine whether the
normal readouts from the G half shall be sent on bus 0
and/or bus 1. Two trouble flip-flops TBL0 and TBL1, when set,
disable both input and output communications between the PS
and buses 0 and 1, respectively.

The selection of input and output buses under normal conditions with an even number of program stores is shown in Figure 9-12B, Bus 1 supplies the address and receives the readout for a word such as a_G in PS 0. Bus 0 supplies the address and receives the readout for the duplicate copy a_H. The same applies to all the other information blocks. This is also true for an odd number of program stores except for the highest numbered pair of H and G information blocks, both of which take the address from bus 0.

E. BASIC MEMORY UNIT

The decoder shown in Figure 9-14 compares the name code received with the names assigned to the two halves of a store. If a match is found, the decoder generates a seventeenth address bit A_{16} which is 0 for the H half, 1 for the G half. The complete address is stored in the address register to be used by the access circuits which select one
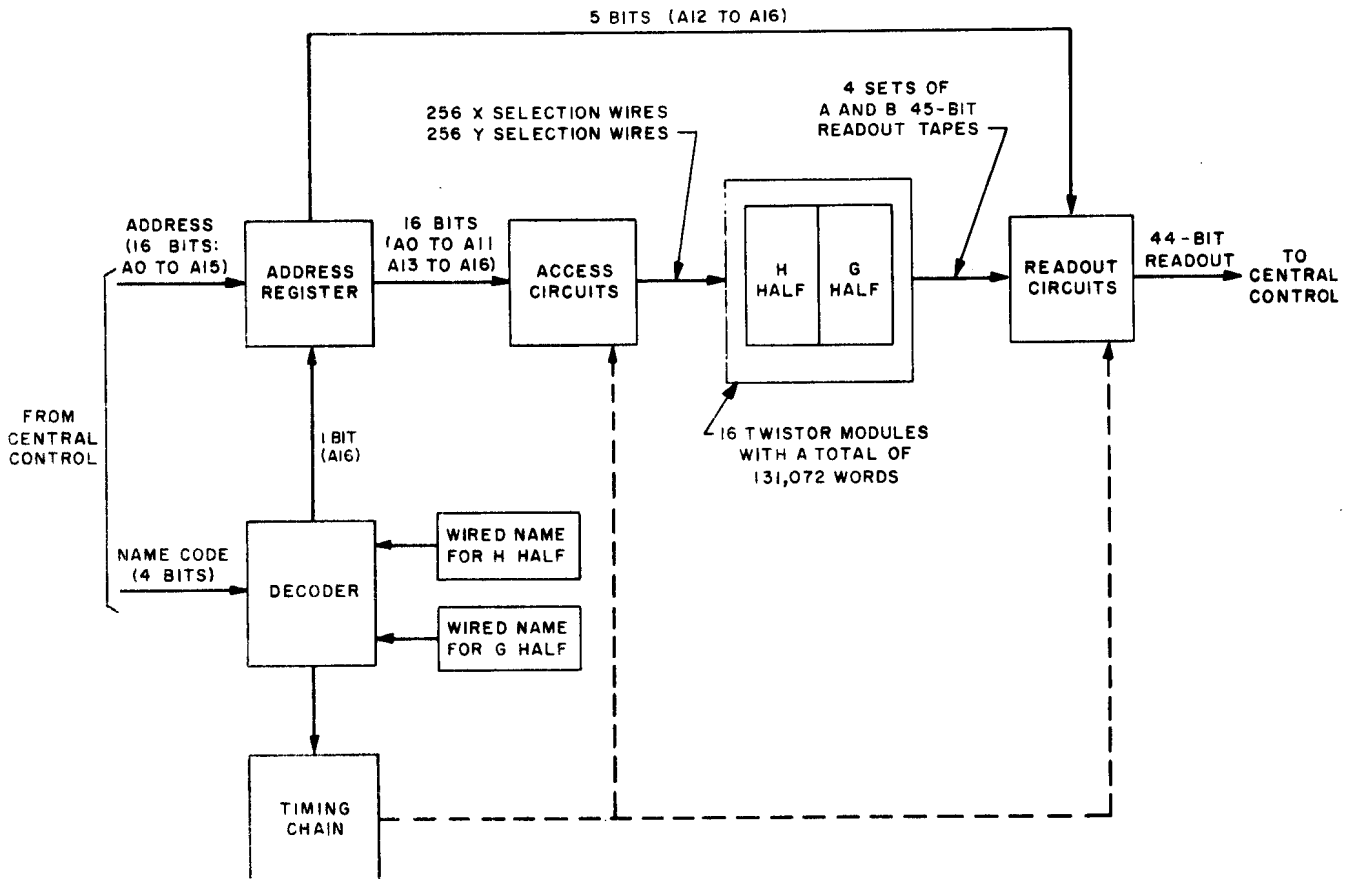

Figure 9-14   Basic Memory Unit

and only one ferrite access core. This is done by pulsing
one of 256 X selection wires and one of 256 Y selection
wires. The magnetic flux of the selected access core is
changed and a pulse is induced in the associated solenoid
loop. This pulse interrogates simultaneously two 44-bit
words on two cards causing simultaneous readouts into two
sets of readout loops which are fed to the readout circuits.
Here a selection is made between A and B readouts on the
basis of address bit A_{12} and a 44-bit output is generated
for transmittal to the CC. An all-seems-well bit and a
synchronizing bit are also transmitted to CC.

F. ACCESS CIRCUITS

Figure 9-15 shows schematically how the selection of a
single access core is achieved through the use of electronic
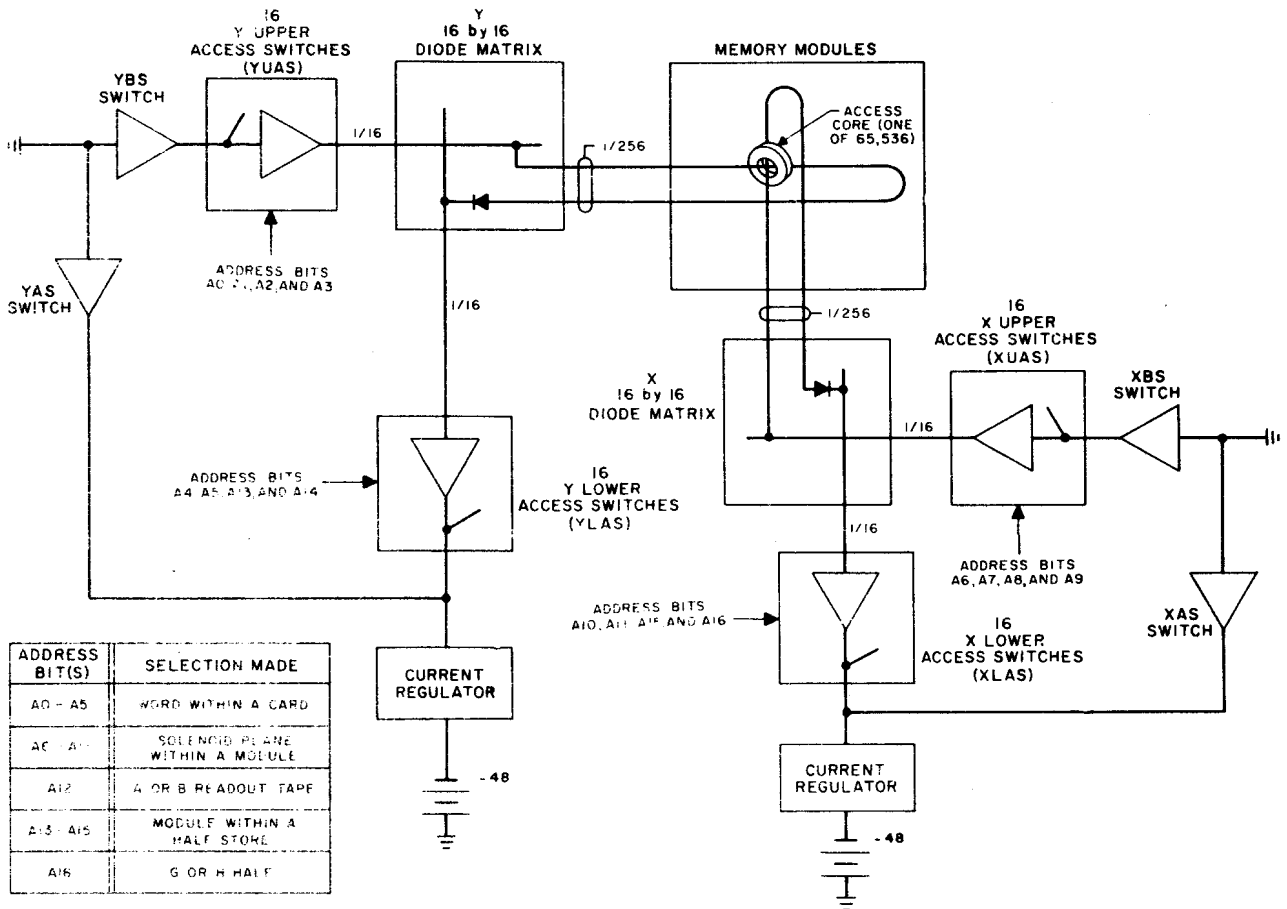switches. The 16 Y upper access switches (YUAS) on the left

Figure 9-15   Method of Selecting a Single Access Core

are controlled by the 16 possible combinations of the four address bits A_6 to A_9. Current can flow through only one YUAS as selected by the four address bits. Similarly, only one of 16 Y lower access switches (YLAS) is closed. In the Y diode matrix, current can flow in only one of 16 horizontals and one of 16 verticals (the diodes eliminate the possibility of sneak paths). Thus, only one of 256 Y wires is pulsed. Similar considerations apply to the selection of one of 256 X wires. When a selection is made, the YAS and XAS switches open. This transfers the regulator current to the selection circuits. When the selection is completed, the normally closed YBS and XBS switches open, the YAS and XAS swithces close, and the current again is shunted to ground. Once the current transfer is completed, the YBS and XBS switches reclose. (All the upper and lower switches are now open.)

G. READOUT CIRCUITS

As shown in Figure 9-16, the A and B readout pairs of four similarly numbered modules are connected together to form a common output to a selector. Each readout pair is shorted at a terminal strip at one end of each module. Of the eight sets of readout pairs, only one is detected on the basis of bits A_{12} to A_{16}. With the arrangement described, when a readout takes place in one module, no X or Y current is present in any other module wired to the same readout pairs. This reduces the noise effects of an X or Y current on the selected readout.

H. MODES OF OPERATION

The main function of the program store is to supply the binary coded information necessary to operate the system. In addition to providing the system program, other modes of operation are necessary for diagnosing troubles within the store and to change the states of various operating conditions.

The address from central control to the program store via the address bus consists of 25 bits. These 25 bits indicate what type of operation the store is to perform, which store or stores are to respond, and the location of the information within the store. The input word structure is one sync bit, four K code bits, four mode bits, and 16 address bits.

TWISTOR MODULE ARRAY

H HALF · · · G HALF

0 MOD 03	1 MOD 07	2 MOD 13	3 MOD 17
1 MOD 02	0 MOD 06	3 MOD 12	2 MOD 16
2 MOD 01	3 MOD 05	0 MOD 11	1 MOD 15
3 MOD 00	2 MOD 04	1 MOD 10	0 MOD 14

44 READOUT PAIRS

SELECTOR
(1 OUT OF 8)

3 2 1 0

ADDRESS BITS
A12 TO A16

TYPICAL SIGNAL
AT SELECTOR INPUT

SAMPLE
INTERVAL

1 mv.

1

0

2 USEC

MAIN AMPLIFIER

SAMPLER

OUTPUT

NOTE: THE 44-BIT A READOUT AND THE 44-BIT B READOUT
ARE EACH CONNECTED IN PARALLEL WITH SIMILAR
READOUTS FROM SIMILARLY NUMBERED MODULES. FOUR
MODULES ARE CONNECTED TO THE SAME OUTPUT PAIRS
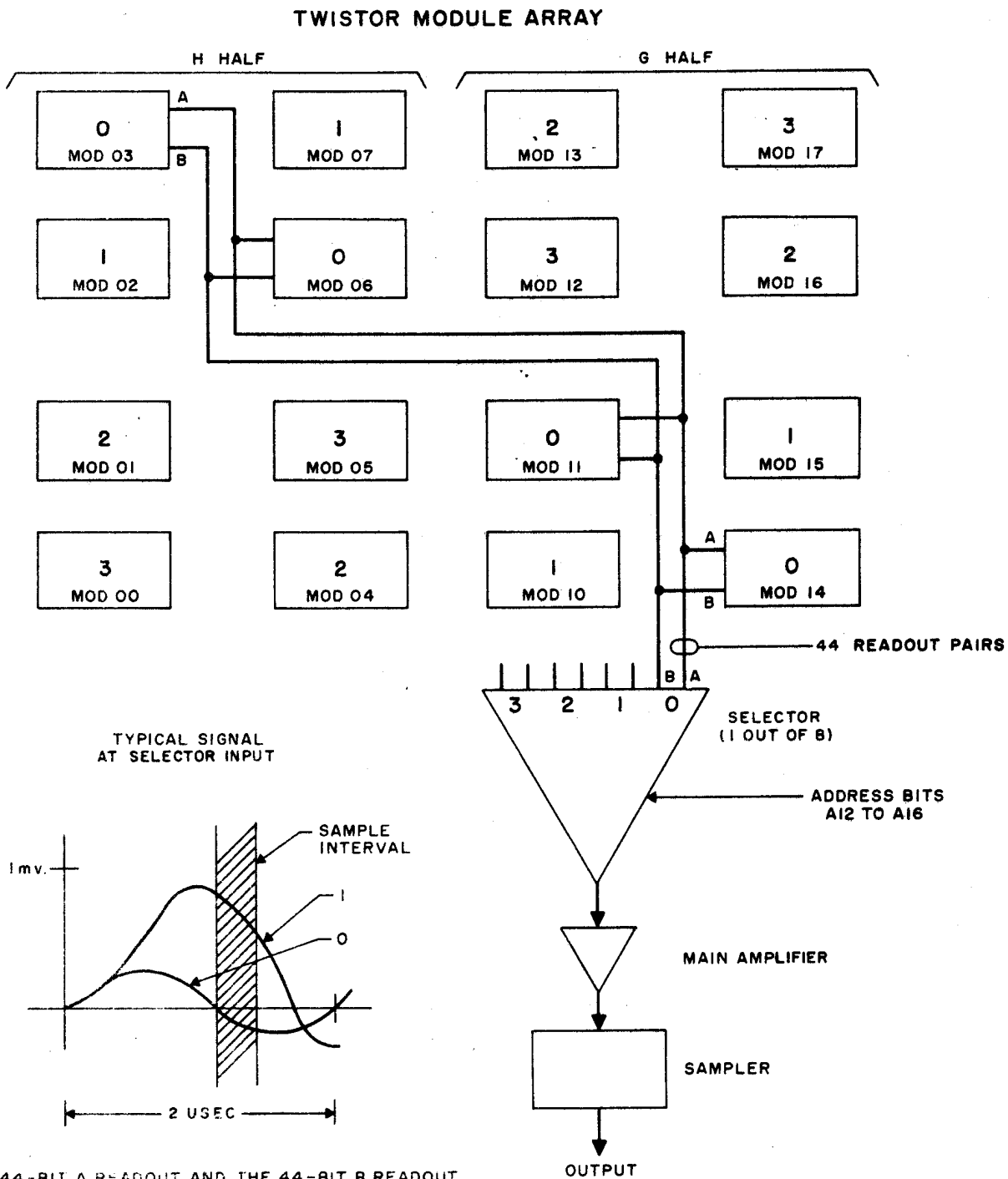IN EACH WIRING PATTERN.

Figure 9-16 Program Store Readout Connections

1. Normal Mode

This mode is used during the routine operation of the central office when central control is obtaining program and translation information from the program store twistor modules. In a normal mode, the choice of address buses to receive on and the choice of answer buses to send on are completely flexible. The program stores are divided into two halves designated H and G. In a central office the information in the H-half of one store will be duplicated in the G-half of another store. During a normal mode, if all systems are functioning properly, two program stores will answer an address sent by central control; one from the H-half of one store and one from the G-half of another store. The information is the same from either store. The address sent to the two program stores can be sent on one bus or on separate buses, but each program store must answer on separate buses.

2. Maintenance Mode

This mode differs from a normal mode in that only one half of one store will respond to the address. In addition, the particular store designated in the maintenance mode will answer on the same bus on which it has received the address. In a maintenance mode the program store delivers a normal twistor readout, but the readout is used for diagnostic checks rather than for system instructions. For example, if an access switch is faulty, central control may instruct the program store to roster through a number of addresses to determine which ones are reading incorrectly and thereby locate the faulty access switch.

There are two maintenance modes, H maintenance and G maintenance. H maintenance instructs the program store to send the information requested in the address from the H side of the store. The G maintenance designates the information be sent from the G side of the program store.

3. Control Mode

In order to allow the system to observe or evaluate conditions within the program store and to permit these conditions to be altered a control mode is provided. The control mode is subdivided into a read control and a write control mode. No access or twistor readout occurs during a control mode.

a. Read Control Mode

For the system to perform its diagnostic tests on the program store, it is necessary to know the status of a large number of points internal to the store. This information can be sent to central control via the bus pairs in the read control mode. The points checked consist of such things as the state of flip-flops, gates, timing packages, and any other conditions needed to locate troubles in a store. During a read control mode there is no drive supplied by the access to the twistor modules and therefore no memory readout. Instead the readout word normally sent to central control is replaced by a word composed of 44 read control bits. To increase the number of read control bits which can be sent, there are four groups of 44 bits, any group of which can be read out during a cycle. Thus, theoretically, the number of available read control bits is increased to 176. Actually only 160 bits can be used since the last four bits of each group are used to indicate which group is being read out. The groups of read control bits are called rows. The bus selection in a read control mode is identical to that of a maintenance mode; the program store must answer on the same bus on which it has received the address.

b. Write Control Mode

The write control mode permits central control to set up a desired set of conditions in the store via the address bus pairs. In a write control mode, no readout occurs from the program store. The function of a write control can be for either diagnostic purposes or the normal changing of routing for example, the

routing of the program store buses. Since
there are a number of functions the write
control can perform, a steering bit is sent
with the write control address to instruct
the program store which condition to institute.

Generally, a cycle in the write control mode is
followed by a read control to verify that the
locations were actually written as specified
by the write control mode.

Besides the internal points in a program store
that are written by the write control mode
there are internal points which are controlled
directly by the central pulse distributor. This
allows the system to maintain some control over
a program store in the event of bus or store
failure.

There are also internal points called scan
points which are not read out by the read
control mode. The scan points are handled in
two ways. Part of them are permanently con-
nected to the master scanner. The remainder of
them can be connected to the master scanner
through the monitor bus. The scan points that
are permanently connected to the master scanner
are critical circuit points that need continuous
monitoring. Connection to the other scan points
through the monitor bus is slow but makes it
possible to diagnose troubles independent of the
program store and the communication buses.
Also, for some of the points in the store it is
just not practical to monitor in any other
manner.

There will be times when a program store will
have to be brought back into service after it
has been out of operation. Central control
will try to do this automatically through the
emergency alarm bus. If central control fails
then the program store is put in operation
manually. The manual control is done at the
master control center. The master control
center communicates to the store via the
override leads.

9.4 CALL STORES

The call stores (CS) provide a temporary, or read-write, type of memory; that is, they provide the means for recording information that later can be read, altered, or erased by the system. This temporary memory is used by the central control (CC) and the signal processors (SP). It serves to store information that is related mainly to the handling of telephone calls (hence, the name call store). The information stored in temporary memory includes:

(a) Busy-idle status of customer lines, junctors, trunks, network links, etc.

(b) Records of network terminations being used for each call in progress.

(c) Digits received.

(d) Digits to be outpulsed.

(e) Customer billing information prior to recording on the automatic message accounting (AMA) tape.

(f) Recent change information related to customer lines and trunks prior to updating the translation information in the program stores (PS).

(g) Maintenance information related to program-controlled diagnostic tests.

The information contained in a CS is organized in words of 24 bits as shown in Figure 9-17. One of these bits is used for parity checking. Each word occupies a word location uniquely identified by an address. Inputs from CC specify the operation to be performed (reading or writing), the address of the location involved, and, in the case of writing, the word to be written. The CS carries out the request and, in the case of reading, transmits to CC the word that it has read. The CS is also capable of performing special operations for control or maintenance purposes.

A single CS has 8,192 word locations, thus providing a total storage capacity of 196,608 bits. The shortest allowable time interval between consecutive store operations is 5.5 usec.

The number of CS's needed depends on the office size. Taking duplication into account, the maximum number of CS's associated with the CC could be 39. Where SP's are provided, each pair of SP's may have up to eight CS's. A call store frame is shown in Figure 9-18.

An example of the storage requirements for a central office with 5,000 lines and 4,500 calls per busy hour is given below:

Requirements independent of office size	3,000 words
Call processing	4,800 words
Network map	2,400 words
Maintenance and administration	1,400 words
	11,600 words (unduplicated)

Figure 9-17 Basic Call Store Word

A. APPARATUS ELEMENTS

1. Ferrite Sheet

The basic storage element in the CS is the ferrite sheet shown in Figure 9-19. The ferrite sheet is approximately one inch square and 30 mils thick. Each sheet contains 256 holes in a 16 by 16 array. The holes are 25 mils in diameter and are placed on 50-mil centers.

The ferrite sheet material (magnesium-manganese) has a square-loop magnetic characteristic (Figure 9-20). After the removal of a magnetizing drive, the ferrite material retains either a positive or a negative remanent magnetization, $+B_R$ or $-B_R$. In order to "switch" or reverse the magnetization from $-B_R$ to $+B_R$, it is necessary to apply a positive magnetizing drive that must exceed a threshold value, $+H_C$. Similarly, in order to switch from $+B_R$ to $-B_R$, it is necessary to apply a negative drive that must exceed a threshold value, $-H_C$.
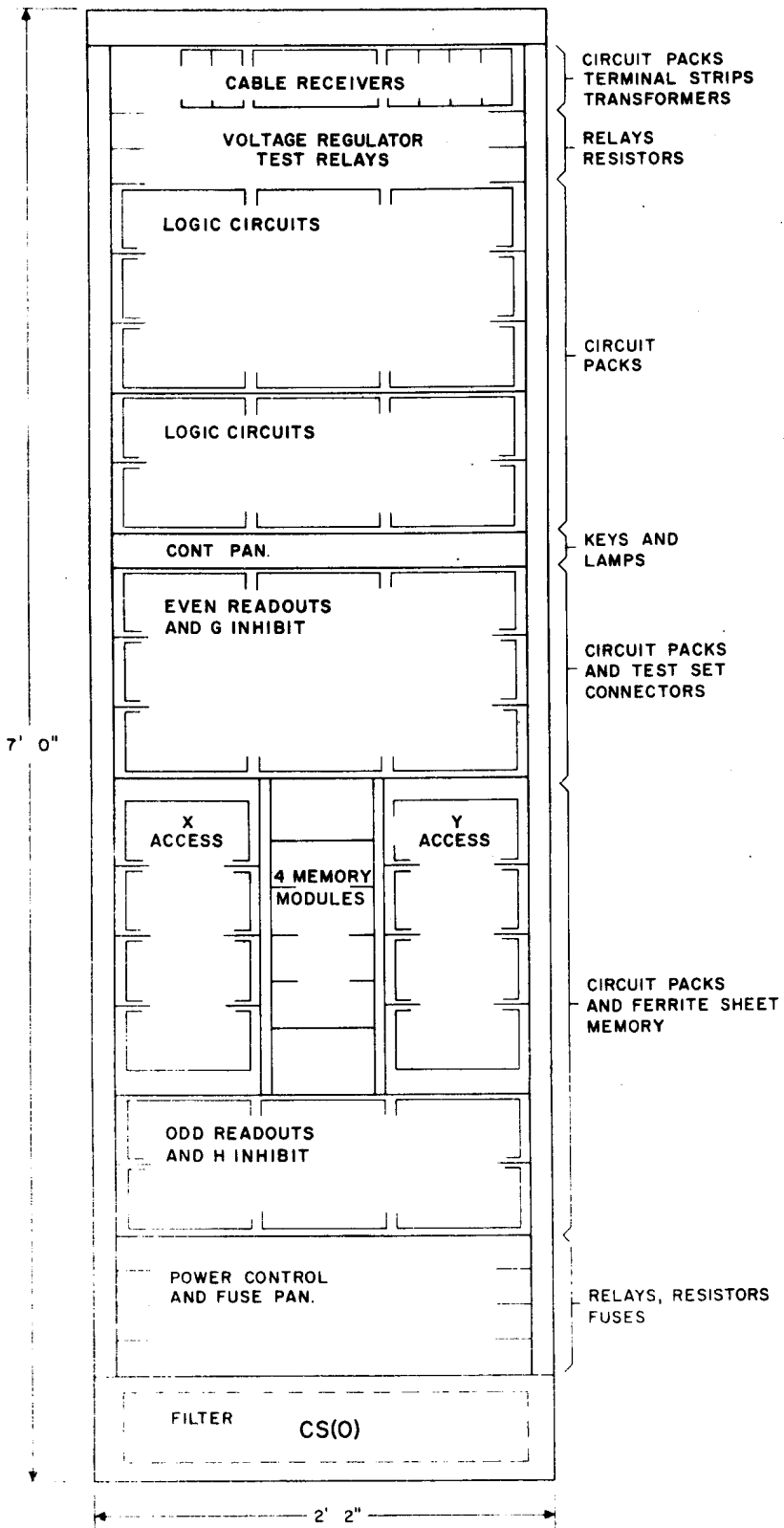
Figure 9-18 Call Store Frame Layout

256 HOLES IN A 16 BY 16 ARRAY
EACH HOLE STORES ONE BIT

Figure 9-20   Square-Loop
               Characteristic
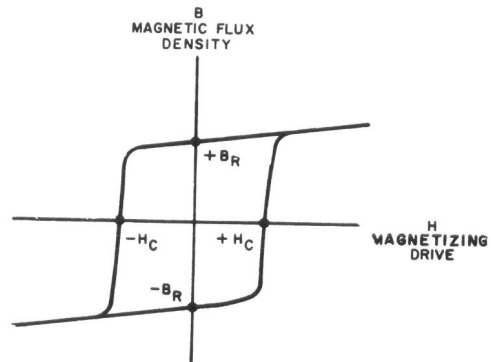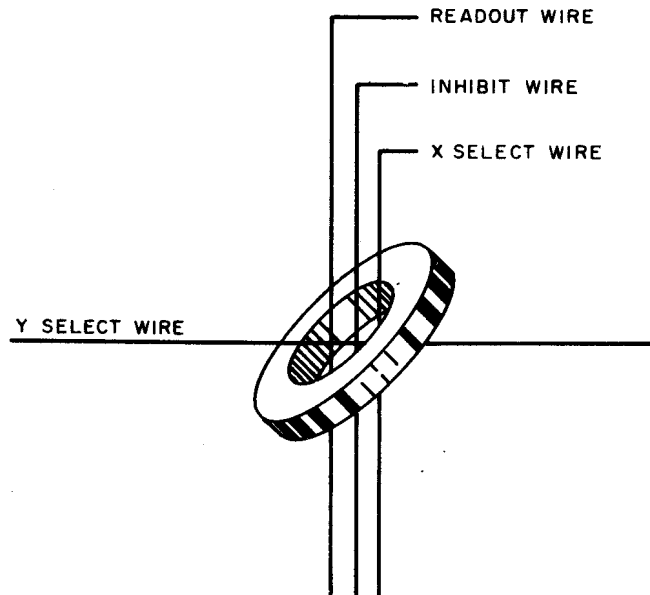
Figure 9-19   Ferrite
               Sheet

If the ferrite material is in the remanent state $+B_R$, a negligible change in magnetization results from a positive drive or from a negative drive that does not exceed H_C. This is due to the fact that the upper and lower sides of the loop are almost horizontal. Similar considerations apply when the ferrite material is in the remanent state $-B_R$ and the applied drive is negative or less than H_C.

A bit of information can be stored in the material immediately surrounding each hole of the ferrite sheet by magnetizing the material either clockwise or counterclockwise. One state of remanent magnetization is identified as the binary value 0 and the opposite state of remanent magnetization is identified as the binary value 1.
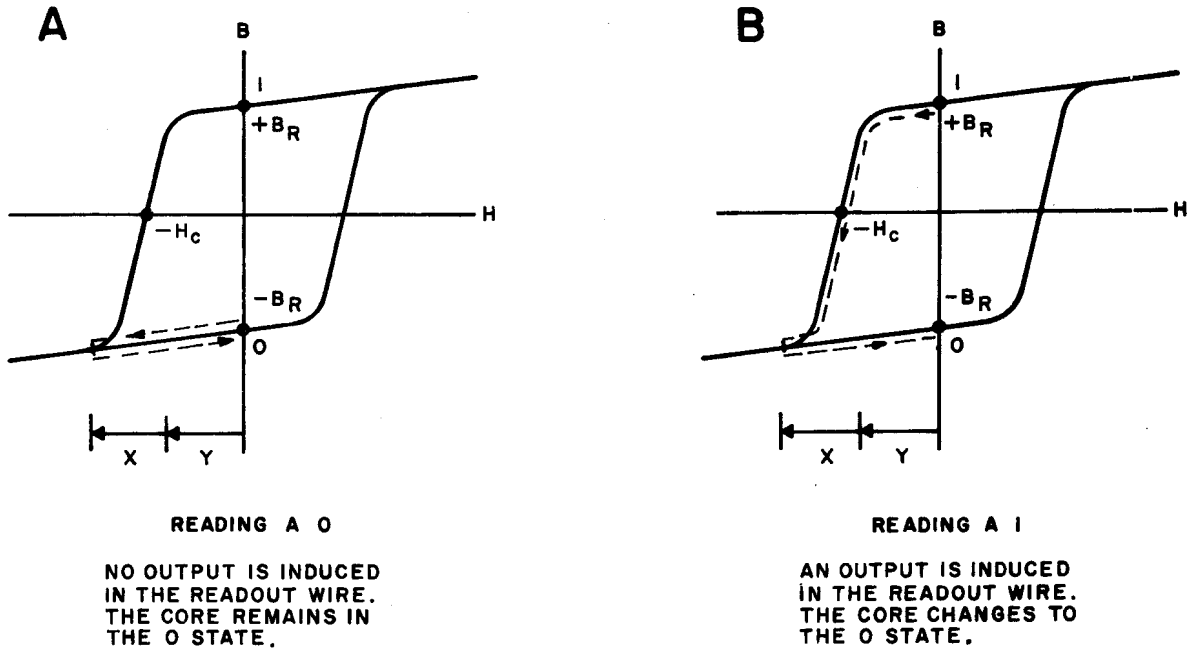
The ferrite sheet can be considered to be equivalent to an array of 256 miniature magnetic cores such as the one shown in Figure 9-21. Four wires are associated with each core: two select wires X and Y, a readout wire, and an inhibit wire.

READOUT WIRE

INHIBIT WIRE

X SELECT WIRE

Y SELECT WIRE

THIS CORE IS EQUIVALENT
TO ONE HOLE IN THE FERRITE SHEET

Figure 9-21   Principle of Memory Core Switching Operation

In order to read the binary content of a core, the
X and Y wires are simultaneously pulsed, each with
a current of 250 ma (Figure 9-22). The combined
drive exceeds the threshold value and is applied
in a negative direction. This drive tends to reset
the core, that is, to put it in the remanent state
associated with 0. If the core happens to be
already in the 0 state, there is a negligible
change in magnetization which results in a negli-
gible output induced in the readout wire. On the
other hand, if the core is initially in the 1 state,
the combined X and Y drives cause a change in
magnetization from $+B_R$ to $-B_R$. This induces an
output of approximately 50 millivolts in the read-
out wire. Thus, the presence or absence of an
output in the readout wire indicates whether the
core was initially in the 1 or 0 state. Regardless
of its initial condition, the core is forced into
the 0 state by the reading operation. For this
reason, the core is said to have a destructive
readout. The information, however, will be re-
stored into the core by writing back whatever was
read out.

A

READING A O

NO OUTPUT IS INDUCED
IN THE READOUT WIRE.
THE CORE REMAINS IN
THE O STATE.

B

READING A I

AN OUTPUT IS INDUCED
IN THE READOUT WIRE.
THE CORE CHANGES TO
THE O STATE.

THE CORE IS INITIALLY IN THE O STATE AS A RESULT OF A READING OPERATION

Figure 9-22   Reading a Memory Core

A

WRITING A I

THE CORE SWITCHES
FROM THE O STATE
TO THE I STATE.

B

WRITING A O

THE PRESENCE OF
THE INHIBIT DRIVE
PREVENTS THE CORE
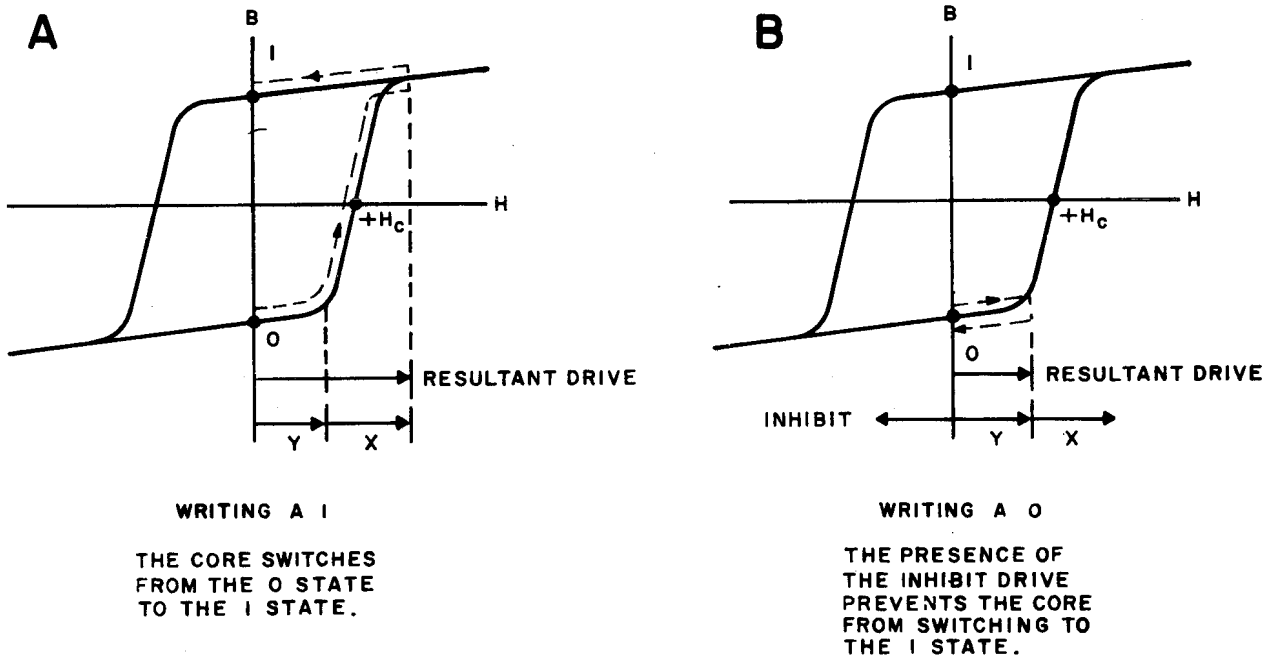FROM SWITCHING TO
THE I STATE.

Figure 9-23   Writing in a Memory Core

9.40

In order to write back a 1 (Figure 9-23A), the
X and Y wires are again simultaneously pulsed,
each with a current of 250 ma. The direction of
the applied drive is now opposite to that used
for reading. Consequently, the core is "set" or
switched from state 0 to state 1. In order to
write a 0 (Figure 9-23B), the X and Y wires are
again pulsed in the positive direction; at the
same time, the inhibit wire is pulsed in the
negative direction. The combined drive due to the
inhibit wire and to the X and Y wires is less than
H_C. Consequently, the core is not switched and is
left in state 0.

When new information is to be written into a core,
a readout is performed first to force the core
into the 0 state. Writing takes place then in the
manner previously described. Whether a pulse is
applied to the inhibit wire is determined, not by
the bit that was read out, but by the bit to be
written. If a 0 is to be written, an inhibit
drive is applied.

B. BASIC MEMORY UNIT

As previously stated, the 8,192 word locations con-
tained in a CS are divided into two information blocks
known as the H half and the G half. Ferrite sheets of
submodules 0 and 1 are in the G half and submodules 2 and 3
are in the H half. Each submodule contains 2,048 words.
Each store-half has a 6-bit "name." The H half is assigned
a fixed name by appropriate cross wiring at the time of
installation. The G half, instead, is assigned a name by
setting an appropriate combination on six flip-flops. The
status of these name flip-flops can be changed under program
control. This flexibility in identifying blocks of memory
permits the physical location of the stored data to be
changed to other call stores in case of trouble. Figure 9-24
illustrates the scheme for duplicated call store memory
blocks.

H	G	H	G	H	G	H	G	H		G	H	G	HALF
0		1		2		3		4		36		0	MEMORY BLOCK
00		01		02		03		04		35		36	CS FRAME

Figure 9-24 Duplicated Call Store Memory Blocks

The addressing scheme used to select an individual word location requires 18 bits. The 12 least significant bits are used to select one of 4,096 words and the 6 most significant bits are used as K code bits which select the memory block with the matching K code name. The bit positions of the central control to call store bus, used for addressing are identified in the call store address structure shown in Figure 9-25.

Ø DIGIT							
BINARY CODE							
BIT POS	A17	A12	A11				A00
FUNCTION	K CODE		ONE OUT OF 4096				

Figure 9-25   Call Store Address Structure

The basic portion of a call store is shown in Figure 9-26. Within each CS, separate access circuits are provided for the G and H halves. If the name code K received by a CS matches the name of the H half or the G half, the appropriate access circuit is activated. The signals received on the order leads R and W determine whether a reading or writing operation is to be performed at the specified word location. Either operation is carried out in two stages.

1. Reading

   During the first stage of a reading operation, access is gained to the desired word location by pulsing one of 64 X leads and one of 64 Y leads in the appropriate store half. The direction of the X and Y currents is such that each bit of the interrogated location is left in the 0 state. The signals from the memory modules go to the readout circuits where they are amplified and then submitted to discriminators. These determine whether each input is to be considered a 1 or a 0 and generate accordingly an appropriate output.
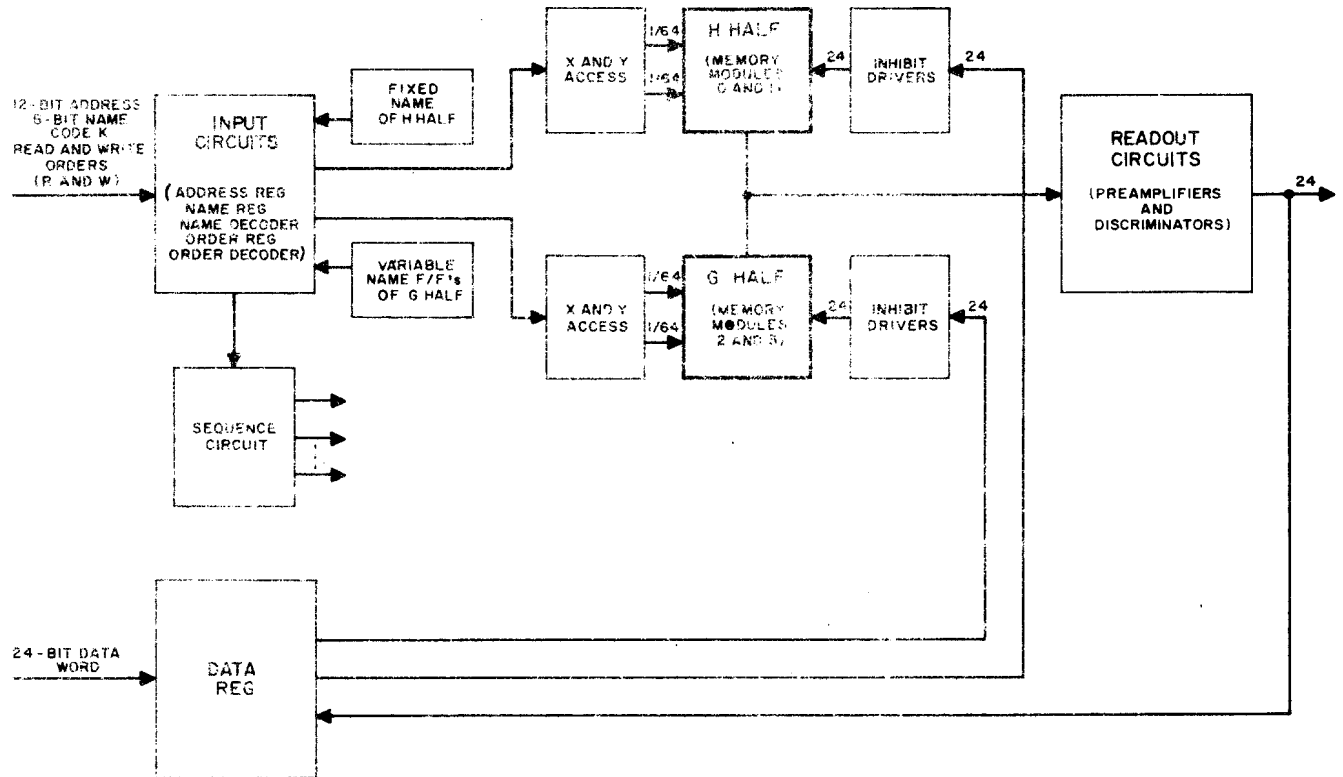
Figure 9-26 Basic Call Store

The outputs of the readout circuits in the read operation are also stored in the data register. During the second stage of a reading operation, the information read out is written back as follows. The word location previously read is again selected by pulsing the same X and Y leads but in the opposite direction. Thus, the X and Y currents tend to write a 1 in each bit of the selected word location. However, any bit of the data register that is equal to 0 activates an associated inhibit drive which applies a pulse to an inhibit wire. This prevents the writing of a 1 in the corresponding bit position.

2. Writing

During the first stage of a writing operation, the specified word location is read out as previously described. However, the outputs of the readout circuits are not gated into the data register. Thus, the net effect of this first stage is to clear the specified word location. The data register is set by 24 bits received via the bus from CC. During the second stage, this information is written into the selected word location in the manner previously described. The sequence control generates all the necessary timing pulses.

C. NORMAL INPUT-OUTPUT CONTROL

As previously described, each store-half information block is assigned a name of six bits. The purpose of this coding is to permit selective communication with a number of CS's using a common bus system. Figure 9-27B shows, as an example, four CS's connected to two duplicate buses. Normally, identical names are assigned to the duplicate information blocks in the G half of one store and the H half of the next store.

Nonmaintenance programs are written without taking into consideration that the information is duplicated. In the example considered, there are actually four pairs of duplicate information blocks: 0_H and 0_G, 1_H and 1_G, 2_H and 2_G, and 3_H and 3_G. However, the programs "see" only the four unduplicated information blocks shown in Figure 9-27A.

For example, assume that a program wants to read the word a in information block 1. As shown in Figure 9-27B, there are actually two copies of this word available, one copy a_G in CS 0 and the other copy a_H in CS 1. The CC identifies the word a by means of an 18-bit address which can be divided into a 6-bit name code K to specify information block 1, and a 12-bit address A to specify the word within information block 1. The name code K and the address A are transmitted by CC on both buses to all the CS's. However, only CS 0 and CS 1 will detect a match between the K code and a name internally assigned. As a result, only these two CS's will use the address A. In CS 0, the access circuit activated is that of the G half since its name matches the name code received. Similarly, in CS 1, the access circuit activated is that of the H half.

A

THE PROGRAM SEES
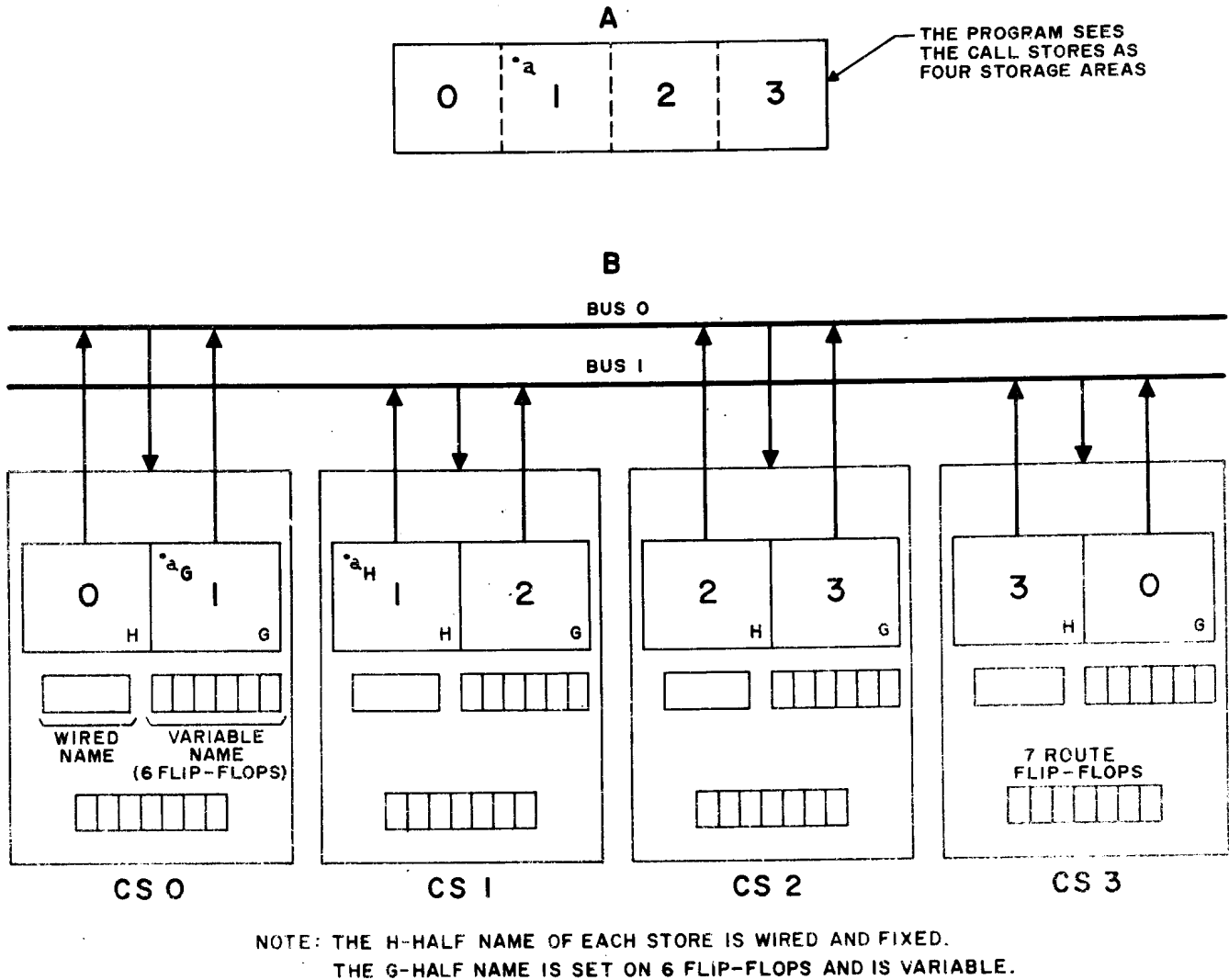THE CALL STORES AS
FOUR STORAGE AREAS

B

Figure 9-27   Call Store Name and Route Flip-Flops

Seven route flip-flops within each CS control the
inputs and outputs to and from the buses. A flip-flop R0
allows the store to receive only from bus 0, if set; from
bus 1, if reset. Two flip-flops HS0 and HS1 determine whether
the normal readouts from the H half shall be sent on bus 0
and/or bus 1. These readouts can be sent on bus 0 if HS0 is
set, on bus 1 if HS1 is set. Similarly, two flip-flops GS0
and GS1 determine whether the normal readouts from the G half
shall be sent on bus 0 and/or bus 1. Two trouble flip-flops
TBL0 and TBL1, when set, disable both input and output
communications between the CS and buses 0 and 1, respectively.

D. INPUTS TO THE CALL STORE

Inputs to the call store consist of three sets coming from the Signal Distributor Applique, the Central Pulse Distributor, and the Central Control Circuits. Another input set consists of the +24 volt, -48 and ground for the store. The inputs from the Signal Distributor Applique Circuit have direct control of relays in the call store and the pulses from the CPD Circuit control certain flip-flops.

There are 53 Central Control Circuit inputs to the store comprised basically of five groups of information - six code bits, three mode bits, 12 address bits, three read-write-parity bits and 24 data bits. There are two buses, bus 0 and bus 1 where the 53 inputs are duplicated.

Five synchronization pulses are provided by Central Control Circuit for these groups of information: one for the code-mode, one each for the address and read-write-parity group, and two for the data bits.

There are four varieties of output leads. The first uses twisted pair to carry dc signals from flip-flops, relays and voltage regulators to the ferrods of the Master Scanner Circuit. The second is a single wire power alarm and the third are test points for battery supplies, internal circuit modes, and the store field test set.

The fourth variety consists of 26 answer leads for the Central Control Circuit duplicated on bus 0 and bus 1. Twenty-four are the call store readouts, one the all-seems-well signal, and the last a sync pulse.

E. MODES OF OPERATION

There are four basic modes of operation in a call store.

(a) Normal mode - In this mode, the call store serves as a memory for the system with ability to read and regenerate the contents of a selected word, or to erase the old contents and write in new information.

(b) Maintenance mode - This mode is almost identical to the normal mode. The normal mode has more flexibility based on K-code matches, while the maintenance mode has less selective options since the use of the K-code matches are limited. This mode is used when Central Control Circuit directs specified maintenance tests of certain locations in a particular store.

(c) Control write - The control write mode can alter the state of call store flip-flops. In addition, sections of the sequence control and memory circuits can be tested without fully addressing the modules.

(d) Control read - The states of key flip-flops and the absence or presence of store pulse points is noted and sent to Central Control Circuit.

F. CALL STORE ORGANIZATION FOR DUPLICATION AND TROUBLE SWITCHING

The number of call stores needed, depends upon the size of the system. A large electronic central office might require as many as 6,000,000 bits of call store memory. However, one-half million bits might be adequate for a small office. Signal Processor Circuits when provided in an electronic central office, may use up to eight call stores for each pair of Signal Processors. Because stored information is duplicated for reliability, these totals include call stores required for complete duplication.

In the actual organization of the central office equipment, the call stores are grouped with Central Control, Signal Processor, and Program Store Circuits in a number of control communities as shown in Figure 9-28. Normally, the Central Control and Signal Processor Circuits operate simultaneously and independently; consequently, the Central Control Circuits and each pair of Signal Processor Circuits must have separate call stores of their own. It must be possible, however, for Central Control Circuits to stop a pair of Signal Processor Circuits and use their call stores. The Central Control Circuits have access to the call stores of a signal processor community via the Signal Processor Circuits in that community.

The control community consists of two duplicate Central Control Circuits and their call stores. The plan of Figure 9-28 also provides for up to two signal processor communities, each consisting of two duplicate Signal Processor Circuits and their call stores.

Two duplicate buses (CC-CS bus 0 and CC-CS bus 1) link together the Central Control Circuits, their call stores, and the Signal Processor Circuits. Each signal processor community has two duplicate buses (SP-CS bus 0 and SP-CS bus 1) linking its Signal Processor Circuits and call stores. Each bus consists of 53 pairs to the call stores and 26 pairs from the call stores. Each call store can communicate on either or both duplicate buses, regardless of whether it is working with a Central Control or a Signal Processor circuit.
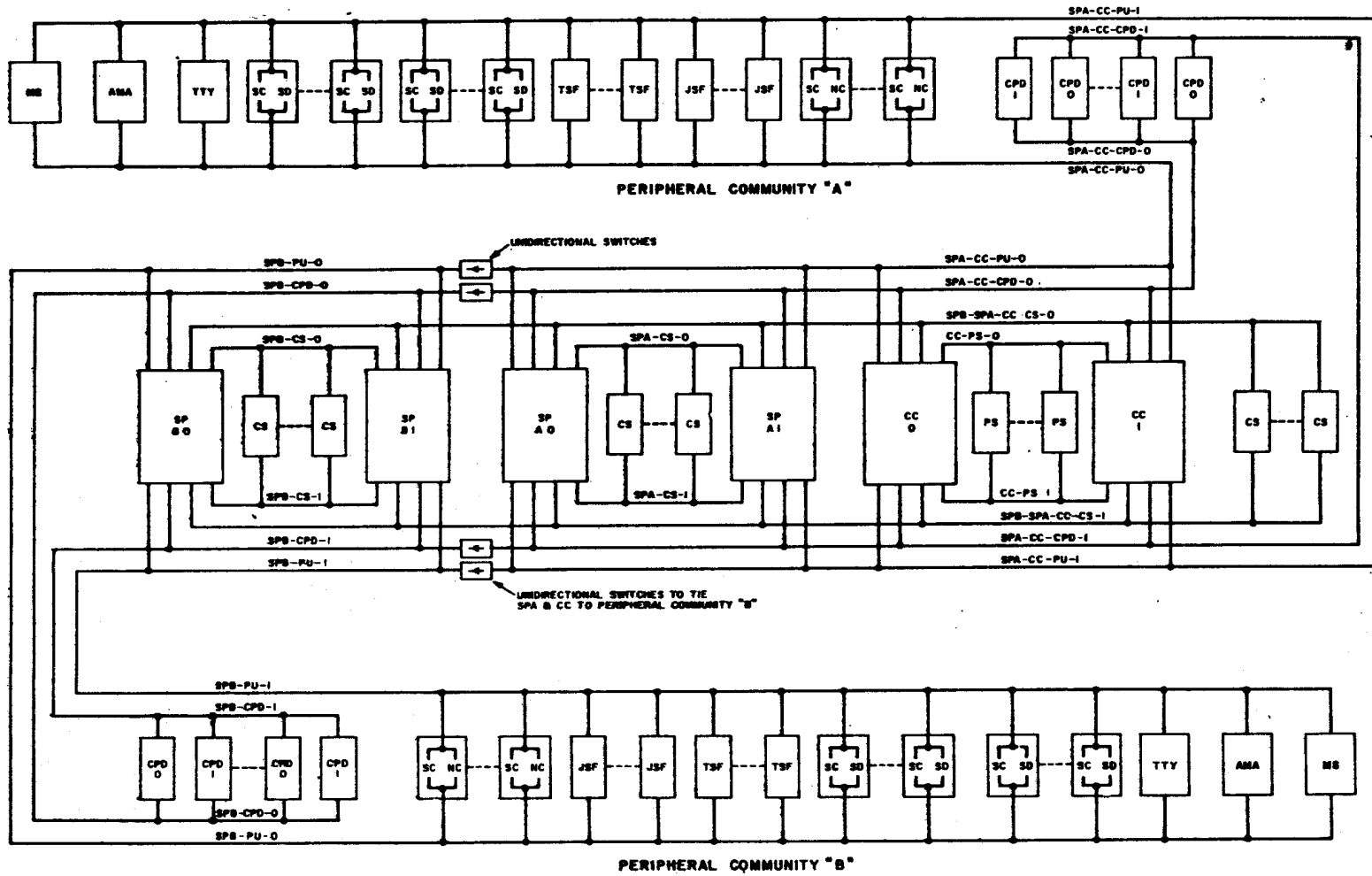
Figure 9-28   Office With Two Pairs of Signal Processors

9.5 CENTRAL CONTROL

1. General

Central Control (CC) is the primary data processing unit of the No. 1 Electronic Switching System. Its purpose is to execute a program or sequence of instructions obtained from a program store. Under direction of the program, the central control receives input information from lines and trunks via the scanners, performs logical and arithmetical operations, and causes basic actions to be carried out in all parts of the system in the process of completing telephone calls and diagnosing system troubles.

The logic circuits used in the central control are assembled on 4-by 7-inch printed circuit boards which plug into rack-mounted connectors. Four 7-foot bays house the equipment for central control. Various types of boards (commonly called packages) provide logic gates, flip-flop register elements, amplifiers, etc. The boards are interconnected to form specific logic functions by wiring together the terminals associated with the connectors. External communications between the CC and other system units are conducted over twisted pair cables which are connected to receiving or transmitting gates in the respective units.

2. General Method of Operation

The object of the central control is to carry out the stored program that has been provided for the system. The stored program is composed of sequences of instructions, each carrying out a data processing step (or steps) that contribute to the task to be performed. The order structure is defined to be the repertoire of instructions from which programs are constructed. Figure 9-29 shows the basic data processor of the No. 1 ESS. This consists of Central Control, Program Store, and Call Store. As will be seen later, the central control also deals with peripheral equipment, but the basic data processing operations are associated with the two stores.
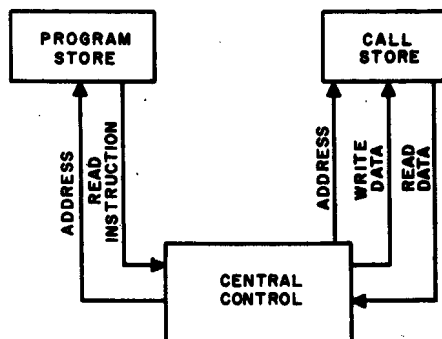
Figure 9-29   Block Diagram of Data Processor

The program store contains the programs for both call processing and system maintenance. In addition, each customer line has associated with it a number of translation constants. These constants are stored as translation words in the program store. In the face of system troubles, the program and translation words must be retained. Accordingly, the program store is a semipermanent memory which is not altered in the course of program execution. It may be addressed in order to read out instructions and data, but it may not be written into.

Temporary, or destructible, memory is provided in the call store. It contains call processing data that changes as calls are established and terminated in the system.

To provide optimum data processing capability, the central control can simultaneously address the program store to request an instruction, and the call store for a data operation.

We, therefore, have as the most basic elements of central control the items shown in Figure 9-30, namely a Program Store Address Generator, a Program Store Data Reception Center, (Buffer Order Word Register), a Call Store Address Generator, and a call store data reception and data transmission register (Buffer Register). The call
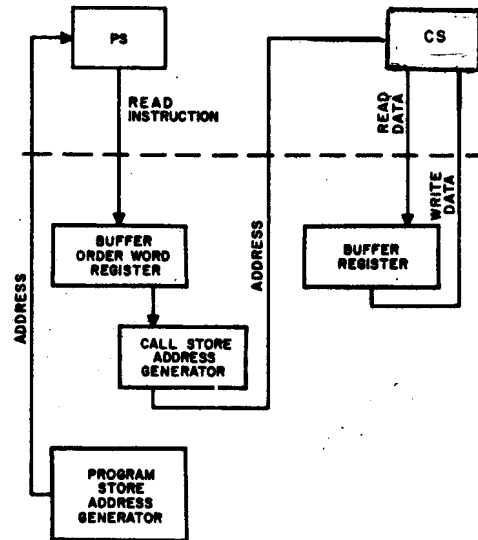
Figure 9-30   Basic Elements of Central Control - Part 1

store address generator will be described later.
The buffer register serves both as a recipient of
information from the call store and as a source
of information to be transmitted to the call store.

A. INDEXING

As shown in Figure 9-31, the Buffer Order Word
Register has associated with it, a buffer order word decoder
so that gates may be controlled on the basis of the instruc-
tions read from the program store. Instructions are coded
pieces of information used to specify for central control the
operations that it must perform. Central control performs
the operations by gating information from one place to
another internally, and by sending signals out to the units
which it controls, such as the call stores and peripheral
units. In order to be able to manipulate information re-
ceived from the call store, CC must contain a number of
internal registers (indexing registers X, Y, Z). These
indexing registers are nothing more than flip-flop groups
that can store a binary word of information.

All index registers are 23 bits long. In terms of
hardware, they become 24 bits long because there are two
flip-flops on a single circuit package. In general, the
extra flip-flop is not always usable for some disassociated
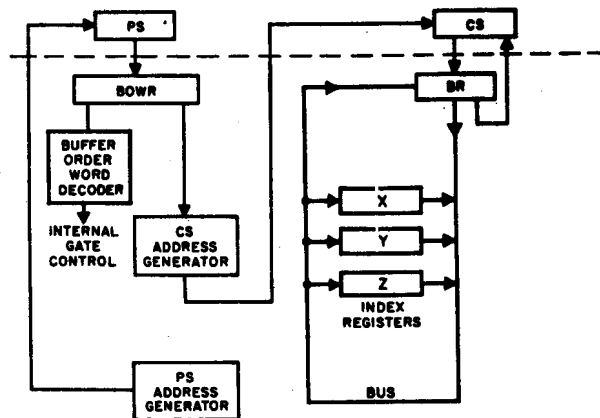function because a common gating input lead is used for

Figure 9-31 Basic Elements of Central Control - Part 2

inserting information into both flip-flops on a package. In
order to gate information into these registers or flip-flop
groups most efficiently, a common bus system is provided.
This bus consists of 23 leads. The index registers gate
information onto this bus, and the bus information may be
gated back into the index registers. The buffer register is
also an index register but has the additional function of
handling communications with the call store.

In order to carry out this process known as indexing,
the block diagram must show an index adder which has access
from the buffer order word register and from the bus system
common to the index registers. The index adder then accepts
information from the two sources, adds the quantities, and
deposits the sum in its internal output register. This is
shown in Figure 9-32.

In the actual detailed block diagram of central
control, the index adder consists of: an index addend
register, which receives information primarily from the
BOWR; an index augend register, which receives information
primarily from the bus system; an index adder to process the
data; and an index adder output register to receive the
result and pulse out to the call stores. Note that the
index adder system encompasses the function of the CS
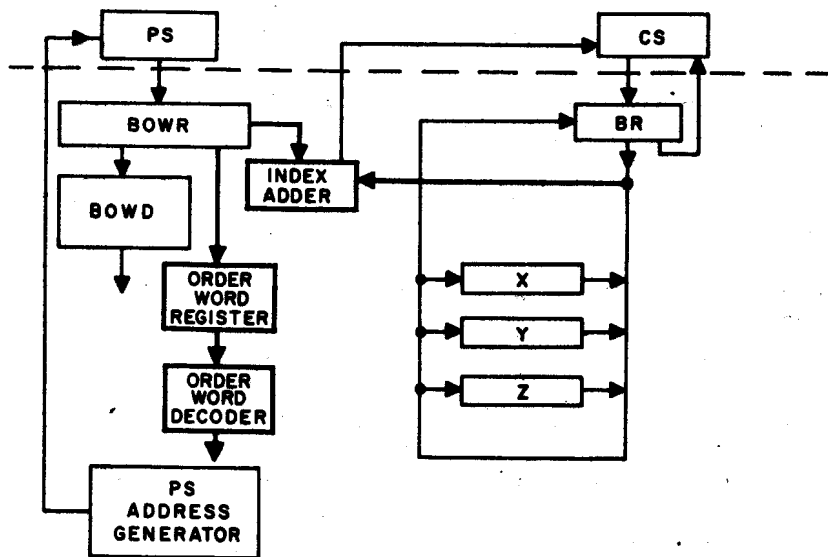address generator of Figure 9-32.

Figure 9-32   Basic Elements of Central Control - Part 3

B. BASIC ORDER WORD STRUCTURE

Figure 9-33A also shows the format for deriving the basic order structure of the binary words sent to central control from the program store. Each 44-bit instruction word consists of a 7-bit hamming and parity check word and a 37-bit instruction. Each instruction is divided into an operation portion and a constant or data-address portion. If the data-address field is to be used as a memory address, it is considered as a 21-bit word extending from bits 0 through 20. The buffer order word decoder then uses a 16-bit operation field (bits 21 through 36 of the instruction as it appears in the buffer order word register) to decode the instruction. If, however, the instruction uses the data-address word as data to be manipulated with the index register system, the data-address field is then extended to 23 bits and the instruction is determined by a 14-bit operation field (bits 23 through 36 of the buffer order word register).

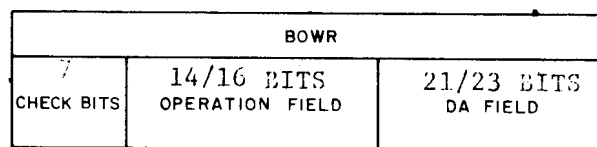| BOWR		
7 CHECK BITS	14/16 BITS OPERATION FIELD	21/23 BITS DA FIELD

Figure 9-33A   CC - Buffer Order Word Register

In the layout of Figure 9-33B the instruction requires that a memory word be moved to the X register. The operation field then contains the binary equivalent of the memory-to-X register instruction (MX in symbolic notation) and specifies register Y in the index register portion. The numeric 3 is shown in the data-address field in the block labeled constant. The conmplete instruction tells CC to read the memory and gate its contents first into the buffer register, which is the primary destination for all data from the call stores, and then gate the buffer register contents into the X register. The constant and index register sections are used in the following way. First, the address in memory that we wish to read must be identified. This is found by taking the contents of one of the index registers (in this case, index register Y is specified) and adding to it the contents of the constant section of the instruction, i.e., 3. We will, therefore, read the contents memory at address Y + 3. Y might be the starting address of a series of words that make up a table relating to an originating register. The constant 3 indicates that we are interested in the fourth word in the originating register. (The first word is 0.)
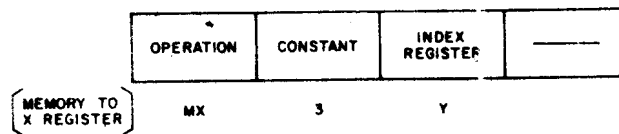
OPERATION	CONSTANT	INDEX REGISTER	———
MX	3	Y	

{MEMORY TO X REGISTER}

Figure 9-33B Basic Instruction Format

C. MASKING OPERATIONS

One of the most frequent operations encountered in central control is that of AND (or product) masking, which is the selecting of only a certain bit or bits of a data word prior to placing that word in a flip-flop register for further data processing. The remaining bits are masked out and are not transmitted to the register. Although most data words are 23 bits long, operational data itself is rarely of that length. For example, a single binary coded decimal digit requires only 4 bits. The memories are used most efficiently when groups of these subwords are packed together in one 23-bit memory word. When a particular subword is summoned by CC, the undesired bits must be masked out so that their presence can have no effect upon further manipulations of the desired subword. Masking will delete unwanted bits. The mask circuit added in Figure 9-34 is controlled by a 23-bit register (the logic register) which can blank any

combination of the bits of a word while not blanking the
rest. The mask function is obtained by combining the con-
tents of the logic register with the data word in AND gates,
on a bit-by-bit basis. Wherever a bit in the logic register
is 1, the corresponding bit of the data will pass through;
wherever it is 0, the data bit will be set to 0. The
following example illustrates how the middle 4 bits of a
sample 8-bit word are retained while the others are AND
masked by the control word.

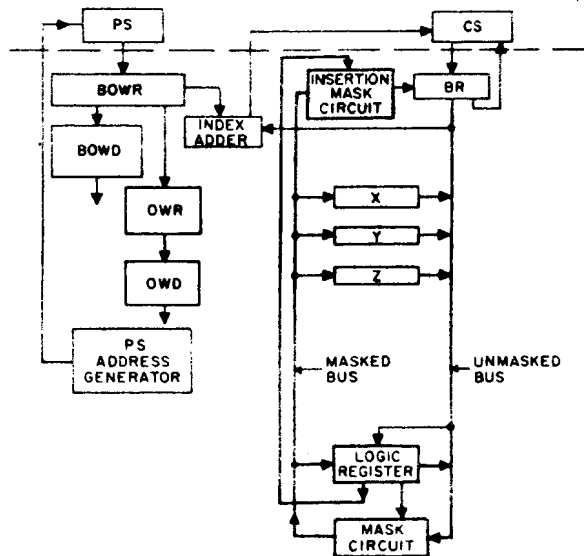|	
10011010	Data
AND	
00111100	Mask Control
00011000	Masked Result

Figure 9-34   Basic Elements of Central Control - Part 4

The mask circuit has also the ability to form the
logical OR and the EXCLUSIVE OR functions in addition to its
normal AND masking ability. These functions are used when
dealing with certain classes of instructions. For example,
the orders UMX, UMY, and UMZ use the OR masking feature of
the mask circuit to form the logical OR of a memory reading
with the contents of the registers X, Y, or Z, respectively.
The resultant word replaces the contents of registers X, Y
or Z, respectively. These orders are carried out by

addressing the memory and moving the contents of X, Y, or Z via the unmasked bus into the logic register. The data obtained by the memory reading is then moved from the buffer register through the mask circuit, where the OR mask is applied, onto the masked bus, and into register X, Y or X.

The mask circuit is placed on the bus system which interconnects the input gating and output gating of the index registers. The mask circuit splits the input and output portions into two buses, the masked bus, and the unmasked bus. In this position, the masking operation is potentially applicable to all transfers of data words from one register to another, or to a transfer between a word in memory and a flip-flop register.

Conventional masking, as described above, is used for normal data operations. There are many instances, however, where it is required to insert subword information into a word that is contained in the buffer register and is to be returned to the call store. Suppose for example, as shown in Figure 9-35, that we wish to insert certain information into bits 0 through 3 of a word A, which has been read from the call store. Under these circumstances, we may wish to retain the information contained in the other bits of the word. An insertion mask circuit provides this ability. The logic register is again used as the source of the mask, but its control differs from the product masking just described. Those bit positions of the buffer register corresponding to bits of the logic register which contain zeroes are left unchanged; the remaining bits are replaced by the selected subword which is gated through the insertion mask circuit by the logic register bits which are ones.
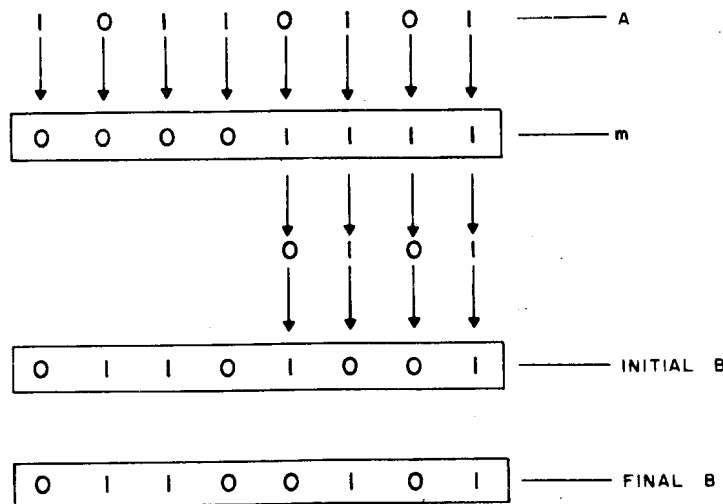
Figure 9-35   Insertion of A into B through Mask m

It should be noted that insertion masking can be applied only to data that is being moved through the mask circuit into the buffer register. In a single data processing step, either product masking or insertion masking may be applied, but never both. Figure 9-34 shows the inclusion of these circuits in the CC block diagram.

D. PROGRAM ADDRESS REGISTER (PAR)

Figure 9-36 shows more details of the program store address generator. In the previous paragraphs the obtaining of orders from the program store and their execution by central control has been explained for a sequence of orders which are located at consecutive addresses in the store. That is, an address is transmitted from the program store address generator in CC to obtain an order to be executed; that address is incremented by 1, and the new incremented address is then sent out to obtain the next order in the sequence. When the CC executes a transfer instruction, the original sequence is terminated and a new sequence of orders is acted upon. The transfer address is defined as the address of the first instruction of a sequence to which a
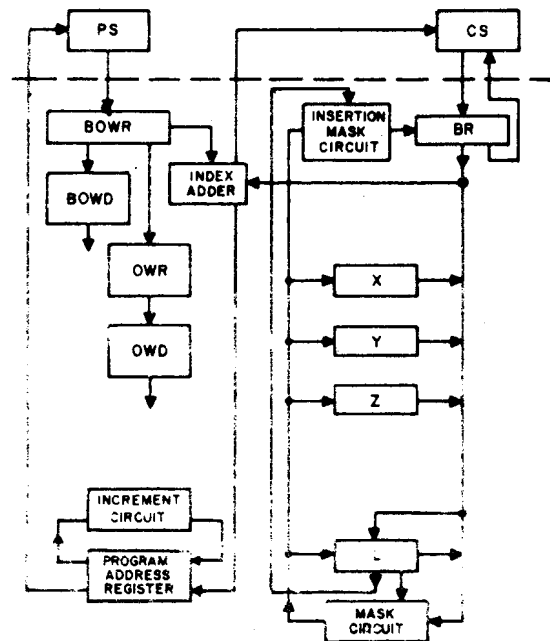
Figure 9-36   Basic Elements of Central Control - Part 5

transfer order passes control. The data-address field and/or
the contents of a specified index register will provide the
transfer address. In Figure 9-36 the PS address generator
has been broken down into its two major components: (1) the
program address register, which controls the address trans-
mission to the program store; and (2) the increment circuit
which updates the address in a stepped manner when proceeding
through a normal program. In order to supply a transfer
address to the program store, connection is made between the
index adder and the program address register. By this path,
a transfer address can replace the normally incremented pro-
gram address as part of the execution of a transfer order.

E. ACCUMULATOR (K)

A K adder and K register (K = accumulator) have been
introduced in Figure 9-37. These two blocks really imply a
complete arithmetic system which performs the majority of
data processing functions. As in the case of the index
adder, the accumulator adder has associated with it an addend
register and an augend register to contain the information
to be processed. The accumulator register normally receives
the results from the adder. The augend register can only be
set to zero or to the value of the accumulator, while
incoming words are inserted into the addend register via
the masked bus. Thus, numbers can either be combined with
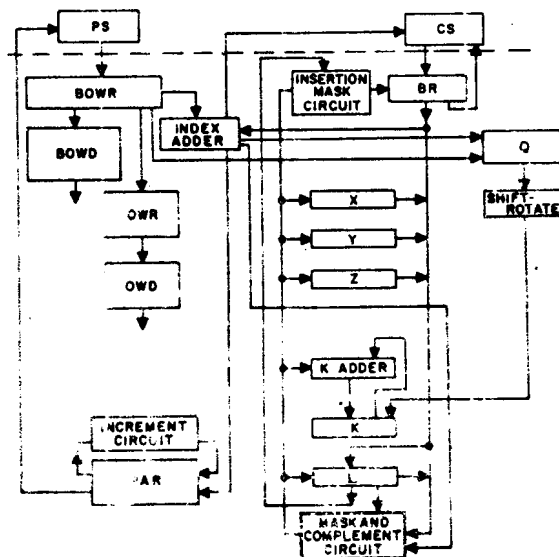zero or with the present contents of the accumulator.

Figure 9-37   Basic Elements of Central Control - Part 6

Each word treated by the accumulator system is a 23-bit binary number (integer) with the least significant bit (or right-most bit) labeled bit 0, the next significant bit labeled bit 1, etc. The most significant (left-most) bit in the data word is designated bit 22. Positive numbers are identified by a 0 in bit 22, negative numbers by a 1. The remaining bits (bits 21 through 0) of a positive number indicate the magnitude of the binary integer. In the case of a negative number, the one's complement of the magnitude is denoted in bits 21 through 0. A negative integer is, therefore, represented with a one in bit 22 (the sign bit) and the complement of the magnitude (bit-by-bit inversion) of the integer appears in bits 21 through 0. For example, the decimal number +25 would be represented in binary form by:

$$00\ 000\ 000\ 000\ 000\ 000\ 011\ 001$$

The number -25 would be represented in the 1's complement form by:

$$11\ 111\ 111\ 111\ 111\ 111\ 100\ 110$$

The facilities for complementing are shown in Figure 9-37 as an appendage to the mask circuit. It is associated with the mask circuit since this is the most convenient place to affect data. Because the 1's complement binary arithmetic system has been selected, the bit-by-bit complement operation in the mask and complement circuit serves for both the logic complementing of data words and the arithmetic complementing of 23-bit numbers.

The accumulator adder has been provided with other properties so that it may perform the logical functions of AND, OR, and EXCLUSIVE OR. These are important when comparing quantities of data, or when examining them for particular characteristics. In special cases, it can perform these operations and activate decision-making circuits without disturbing the contents of the accumulator register.

Shift and Rotate Functions - Another function which has been incorporated into the accumulator is the ability of shifting or rotating information to the left or the right within the accumulator. Shifting is a frequent operation and is commonly applied when information in a word is not located in the bit positions most convenient for use. The example below shows how an 8-bit word A is affected by a shift to the right by three positions:

```
100 11 010   Initial word A
000 10 011   Word A shifted
```

The same 8-bit word rotated three positions to the right:

        10011010 Initial word A
        01010011 Word A rotated

Note that the operation is similar to a shift, however, the only difference is that no bits are lost. As shown in Figure 9-37, inputs to the rotate shift circuit are from the Q register.

F. FIRST ONE REGISTER (F)

      Another function associated with the accumulator is that of being able to inspect the accumulator contents and detect the position of the rightmost 1. A detect first one circuit is attached to the accumulator which examines all bits and forms a 5-bit quantity representing the position of the rightmost 1. This 5-bit quantity may be placed in the F register as part of the execution of two special transfer orders, TKZRFU and TKZRFZ. These orders include the decision to transfer to a new sequence of instructions if the contents of the accumulator register is +0 (all 0's, including the sign bit). Otherwise the binary value of the rightmost 1 is placed in the F register. The rightmost 1 detection function is very useful in dial pulse scanning to find which of a number of dial pulse receivers recorded activity during this particular scan; or in supervisory scanning, to determine which trunk had reported a seizure or disconnect. An example is shown in Figure 9-38.
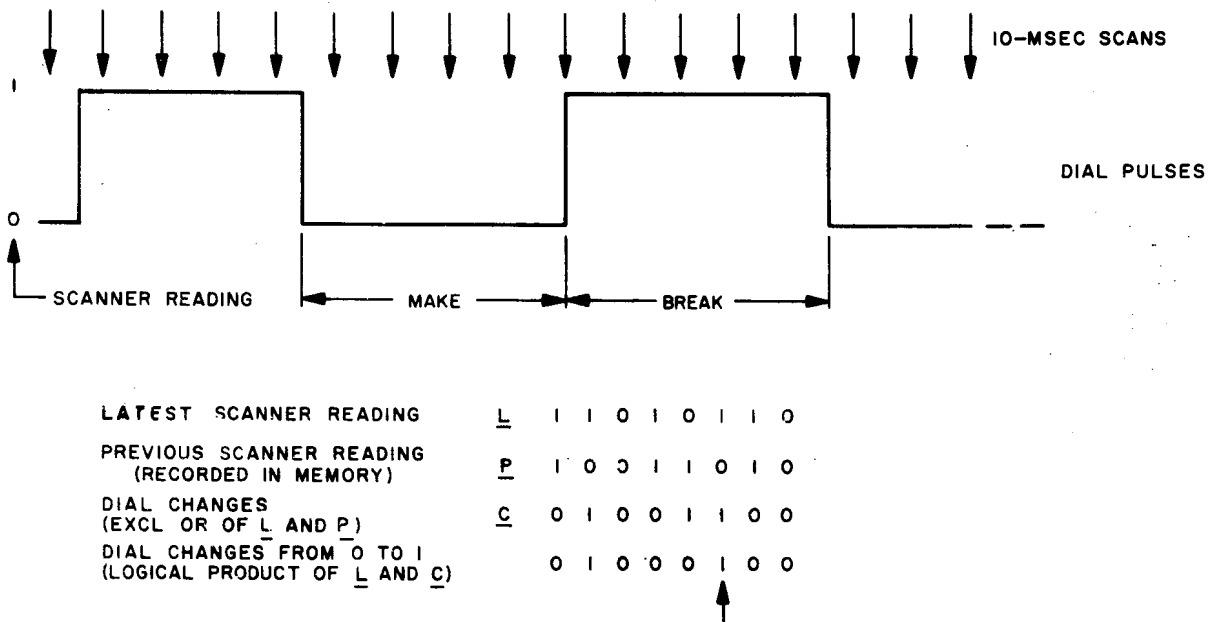

LATEST SCANNER READING	L	1	1	0	1	0	1	1	0
PREVIOUS SCANNER READING (RECORDED IN MEMORY)	P	1	0	0	1	1	0	1	0
DIAL CHANGES (EXCL OR OF L AND P)	C	0	1	0	0	1	1	0	0
DIAL CHANGES FROM 0 TO 1 (LOGICAL PRODUCT OF L AND C)		0	1	0	0	0	1	0	0

Figure 9-38 Use of Logical Operation of Count Dial Pulses

G. MEMORY ADDRESS DECODER (MAD)

Figure 9-39 indicates one of the more complicated aspects of central control operations, the process of reading data from the program store. As was indicated earlier, the program store is primarily a source of instructions, the call store primarily a source of data. However, translation information in the form of data is made available in the program store and facilities must be provided in the system so that this information is recognized as data and not as an instruction. Most of the memory reading instructions can be used to obtain data from the call store or the program store. This is accomplished by providing different addresses for call store and program store locations. The range provided by the 21-bit data-address field of memory reading instructions is sufficient to specify any call store or program store location within the physical limitations of No. 1 ESS store capacity. A memory address decoder circuit is used to examine the output of the index adder whenever a memory operation is called for. Whenever a memory instruction is being executed and a call store address is formed in the index adder, the memory address decoder will send the output of the index adder directly to the call store and readings will proceed in the normal fashion. If the memory address decoder recognizes an address associated with data in the program store, it must initiate a sequence operation which will be controlled by a sequence circuit. This step is required because the central control cannot simultaneously obtain from the program store both an instruction and the data that it is to manipulate.
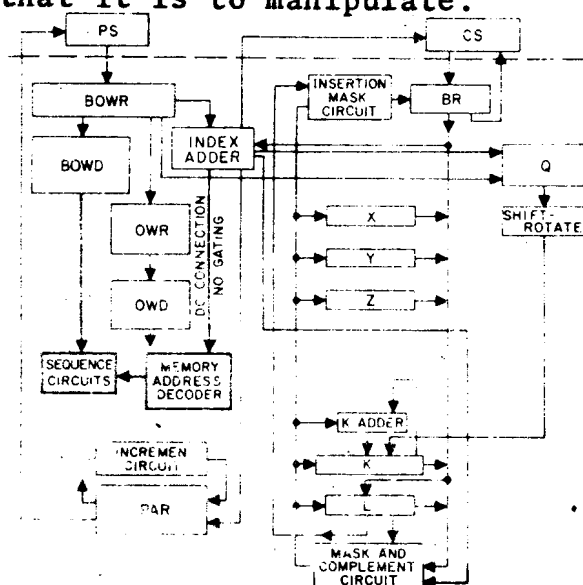

Figure 9-39   Basic Elements of Central Control - Part 7

H. CENTRAL CONTROL TIMING

The central control is a synchronous data processor using a multiphase clock. The basic cycle time is 5.5 microseconds. Each 5.5 usec cycle is subdivided into 22 intervals numbered from 0 to 21 as shown in Figure 9-40. Identification of a particular clock pulse is given by naming the interval which contains the clock pulse leading edge, followed by the letter T, followed by the interval number of the clock pulse trailing edge. For example, a pulse which commences at time 3 and continues until time 5 is identified as 3T5. In this manner, the 22 intervals, each of 0.5 usec duration, are numbered 0T2, 1T3, 2T4, through to 19T21 and 20T22. Note that T22 of one cycle corresponds to T0 of the next. There are three principal phases of the clock which are used to control the transmission of data over the internal bus system. These are 0T8, 10T16 and 16T22. Associated with each of the three principal clock phases are shorter phases (or associated sampling pulses) 0T6, 10T14 and 16T20. As indicated in Figure 9-40, the longer phases are used to gate information from a register onto a bus. The associated sampling pulses are used to sample the contents of a bus for gating into a flip-flop register. The half-microsecond guard interval ensures that the bus being sampled is not changing at the end of the sampling pulse. The half-microsecond pulses, in general, provide the timing required for all other internal functions, and are used to control the communication links between the central control and associated system equipment.
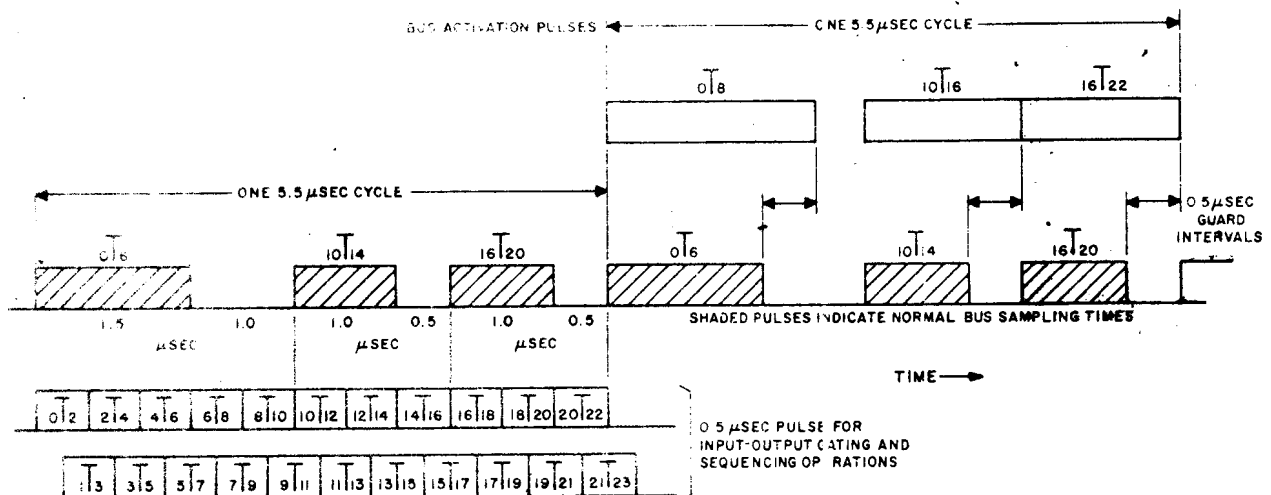

Figure 9-40   Central Control Timing Pulses

Table 9-1 shows what happens in consecutive time slots. Let us assume that the instruction at address AA is the instruction "memory to the X register at the address BB plus Y." Assume that BB plus Y is a program store address. At time 1, the order word register (OWR) has the previous instruction, the buffer order word register (BOWR) has the instruction in question, and the program store address register (PAR) has the address of the next instruction and, in fact, has already sent this address to the program store.

TABLE 9-1

TIME SEQUENCE OF WORDS PASSING THROUGH
BOWR, OWR AND PAR WHEN
READING DATA FROM PROGRAM STORE

TIME SLOT	BOWR	OWR	PAR
1	(AA)	(AA-1)	AA+1
2*		(AA)	BB+(Y)
3*	(BB+(Y))	(AA)	AA+1
4	(AA+1)	(AA)	AA+2
5	(AA+2)	(AA+1)	AA+3

(-) Symbol meaning word stored at this address or in this register.
Instruction at address AA is MX,BB,Y,-; BB+(Y) is an address of data in the program store.

*These actions are controlled by central control internal sequence circuits since the operation covers more than one central control cycle time.

At time 2, this reading, which is the instruction stored at address AA plus 1, has been received and the instruction AA has been gated to the order word register. In the meantime, the program store data word has been recognized, and address BB plus Y has been gated into the program store address register. A sequence circuit causes the rejection of instruction AA plus 1 from the buffer order word register since it must be prepared to receive the data which is stored at BB plus Y. At time 3, the buffer order word register receives this data, the order word register still retains the instruction in question, and the program store address register is now set to address AA plus 1. This address, AA plus 1, was saved in the increment circuit associated with the program store. The information from the buffer order word register is now passed via the index adder and the mask and complement, the masked bus, and the insertion mask to

the buffer register. The buffer register, in turn, passes the information via the bus to the X register under the control of the order word decoder, just as if the instruction had been a conventional call store data reading. At time 4, the instruction is actually executed, that is, the information is gated to the X register. The new instruction is now in the buffer order word register, the program store address register has already advanced to the next instruction, and at time slot 5, the normal fetching and executing of the sequence of orders continues. It may be noticed that the time required to read data from the program store is three cycles as opposed to the conventional single-cycle operation required for reading data from the call store. The three cycles arise because one cycle is necessary for the basic instruction, one extra cycle is necessary because the reading of the next instruction from the program store arrived before it could be used, and the third cycle is necessary to read the data from the program store.

I. OVERLAP OPERATION

There is a degree of overlap operation within the CC. This means that two orders are normally processed simultaneously with due care taken that the demands of the two never conflict. Normally, central control requests an instruction from the program store every 5.5 usec. Actually, in most 5.5 usec cycles, CC is at the same time:

    (a) Completing the execution of the instruction at some address, say 200

    (b) Carrying out the preliminary operations of checking, indexing, and index register modification for the instruction at address 201, and

    (c) Sending the address 202 to the program store as shown in Figure 9-41.

To make possible this overlap type of operation, when indexing is completed, the 16 bits of the operation field are sent to the order word register (OWR). Note that the check bits are no longer needed and that the DA field, possibly modified, is available at the IAOR. Thus, the BOWR can be made available to receive the next instruction. While the execution of one instruction is completed under the control of the OWR, the indexing for the next instruction is carried out under the control of the BOWR.

Decoders are associated with the BOWR and the OWR. The BOWR controls whatever gates are necessary to carry out the indexing operation for the instruction currently in the BOWR. The OWR controls the gates that are necessary to complete the execution of the instruction in the OWR.
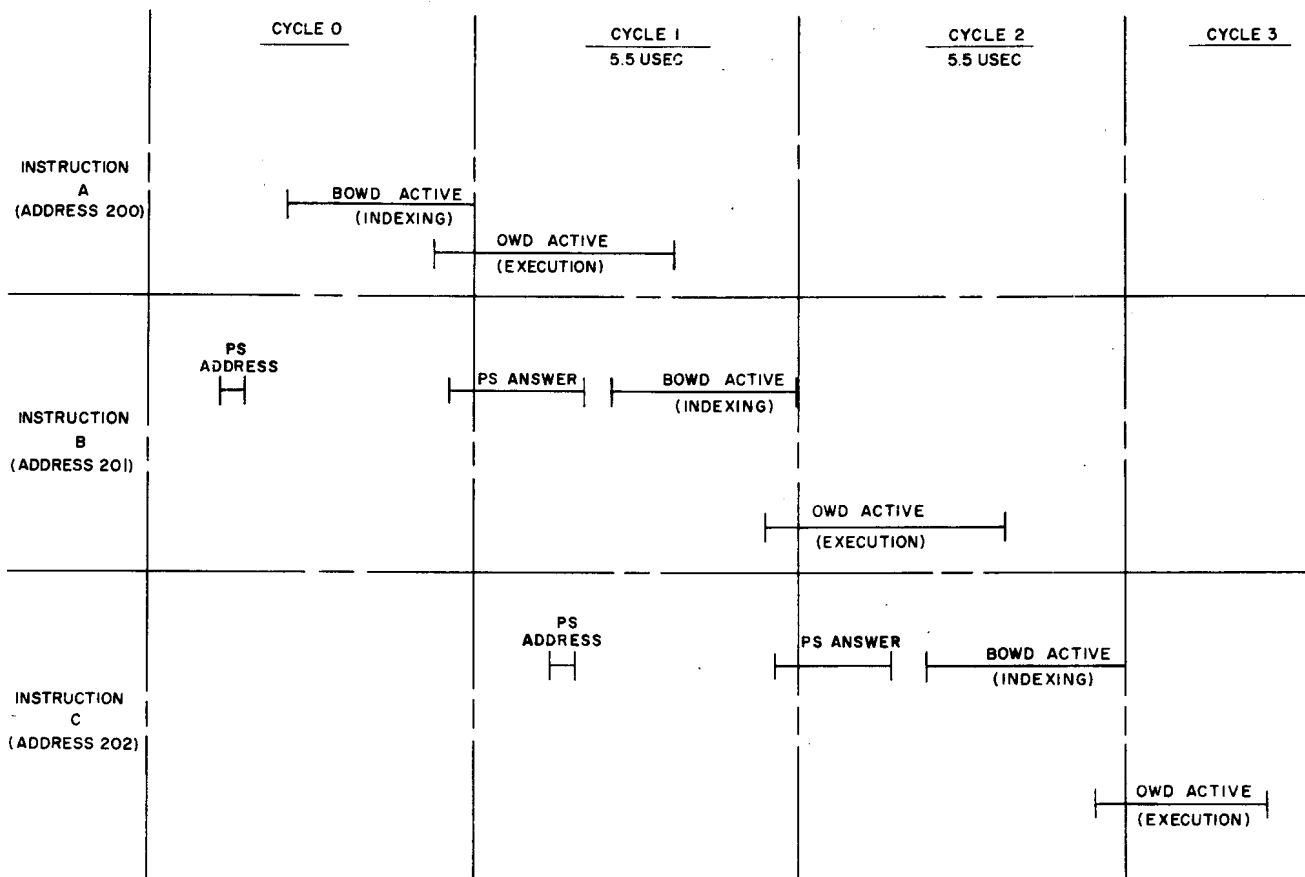

Figure 9-41 Overlap Operation

J. SEQUENCING CIRCUITS

Sequencing circuits are needed whenever the information in the order word and buffer order word registers is insufficient, on a combinational circuit basis, to specify

all actions within the system. They supplement the functions performed by the OWD and BOWD in cases that require the extension of cycle time to complete an instruction. Sequencing circuits are needed for the following operations.

(a) If the information from the program store is incorrect as determined by an error-detecting circuit, in one or more bits, an error correction circuit is available in the central control to remedy the situation. Before the information in the buffer order word register can be used, the error must be corrected. If a single bit in the BOWR is in error, the error correction sequencing circuit causes one cycle to be skipped and corrects the information in the buffer order word register during this cycle, or requests a retransmission if the error is incorrectable. Whenever an indication occurs in central control that a program store reading was in error and cannot be corrected, a reread is automatically initiated by the error correction circuit. A reread is required when a double error is detected, when an address error is detected, or when no All-Seems-Well pulse was returned from the program store with the original reading.

(b) A special sequencing circuit is required to read data words from the program store. The read-write sequencer is used for this purpose. It is also used to write control words into the program store.

(c) In the same way that data can be read from the program store, instructions can be read from the call store. However, each instruction requires two call store readings since one 23-bit call store word does not contain sufficient information to define the operation and data-address fields. A sequencing circuit is provided to control the reading of two consecutive call store addresses based on the address stored in the program address register, and to store the contents of these readings in the buffer order word register. (They must not go into the buffer register since this register is used only for data manipulation.)

(d) If a parity failure occurs on call store readings, or if an All-Seems-Well does not arrive from the call store, then the call store must be reread. The same is true for writing operations when the call store senses that a faulty transmission has occurred. Under the control of sequencing circuits the information must be reread or rewritten.

(e) The central control includes a multilevel interrupt system. Certain timing signals or hardware check failure signals that are generated either internally or externally to central control will activate the interrupt system. Activation of this system causes whatever sequence of orders is presently being executed to be interrupted and control is transferred to a pre-determined interrupt program sequence. An interrupt sequence circuit effects this transfer and stores the contents of certain central control registers in the call store. The stored information indicates, among other things, where a transfer must be made to return program control to the interrupted sequence. In most instances, such a return to the point of interruption is made after the function initiated by the interrupt signal has been performed. The various interrupt signals are assigned to one-of-ten priority levels: A, B, C, D, E, F, G, H, J or K, where A represents the highest priority level and K is the lowest. The interrupt system provides simultaneous and sequential lockout of interrupt signals, so that only higher priority interrupts can break into interrupt or program sequences caused by a lower-level interrupt. When no interrupt signal is being honored by the interrupt system, the central control is said to be operating in the base level, or level L.

(f) The go-back-to-normal sequencing circuit performs the inverse function of the interrupt sequence circuit. Following an interruption, the work that had been interrupted must be resumed. The sequencing circuit restores the original contents of the program address register and the buffer register so that the interrupted program may be resumed as if no interrupt had occurred.

(g) A special sequencing circuit is required to read signal processor call stores. Signal processor call store readings require a 2-cycle operation. The signal processor call store sequencing circuit, therefore, introduces an extra cycle of delay so that the information from the signal processor call store may return to central control in time for processing.

(h) The peripheral sequencing circuit is a special sequencing circuit associated with communications between central control and the central pulse distributor and peripheral equipment.

(i) In No. 1 ESS there are two central controls, one serving in standby status as a potential replacement in case the other central control experiences a hardware trouble; the other unit is designated as the active CC and actually is in control of the switchgear of the No. 1 ESS. The active control can perform tests on the standby. Certain of these tests (off-line operation) require the aciive CC to stop the standby's execution of instructions, place new data in the standby, and restart it⋅for further tests. A start-stop sequence circuit is provided which, in the standby unit, responds to stop signals transmitted from the active unit. The enabling of the start-stop sequencer causes it to inhibit the decoders and remaining sequence circuits. Similarly at the end of the sequence, start signals from the active CC reactivate the standby's decoders and sequencers. These inhibit signals stop the obtaining and executing of program orders.

(j) The transfer sequencing circuit carries out the steps for direct and indirect transfers. It not only steers the transfer address to the PAR and blocks the decoders during the cycles required to effect the transfer, but it also handles index modification and return address options associated with transfer orders.

(k) When the No. 1 ESS includes a Signal Processor Circuit, the signal processor normally has control over the central pulse distributor and peripheral equipment. A signal processor lockout sequencer provides for an automatic and essential delay of one cycle of central control operations for certain orders and conditions. Program execution in the central control and the signal processor are not in step with one another. In certain CC program sequences, momentary access to the central pulse distributor and/or peripheral equipment may be required with the execution of peripheral orders. The central control responds to such orders by transmitting stop pulses to the signal processor to ensure that it does not also attempt

to address the same peripheral unit. The signal processor lockout sequencer responds to the first of a chain of peripheral orders by allowing the first signal processor stop pulse to be transmitted while delaying the execution of the CC's peripheral order for one machine cycle. This delay ensures that the signal processor has completed any communication with the CPD or peripheral equipment in question that may have been in progress at the time that the CC received the peripheral order. Once central control seizes control, the second and following of a chain of peripheral orders are executed without additional delay cycles. It should be noted that a peripheral order requires two central control cycles for completion (the peripheral sequencer provides the gating for the second cycle). Accordingly, a chain of peripheral orders is a set that is executed every second cycle. In most instances, the orders appear in the following sequence:

Address	Instruction
AA	Peripheral Order
AA+1	Nonperipheral Order
AA+2	Peripheral Order
AA+3	Nonperipheral Order
AA+4	Peripheral Order
.	.
.	.
.	.

K. COMPARE AND TRANSFER OPERATIONS

Compare instructions and transfer facilities are illustrated in Figure 9-42. Compare instructions are instructions which compare internal data or a memory word with the contents of some register and gate the results onto the bus to which are attached sampling gates and flip-flops. These flip-flops, called the C flip-flops, can store the overall comparison status of the data on the bus without storing the full 23-bit bus information. One C flip-flop stores the sign bit, i.e., bit 22, the most significant bit on the bus. The other C flip-flop indicates whether the bus contained all 1's or all 0's (homogeneity) or a non-homogeneous quantity. Therefore, this C flip-flop indicates
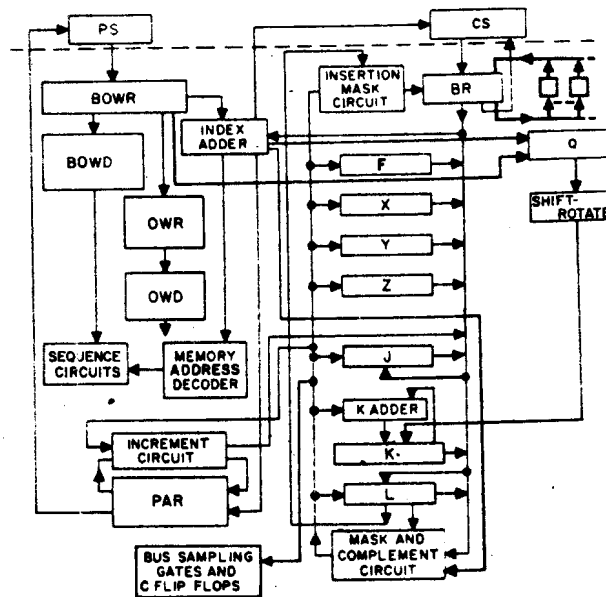
Figure 9-42   Basic Elements of Central Control - Part 8

whether or not the bus was arithmetic 0. When examined, the two C flip-flops, in combination, will tell central control whether one-of-eight particular transfer conditions has been met. The eight states used in transfer orders and their mnemonic representations are:

P	Plus	Sign = 0
M	Minus	Sign = 1
AZ	Arithmetic zero	Homogeneity = 1
AU	Arithmetic unzero	Homogeneity = 0
LZ	Logical zero	Sign = 0 and homogeneity = 1
LU	Logical unzero	Sign = 1 or homogeneity = 0
GE	Greater than or equal to	Sign = 0 or homogeneity = 1
LE	Less than or equal to	Sign = 1 or homogeneity = 1

A comparison between the contents of an index register and a constant (specified in the data-address field of a Compare instruction) can be determined using the index adder. The contents of the index register is moved via the unmasked

bus, the mask and complement circuit (when complementing is performed), and the masked bus into the index adder. The index adder subtracts the numbers by adding the constant to the complement of the contents of the index register. The result is gated to the masked bus and to the C flip-flops. The results of the comparison may be determined by orders which examine the state of the C flip-flops.

Similarly, an internally generated data word, W, or a data word, M, obtained from memory, can be compared with the contents of the accumulator register in the accumulator adder, and the difference gated directly from the adder to the C flip-flops.

Conditional transfer orders (transfer orders are pre-fixed by the letter T in their mnemonic representation) include orders which examine the C flip-flops. If the state of the C flip-flops match the transfer condition specified by the conditional transfer order, a transfer of program control will be effected; otherwise, the execution of the next order in sequence will proceed. In addition, condi-tional transfer orders are provided which examine the state of the accumulator register directly. There are also conditional transfer orders which transmit the contents of a specified index register to the C flip-flops. The state of the C flip-flops and the conditions of the transfer order then determine whether a transfer is to be made or the sequence of orders is to continue.

In addition to the conditional transfer orders, the order structure includes unconditional transfer orders. When these latter orders are executed in central control, the transfer is always made; that is, the transfer of program control is not conditional on the state of some flip-flop or register in central control. Most conditional and uncondi-tional transfer orders are provided with an indirect addressing option. If the option is not specified, the transfer order is said to be provided with direct addressing or the order is a direct transfer order. In either case, an address is generated in the index adder which consists of the contents of the data-address field of the transfer order, the contents of a specified index register, or the sum of the two. In the case of direct transfers, the resulting address is the transfer address and is gated from the index adder directly to the PAR to effect the transfer. When the indirect address option is specified, the address is con-sidered to be a memory reading address. The data obtained from the corresponding memory location is gated to the PAR as the transfer address.

L. "J" OPTION

Transfer orders are used to shift the execution of program sequences (program control) from one sequence to a second sequence. In many instances, upon completion of the execution of the second sequence, program control is to be returned to the first sequence. To provide a link for the return, the central control attaches special significance to index register J as a "jump" or return address register (see Figure 9-42). A J option may be specified with the transfer orders. When the option is specified, the execution of the transfer to the second sequence is accompanied by the transmittal of the contents of the add one logic circuit (the unincremented contents of that circuit) onto the unmasked bus and from there into the J register. The J register thus contains the address of the point of departure from the first sequence to the second. Its contents may be used by transfer orders in the second sequence to return program control to the first sequence. This ability permits many first sequences to share a common function in a second sequence, thus conserving the number of program orders required to carry out the overall call processing and automatic maintenance functions of the No. 1 ESS.

M. MISCELLANEOUS FLIP-FLOPS

There are a number of miscellaneous flip-flop groups in central control such as the match registers, the match and mode control registers, the CPD echo register, and the bus control flip-flops (this last group selects which of duplicate buses the central control is currently using in communicating with program store, call stores, CPD's, etc.). The contents of these registers may be interrogated and altered by memory reading and writing orders just as if the registers were memory locations in a call store. The memory address decoders respond to addresses assigned to these registers to: (a) transmit information from a specified one of the miscellaneous registers to the buffer register for memory reading orders or (b) transmit information from the buffer register to a specified one of the miscellaneous registers for memory writing orders. The register groups are indicated in the upper right portion of Figure 9-42.

N. COMMUNICATION WITH PERIPHERAL EQUIPMENT

The instructions for addressing peripheral equipment can be summarized as follows. First, there are instructions for addressing only the central pulse distributor. Such instructions are used to set and reset unit status and bus

routing flip-flops in the various units (central control, program stores, etc.) at electronic speeds. In addition, there are general purpose peripheral orders which cause the contents of the F register (set to the proper value by a previously executed order) to be transmitted through the translators and onto the CPD address and CPD execute buses. The same orders also load the addend K register and gate a translated form of this information onto the peripheral unit address bus. Note, as indicated in Figure 9-43, that one-of-seven peripheral unit translators may be selected, based on the contents of the F register. Included in the general purpose peripheral orders are scanning orders which cause the logic register to be reset and its inputs to be connected to the peripheral unit reply bus to obtain the scanner response. There are also special purpose peripheral orders which carry out the peripheral actions described above and also other data processing actions. For example, execution of the order JKMSF causes the contents of register J to be transmitted to the accumulator register and to the C flip-flops. This action is followed by the gating of a memory reading from the buffer register to the addend K register. Finally, the peripheral sequencer is enabled to carry out the CPD and peripheral actions for one scanning operation.
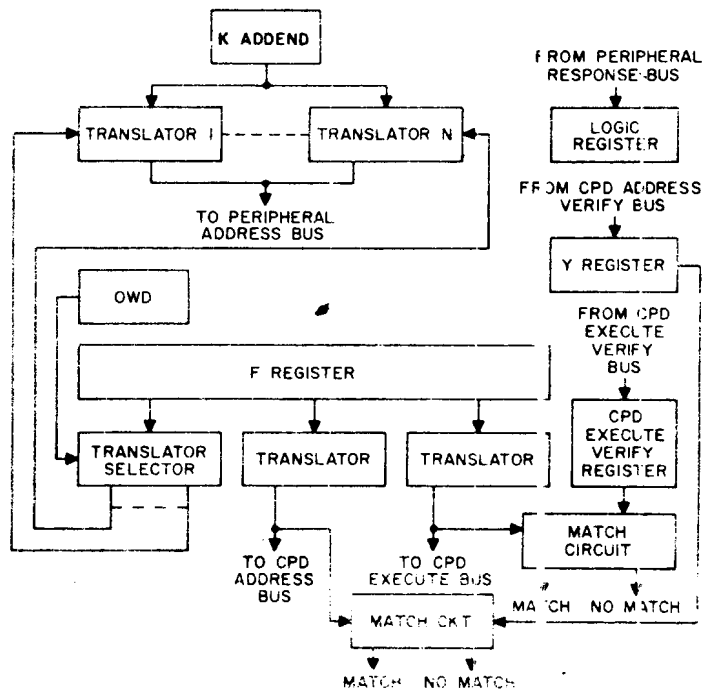

Figure 9-43   Central Control Communication With
               Peripheral Equipment

O. PERFORMANCE AND RELIABILITY

In order to meet reliability specifications, the central control is fully duplicated. The two CC's are referred to as either the active or the standby unit. The active unit performs the actual system functions, while the standby continuously checks the operation of the active. As trouble develops, the status of the units can be switched and diagnostic routines instituted to assist in pinpointing the difficulty.

Within each central control are two internal match buses which provide access to selected information processing points; these are labeled internal match bus 0 and internal match bus 1. Under control of the match control decoder, information from selected points is transmitted to these internal match buses and from there, other gates are enabled to place this information into internal match registers and from there transmit the sampled information to the other central control unit. The match control decoders in both central controls are normally operated in step so that the information transmitted from the first central control to the second is stored in external match registers. Two match circuits serve to compare the contents of these registers. According to the state of the mode control register and the presence or absence of the match condition, the match control decoder generates the corresponding output signals. For example, when the matching circuits are employed in the routine matching mode, a selected sequence of common match points in each central control is matched at the rate of 2 matches per cycle; the detection of a mismatch condition generates a maintenance interrupt signal and further matching is automatically halted.

If the interrupt program cannot be correctly executed, the emergency action circuit quickly times out again and re-starts the interrupt program with a new trial configuration of central controls, program stores, and interconnecting buses. Once the trouble is eliminated from the active portion of the No. 1 ESS, the emergency action circuit is retired and other maintenance programs continue to isolate the trouble.

In the event that the central control cannot cure its own difficulties, the difficulty is displayed via trouble indicator circuits in central control that are wired to audible and visual alarms in the Master Control Center. This center includes indicator lamps which show which CC is the active unit; whether or not a central control is in

trouble; whether or not the emergency action circuit is involved in a maintenance action, etc. The maintenance man, upon analyzing this display, may operate keys or pick selected buttons on the master control center display panel to force a configuration of the central processor to regain a working system. Such actions constitute the last line of defense against system troubles and generally are not to be called upon until all the previously described maintenance hardware and programs fail to clear the trouble.

The data processing capability of the central control is limited in large, busy ESS offices because of the time absorbed in communicating with the peripheral units for the purpose of line and trunk scanning for call originations, disconnects, dial pulse register updating, etc. The Signal Processor has been developed to relieve the CC of these routine tasks. With its own battery of call stores, the SP effectively assumes all the CC's responsibility to the input/output system (without, however, divorcing the CC from that system). The central control is then freed to concentrate on its specialized job of processing the already assembled data.

In very large offices, the central control can accommodate additional peripheral units by serving two separate signal processor communities.

The communication link between central control and signal processor is the same as that with a call store, i.e., the SP occupies a position on the CC-CS bus and is identified by a similar address code.

Recently the No. 1 ESS has been adapted for data communications. Although the demands of a data system differ significantly from a telephone system, the central control is affected mainly from a program standpoint rather than hardware modification. In the same way as the signal processor was used to isolate the CC from the input/output facilities, the Buffer Control is used as an intermediate device to monitor the raw input/output data and assemble it in a form compatible with the speed and format required by the CC.

In a data office, the buffer control inherits the signal processor's position and identifying address on the call store bus.

The signal processor also meets the same reliability and performance standards found in central control. The signal processor is fully duplicated. The two SPs are referred to as either the active or the standby unit. The active unit performs the actual control of the peripheral equipment, while the standby continually monitors the performance of the active. When an occasional trouble develops, the status of the units can be switched by CC, which would then institute maintenance procedures. As part of the remedial action, the CC can divorce the SPs from parallel operation. Call processing is momentarily suspended while CC attempts to recognize the faulty situation. If it establishes that the active SP of the pair is troublefree, CC enlists its aid in diagnosing the faulty unit, meanwhile reestablishing call processing with the good unit. If the active SP is suspected of trouble, the units are switched to place the previous standby unit into control.
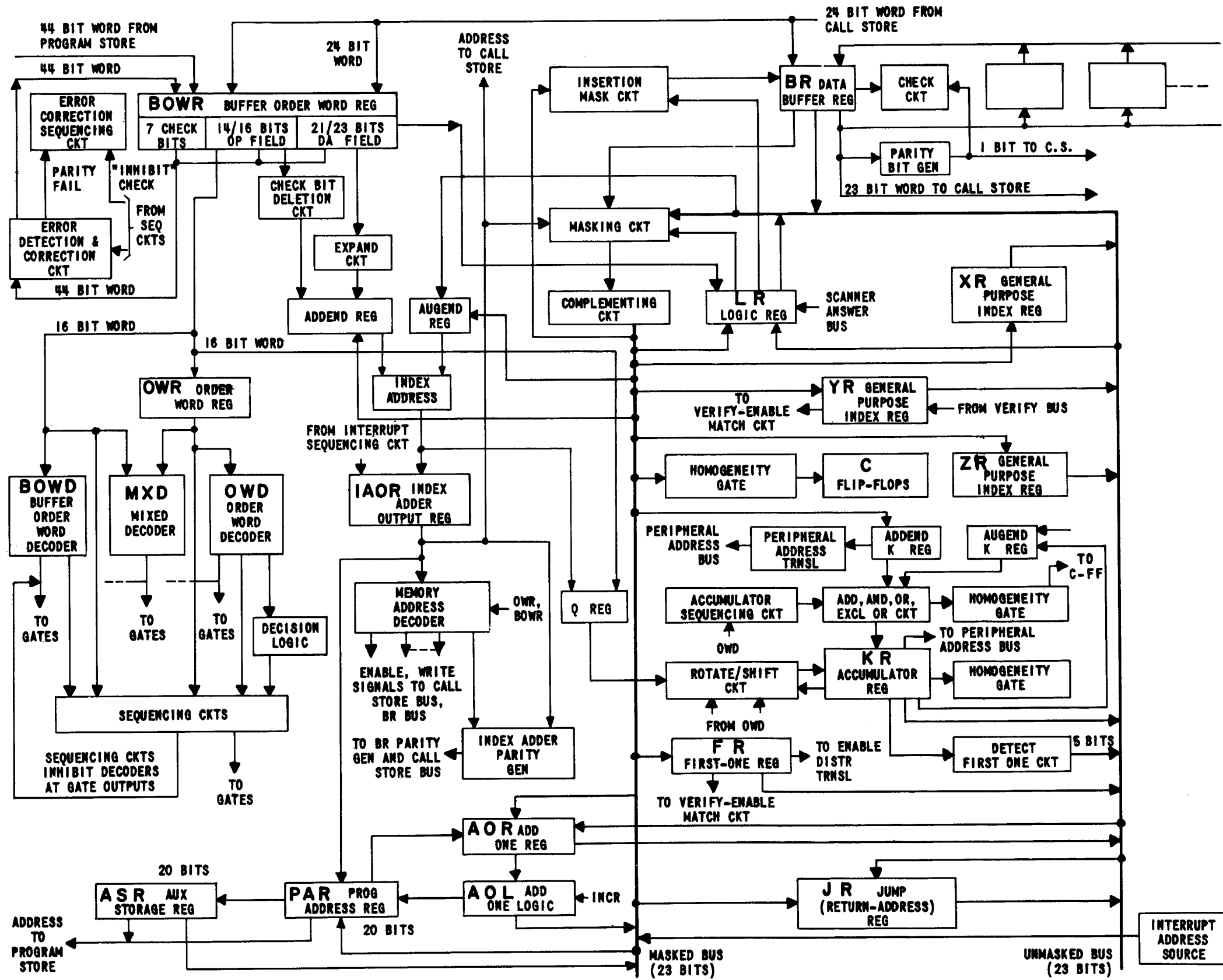
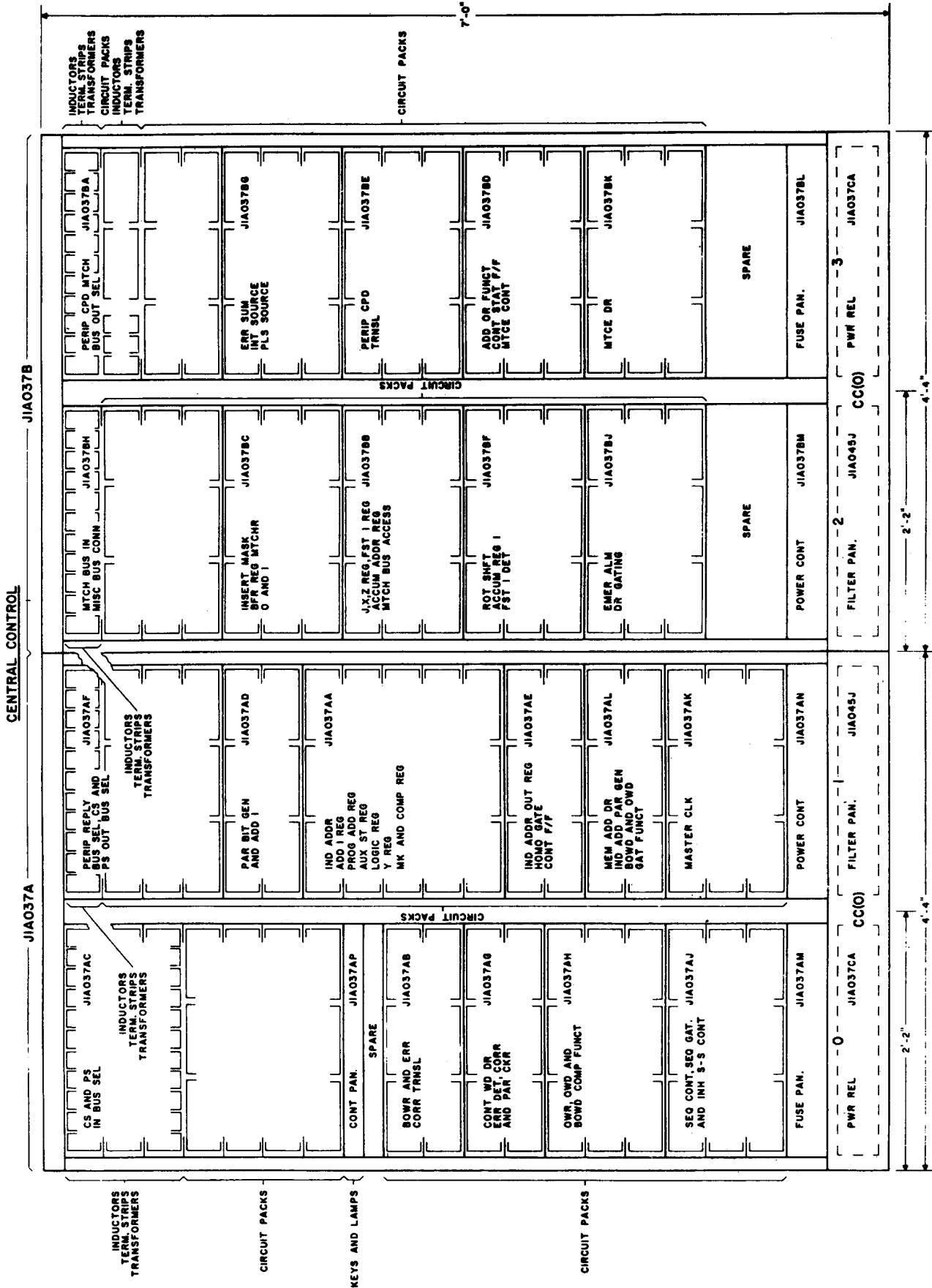Figure 9-44 Central Control - Organization

9.77

Figure 9-45 Central Control Frame

9.6 BUS SYSTEM

Information is exchanged among units over routes of the type shown schematically in Figure 9-46. A group of leads, referred to as a bus, provides a common highway that serves a multiplicity of units. A gating scheme allows the bus to be time-shared by the different units it serves. This arrangement eliminates the need for many individual unit-to-unit interconnections. With very few exceptions, the flow of information on any particular bus lead is always in the same direction.

In a No. 1 ESS without any SP's there are four major bus systems. These connect the two CC's with: (a) PS's, (b) CC CS's, (c) CPD's and (d) PU's.
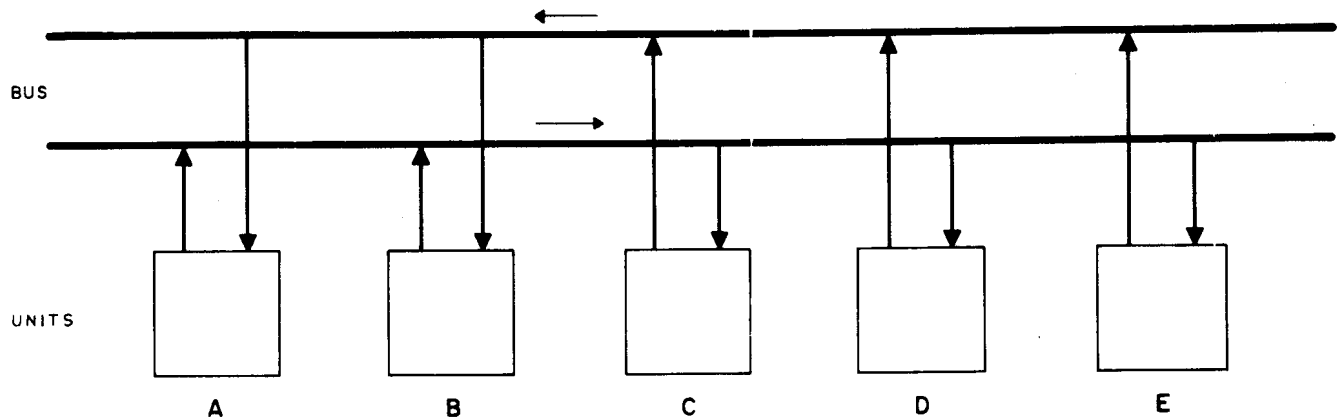
Figure 9-46   Basic Bus Scheme

Two methods are used to select, or enable, the unit that must respond to information transmitted over a bus having access to several other units. The first method is used to enable CS's, PS's and SP's. These units are assigned "names" in the form of unique binary combinations. Simultaneously with the information to be acted upon, a "code" is transmitted over a number of bus leads to all the units on the bus. A unit can receive the rest of the information only if it has a name that matches the enabling code. The second method of enabling is used for CPD's and PU's. Via a CPD, an enabling pulse is transmitted over a private path to the desired unit.

A. ELECTRICAL FEATURES OF BUSES

Signals are transmitted over the buses by means of 12-volt pulses approximately 0.5 usec wide. These pulses may be applied as often as once every 5.5 usec. Thus, the buses must be able to transmit high-frequency signals; they must also be relatively insensitive to ambient electrical noise.

A balanced-to-ground, twisted pair of 26-gauge wires is provided for each bit in a bus. As an example, Figure 9-47A shows a pair for transmitting an address bit from the CC to the program (or call) stores. To minimize reflections that would cause undesired multiple operations, the pair is terminated at both ends with a 100 ohm nominductive resistor. A center-tapped inductor is bridged across the pair to provide a path to ground for unwanted longitudinal signals. Each pair is transformer-coupled to a number of cable drivers and cable receivers. The driving transformers are bridged across the bus pair, whereas the receiving transformers are connected in series. The transmission time over a pair is 2 usec per 1,000 feet; the loss introduced is 6 db per 1,000 feet. Figure 9-47B is the circuit representation of Figure 9-47A.
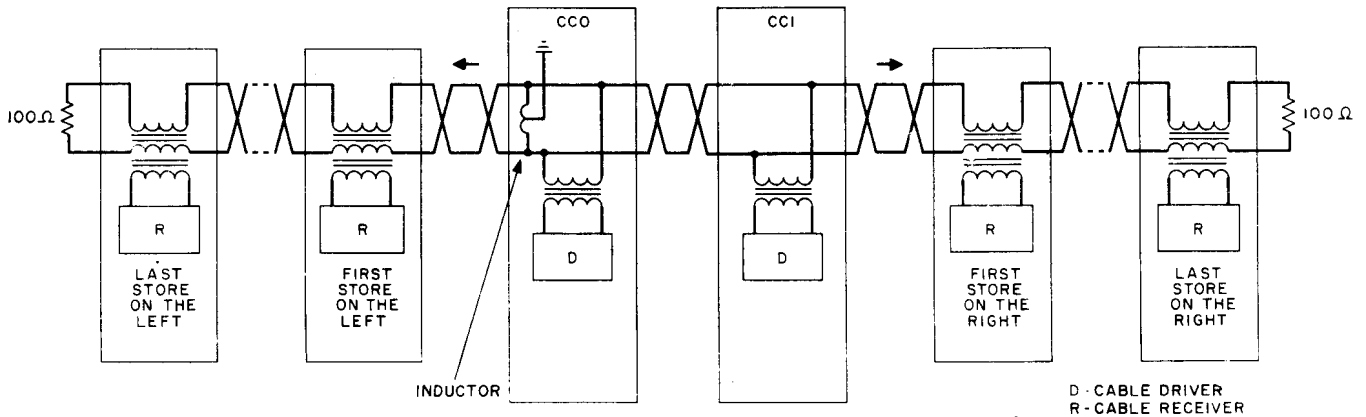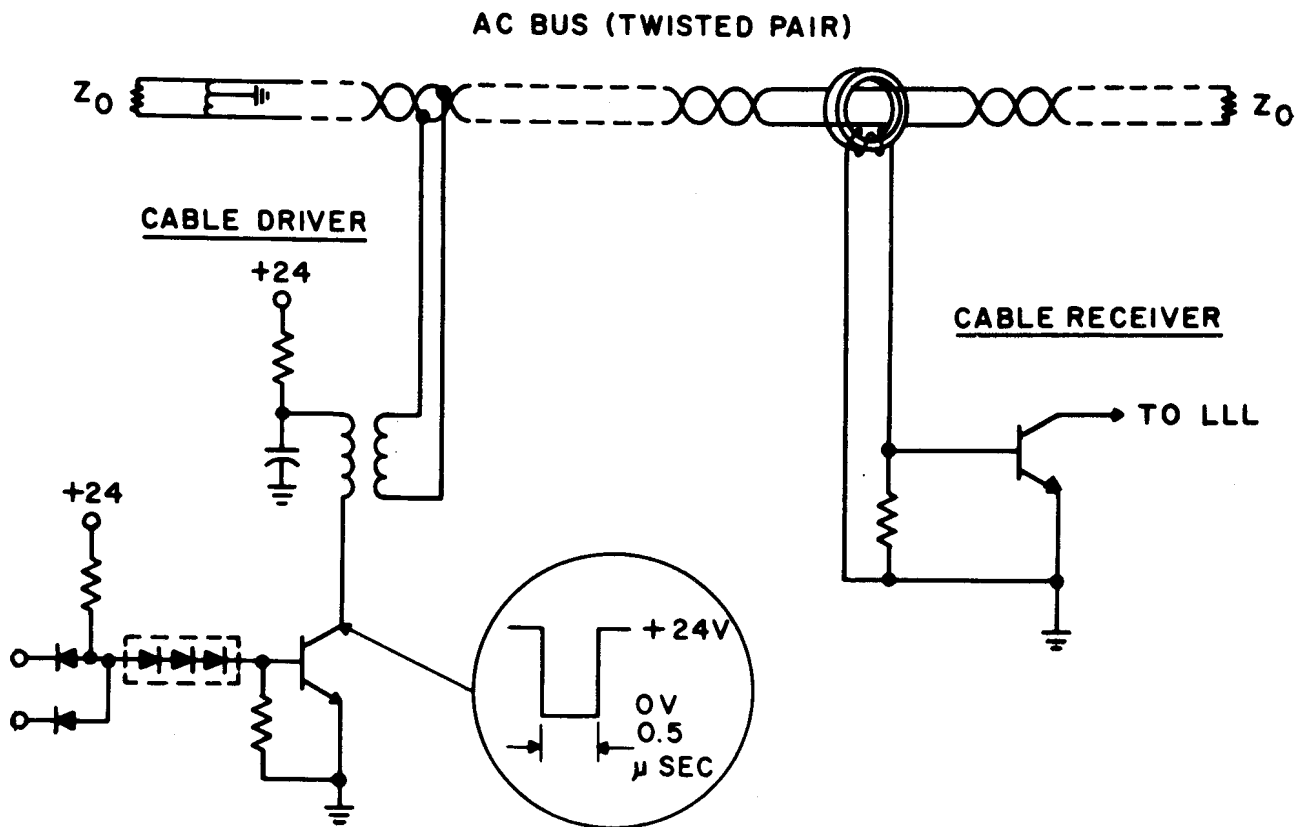

Figure 9-47A Typical Bus Pair

AC BUS (TWISTED PAIR)

Figure 9-47B Typical Bus Pair Schematic

9.7 CENTRAL PULSE DISTRIBUTOR

A. GENERAL

Central pulse distributors (CPD's) provide central control (CC) with fast access to many points throughout the central office.

Upon receiving an order from CC, a CPD selects and pulses one of 768 outputs, as specified by the address from CC. Of the outputs, 512 are unipolar; that is, pulses of only one polarity can be supplied by them. The remaining 256 are bipolar; that is, each can supply a pulse of either polarity (positive or negative). The outputs are connected over private paths to the points controlled.

Unipolar outputs are used mainly to enable peripheral units (PU). Bipolar outputs are used to control flip-flops and other logic circuits in various units. The minimum interval between consecutive requests from CC to a CPD is 11 usec.

The interconnections between CC and the CPD's are shown in Figure 9-48. The CC determines which of the two buses is to be used and transmits a signal to all CPD's over the bus choice lead of that bus.
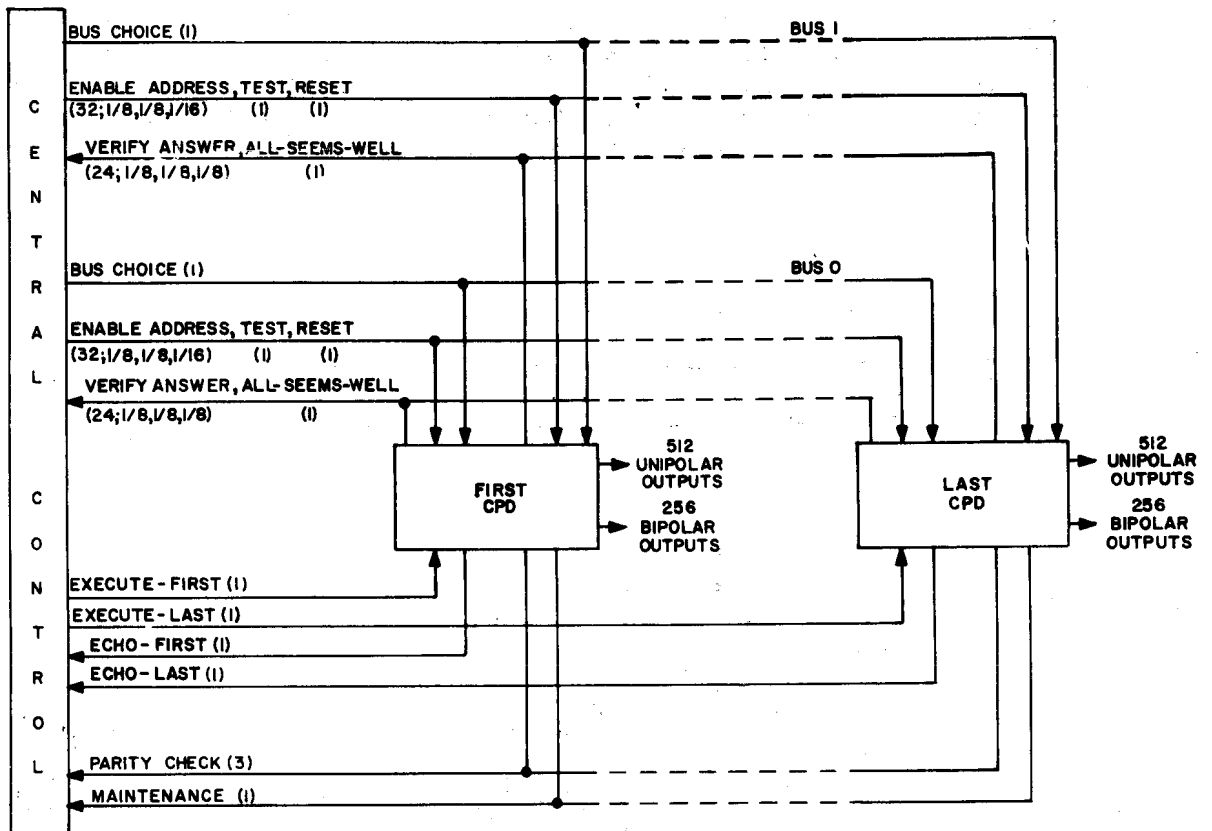

Figure 9-48 Communication Between Central Control
and Central Pulse Distributors

Then, via the chosen bus, CC transmits an address which is received and stored by all CPD's. The address consists of three parts: a 1-out-of-8 X code, a 1-out-of-8 Y code, and a 1-out-of-16 Z code. This information specifies

one of the 512 unipolar outputs or one of the 256 bipolar
outputs together with the polarity of the pulse to be sup-
plied by it. Finally, CC transmits an execute signal over
a private path to the CPD that is to execute the order.

Figure 9-49 shows the basic organization of a CPD.
The predecoder, decoder, and matrix are three consecutive
stages of selection. In each stage, an output is activated
when one of the horizontal inputs and one of the vertical
inputs are activated in coincidence.

When a PU controller receives an enable pulse from a
unipolar CPD output, it returns a verfiy signal over the
same path. The matrix steers this verify signal to the
encoder which translates it into a verify answer in a
1-out-of-8, 1-out-of-8, and 1-out-of-8 code. The verify
answer is sent to CC where it is compared with the enable
address initially transmitted.

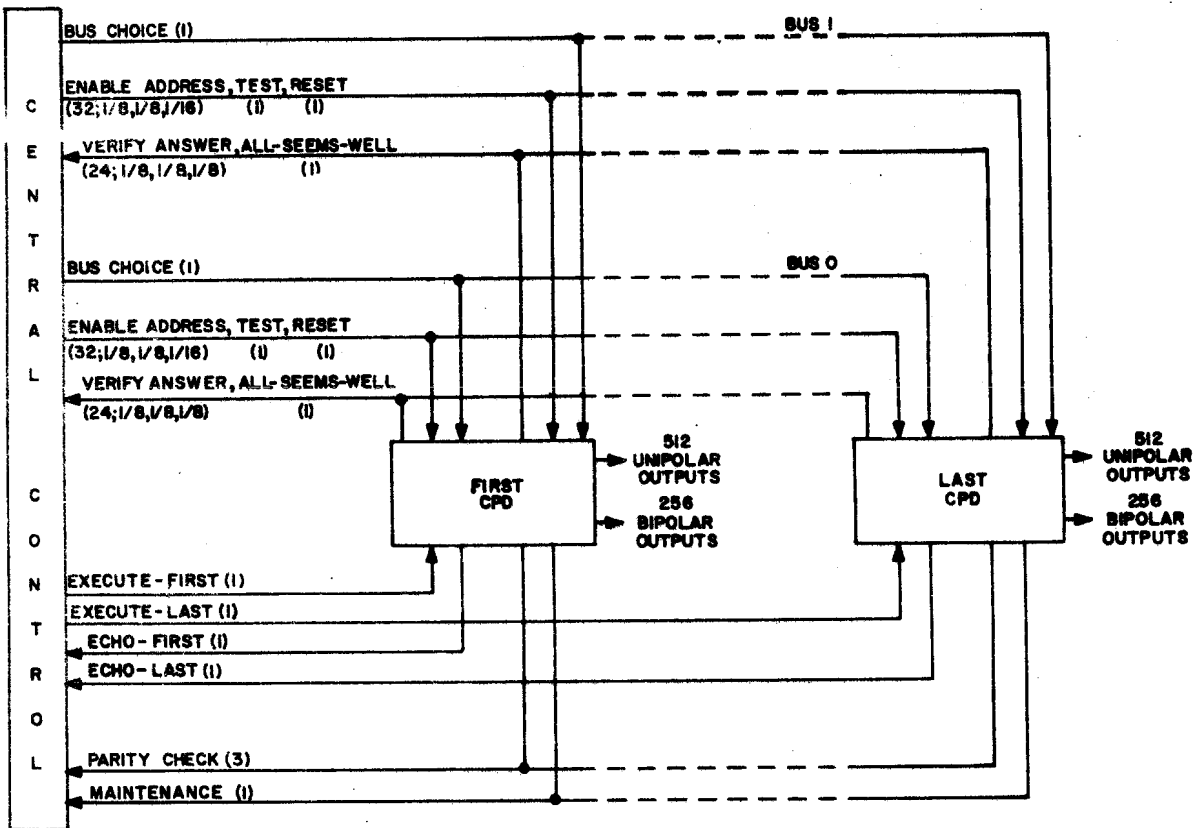Figure 9-49   Basic Central Pulse Distributor

B. METHOD OF OPERATION

1. General

The CPD requires three communications in rapid succession from CC: The bus choice, the address, and the execute signal (see Figure 9-50).
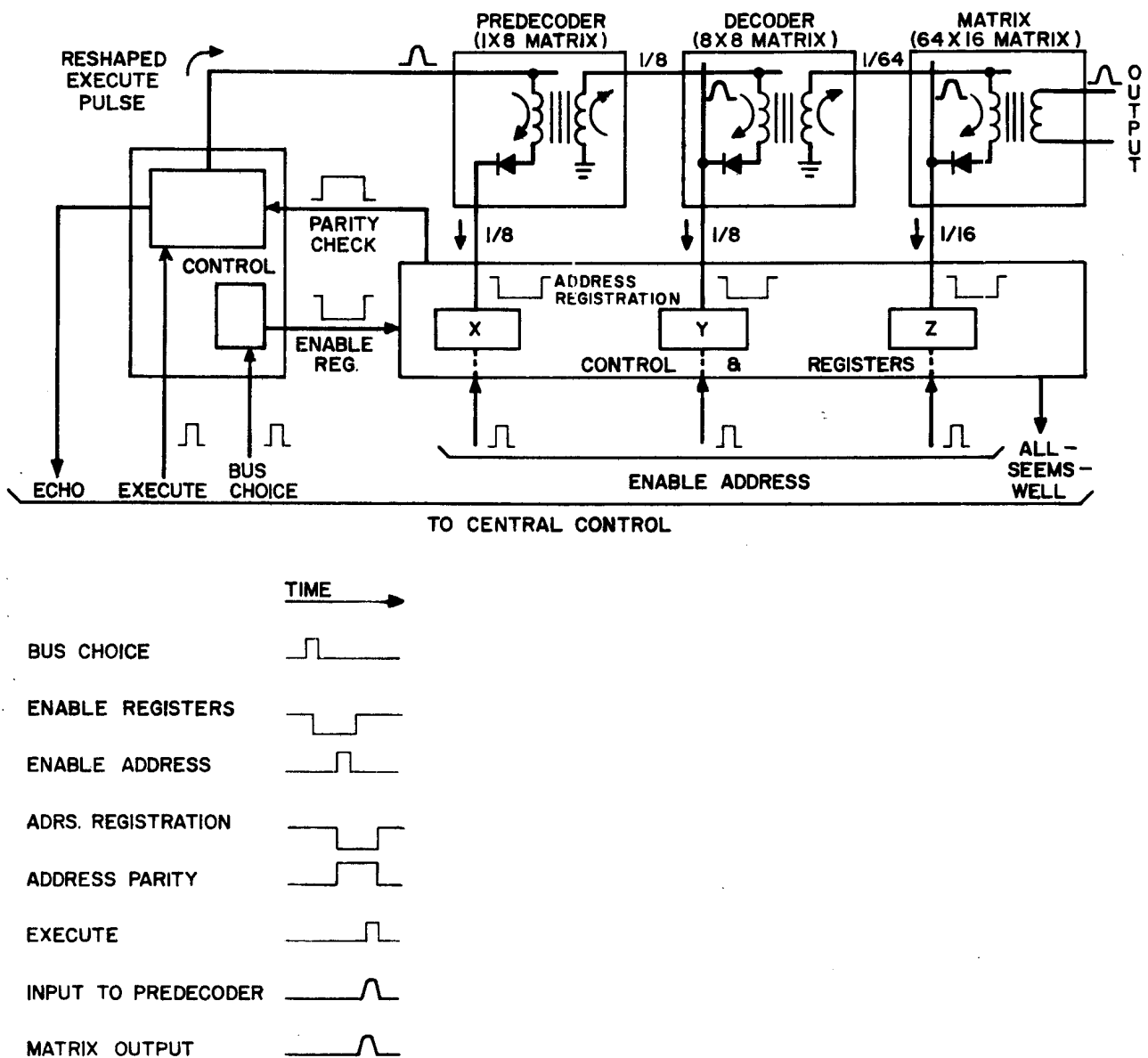
Figure 9-50   Communications From Central Control

When the 0.5 usec bus choice pulse is received, it generates a 2 usec pulse that enables three sets of registers (X, Y and Z) to receive the address pulses from the bus designated by the bus choice. The bus choice pulse also generates a 4 usec pulse, during which both verify answer buses are inhibited and at the end of which trouble detecting circuitry is returned to normal.

When the address pulses arrive and are registered, the control circuitry makes a parity check to determine whether a legitimate address has been received. The address is registered long enough to enable the execute pulse to activate the corresponding matrix output.

When the execute pulse is received, it is reshaped and applied to the predecoder input if the address parity check has been successful. The reshaped execute pulse is transmitted from the decoder input to the matrix output via three transformer-coupled stages shown in Figure 9-51. In addition, the 0.5 usec execute pulse causes the following circuit operations:

(a) An echo pulse is returned to CC which uses it to verify that the execute pulse has been received by the proper CPD.

(b) If the address parity is correct and the output pulse has an appropriate value of current, an all-seems-well (ASW-CPD) pulse is transmitted to CC.

(c) The results of the X, Y and Z parity checks are transmitted to CC.

C. DUPLICATION AND MAINTENANCE

CPD's are provided in pairs up to eight. The units in each pair operate independently of one another. One CPD of each pair is even-numbered; the other, odd-numbered.

For the CPD output signals used to enable PU's, redundancy is provided by having four paths by which CC is given access to each PU. Which of the four paths is used is determined by route information stored in the call store (CS).

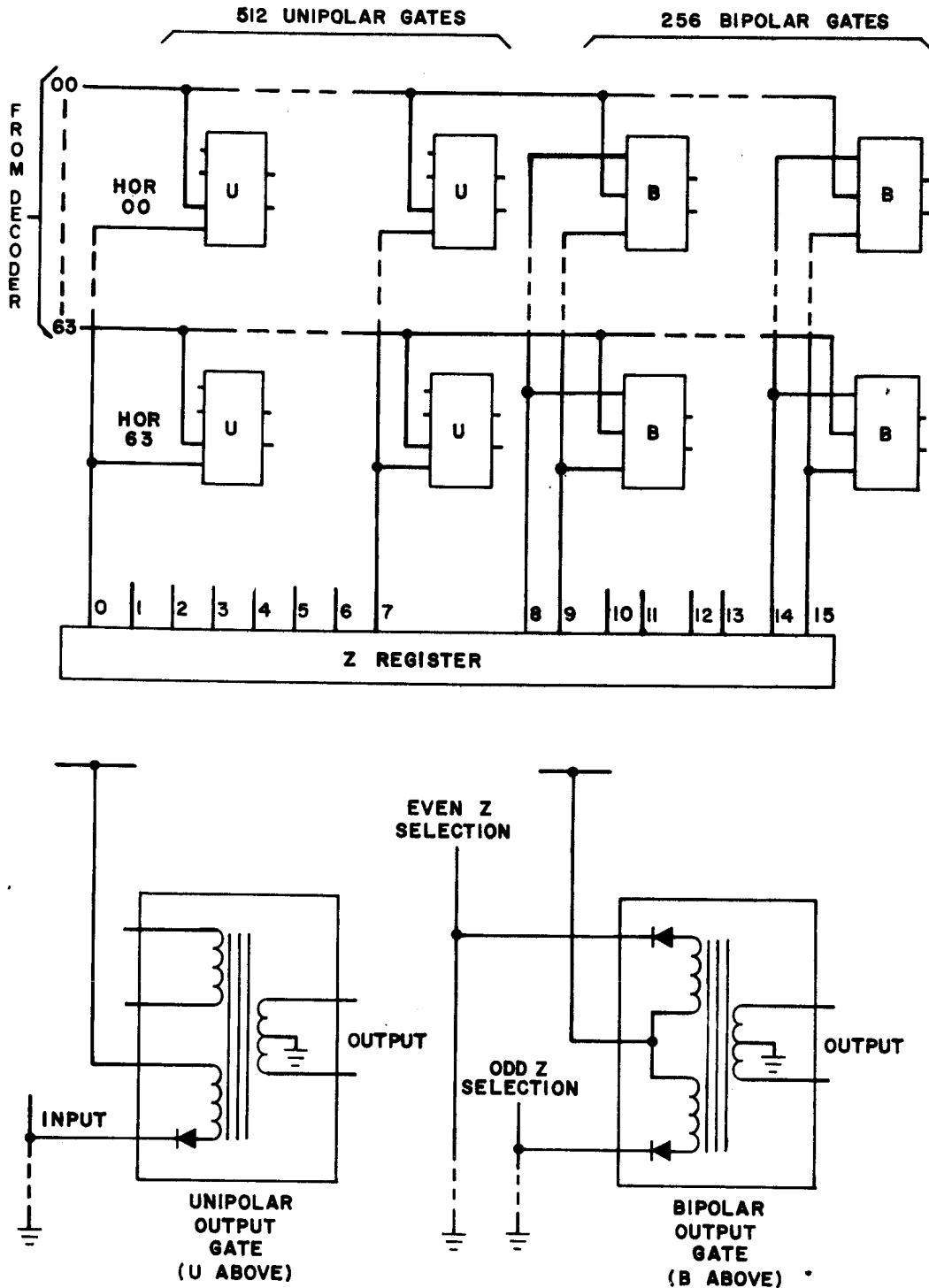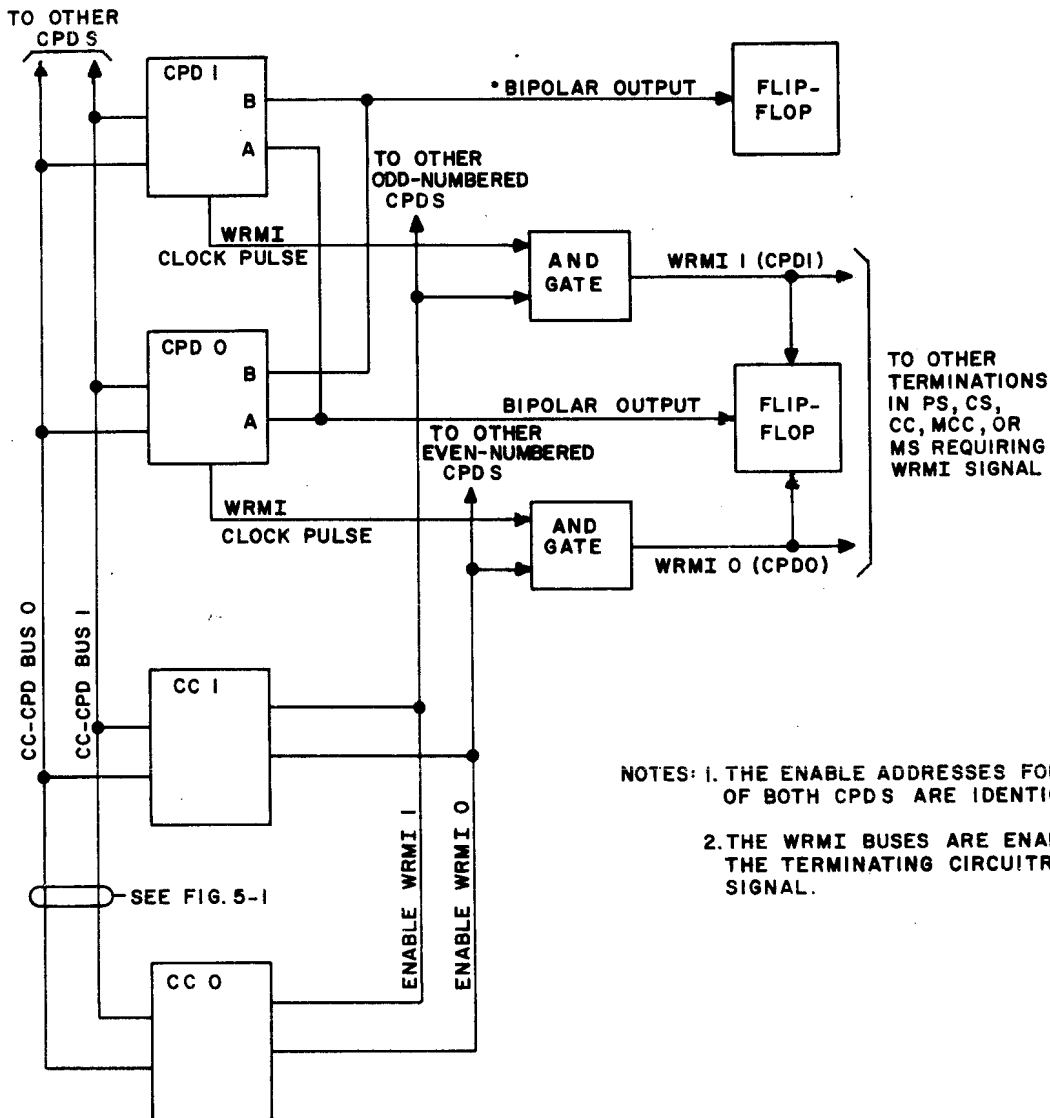Figure 9-51   Transmission of Execute Pulse Through the Matrix

As shown in Figure 9-52, full duplication is provided for the bipolar CPD outputs which are used to control flip-flops and logic circuitry throughout the central office. Two CPD outputs having identical enable addresses in the two CPD's of a pair are multipled and then wired to the terminating circuitry.

Figure 9-52   Duplication of Bipolar Outputs

Some bipolar outputs are used to control flip-flops that can critically affect the operation of the system. For these outputs, a safeguard is provided to prevent a noise signal on a CPD output from causing an undesired change of state in the associated flip-flop. A pulse on a protected CPD output is not effective unless a we-really-mean-it (WRMI) signal is simultaneously present on a common lead.

Whenever a CPD receives an execute pulse, if the parity check of the address was successful, it generates a WRMI clock pulse (Figure 9-52). CC generates an enable WRMI signal only when required by the nature of the flip-flop to be reached. At the CPD frame where both a WRMI clock pulse and an enable WRMI signal are present, a WRMI pulse is generated and fanned out to all the units that are served by that CPD and require the WRMI signal.

1. Maintenance Modes

> Many detected troubles are treated by denying to CC the use of a particular bus choice or CPD choice. This is done by altering a route record which is kept in a CS. This mode of operation is called marked-in-trouble mode (MITM) with the words "in memory" implied. When a CPD is in this mode, a diagnosis has been or will be made. When the fault is cleared, the route record is updated to permit CC to use the route previously denied.

> Certain matrix troubles produce parity check failures despite the fact that valid enable addresses have been received by the CPD. In this situation, CC orders the other CPD in the pair to pulse a bipolar output which activates circuitry within the faulty CPD. This circuitry then causes the CPD to ignore any parity check failures. This mode of operation is called parity-inhibited mode (PIM). When a CPD is in this mode, a diagnosis has been or will be made. CC can still make use of the CPD. To return the CPD to the normal mode of operation, CC orders the other CPD in the pair to produce a pulse that deactivates the circuitry formerly activated.

> Should a CPD start generating output signals without orders from CC, power to generate these outputs must be quickly removed. In this situation, CC orders the other CPD in the pair to pulse a

bipolar output which is connected to circuitry within the faulty CPD. This circuitry then releases the normally operated power distributing relay. This mode of operation is called the quarantine mode (QM). In this mode, a diagnosis has been or will be made, and the CPD is not available for system use. To return the CPD to normal mode of operation, CC uses either of two methods to reoperate the power distributing relay:

(a) Transmitting a signal on the restore (RO or R1) lead that is common to all CPD's.

(b) Ordering the other CPD in the pair to pulse an appropriate bipolar output.

D. POWER

Each pair of CPD's is supplied with +24 volts over two power buses. The power for the even-numbered CPD is fed by the +24-0 bus; for the odd-numbered CPD, by the +24-1 bus. Power can be manually removed at the CPD frame.

E. EQUIPMENT ARRANGEMENTS

A CPD is mounted on a single frame. Communication bus apparatus occupies five 4-inch mounting areas at the top of the frame. Presently CPD pairs occupy a double framework.

9.8 SCANNERS

A. GENERAL

Unlike previous dial central office systems, the No. 1 ESS has no individual line or supervisory relays to indicate call originations or terminations on lines and trunks. In addition to supervising on-hook and off-hook conditions, the system must monitor dial pulses and observe the electrical state of various points within the central office for administrative, diagnostic and other purposes.

Input information of this nature is furnished to the No. 1 ESS by the operation of scanners which sample or scan lines, trunks and various other circuits at discrete intervals of time as directed by the system.

Each point to be scanned is connected to a current sensing device called a ferrod sensor. Ferrods are organized in groups of 16 within arrays or matrices of 16 by 16 (256), 16 by 32 (512), or 16 by 64 (1,024) scanpoints. A scanner

can select and interrogate any group of 16 ferrods as specified by information received from the central control (CC) or signal processor (SP). To simplify the description, only CC will be mentioned as the unit controlling the scanners. It is to be understood, however, that an SP can perform this function in larger offices equipped with SP's.

Depending upon the state of the scanned circuit, each of the 16 ferrods interrogated results in a pulse or no pulse output which is referred to as a 1 or 0 readout, respectively. Thus, in response to signals from CC, a scanner produces a 16-bit output word that is transmitted to CC where it is interpreted.

The main inputs and outputs for a scanner are shown in Figure 9-53. When a scanner operation is needed, CC sends to the central pulse distributor (CPD) information that identifies the particular scanner to be activated. The CPD accordingly sends an enable signal to that scanner on a private pair of leads. The scanner sends back a verification signal on the same pair of leads. A scanner address is transmitted by CC on the common peripheral unit address bus 0.5 usec after the enable pulse. Only the scanner that has received the enable pulse can respond to the address which specified a particular group of 16 ferrods to be interrogated. The resulting readout, or scanner answer, is sent back to CC. Under normal conditions, an all-seems-well scanner (ASW-S) signal is also transmitted by the interrogated scanner. The all-seems-well signal indicates that, as intended, one and only one group of ferrods has been interrogated.

The operate time of a scanner is between 1.8 usec and 2.5 usec, measured from the time an address is received from the bus to the time the readout is applied to the answer bus. A scanner may be addressed at a maximum rate of once every 11 usec.

Five types of scanners, shown in Table 9-2, are used in No. 1 ESS. The scanners differ mainly in the number and type of ferrods used. The control of all scanners is essentially identical. The total number of scanpoints required in a central office is about 1.5 times the number of lines in the office.

TABLE 9-2

TYPE OF SCANNERS

Type of Scanner	Location	Function	Matrix Size	Ferrod Sensor Assembly
Line	Line Switch Frame (4 to 1) (Basic & Supplementary)	Detection of call origination by customer (off-hook)	16 by 64 (1,024)	
	*Line Switch Frame (2 to 1) (odd or even numbered)		16 by 32 (512)	1B
Junctor	Junctor Frame	Supervision of intra-office calls	16 by 32 (512)	1C
Universal Trunk	Universal Trunk Frame	Supervision of inter-office calls	16 by 32 (512)	1C and 1D
		Supervision of miscellaneous trunk and service circuits		
Master	Master Scanner Frame	Monitoring of dial pulses. Monitoring of points within the electronic central office for various purposes such as routine tests, trouble diagnosis, administration, and other requirements.	16 by 64 (1,024)	1D

*For each pair of odd and even numbered frames, the control for both 512-point matrices are located on the even numbered frame.
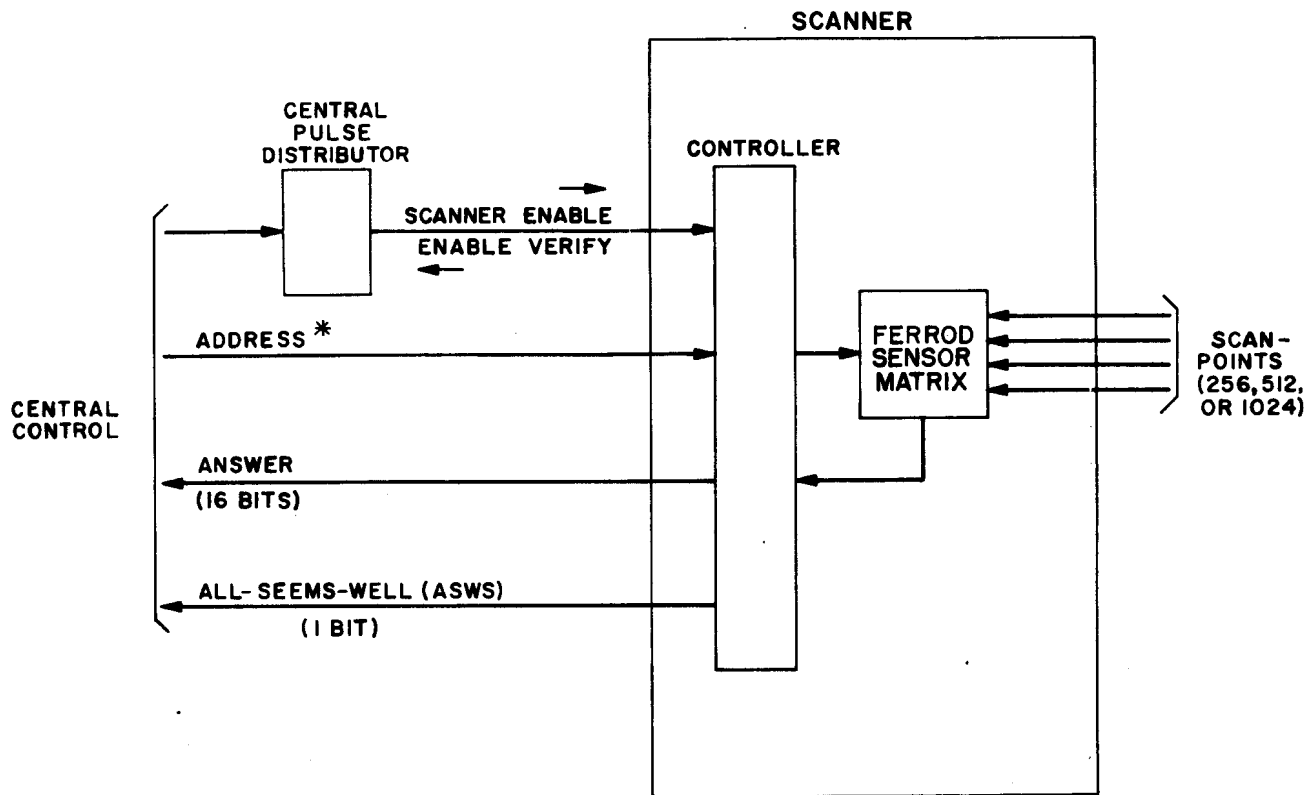
* 8,12, OR 16 BITS, DEPENDING ON SIZE OF SCANNER

Figure 9-53 Main Inputs and Outputs for Scanners

B. THE FERROD SENSOR

It is necessary to understand the operation of the
ferrod sensor before the scanners can be described further.
The ferrod is essentially a transformer in which the magnetic
coupling between the interrogate and readout windings is
determined by the current in the control windings. This
current, in turn, reflects the state of the circuit to be
sensed, such as the on-hook or off-hook condition of a line.
A typical ferrod arrangement is shown in Figure 9-54. Two
control windings are wound around a rod of ferrite material.
In addition, a single-turn interrogate winding and a single-
turn readout winding are threaded through two holes in the
center of the ferrite rod. The control windings are con-
nected in series with the circuit to be sensed or supervised,
for instance, a customer line.

TO CUSTOMER LINE, JUNCTOR, TRUNK,
OR OTHER CIRCUIT TO BE SENSED OR SUPERVISED

FERRITE ROD

CONTROL WINDING

-48

INTERROGATE WINDING

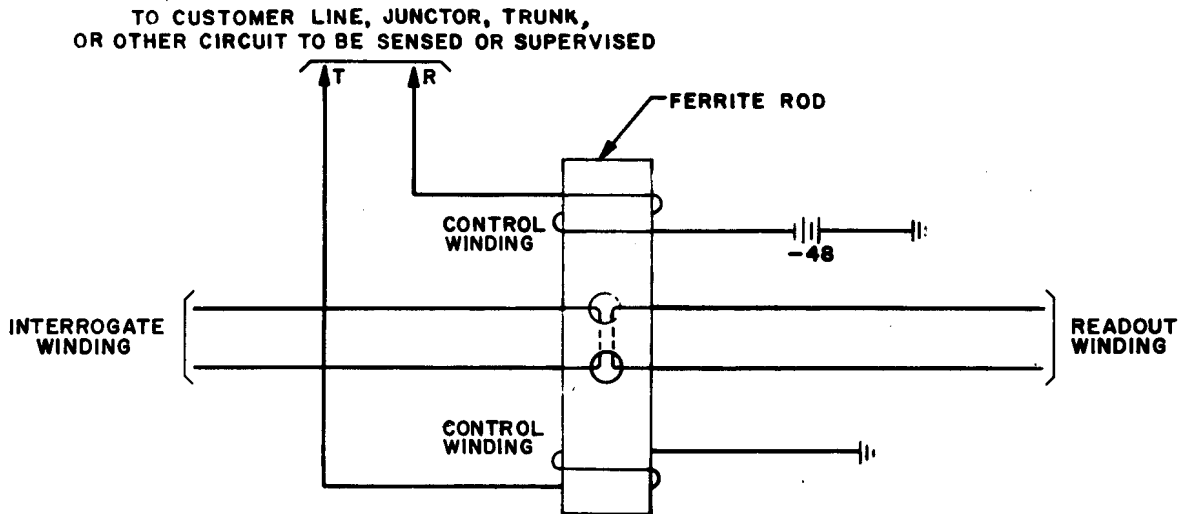READOUT WINDING

CONTROL WINDING

Figure 9-54   Typical Ferrod Arrangement

When a pulse is applied to the interrogate winding while the control windings are energized, practically no signal is induced in the readout winding and the readout is said to be 0. This is because the magnetic flux caused by the current in the multiturn control windings saturates the ferrite rod; consequently, the magnetic coupling between the single-turn interrogate and readout windings is greatly reduced. On the other hand, when a pulse is applied to the interrogate winding while the control windings are not energized, a change of flux is induced in the area immediately surrounding the two holes in the ferrite rod. A pulse is induced in the readout winding and the readout is said to be 1. Thus, when an interrogate pulse is applied, the presence or absence of a readout pulse indicates whether the circuit being observed is open or closed, respectively. If the circuit being observed is, for instance, a customer line, the on-hook (open) condition results in a 1, the off-hook (closed) condition in a 0.

C. TYPES OF INDIVIDUAL FERRODS

There are four basic types of individual ferrod units which are combined to make up three types of ferrod assemblies.

1. Type 1 - Loop-Start Line Ferrod

The type 1 ferrods are used in line scanners to recognize the initial request for service from ordinary customer lines which operate on a loop-start basis. In loop-start operation, a call is originated by closing the tip and ring loop through the customer telephone set. A contact protection network is connected across the control windings of the ferrod to protect the ferreed cutoff contacts. These contacts are used to disconnect the line ferrod after the central office equipment has responded to the request for service. (This is similar to the cutoff of the line relay in other telephone systems when the operator answers or when the dial system starts to process the call.)

The loop/start circuit will work satisfactorily over the expected range of No. 1 ESS battery voltages (43-52 volts) with a maximum external loop, including subset, of 2,800 ohms. A minimum tip-to-ring leakage resistance of 10,000 ohms is permissible.

2. Type 2 - Combination Loop-Start or Ground-Start Line Ferrod

Type 2 ferrods are also used in line scanners to recognize initial requests for service. By means of optional wiring, the type 2 ferrod can be adapted to loop-start operation of ordinary customer lines or to ground-start operation of coin and PBX lines. (In ground-start operation, a call is originated by grounding one side of the line at the coin station or PBX.)

The ground-start circuit will work satisfactorily over the expected range of battery voltages with a ground potential variation of ± volts, if the maximum external resistance is less than 1,800 ohms. A minimum leakage resistance of 10,000 ohms is permissible. An auxiliary line circuit can be used for either loop-start or ground-start operation, in cases where there is excessive ground potential, longitudinal current, or leakage.

3. Type 3 - Junctor Ferrod

The type 3 junctor ferrods are used in junctor scanners to supervise either side of line-to-line connections. Junctor ferrods are also used in trunk scanners to supervise the local customer side of line-to-trunk and trunk-to-line connections. The distant office side of interoffice connections is supervised by a type 4 ferrod which is a more sensitive device. Typical circuit applications of the type 3 junctor ferrod are shown in Figure 9-55. In these circuits a transmission path is provided between two lines or between a line and a trunk. At the same time, each line or trunk has a separate dc circuit for supervisory purposes and to supply talking battery. These circuit arrangements are similar to the methods used to split supervision in other dial central office systems and operator cord circuits.

The junctor ferrod can supervise a maximum external loop of 1,900 ohms, measured at the tip and ring terminals of the junctor circuit, over the expected range of central office battery voltages. A minimum leakage resistance of 10,000 ohms is permissible.

4. Type 4 - Trunk Ferrod

The type 4 ferrods are used in the master scanners to supervise miscellaneous trunk and service circuits and to supervise the distant office side of interoffice connections. They are also used in the master scanner (MS) to monitor various points within the circuitry of the electronic central office units.

The trunk ferrod is the most sensitive used in No. 1 ESS. It can supervise loops up to 10,700 ohms resistance external to the ferrod. Tip-to-ring, or equivalent, leakage resistance of the trunk must be greater than 30,000 ohms.

D. FERROD ARRAYS

The basic apparatus mounting for ferrods contains 128 cells arranged in an 8 by 16 array. Each cell holds one assembly of two ferrods; therefore, each apparatus mounting contains 256 ferrods. The steel box and separators serve as a magnetic and fire shield between ferrod assemblies. A scanner is made up of one, two, or four apparatus mountings to hold a total of 256, 512, or 1,024 ferrods.

JUNCTOR CIRCUIT

NOTE: CTI AND CT2 ARE CUT-THROUGH RELAYS OPERATED BY SIGNAL DISTRIBUTOR
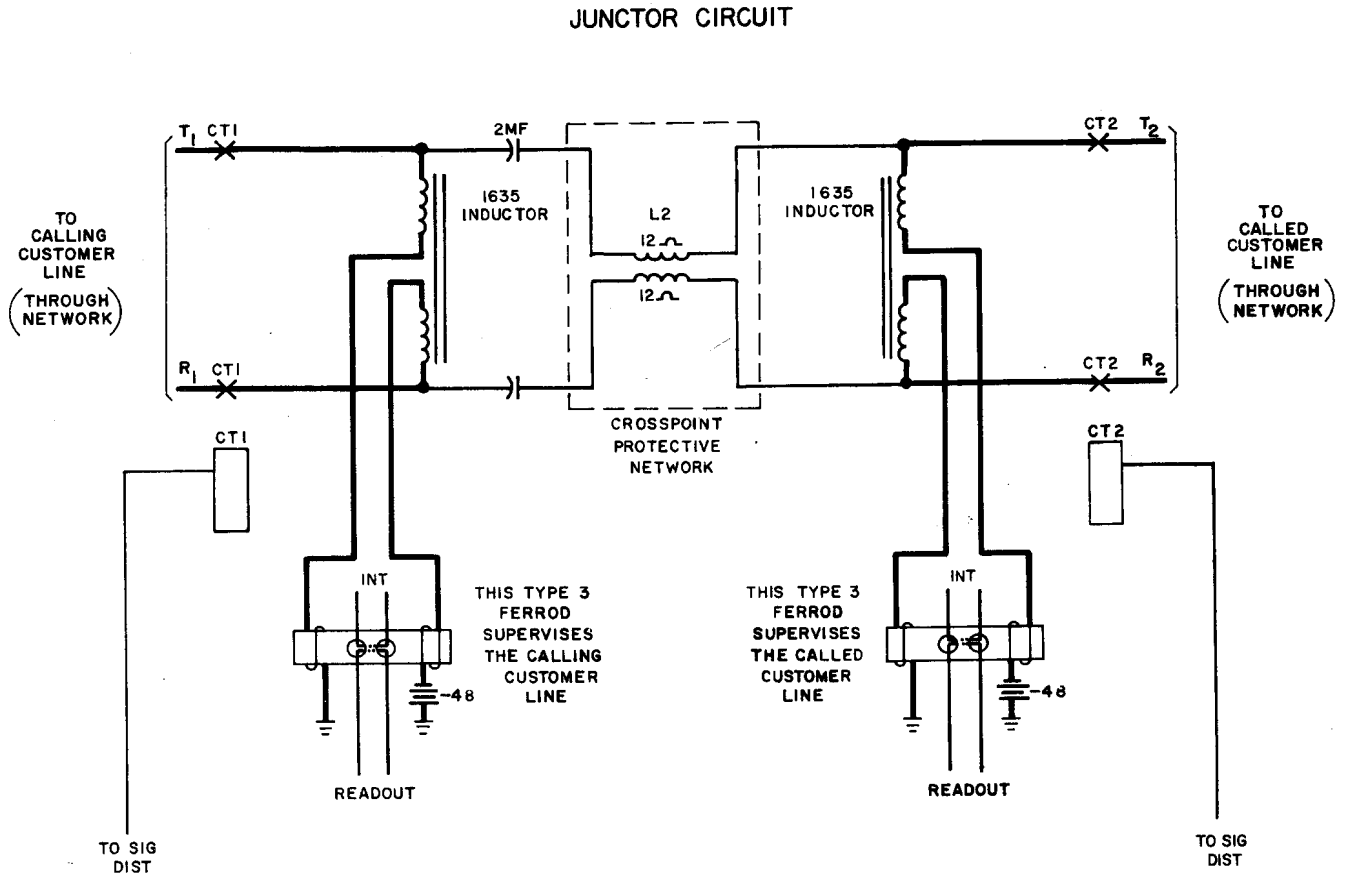
Figure 9-55   Junctor Supervision Using Type 3 Ferrods

E. METHOD OF OPERATION

There are two main sections in each scanner: the current-sensing ferrods, which are wired to the points to be supervised, and a controller. The controller is used by CC to gain access to the interrogate windings of the ferrods and to detect the readout from a selected group of 16 ferrods.

The basic operation of scanners based on a 512-point unit is illustrated by the simplified diagram in Figure 9-56. Duplication and other considerations will not be covered.

9.97

Figure 9-56   Scheme for Coincident Current Selection of
One Group of Sixteen Scanpoints

All scanners on the same bus system are addressed simultaneously but only one scanner receives an enable signal. The size of the address varies with the size of the scanner. In a 512-point scanner, the address consists of 12 bits in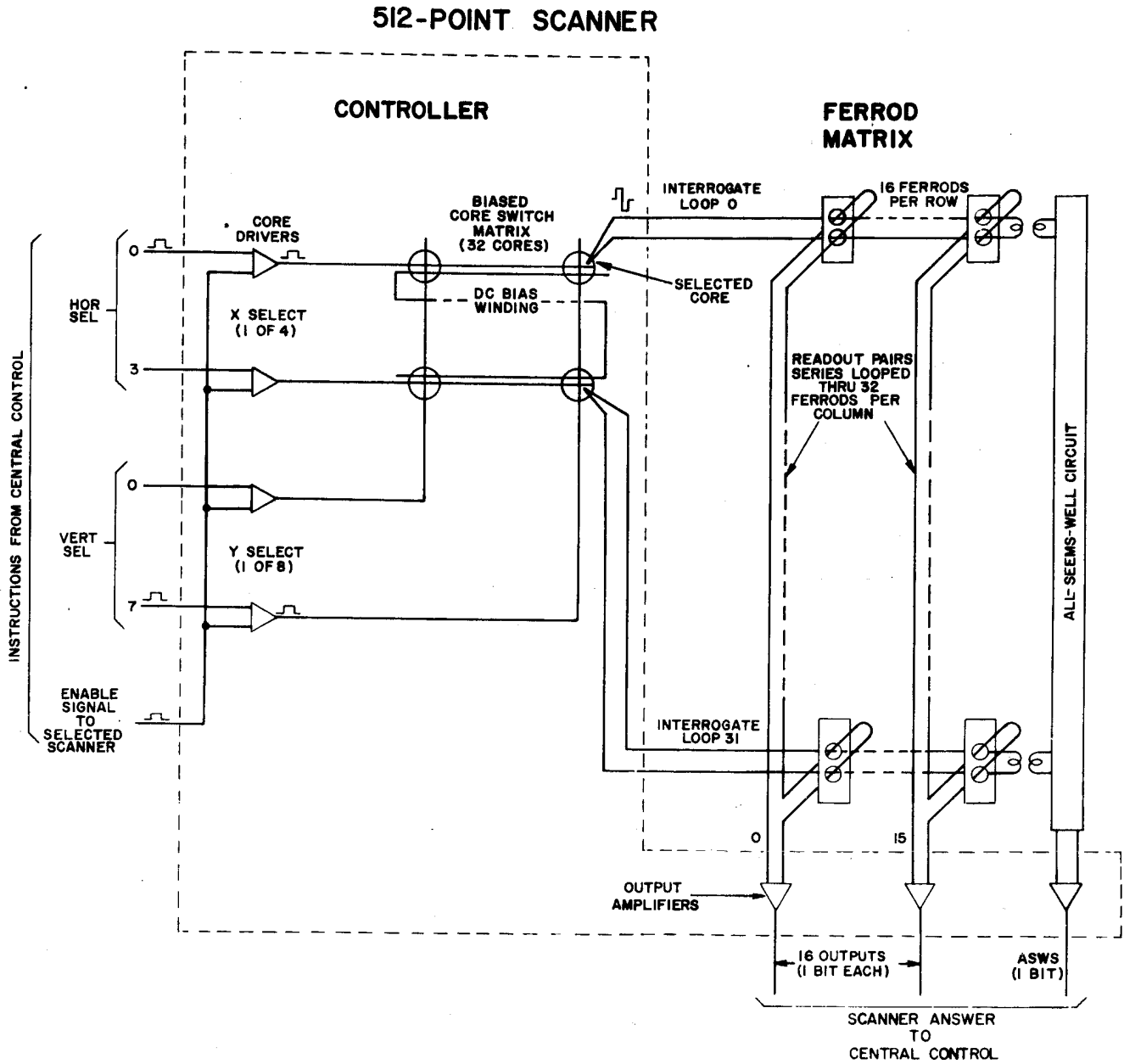 a 1-out-of-4 (1/4) and a 1-out-of-8 (1/8) code. The address for a 256-point scanner has 8 bits (1/4 and 1/4 code) and for a 1,024-point scanner, it has 16 bits (1/8 and 1/8 code). In the example of Figure 9-56 for a 512-point scanner (1/4 and 1/8 code), a pulse is present on only one of the upper four and one of the lower eight leads on the left. Only the two core drivers, whose inputs are both 1, generate pulse outputs which select a particular row and column in the biased core matrix. Only the magnetic core at the intersection of the selected row and column receives a drive in both the X and Y leads. This combined drive is sufficient to overcome the dc bias and switch the core. When the core switches, a pulse is induced in the associated interrogate loop. A similar interrogate loop is associated with each of the 32 cores of the matrix. Only one interrogate loop is pulsed for each address.

Each interrogate loop passes through 16 ferrods in series; therefore, pulsing one interrogate loop results in the readout of 16 bits. As previously explained, the presence or absence of current in the control windings of each ferrod determines whether the corresponding readout bit is 0 or 1, respectively. In this manner, 16 scanpoints are observed at the same time.

F. MODES OF OPERATION

Three different control modes can be established in a scanner under program control:

(1) Normal: In this mode, either controller can be used to interrogate the ferrods. When one controller is operating the ferrod matrix, the other controller is considered to be in ready-standby.

(2) Marked-In-Trouble: In this mode, one controller is recorded in the temporary memory as being in trouble and is not to be used to interrogate the ferrod matrix for normal call actions.

(3) Quarantine: In this mode, power is removed from the controller by the program. Interlocks are provided to prevent both controllers from being quarantined simultaneously.

9.9 SIGNAL DISTRIBUTOR

A. GENERAL

Signal distributors (SD) are provided in trunk frames and junctor frames to give central control (CC) the necessary access to relays in trunk and junctor circuits. Thus, they are the buffers between the high-speed CC and the low-speed relays.

The basic SD is composed of a controller and a relay contact tree as shown in Figure 9-57.

Information from CC, called the address, is accepted and stored by the controller. Through the relay contact tree, the controller closes a unique metallic path to the specified relay winding and applies to it an appropriate signal to operate or release. The controller senses the operation or release of the selected relay and then returns itself and the relay contact tree to normal.

The controller is unavailable or busy to CC during the 25-msec interval between the storing of the address and the return to normal.

B. APPARATUS ELEMENTS - MAGNETICALLY LATCHING RELAY

Each output of the SD is connected to a magnetically latching wirespring relay. Two such relays are combined on one assembly.

The main characteristic of these relays is the remanent core material which retains enough residual magnetism to hold a relay operated after the operating current is removed. The relay releases when the residual magnetism is reduced by a current pulse in the direction opposite to that of the operating current. This characteristic makes possible the use of a single lead for operating and releasing a relay.

C. METHOD OF OPERATION

The basic SD, shown in Figure 9-57, provides 384 output terminals. Two of these basic units make up an SD as shown in Figure 9-58. In the normal mode of operation, known as the split mode, the two basic units operate independently.
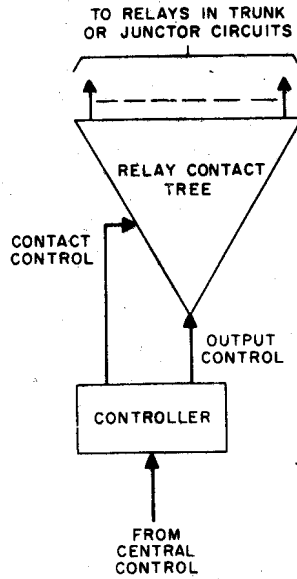
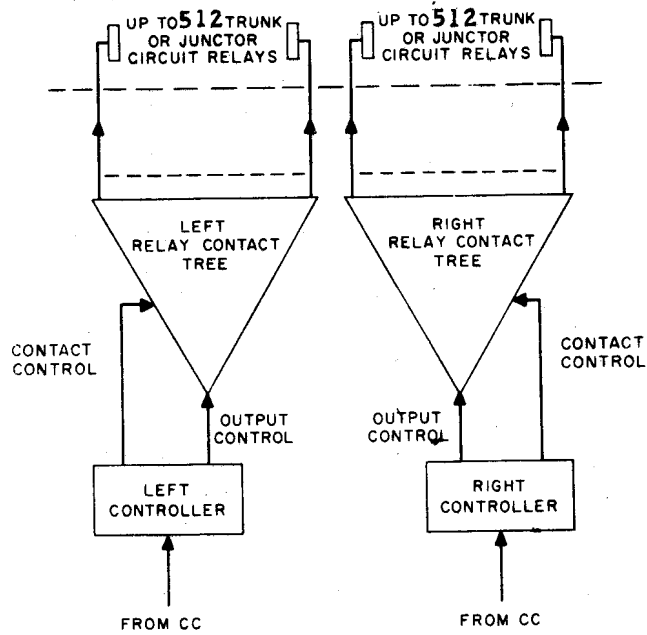Figure 9-57   Basic Signal Distributor, Block Diagram

Figure 9-58   Signal Distributor, Block Diagram
              Split Mode of Operation

The CC orders the central pulse distributor (CPD) to set a flip-flop in the enable-verify circuitry of the controller (Figure 9-59). This flip-flop, when set, changes the status of the controller from idle to busy and causes the generation of two pulses: one is sent back to the CPD for verification, the other enables the buffer registers to accept the address from the peripheral address bus.

The number of flip-flops in each buffer register is indicated by the numeral within the register. Thus, there are eight flip-flops in the A register, eight in the B register, and so on. The address sets only one flip-flop in each register. Each set flip-flop operates an associated mercury contact relay. For registers A, B and D, each operated mercury contact relay operates, in turn, a multi-contact wirespring relay.

As shown in Figure 9-60, a path is closed from either +24 or -48 volts to the selected magnetically latching relay. The -48 volt supply is used to operate the relay; the +24 volt supply to release it. The operation or release of the relay momentarily disconnects a resistance in parallel with the winding; this causes a change in current which is sensed by detecting circuitry in the controller. Figure 9-59 shows that the detection of this current change causes the resetting of all flip-flops in the controller. With these flip-flops reset, the controller status indication is immediately changed from busy to idle; the mercury contact relays and the wirespring relays are released.

D. DUPLICATION

As previously shown, the controlling circuitry of the SD is duplicated but not in the sense that one controller operates the whole SD while the other stands by ready to take over. Normally, one controller offers access to one half of the output terminals while the other controller offers access to the other half.

In each controller, all the flip-flops of the buffer registers are equipped to accept an address from either of the duplicated buses from CC (Figure 9-61). Each controller has two enable-verify circuits with enable flip-flops. The bus from which the address is to be taken depends upon which of the enable flip-flops is set by the CPD. If enable flip-flop 00 or 10 is set, the address is taken from address bus 0; if flip-flop 01 or 11 is set, from address bus 1.
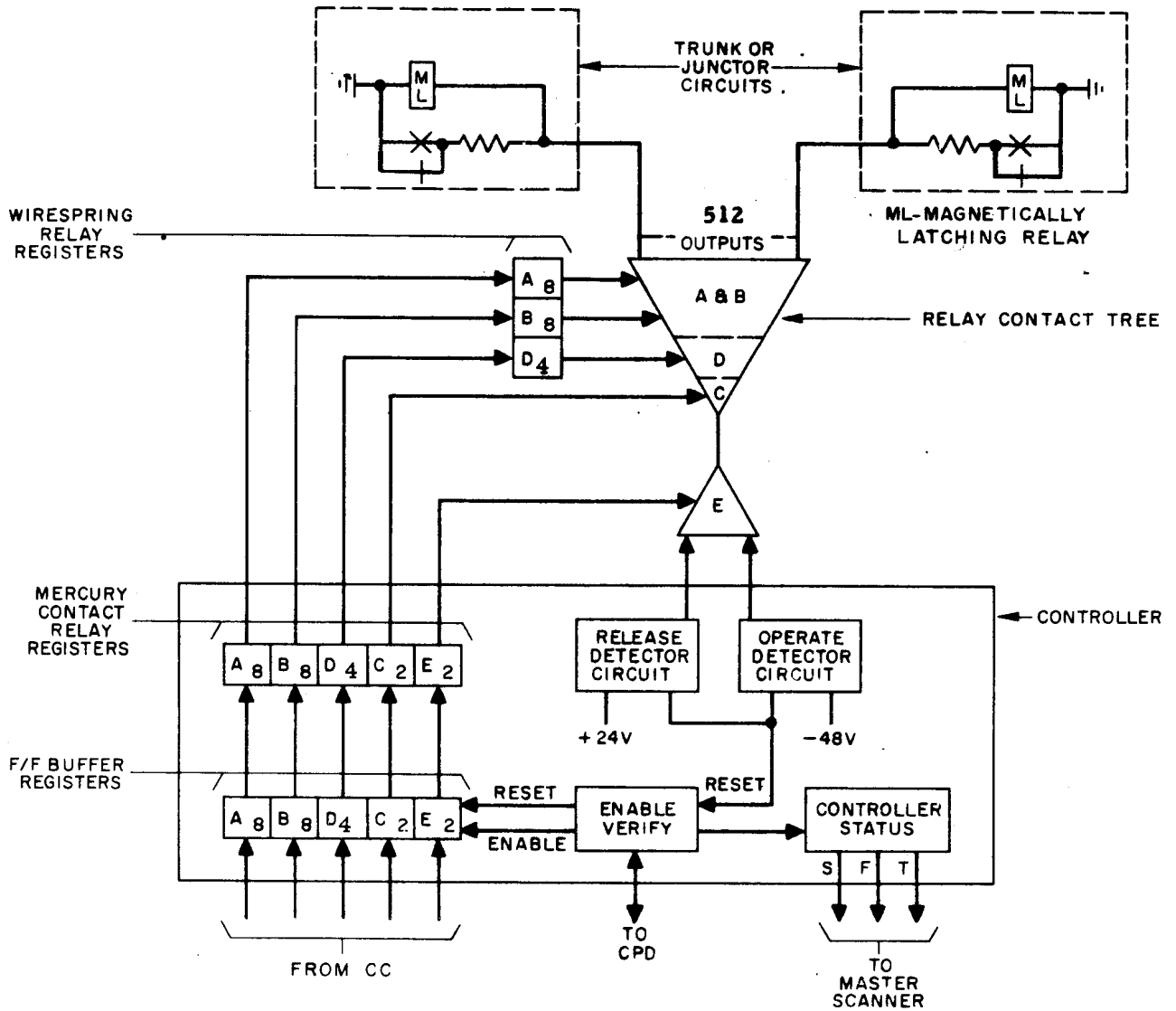
Figure 9-59   Basic Signal Distributor

E. RESET OF CONTROLLER FLIP-FLOPS BY CENTRAL CONTROL

When the selected magnetically latching relay operates
or releases as a result of an order, the controller detector
circuit resets all flip-flops, including the enable flip-
flop. The CC periodically checks each controller's busy-idle
status which is indicated by the state of the enable flip-
flop. If a controller is found to have been busy for longer
than the normal 25 msec, CC can reset, via the bus, all flip-
flops in that controller.

9.103
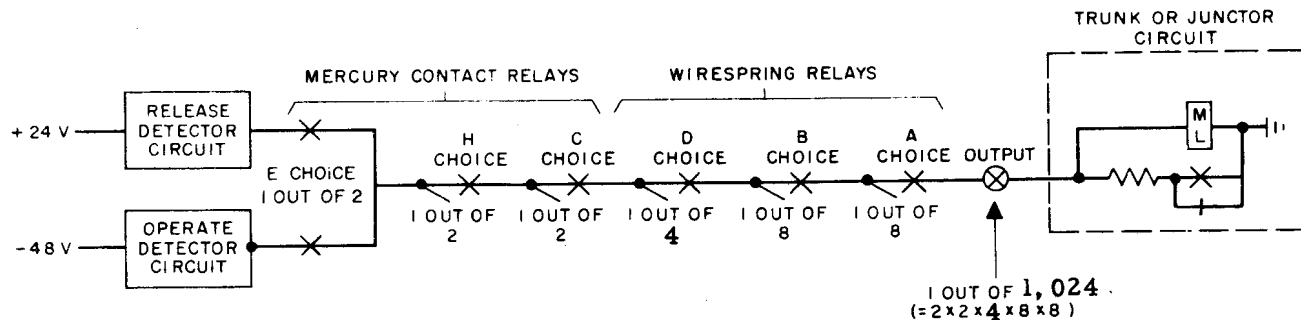
Figure 9-60   Complete Selection Path to Operate or
Release a Magnetically Latching Relay
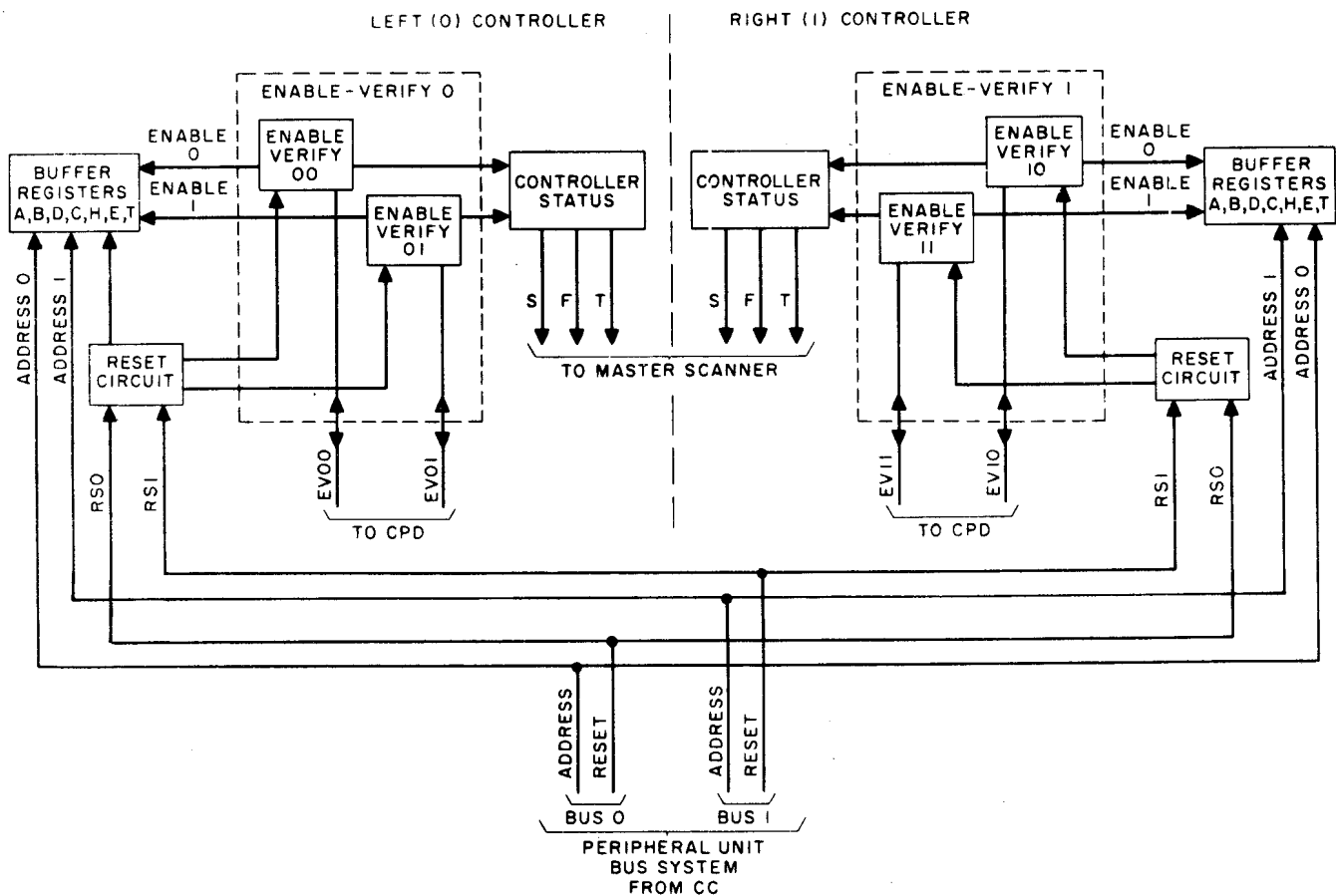
Figure 9-61   Bus Duplication and Reset by Central Control

9.104

Note in Figure 9-61 that each bus from CC has one reset lead. Lead RS-0 is activated to reset the buffer register flip-flops and the 00 and 10 enable flip-flops; lead RS-1, to reset the buffer register flip-flops and the 01 and 11 enable flip-flops.

Since there is no controller selection on a reset by CC, the buffer register flip-flops and the enable flip-flops of all controllers are subject to being reset.

F. CONTROLLER STATUS INDICATION

An indication of the status of each controller is available at all times to the CC via the master scanner (MS) (see Figure 9-61).

G. MAINTENANCE MODES OF OPERATION

Maintenance relays are provided to establish modes of operation other than the normal or split mode previously described. These modes are used under trouble conditions and/or to perform maintenance tests.

H. QUARANTINE MODE

In this mode, the operation of quarantine relay LQ or RQ removes a faulty controller from service and gives other controller access to all the magnetically latching relays.

I. RETURN TO SPLIT MODE OF OPERATION

In the split mode no maintenance relays are operated; therefore, to return to this mode some operated maintenance relay must be released. This is accomplished by the momentary operation of relay R28 (or L28). This relay opens the locking path of the other maintenance relays.

J. POWER

An SD is supplied +24 volt and -48 volt power. The +24 volt power for the left side of the SD is fed by the +24-0 bus; for the right side, by the +24-1 bus. The -48 volt power for even-numbered trunk and junctor frames is fed by the -48-0 bus; for the odd-numbered frames, by the -48-1 bus. However, when only one frame of a particular type is provided, both -48 volt buses feed the frame. The buses are branched through twelve fuses at the fuse panel on the frame.

During a manual quarantine, all power is removed from the quarantined side of the SD except for the windings of the A, B and D wirespring relays.

K. EQUIPMENT ARRANGEMENTS

An SD is located below the scanner on bay 1 of each universal trunk frame and junctor frame and a supplementary signal distributor (SSD) when required is mounted on the miscellaneous trunk frame.

9.10 SWITCHING NETWORK

A. GENERAL

The switching network is used to establish 2-wire metallic paths for voice transmission and signaling through eight stages of switching. Beside connecting lines to lines, lines to trunks, and trunks to trunks, the network is used to connect lines or trunks to various types of service circuits such as tones, signal transmitters, signal receivers, coin supervisory circuits, ringing circuits, and maintenance circuits.

Figure 9-62 shows the network as consisting of a number of line link networks (LLN) and trunk link networks (TLN) interconnected through the junctor grouping frame. Each path shown represents two wires, tip and ring. The number of LLN's and TLN's required depends on the traffic characteristics of the office. This number may vary from one to sixteen for each type of link network.

The junctor grouping frame provides the means for terminating the wire junctors used to interconnect the LLN's and TLN's. They also provide the terminations for the junctor circuits used for intraoffice calls through the LLN's. Plug-ended patch cords and connectors are used to interconnect the junctors in a pattern suited to the size and traffic characteristics of the switching network provided.

Line link networks are made up of two types of frames:

(a) Line switch frames (LSF)

(b) Junctor switch frames (JSF).

Trunk link networks are also made up of two types of frames:

(a) Junctor switching frames (JSF)

(b) Trunk switch frames (TSF).

A path through a network is made up of links connected by switches. Each link consists of two wires, tip and ring.
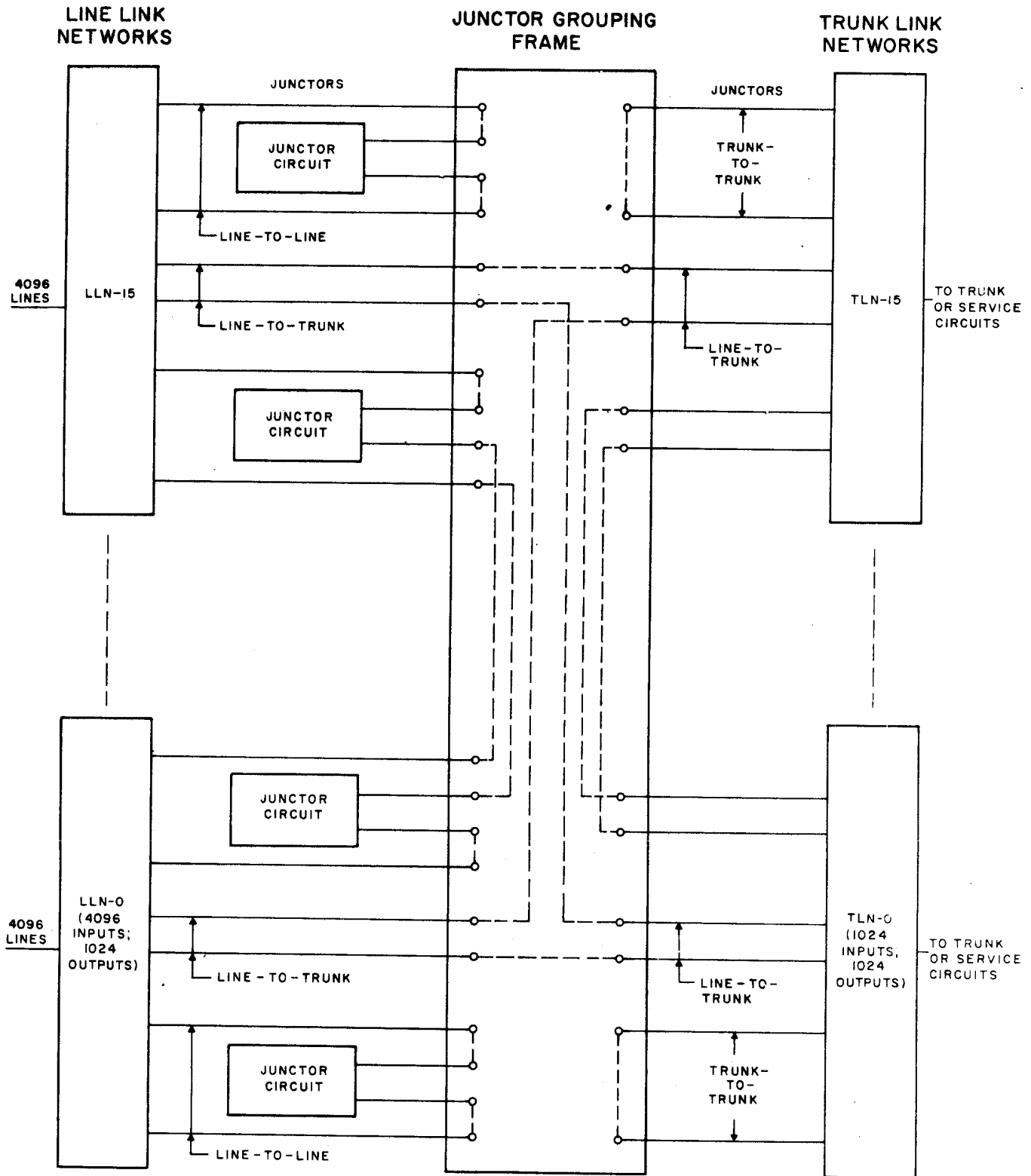
Figure 9-62   Switching Network

B. CROSSPOINT SELECTION

The principle on which crosspoint selection is based is illustrated by Figure 9-63. The control windings of the ferreeds in the switch are shown connected in series along rows and columns. One end of each row and column is connected to a common multiple and wired to wire-spring path select relays, which are controlled by the information from the peripheral bus. Operation of these relays allows a pulse of current to flow only through one row and one column. As a result, the ferreed at the intersection will close its tip and ring contacts. Each of the other ferreeds in the selected row and column has only one winding energized, and consequently, opens the tip and ring contacts.

C. APPARATUS

The basic switching device in the network is called the ferreed. There are two types of ferreeds. One type is used to provide the crosspoint contacts for the four stages of switching in any path through an LLN or a TLN. The other type is used to:

(a) Disconnect a customer line from its scanner ferrod.

(b) Gain access to a test vertical which is connected to FCG, no-test, and restore-verify circuits.

Devices of the first type will be referred to as crosspoint ferreeds or simply ferreeds. Devices of the second type will be referred to as bipolar ferreeds.

1. Crosspoint Ferreed

An exploded view of a crosspoint ferreed is shown in Figure 9-64. The ferreed consists of two miniature glass-enclosed reed switches which are operated or released by controlling the magnetization of the two adjacent remendur plates. (Remendur is a square-loop magnetic material containing iron, cobolt, and vanadium.) The remendur plates are divided magnetically into two independent halves by a steel shunt plate positioned at the midpoint of the tubular coil form. When the two halves of the plates are magnetized series-aiding (adjacent ends poled opposite), part of the magnetic flux returns through the reeds
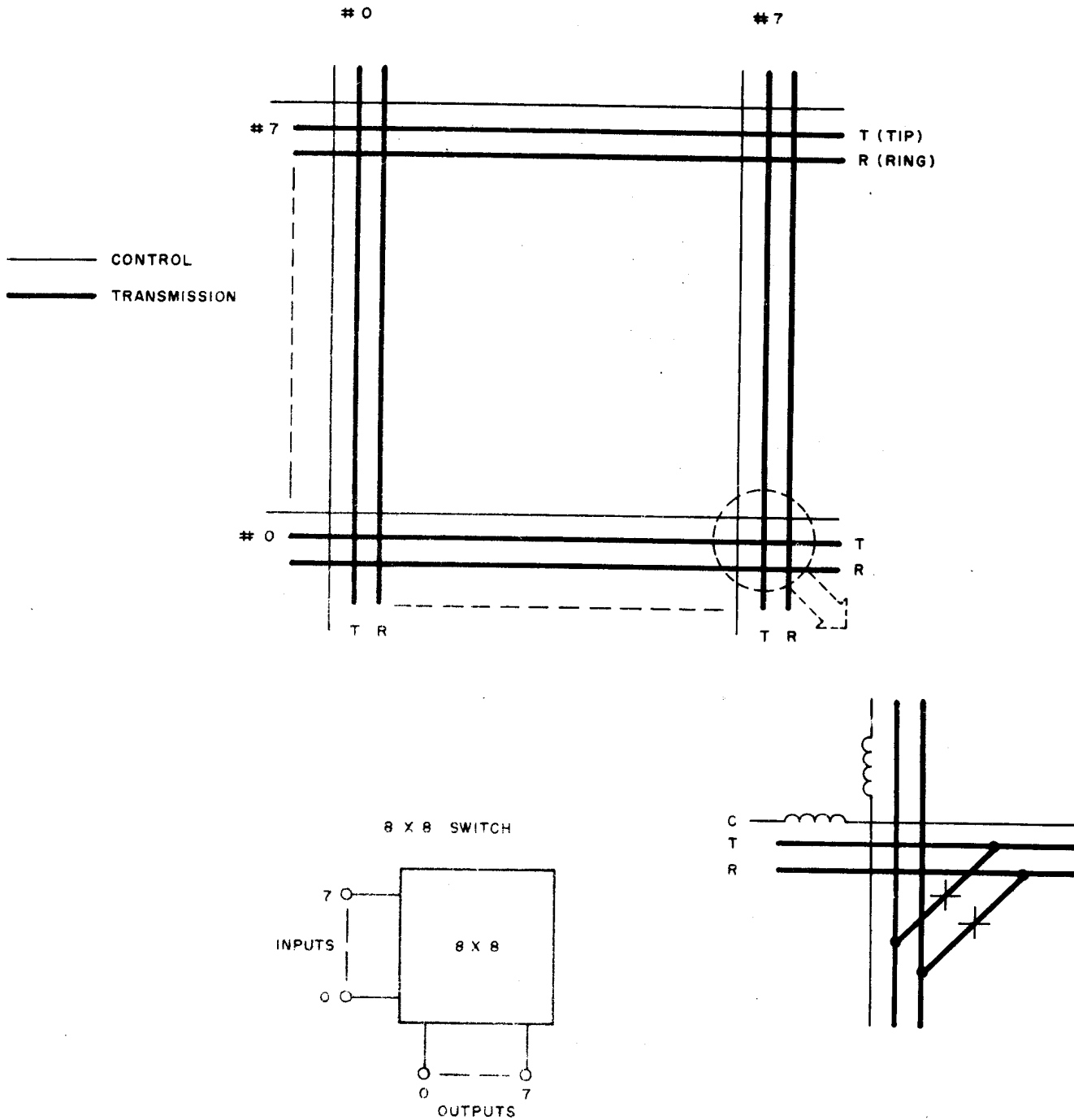
Figure 9-63 Typical Switch and Crosspoint Selection

HORIZONTAL METAL
STRAPS

MOLDED CONTACT
ASSEMBLY

REMENDUR
PLATES

237B SEALED
CONTACT ASSEMBLY
2 PER MOLDED ASSEMBLY

39-TURN COIL

18-TURN COIL

SHUNT PLATE

COIL FORM

VERTICAL METAL
STRAPS
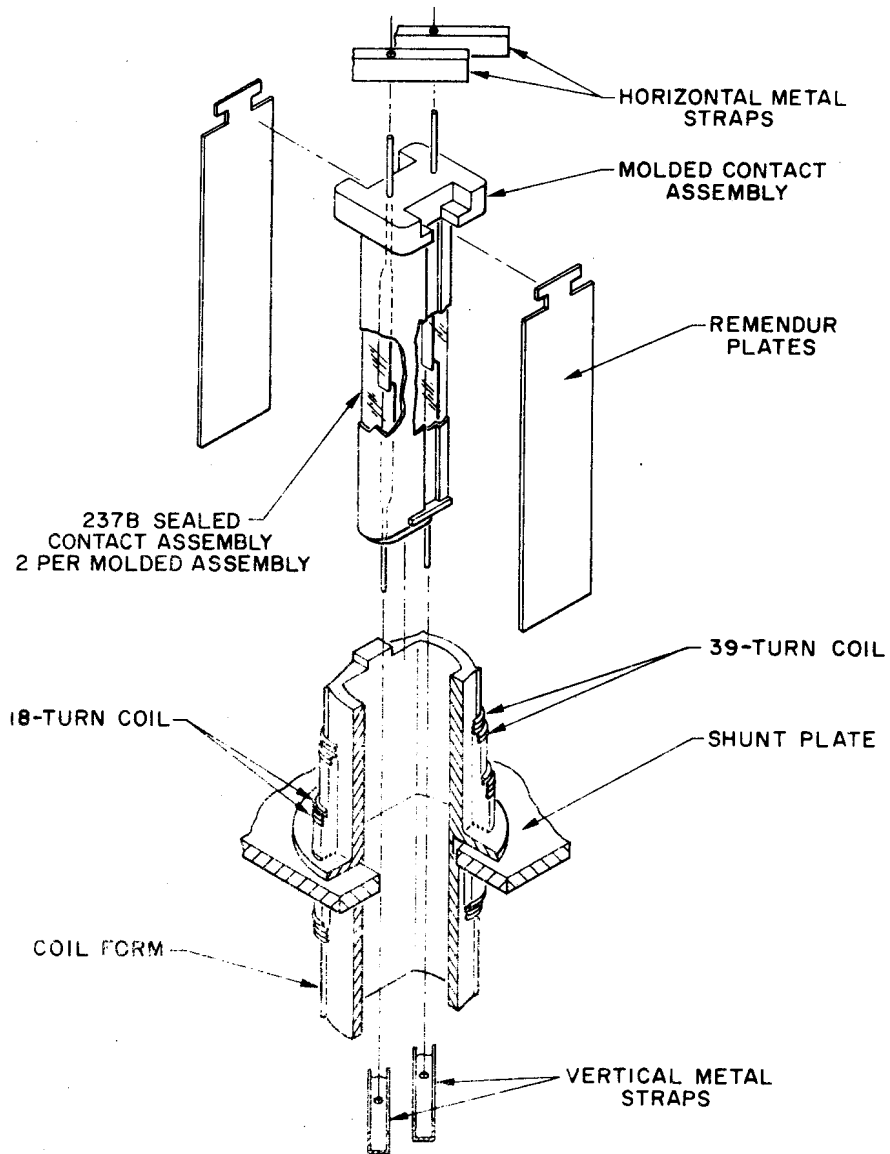
Figure 9-64 Exploded View of Crosspoint Ferreed

RELEASE STATE
A

OPERATE STATE
B
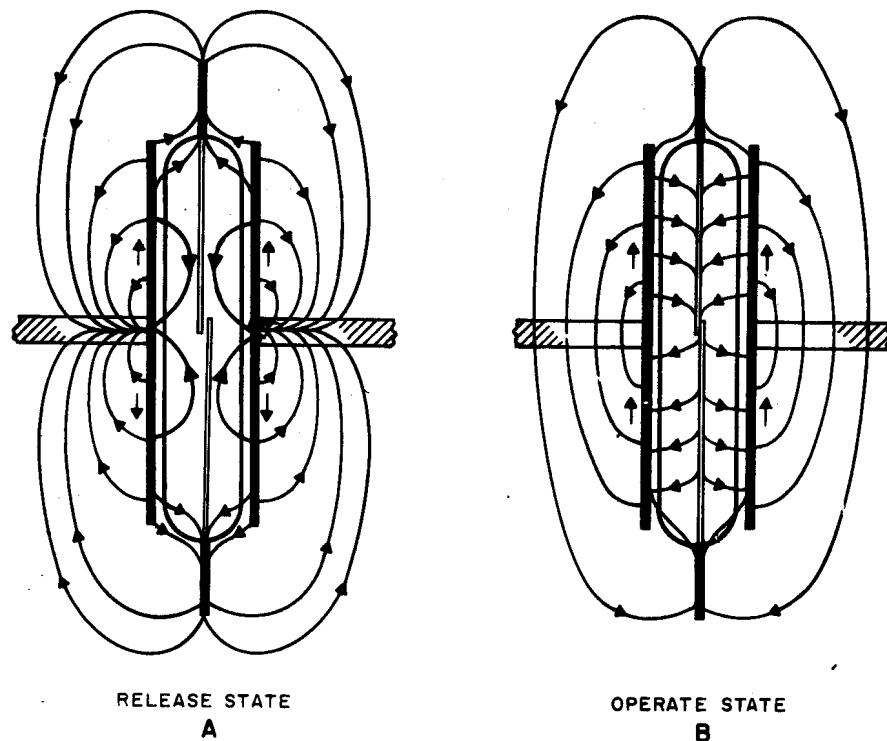
Figure 9-65   Magnetic Flux Patterns in Crosspoint Ferreed

causing contact closure (Figure 9-65B). When the two halves are magnetized in series-opposition (adjacent ends poled alike), there is very little flux through the reeds and their normal tension opens the contacts (Figure 9-65A).

When only one winding is energized, the two halves of the plates are magnetized in series-opposition and the contacts are opened. When both windings are energized simultaneously with equal currents, the two halves of the plates are magnetized series-aiding, causing the contacts to close. The contacts are "dry" when switched; that is, no battery voltage is applied.

When a 0.3-msec pulse of nine to thirteen amperes is applied simultaneously to both windings of the ferreed element, the reed contacts will close within 3 msec. The remendur plates retain their magnetic polarity after the pulse current stops; this keeps the contacts closed.

2. Bipolar Ferreed

The permanent magnet of cunife material has a coercive force of 500 oersteds. The semipermanent magnet of remendur has a coercive force of 50 oersteds. When the winding is pulsed in one direction, the reed contacts are closed (Figure 9-66A). When the winding is pulsed in the opposite direction, the reed contacts are opened (Figure 9-66B). In the latter case, the reeds are bypassed by the magnetic flux and their normal tension causes the contacts to open. When the current in either direction is removed, the semipermanent magnet retains the resulting magnetization and the contacts remain operated or released.

Bipolar ferreeds are arranged in 1 x 8 switch **assembles**

A. CONTACTS CLOSED

MAGNETIC FIELD
CONCENTRATED THROUGH
REED CONTACTS

B. CONTACTS RELEASED

MAGNETIC FIELD
SHUNTED FROM
REED CONTACTS

PERMANENT
MAGNET

SEMIPERMANENT
MAGNET
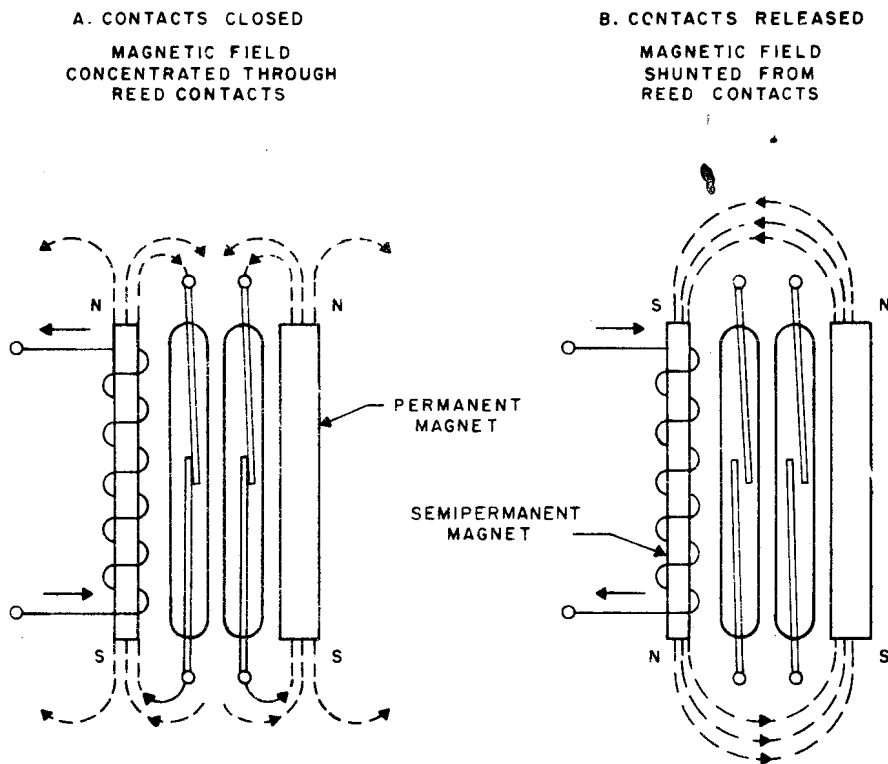
Figure 9-66   Flux Patterns in Bipolar Ferreed

D. NETWORK SWITCHES

A basic switch assembly contains 64 ferreeds arranged in a square array of eight columns and eight rows.

The reed switches are soldered to horizontal straps on one side and to vertical straps on the other side. These horizontal and vertical multiples, when connected by reed contacts, form the tip and ring paths through the switch.

Electrically, there are four types of switches which differ in the arrangement of the tip and ring strapping. These four types are schematically described in Figure 9-67.

E. NETWORK ORGANIZATION

The organization of LLN's and TLN's will be considered in terms of frames and switches within the frames.

1. 2 to 1 Line Link Network

A line network (LLN) has four line switch frames designed for a 2 to 1 concentration ratio and four junctor switch frames.

Each line switch frame contains 16 concentrators. Each concentrator, in turn, has two switches in stage 0 and two in stage 1. Each switch in stage 0 is electrically equivalent to four 4 by 4 switches. Each switch in stage 1 is electrically equivalent to two 8 by 4 switches.

Concentration ratios of 2.5 to 1, 3 to 1, 3.5 to 1, and 4 to 1 are achieved by using four junctor switch frames with five, six, seven, or eight line switch frames of the 2-to-1 design and by multiplying the B-links (see Table 9-3). There are two designs of line switch frames: one for 4-to-1 concentration ratio, one for 2-to-1. It should be noted, however, that a particular office uses only one type of line switch frame and that all line link networks have the same concentration ratio.

2. 4 to 1 Line Link Network

There are four basic line switch frames (BLSF), four supplementary line switch frames (SLSF), and four junctor switch frames (JSF). An LLN may be partially equipped with line and junctor switch frames.

BASIC 8 X 8 SWITCH
(USED IN BOTH STAGES
OF JUNCTOR SWITCH FRAMES &
TRUNK SWITCH FRAMES)
8 INPUTS

8 OUTPUTS

A

TWO 8 X 4 SWITCHES
(USED IN STAGE I OF 4:I
OR 2:I CONCENTRATOR-
LINE SWITCH FRAME)
8 INPUTS

8 OUTPUTS

8 INPUTS

B

16 X 4/8 SWITCH
(USED IN STAGE 0
OF 4:I CONCENTRATOR-
LINE SWITCH FRAME)
8 INPUTS

8 OUTPUTS

8 INPUTS

C

FOUR 4 X 4 SWITCHES
(USED IN STAGE 0
OF 2:I CONCENTRATOR-
LINE SWITCH FRAME)
8 INPUTS

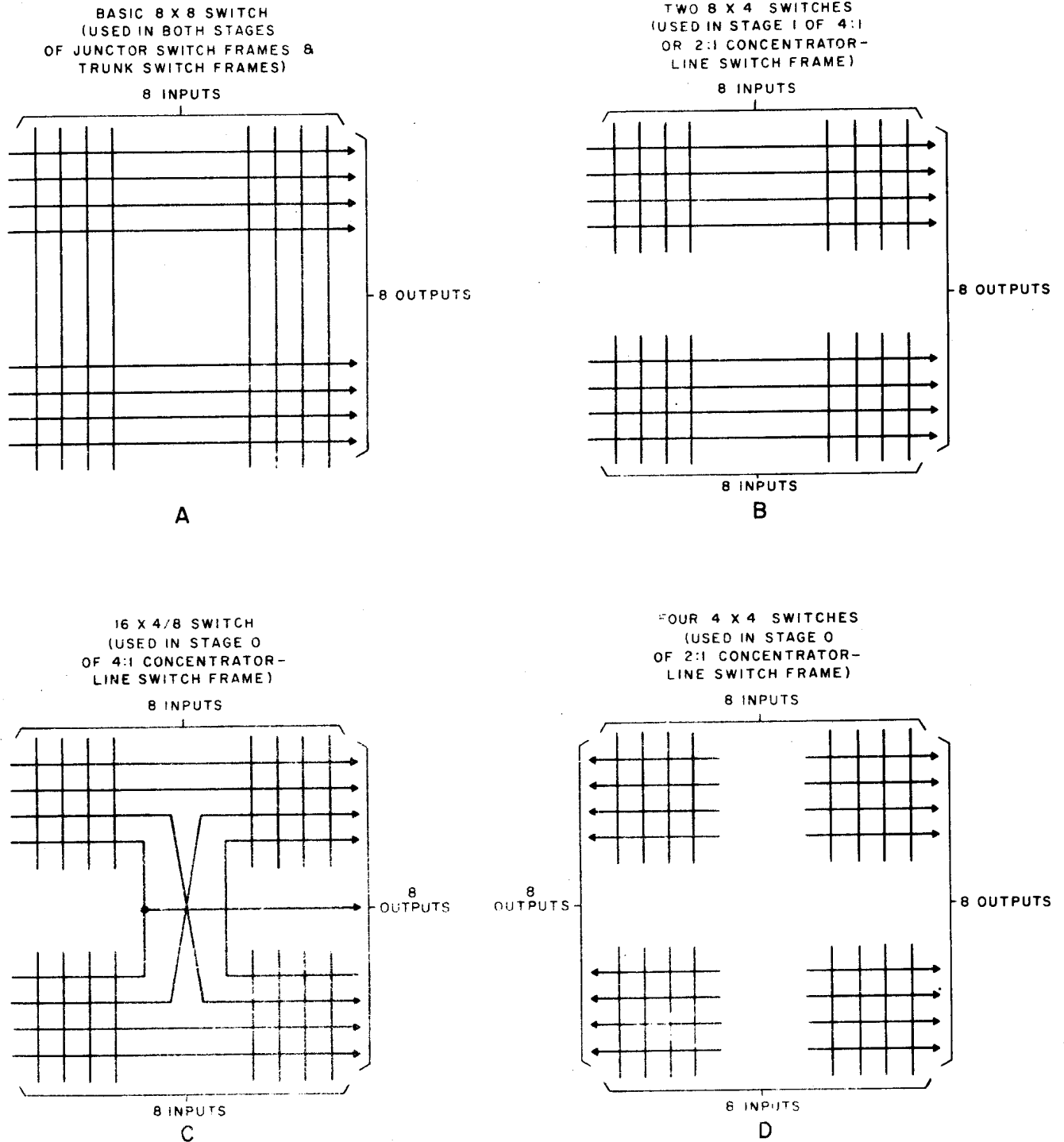8 OUTPUTS

8 OUTPUTS

8 OUTPUTS

8 INPUTS

D

Figure 9-67 Tip and Ring Wiring Schematic for Four Types of
Network Switches

9.114

Each line switch frame, whether basic or sup-
plementary, contains eight concentrators. Each
concentrator has four switches in stage 0; each
of the 16 inputs of a switch has access to only
four of the eight outputs. For each of the four
switches in stage 0, there are two switches that
provide 16 pairs of cutoff contacts. Stage 1 of
a concentrator has two switches, each electrically
equivalent to two 8 by 4 switches.

Each junctor switch frame contains four grids.
Each grid has eight 8 by 8 switches in each of the
two stages. In addition, a 1 by 8 switch is asso-
ciated with each switch in stage 1. The 1 by 8
switch provides access to a common test vertical
which is connected to FCG, no-test, and restore
verify circuits.

Concentration ratios of 5 to 1, 6 to 1, 7 to 1, or
8 to 1 are achieved by using four junctor switch
frames with five, six, seven, or eight basic and
supplementary line switch frames, respectively, and
by multiplying the B-links to the added line switch
frames (see Table 9-3).

F. NETWORK PATHS

A network path is formed by a combination of links and
junctors joined into a chain by the closure of the appro-
priate crosspoint contacts. Figure 9-68 shows, as an example,
an intraoffice talking path. While a line is idle, its
associated crosspoint contacts in stage 0 of the LSF are
open. At the same time, its cutoff contacts are closed, thus
connecting the line to its scanner for supervision. When a
path is to be established through the LLN, a partial path is
set up first by contacts in stage 1 of the LSF and in
stages 0 and 1 of the appropriate JSF. By means of contacts
in the same JSF, an FCG[1] (false cross and ground) detector is
then connected to check the path. Next, the appropriate
crosspoint contacts in stage 0 of the LSF are closed, while
the cutoff contacts in the LSF and the F contacts in the JSF
are opened. The preceding considerations apply to the paths
associated with both the calling and the called lines.
Finally, cut-through contacts in a junctor circuit are closed
to establish a talking connection.

TABLE 9-3

LINE LINK NETWORK SIZES

LSF Conc Ration	LSF's Per LLN	Ratio of Lines to Junctors	Customer Lines Per LLN	Max. No. of LLN's Per Office	Max. No. of Lines Per Office
For Heavy Customer Usage					
2 to 1	4	2.0 to 1	2,048	16	32,768
2 to 1	5	2.5 to 1	2,560	16	40,960
2 to 1	6	3.0 to 1	3,072	16	49,152
2 to 1	7	3.5 to 1	3,584	16	57,340
2 to 1	8	4.0 to 1	4,096	16	65,536
For Regular Customer Usage*					
4 to 1	4	4 to 1	4,096	16	65,536
4 to 1	5	5 to 1	5,120	14	65,536
4 to 1	6	6 to 1	6,144	12	65,536
4 to 1	7	7 to 1	7,168	10	65,536
4 to 1	8	8 to 1	8,192	8	65,536

*LSFs for a 4-to-1 concentration ratio are made up of one basic and one supplementary frame.

TABLE 9-4

TRUNK LINK NETWORK SIZES

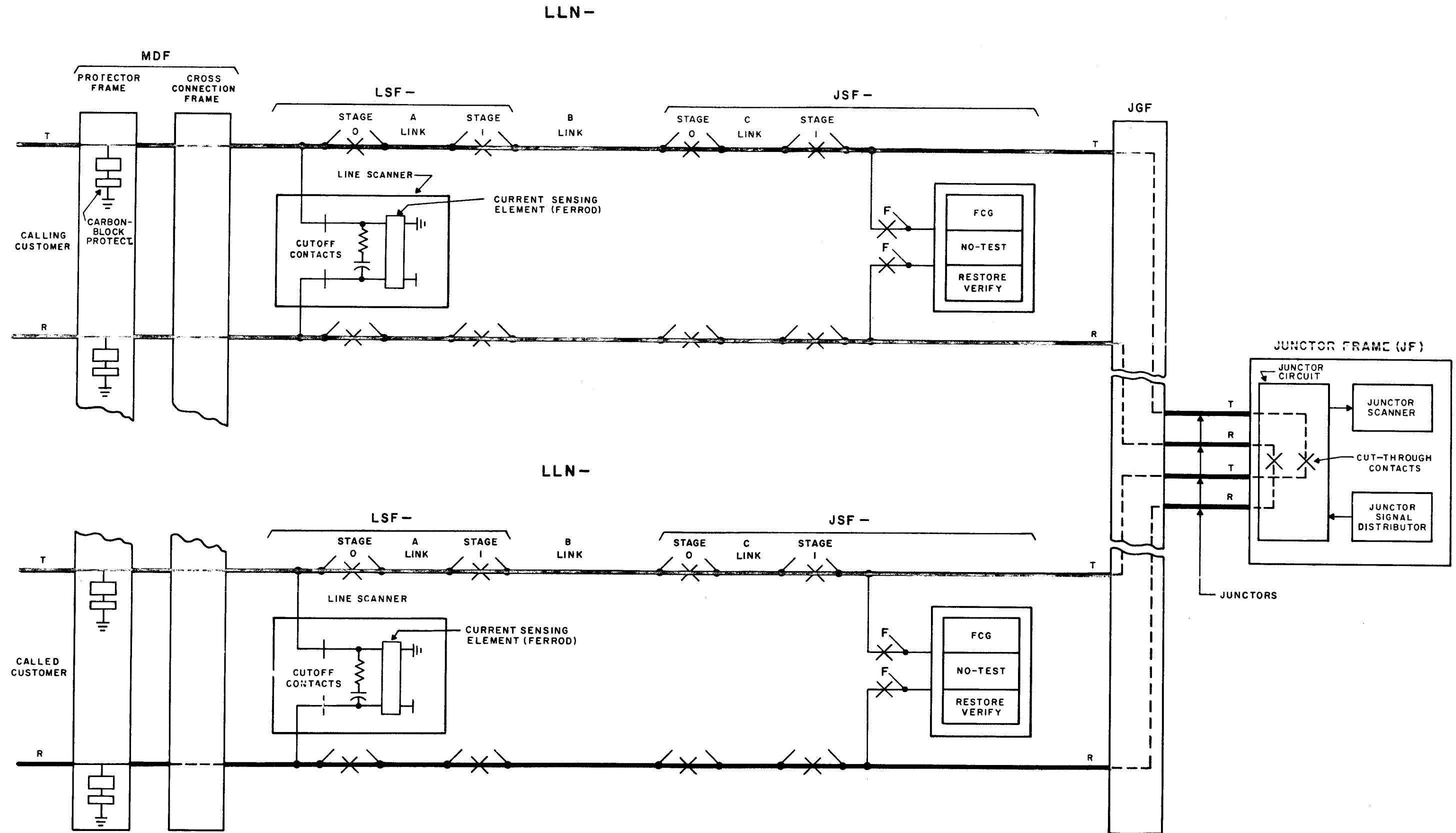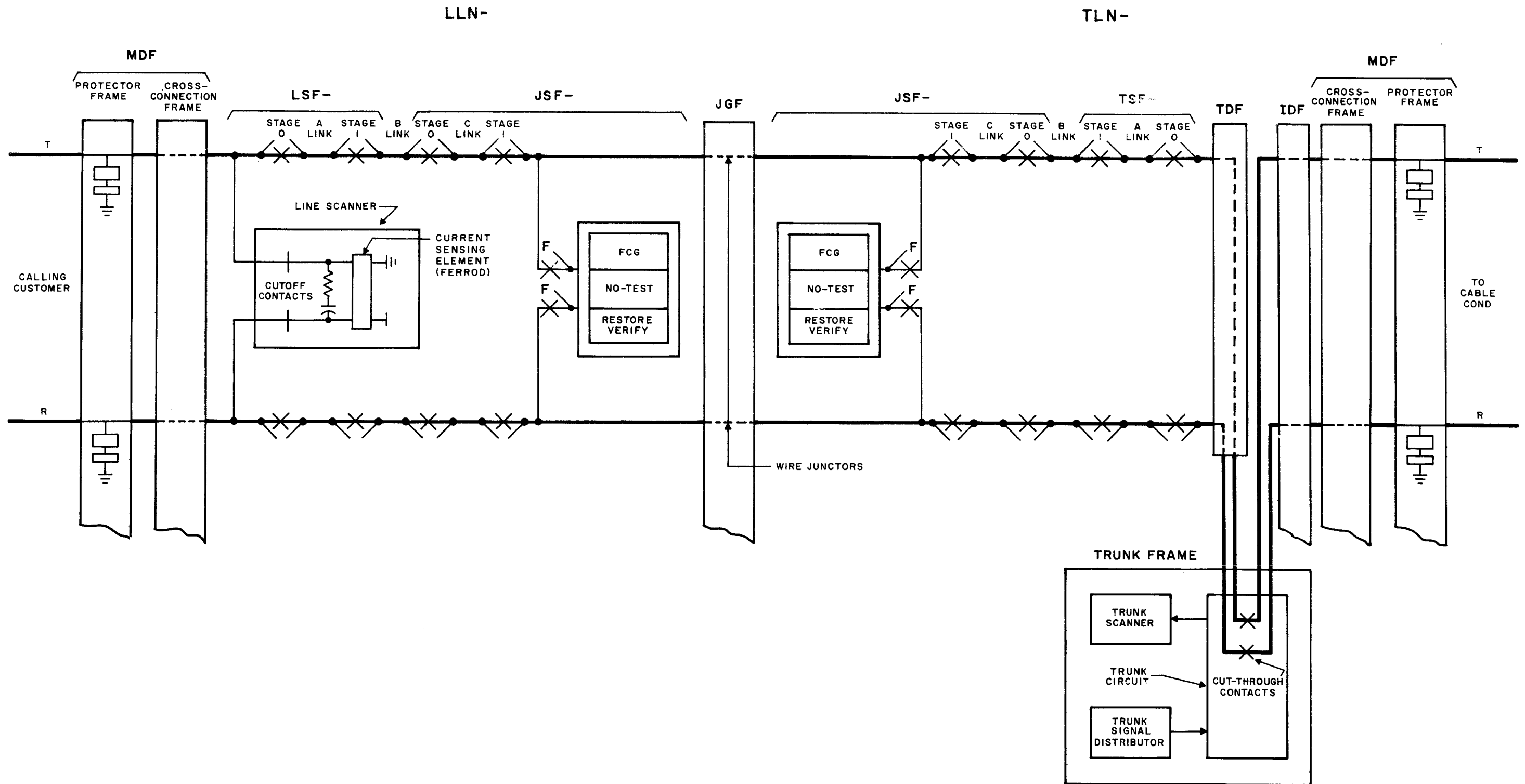| Ratio of Trunks to Junctors	TSF's Per TLN	Trunk Term. Per TLN	Junctors Per TLN	JSF's Per TLN
1.00 to 1	4	1,024	1,024	4
1.25 to 1	5	1,280	1,024	4
1.50 to 1	6	1,536	1,024	4
1.75 to 1	7	1,792	1,024	4
2.00 to 1	8	2,048	1,024	4

Figure 9-68 Intraoffice Talking Path

9.117

Figure 9-69 Interoffice Talking Path

9.119

At any time during the conversation, it is possible to monitor the call by closing the F contacts in the JSF and by connecting the no-test circuit. At the end of the conversation, the connection is released by opening the cut-through contacts in the junctor circuit. While the LLN paths for the calling and called lines are still closed, the system closes, for each line, the cutoff contacts in LSF and the F contacts in the JSF and connects the restore verify circuit. This puts a resistor across the tip and ring and simulates an origination which is observed via the line scanner. Having verified its ability to detect any subsequent originations on the line, the system opens the crosspoint contacts in stage 0 of the LSF. Figure 9-69 shows an interoffice talking path.

   (1) FCG test consists of monitoring for current in a
       loop that contains the tip and ring conductors of
       the test vertical. A sensitive type of ferrod is
       used as a current sensing device.

G. CONTROL

Each switch frame in the network contains two controllers. The switches within a frame are divided into two equal groups, each assigned to a controller. Under normal conditions, each controller operates with its assigned switch group. Two simultaneous path selections at most can be made within a frame, one in each switch group. However, when a controller is in trouble, its mate takes over the control of both switch groups. Under these conditions, only one path selection can take place at a time within a frame.

The selection of crosspoints to set up a path in the network is a function of central control (CC). In its call store (CS), CC maintains an up-to-date record of the busy-idle states of all the network links (network map); it also maintains a record of the end terminals of all paths in use or reserved in the network (path memory). When a selection is to be made between a line and a junctor or a trunk and a junctor, the network map is examined. A path is then chosen on the basis of the busy-idle states of all the possible A-, B-, and C-links between the line (or trunk) and a selected junctor group. After a path is chosen, the network map is brought up to date and a record of the line-junctor-trunk association is entered in the path memory. Appropriate network instructions are then prepared by CC. These instructions and the identity of the network frames to which they pertain are recorded in the CS in one of a number of

peripheral order buffers (POB) (also called work lists). There is a work list associated with each call requiring a network connection. At intervals of 25 msec, instructions are read out of the work lists, one at a time, and transmitted to the appropriate network controllers. The network controllers cause the appropriate crosspoint contacts to close.

The path selection within a network frame is controlled by wirespring relays in the network controllers. The operation of a particular set of wirespring relays determines the crosspoint control windings to be pulsed. This results in the closure of those crosspoint contacts whose horizontal and vertical control windings are simultaneously pulsed.

1. Network Controllers

Figure 9-70A shows the basic arrangement of a typical network controller.

The controller is enabled via the central pulse distributor (CPD). Via one of the duplicate peripheral address buses, the enabled controller receives an instruction from CC and stores it in the buffer register. Figure 9-70B shows the make-up of the order data and link data for the 4 to 1 line switch frames. The order data consists of six bits in a one-out-of-two (1/2) and a one-out-of-four (1/4) code. This information is used by the translator to operate one of the six order relays. Similarly, the link data is used to operate one relay in each of the A, B, C and D groups and to select between the basic and supplementary frames.

Three test circuits are provided within each controller to monitor its operation. These circuits will prevent the controller from processing an order if an invalid address or a malfunction is detected. In such a case, the controller will remain in the state it was in at the time the malfunction was detected. Before the controller can be reenabled, it will be necessary to send a signal over the reset lead of the peripheral bus. The test circuits operate as follows:

(a) A group check circuit verifies that only one relay has been operated among the order relays and in each access relay group.

NETWORK CONTROLLER

LINE SWITCH FRAME

CENTRAL PULSE DISTRIBUTOR

ENABLE

RESET

PULSER AND CHECK CIRCUITS

ORDER RELAYS

ACCESS RELAYS

FERREED CONTROL WINDINGS

OR-

A-, B-, C-, & D-

MASTER SCANNER
S
F
T

DIAGNOSTIC BUS

CONTROL LOGIC

RESET

FCG

PERIPHERAL UNIT ADDRESS BUS

ORDER AND LINK DATA (36 BITS)

BUFFER REGISTER

TRANSLATOR

A

ORDER DATA

LINK DATA

BIT: | 35 34 | 33 32 31 30 | 29 28 | 27 26 25 24 | 23 22 21 20 | 19 18 17 16 | 15 14 13 12 | 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

CODE: 1/2   1/4   1/2   1/4   1/4   1/4   1/4   1/4   1/4   1/4

SELECTION: 1-OUT-OF-6 ORDER RELAYS   1-OUT-OF-4 A RELAYS   1-OUT-OF-16 C RELAYS   1-OUT-OF-16 D RELAYS   1-OUT-OF-16 B RELAYS

1-OUT-OF-2 FRAMES (BASIC OR SUPPLEMENTARY)

B
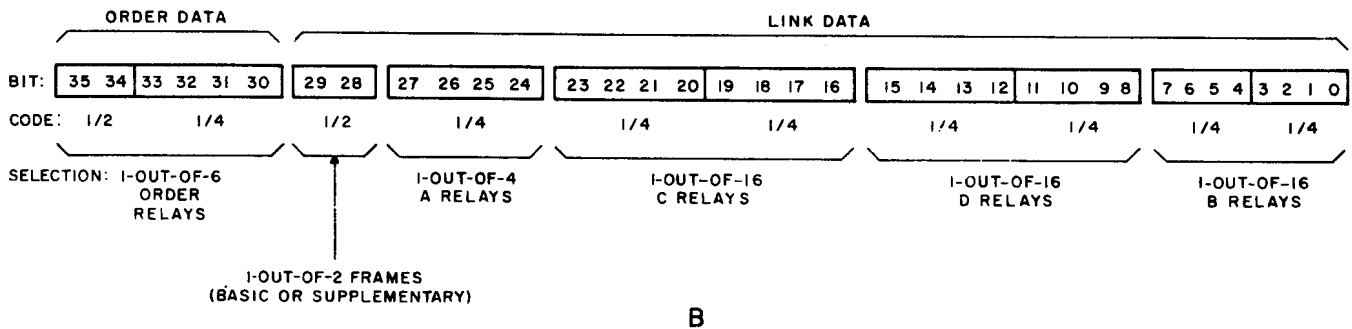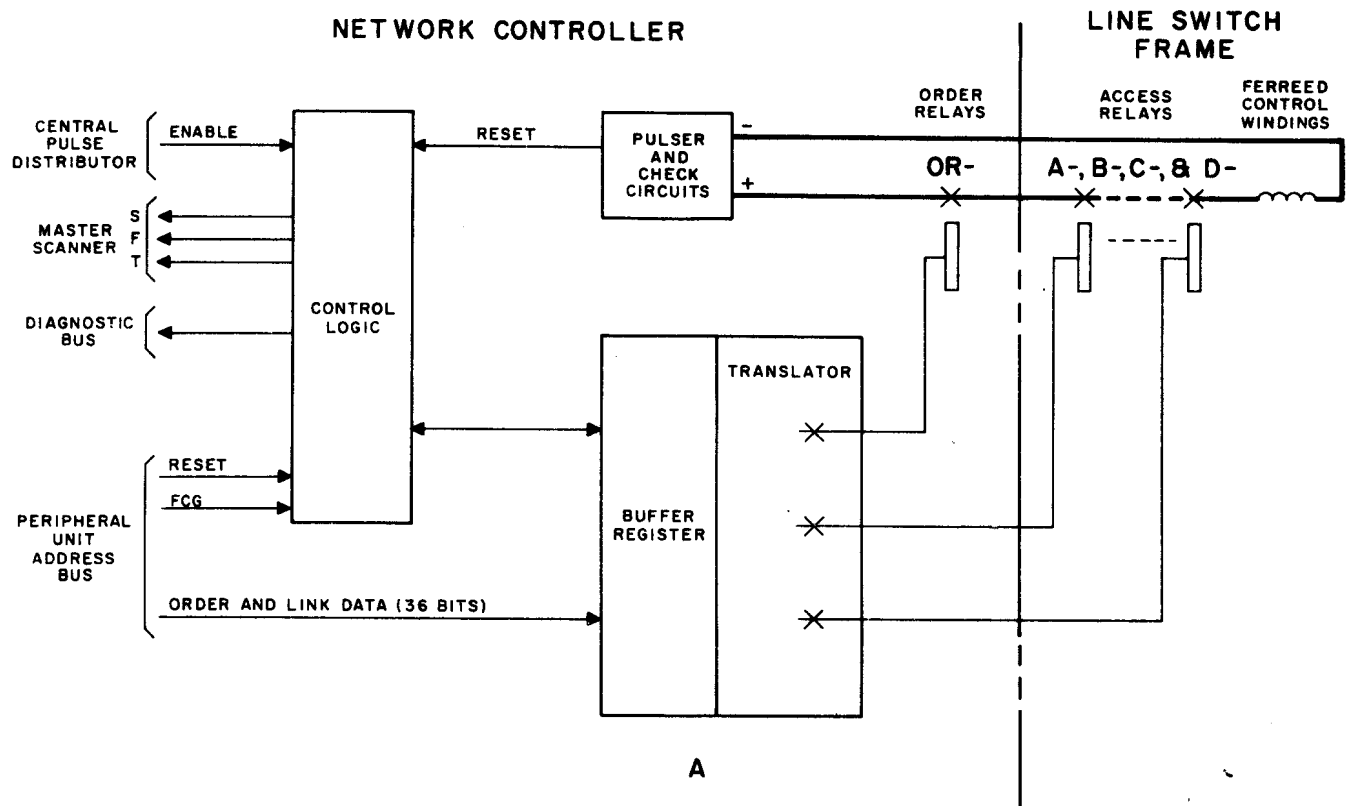
Figure 9-70   Pulse Path Selection to Ferreed Windings

    (b) A path check circuit prevents the pulses from being fired unless the pulsing path is continuous.

    (c) A pulse verification circuit resets the controller to the idle state only if the pulser has generated a current pulse of sufficient amplitude to operate the ferreeds.

Twelve internal test points are provided to enable the system to test and diagnose a controller. Some of these points, for instance, can indicate whether all relays are released in each of the various access relay groups. The twelve test points can be connected to a diagnostic bus which is common to all network controllers. This bus, which is not duplicated, can be observed via the master scanner (MS). In addition, there are three scanpoints per controller permanently connected to the MS; these points, labeled, S, F and T, are used to observe the various internal states of the controller.

2. Duplication

As previously stated, each switch frame has two controllers, each assigned to one half of the switches on the frame. Figure 9-71 shows schematically how each controller can operate independently of the other under normal conditions and can take over the entire frame when the mate controller fails. Each controller has its own group of order relays and path selection relays. Each of these relays has two windings. In an order relay, either of the two windings can be controlled by the same controller. In a path selection relay, one winding can be controlled by one controller, the other by the mate controller. The pulser of either controller can be used to operate the ferreeds in either switch group of a frame.

3. Modes of Operation

The following modes of operation are available for a network controller:

(a) Normal mode of operation (NM)

(b) Test point access mode (TPAM)

(c) Quarantine mode (QM)

(d) Manual power removed mode (MPRM)
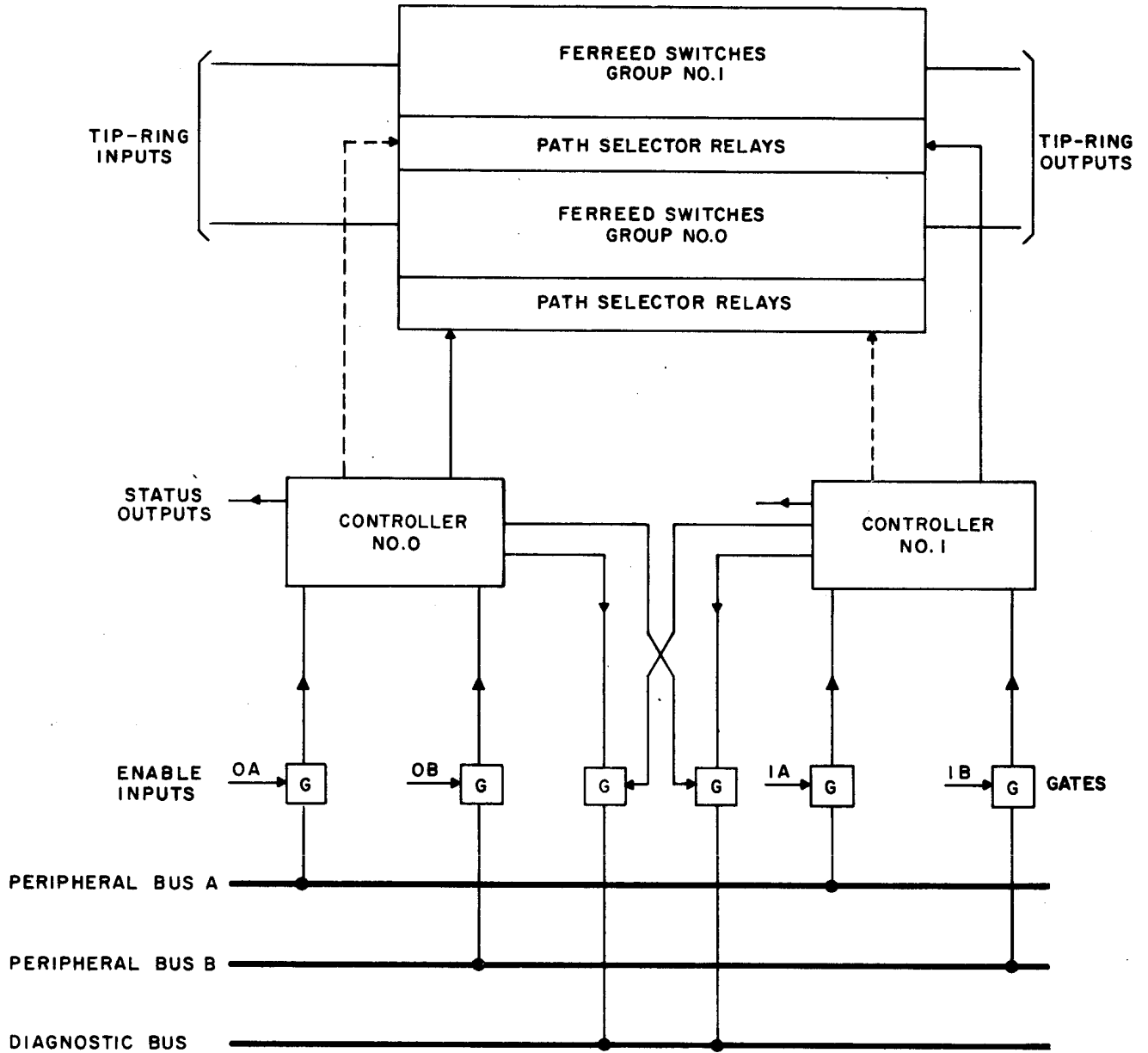
(e) Combined mode (CM).

Figure 9-71   Frame Control

In the NM, each of the two controllers on a frame
is active and controls its half of the frame. If,
while the NM, a controller receives an order to
operate the equipment in the other half of the
frame, the order will be regarded as invalid and
the operation will be inhibited by the internal
test circuits.

In the TPAM, a relay connects the twelve test
points of a controller to the diagnostic bus.
Only one controller should be associated with the
diagnostic bus at any time.

The QM is used to remove a controller from service
when a trouble is detected. In this mode, the
controller is prevented from operating any path
selection relays and will not return an enable
verify signal. A controller in QM can still
receive enable signals and signals from the periph-
eral bus system. It can also carry out orders up
to the point where the wire-spring relays would
normally be operated. This makes possible a
partial diagnosis of the equipment. The internal
test circuits can be exercised and monitored by
the system.

In the MPRM, all power is removed from a controller.
This mode is initiated manually at the frame.
Power may be removed from only one of the two con-
trollers at a time.

A controller is automatically placed in the CM
whenever its mate controller is either in QM or in
MPRM. In this mode, the controller assumes
control of all the common equipment in the frame.

4. Mode Control

All modes of operation are controlled by the system
except for MPRM, which is initiated manually. To
place a controller in either the TPAM or QM, a
"Test" order is sent to the mate controller with
link data specifying TPAM or QM. A controller may
be placed in both TPAM and QM by means of two
separate orders. To release a controller from
TPAM or QM, a "Test" order may be sent to the
controller with link data specifying release.
Restoring power to a controller after an MPRM can
only be done manually.

H. NETWORK ORDERS

As previously shown, each line, junctor, or trunk switch frame provides two stages of switching. In addition, line switch frames contain bipolar ferreeds for line scanner cutoff; junctor switch frames contain bipolar ferreeds for access to a test vertical. The function of the CC is to determine, under program control, the complete network path required for a particular phase in the processing of a call. The information for establishing the selected path is then sent to the appropriate switch frames. One at a time, these frames receive the necessary information from CC via the peripheral bus. This information consists mainly of:

(a) An order specifying the type of action to be carried out.

(b) An address specifying the links to be selected.

Figure 9-72 describes the types of orders that can be carried out by the various switch frames. For instance, the top item of Figure 9-72B shows that, as the result of the order "Connect (with FCG)," the controller of an LSF opens stage 0 of some specified path, closes stage 1, and leaves the associated cutoff contacts unchanged (closed). At the same time, a line junctor switch frame executes a similar order (see top item of Figure 9-72C). The combined actions of the LSF and JSF establish a partial path that involves three stages of switching and is connected to an FCG detector.

Later, the LSF will execute the order "Connect (with CO open)" while the JSF executes the order "Connect." This establishes a normal 4-stage path without any connections to either a line scanner or a test vertical.

To monitor an established connection, the order "Operate No-Test" is sent to the JSF; this connects the path to a no-test termination via the test vertical. Later, the order "Restore No-Test" will remove this connection.

As previously explained, when a path through the LLN is to be released, it is necessary to check the ability of the system to supervise the line involved. This is done by sending the order "Connect (with CO closed)" to the LSF and the order "Connect verify (loop start)" or "Connect verify (ground start)" to the JSF. As the restore verify circuit connected to the test vertical, a resistor is connected

LSF   JSF   JSF   TSF
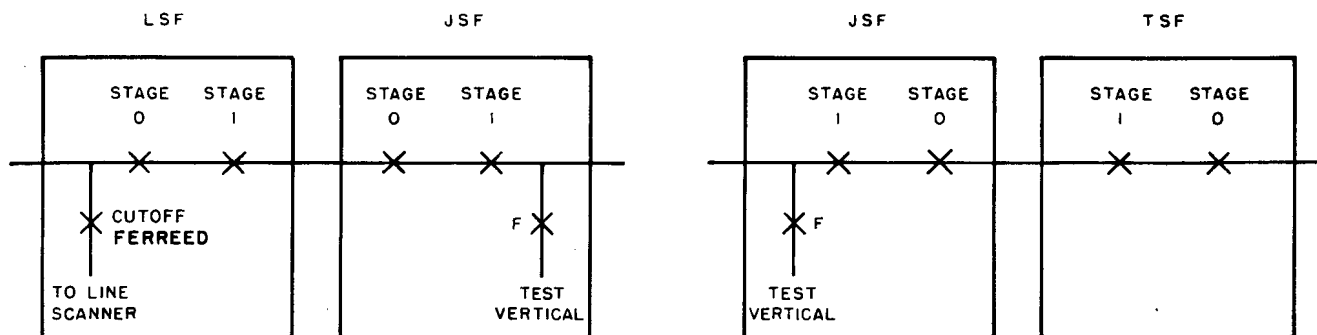
A

LSF ORDERS

ORDER	CUTOFF	STAGE 0	STAGE •1
CONNECT (WITH FCG)	N	O	C
CONNECT (WITH CUTOFF OPEN)	O	C	C
CONNECT (WITH CUTOFF CLOSED)	C	C	C
RESTORE CUTOFF	C	O	N
HIGH & DRY	O	O	N
TEST	N	N	N

O = OPEN
C = CLOSED
N = NO CHANGE

B

JSF ORDERS

ORDER	STAGE 0	STAGE 1	F	CIRCUIT CONNECTED TO TEST VERTICAL
CONNECT (WITH FCG)	C	C	C	FCG
CONNECT	C	C	O	——
OPERATE NO-TEST	N	N	C	NO-TEST
REMOVE NO-TEST	N	N	O	——
CONNECT VERIFY (LOOP START)	C	C	C	LOOP START TERMINATION
CONNECT VERIFY (GROUND START)	C	C	C	GROUND START TERMINATION
TEST	N	N	N	——

C

TSF ORDERS

ORDER	STAGE 1	STAGE 0
CONNECT	C	C
TEST	N	N

D

Figure 9-72   Network Orders

9.128

between tip and ring for a loop start and between ring and ground for a ground start. Later, the LSF will be requested to execute the order "Connect (with FCG)." If the restore verify circuit is not available, the path is released directly by means of the order "Restore Cutoff."

The "high and dry" order to an LSF is used whenever it is desired to isolate a line from the system because of service denial or trouble on the line.

The "test" order to a switch frame is used to control the mode of operation of a controller and does not affect any crosspoints.

It should be noted that none of the network orders requests the opening of any crosspoint contacts in stage 1 of an LSF or stages 0 and 1 of either a JSF or a TSF. These contacts will be opened in the process of establishing new paths. Further illustrations of the network orders described above are shown schematically for the LSF, JSF and TSF in Figure 9-73 through 9-75.

I. JUNCTOR GROUPING FRAME

The junctor grouping frame (JGF) provides the means for interconnecting the LLN's, TLN's and the junctor frames (JF). The junctor pattern for a particular office depends on its size and on the type of traffic.

The junctors from the LLN's, TLN's, or JF's are arranged in subgroups of 16 tip and ring pairs. Via terminal strips on the rear of the JGF, the 16 pairs of a subgroup are connected either to a connector or to a plug-ended path cord on the front.

All offices have at least two JGF bays (Figure 9-76), each bay consists of eight horizontal sections. Each section has 18 connectors in two rows of 9, 18 patch cords - each connected to a plug, and a shelf for storing the excess slack of the cords.

The connectors and plug-ended patch cords in the eight horizontal sections form nine vertical files on the bay. Each file has 16 plugs and 16 connectors and thus a capacity for 32 by 16 or 512 junctors; the total capacity of a bay is then 9 by 512 or 4,608 junctors. The 1,024 junctors from each LLN or TLN are distributed over two files on separate bays. The 1,024 junctors from two JF's are distributed over two files; half of the 512 junctors from each JF goes to each file.
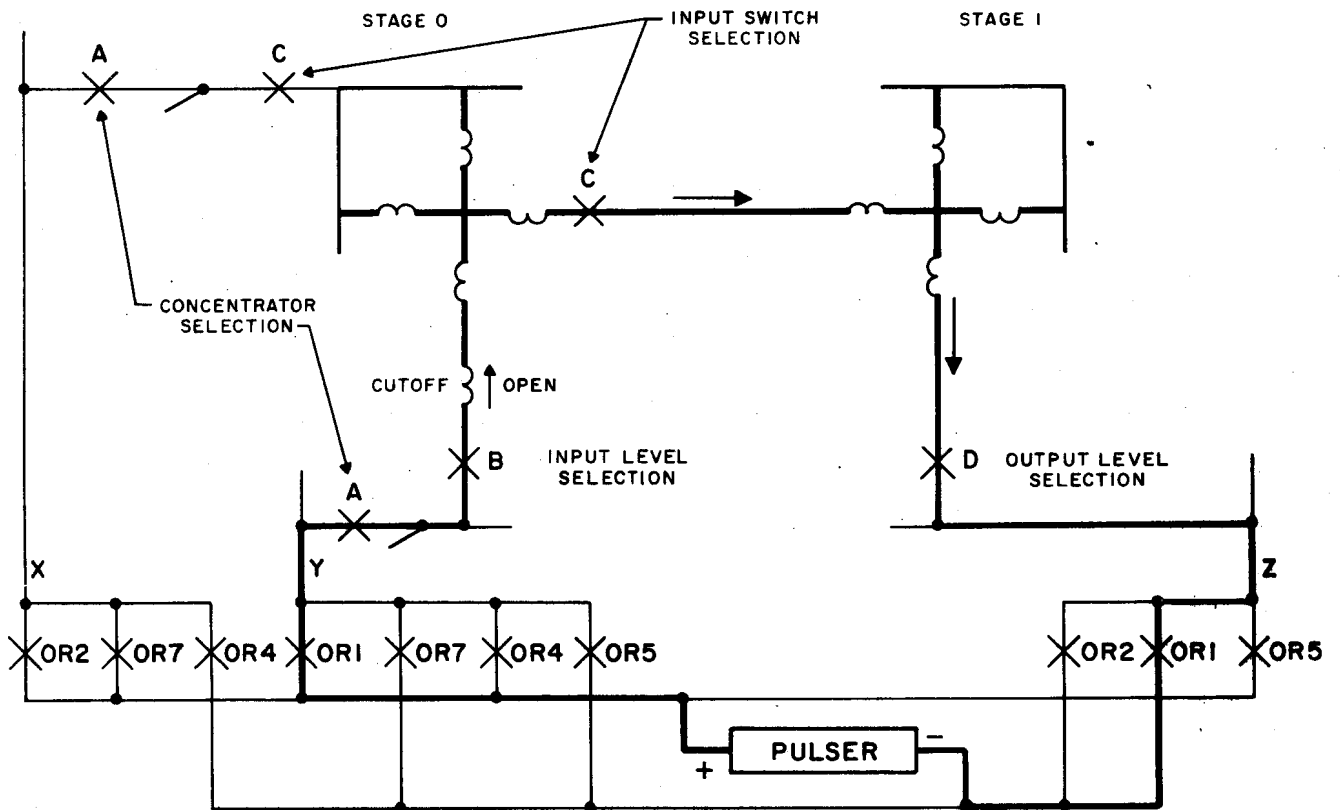
TYPICAL FRAME ORDERS AND PATH SELECTIONS IN A LINE SWITCH FRAME

NETWORK OPERATION	ORDER RELAY	FERREED OPERATIONS IN TIP-RING PATH			PULSER CONNECTION	
		CUTOFF	STAGE 0	STAGE 1	+	−
CONNECT CUTOFF OPEN	OR1	O	C	C	Y	Z
FCG	OR2	N	O	C	X	Z
HIGH AND DRY	OR4	O	O	N	Y	X
CONNECT CUTOFF CLOSED	OR5	C	C	C	Z	Y
RESTORE CUTOFF	OR7	C	O	N	X	Y

O - OPEN
C - CLOSED
N - NO CHANGE

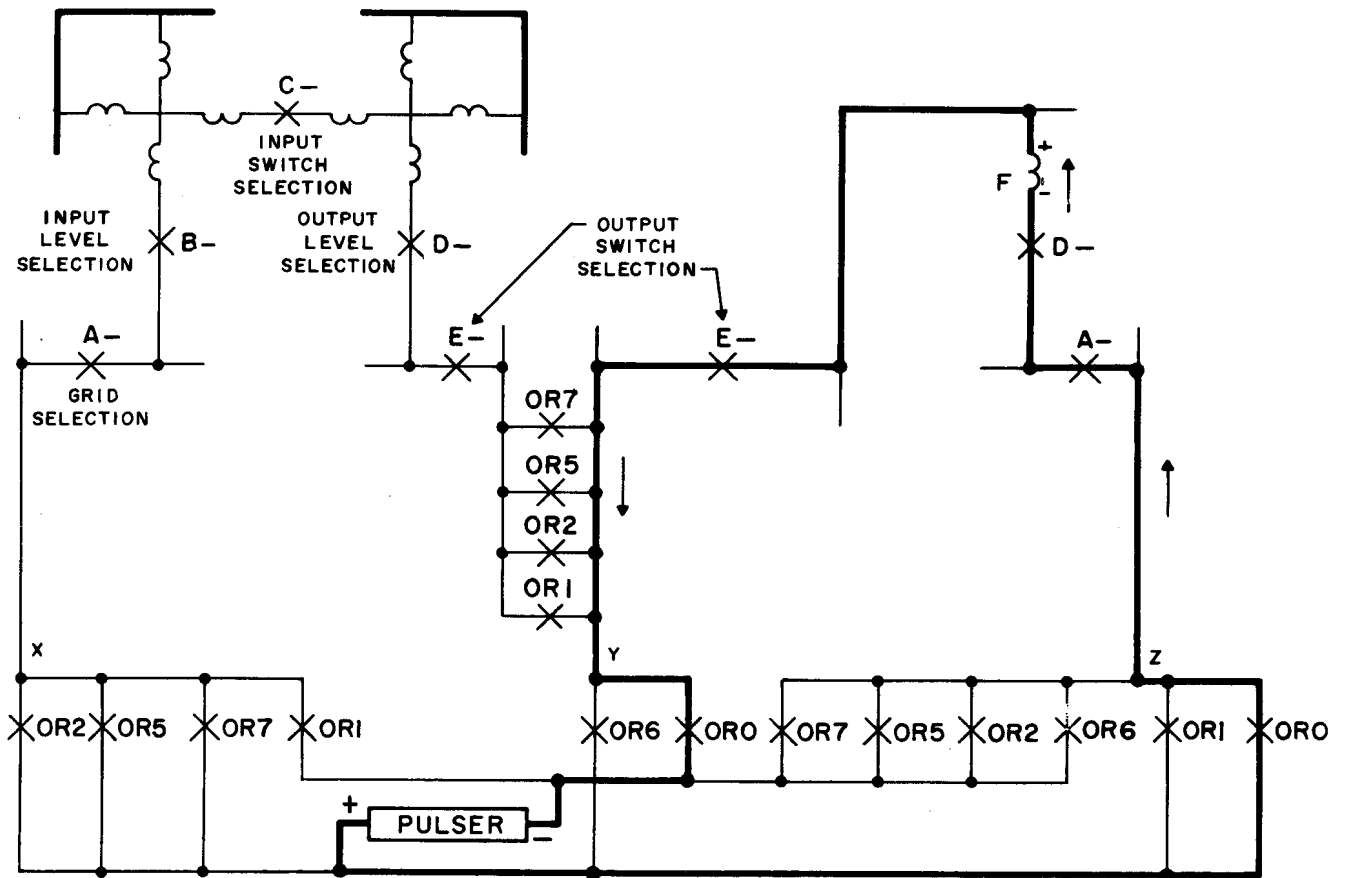Figure 9-73 Pulse Path for "Connect (with CO Open)"

TYPICAL FRAME ORDERS AND PATH SELECTIONS IN JUNCTOR SWITCH FRAME

NETWORK OPERATION	ORDER RELAY	FERREED OPERATIONS IN TIP-RING PATH			PULSER CONNECTION	
		F	STAGE 0	STAGE 1	+	−
REMOVE NT, FCG,OR VERIFY	OR0	O	N	N	Z	Y
CONNECT	OR1	O	C	C	Z'	X
FCG	OR2	C	C	C	X	Z
CONNECT VERIFY (LOOP ST.)	OR5	C	C	C	X	Z
OPERATE NT	OR6	C	N	N	Y	Z
CONNECT VERIFY (GRD ST.)	OR7	C	C	C·	X	Z

O = OPEN
C = CLOSED
N = NO CHANGE

Figure 9-74   JSF - Simplified Pulse Path

9.131
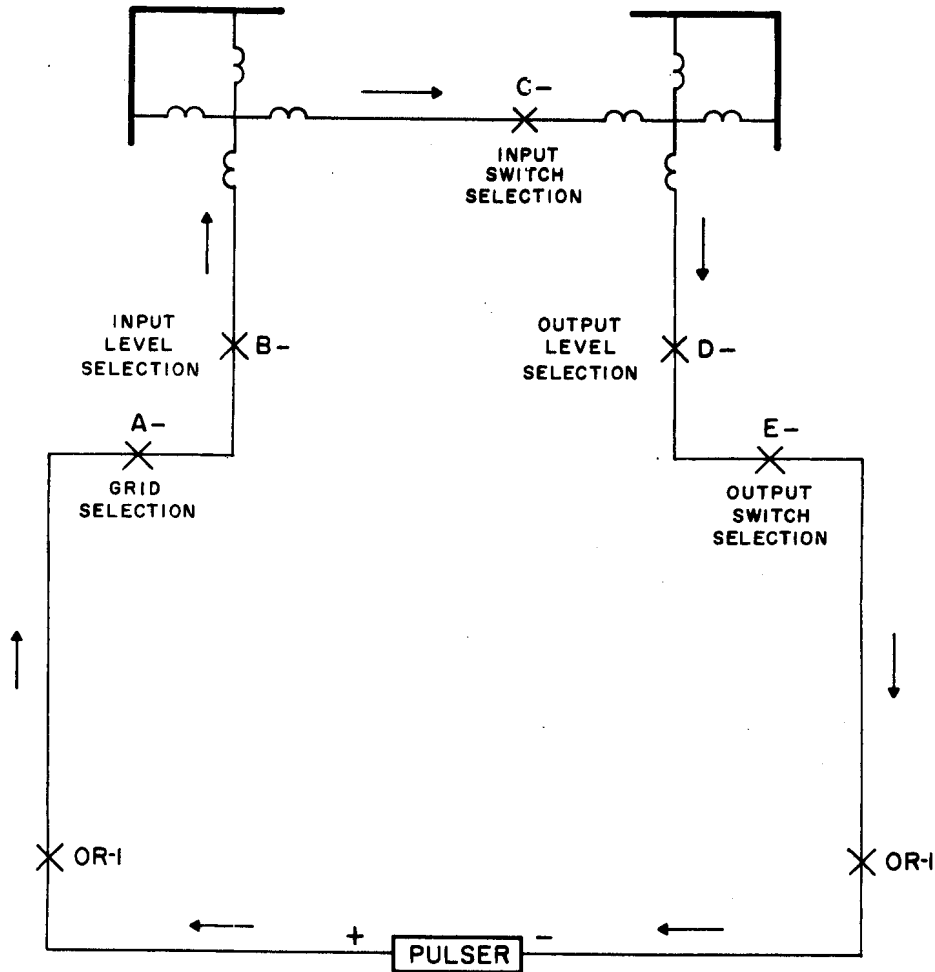
Figure 9-75   TSF - Connect Pulse Path

For a fully equipped LLN or TLN, either a plug or a connector is used to terminate the 16 junctors that have the same switch number and the same switch level number. For instance, a plug is used to terminate the 16 junctors that come from level 2 of the 16 No. 6 switches that exist in the 16 grids of the four junctor switch frames in the LLN or TLN. Since there are eight switches in stage 1 of a grid and eight levels in each switch, there are 64 groups of 16 junctors. Of these 32 go to one JGF bay, 32 to the other. Of the 32 going to each JGF, 16 are terminated on plugs and 16 on jacks. Terminating one half of the junctors in a vertical file on plugs and one half on connectors provides the flexibility needed to interconnect the frames within the switching network.

Figure 9-76 Typical Junctor Grouping Frame Layout

JGF bays are always added in pairs up to eight pairs. For each pair, one bay is added to the left and one to the right of the bays already installed.
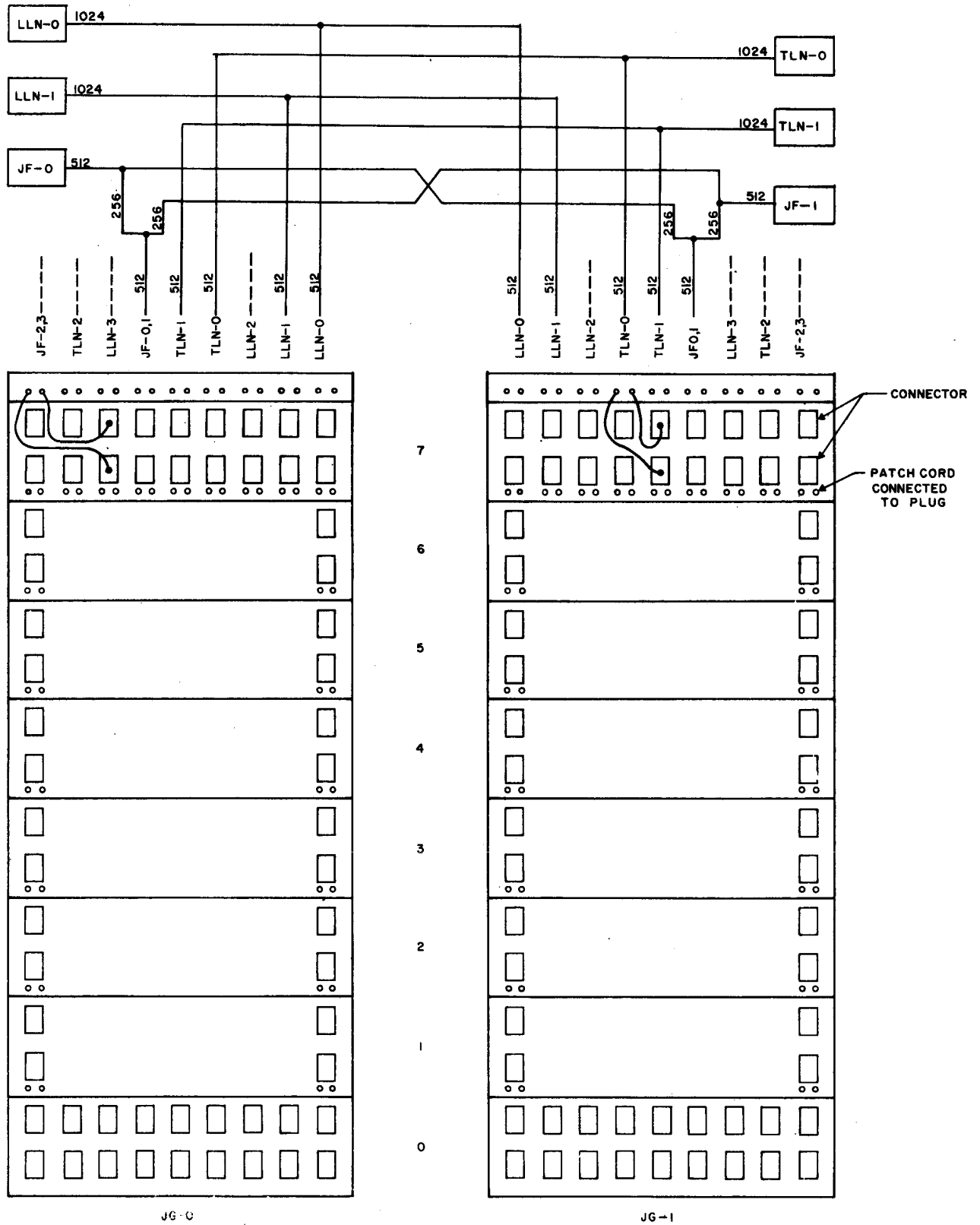
Except in rare instances, a cord is always plugged into a connector on the same shelf level. When two bays are involved in the connection, both must be in the same half of the line-up of JGF bays.

9.11 JUNCTOR, TRUNK, AND SERVICE CIRCUITS

A. GENERAL

Junctor, trunk, and service circuits have the following common characteristics:

(a) They are used to complete and supervise paths established through the switching network.

(b) They have very little, if any, autonomy. With very few exceptions, relays within these circuits operate only under the direction of the central (CC) via a signal distributor (SD) or central pulse distributor (CPD). Via a scanner, CC detects any change in the trunk or loop conditions that result from relay operations or from actions by a customer or a distant office.

The junctor circuit is used only in talking paths for intraoffice calls and has both ends connected to line link networks.

A trunk circuit is a switching circuit at one end of a trunk. (A trunk is a communication channel between two switching machines.) Trunk circuits are used to complete interoffice or operator calls. The trunk circuits of the No. 1 ESS are considerably simpler than those of electromechanical systems. Their functions are limited mainly to transmission and supervision. All other functions of conventional trunks such as pulsing, charging, timing, etc. are delegated either directly to the stored program control or to the service circuits which in turn are under program control.

Service circuits are auxiliary circuits connected through the network to lines or trunks, as required. They perform functions which can be handled more economically by a few special circuits than by providing additional equipment in each trunk.

All junctor circuits are on plug-in units mounted on junctor frames. Most trunk circuits and some service circuits are on plug-in units mounted on universal trunk frames.

The plug-in design imposes certain restrictions on the size of the circuit and on the maximum number of scan and distributor points per plug-in unit (four scanpoints, six SD points, no CPD or master scanner (MS) points.) Trunk and service circuits that do not lend themselves to the plug-in design are built on 25-inch mounting plates and installed on miscellaneous trunk frames; they are known as wired-in units.

B. JUNCTOR CIRCUIT FUNCTIONS

The junctor circuit is used to complete intraoffice calls. It includes a transmission circuit which provides ac coupling between the two lines and supplies talking battery individually to each line. It also includes two magnetic latching cut-through relays, CT1 and CT2. These relays connect battery after the network path has been closed and remove battery before the network path is opened, in order to protect the network ferreeds. Supervision of each line is provided by feeding the talking battery through an associated ferrod.

C. TRUNK CIRCUIT FUNCTIONS

In line with established practice, No. 1 ESS trunks are classified as outgoing, incoming, or 2-way depending on whether the local office, the distant office, or both can originate a call. They may be further classified by the type of supervision used, by special features provided, etc.

All connections between No. 1 ESS trunk circuits and service circuits are made through trunk link networks. At times, a trunk circuit must be reduced to a mere pair of wires to allow the associated service circuit to accept certain pulsing and supervisory signals; this is called the bypass state. In this state, all transmission elements and supervisory bridges are switched out to provide a clear metallic path through the network.

The trunk repeat coil of some trunk circuits can be switched in or out as required for local or tandem calls. Similarly, a compensating coil is inserted on local calls and bypassed on tandem calls to provide a fairly constant transmission level. A 900-ohm termination is connected across the trunk to keep associated repeaters from oscillating when the trunk circuit is open-circuited at the trunk link frame side.

Supervision of the local side of a trunk is effected in the local talking state by feeding battery and ground toward the customer's set through ferrod sensors. To supervise the distant office, arrangements which are compatible

with the trunk circuit at the far end are provided. For example, outgoing loop type trunks arranged for reverse battery supervision use a polarized ferrod sensor bridge to detect reversals. Where ferrods cannot be used directly as for sleeve lead supervision, relays are used to detect the supervisory signals. These relays then activate ferrod sensors.

D. SERVICE CIRCUIT FUNCTIONS

Examples of service circuits include transmitters and receivers for handling the signaling information needed to set up calls, ringing circuits for alerting called customers, tone circuits, and coin control circuits for collecting or refunding coins. Most of these circuits are mounted on the miscellaneous trunk frame.

E. CUSTOMER DIAL PULSE RECEIVER CIRCUIT

The customer dial pulse receiver circuit (CDPR) furnishes dial tone to the customer and detects digits pulsed from a dial set. A relay in the CDPR detects the dial pulses and supervises the customer's switchhook.

F. TOUCH-TONE RECEIVER CIRCUIT

The TOUCH-TONE receiver can detect TOUCH-TONE signals as well as dial pulses. It consists of a CDPR combined with a TOUCH-TONE calling detector circuit. (Information derived from a translation of the customer's line scanner equipment number tells the system whether to connect a CDPR or TOUCH-TONE receiver to the line.) A TOUCH-TONE signal involves two frequencies, one from a low group (697,770,852, or 941 hz) and one from a high group (1209,1336,1477, or 1633 hz). For each of the eight frequencies, there is a bandpass filter tuned to that frequency. Each filter output connects to a scanpoint which is activated when the corresponding resonant frequency is transmitted. A ninth scanpoint gives a signal present indication. When a call is originated from a TOUCH-TONE set, the line relay in the CDPR supervises the customer's switchhook as for a dial set. However, the relay will not respond to the relatively high frequencies of the TOUCH-TONE signals. These pass over the bridged connection to the TOUCH-TONE detector. If a legitimate signal is present, two of the eight frequency scanpoints in the trunk scanner will become active. If both of the tones received persist for a certain time interval, the SP scanpoint will become active. When CC detects an output from the SP point, it reads the eight frequency scanpoints to recognize the transmitted digit. The frequency scanpoints are not inspected again until the SP scanpoint goes down and comes up again for the next digit.

G. INTEROFFICE RECEIVERS

The completion of a call made over an incoming trunk requires that some form of receiver be connected to the trunk. The receiver must accept the particular type of pulsing being transmitted and convert it into a form that the CC can observe via a scanner. Three types of receivers, MF (multifrequency), DP (dial pulse), and RP (revertive pulse) are provided. A point of similarity in these circuits is that they all employ some form of detector whose outputs control scanner ferrods. If the associated trunk circuit is in the bypass state, the receiver must provide disconnect supervision.

H. TRANSMITTERS

The basic job of transmitters in No. 1 ESS is to pulse information to a terminating office to control switching equipment there. Four types of transmitters are provided: MF, DP, RP, and PCI (panel call indicator). The transmitter selected depends, of course, on the type of receiver at the distant office. However, if all the trunks in a primary route to a called office are busy, the system can select an alternate route using a different trunk group. The type of pulsing is not necessarily the same for primary and alternate routes. Information derived from a translation of the trunk group number tells the No. 1 ESS which type of receiver to connect to the outgoing trunk.

Before a transmitter can begin pulsing, certain preliminary tests must be made and certain signals received from the distant end indicating that it is ready to receive digit information. The type of trunk being served by the transmitter will determine which tests are to be performed. In general, loop-type trunks, including the trunk circuit at the distant office, arranged for reverse battery supervision will be tested for dc continuity and proper polarity. For nonloop-type trunks, a test of the network continuity between the trunk and the transmitter will be made. Polarity may or may not be tested. A short reversal of the loop known as a wink signal tells the No. 1 ESS that a receiver has been attached to the trunk at the distant. About 300 msec after the wink has been received, pulsing begins.

Whether or not the trunk loop is supervised depends on many factors. For example, on mf calls, once the wink has been received, pulsing will go ahead regardless of the trunk polarity. On dp calls, the transmitter may be required to monitor the trunk loop for polarity changes to be interpreted as delay dial, stop dial, etc., as determined by the program. At any rate, the facilities for supervising the trunk loop are built into the transmitters and are available, if required.

A transmitter does not supervise the calling line; this is done by the CDPR which normally remains connected to the line until outpulsing is finished. However, if the system cannot find an idle CDPR for a new customer, it searches for a connection which is in the outpulsing state. It then releases the CDPR involved and reconnects the associated line to its line ferrod which takes over supervision of the line. The released CDPR can now be connected to the new customer.

I. RINGING CIRCUITS

Two types of ringing circuits, regular and special, are provided in No. 1 ESS. The regular circuit performs the bulk of the ringing jobs and isused for calls to individual, 2-party, PBX, and coin lines. The special circuit provides coded, superimposed, reverting and rural ringing, and off- and on-hook ringback; it is provided in relatively small quantities for the special jobs that the regular circuit cannot handle. In order to connect the required type of ringing to the customer's line, the SD operates appropriate combinations of relays in the ringing circuit as ordered by the program. However, before ringing current is applied, the line is tested for a power cross (to 50 volt dc or 110/440 volt ac) and for a grounded tip or closed loop. Then, when ringing is connected, a continuity test is performed by monitoring the current flow. When the called customer answers, a dc path is closed operating a tripping relay which disconnects the ringing current. This is one of the cases where a trunk circuit relay operates independently of the system.

J. TONE OR RECORDED ANNOUNCEMENT CIRCUIT

Various standard tones an announcements are used to inform customers and operators of conditions encountered during the progress of a call. Access to any of these facilities is via a tone or recorded announcement circuit. Circuits of this type are located on the universal trunk frame. They are connected to the required tone or announcement equipment.

K. COIN CONTROL CIRCUIT

The coin control circuit (CCC) has three basic functions: to test for the presence of a coin, to collect a coin deposit, and to return a coin deposit. At some stage of every coin call, a CCC will be connected to the line to dispose of the initial deposit. If the called line is busy or does not answer, the coin will be returned when the calling line disconnects. If the called line answers, the coin will be collected upon disconnect or at the expiration of a timed talking period. At various times the CCC will be connected to determine whether an overtime coin deposit is present. The CCC also performs functions which minimize faulty operation. It drains the loop of residual electric charges by connecting a high resistance leak. It is also arranged to prevent false operation of the coin-box relay.

L. CONFERENCE CIRCUIT

The conference circuit permits a maximum of four customers to carry on a joint conversation through the No. 1 ESS network. It has four separate appearances or ports at the trunk link network. Each port has three talking states, local, trunk, and split. The local state is used when a customer of the local office is connected to a port and provides supervision of the customer line. The trunk state is used when a trunk from a distant office is to be connected to one of the conference circuit ports. In this state, supervision of the distant office is performed by the trunk circuit, not the conference circuit. In the split state, the line or trunk is connected to the port for supervision but not for conversation.

M. NETWORK ACCESS CIRCUIT

This circuit provides a means for connecting test circuits in the trunk and line test panel of the master control center to trunks or lines via a network path. Its primary function is to furnish a clear metallic path for voltmeter tests. It is also used as a holding circuit for a line showing a permanent signal and is arranged to hold a line with a leak condition that would not ordinarily hold a junctor circuit or trunk circuit.

N. MAINTENANCE

The junctor circuits and most of the trunk and service circuits are functionally tested while they are performing their normal jobs. A teletypewriter printout plus an alarm will inform the maintenance man when a circuit is in trouble. His subsequent action depends on the type of equipment (plug-in or wired-in) and on whether an incoming or outgoing circuit is involved. Incoming circuits must be made busy at the distant end. Outgoing circuits or service circuits which are selected by the No. 1 ESS are made busy via a teletypewriter message. If the circuit is in trouble is part of a dual unit, the mate circuit must also be made busy. This is true for both incoming and outgoing circuits. If the circuit in trouble is of a plug-in type, it will probably be removed and replaced by a good unit. In the case of wired-in circuits, techniques similar to those presently used by telephone office maintenance personnel will be used to clear the trouble.

9.12 MASTER CONTROL CENTER

A. GENERAL

Communicating between the No. 1 ESS and its operating personnel is achieved by the following means:

(a) Conventional or relay controlled office alarm systems.

(b) Local alarm circuits, display lamps, and power removal switches it the individual system units.

(c) Teletypewriters which may be in the same or other offices, visual displays, and manual controls at the master control center (MCC).

Whenever trouble is detected by a local alarm circuit, the office alarm system alerts the maintenance man; by means of pilot lamps, it directs him to the faulty equipment unit. Most troubles, however, are detected by the system under program control. In this case, the office alarm system directs the maintenance man to the MCC.

For a locally detected trouble, the alarm is retired at the faulty unit by removing power. For a system-detected trouble, the alarm is retired at the MCC where a diagnostic printout is given at the teletypewriter. Using this printout, the maintenance man consults a dictionary to obtain the location of the fault.

The teletypewriters are used by the operating personnel to type into the system recent changes of translation information, requests of various types, etc. The system, in turn, uses the teletypewriters to print out test results, traffic information, permanent signal conditions, etc.

Additional facilities are provided at the MCC for storing AMA information on magnetic tapes, for updating the translation information contained in the program stores (PS), and for testing lines and trunks. Thus, the MCC represents the maintenance and administration center of the office.

The Master Control Center consists of five major sections:

1. Alarm display and manual control panel

2. Line and trunk test panel

3. Teletypewriters

4. AMA recorder

5. Memory card writer

B. ALARM DISPLAY AND CONTROL PANEL

The alarm display and control is the centralized control point for the No. 1 ESS. In addition to a number of rotary switches, the panel contains various lamps and keys of either the locking or nonlocking type. In each key, a lamp mounted in the spring pile-up behind a transparent button serves as a visual indication of an operated and locked position. A locked key is restored to normal simply by pushing back to its regular position.

1. System Alarm

   All system detected troubles result in an audible alarm and either a MINOR or MAJOR lamp indication. The alarm is retired by operating the ALARM RELEASE key at the bottom right of the sloping panel.

2. Status Display of System Units

   The lamps in this group display the status of individual units or groups of units. Each signal processor (SP) and each central control (CC) has two lamps: one is labeled TBL and lights when the

unit is in trouble; the other is labeled ACT and lights when the unit is in active status. Each PS has a lamp that lights when the store is out of service. Two lamps are provided for the line switch frames. Similar considerations apply to the other groups of units (junctor switch frames, trunk switch frames, etc.)

3. Signal Processor Control

By depressing the nonlocking STOP or ST key, the operating personnel can stop or start the SP community previously selected by depressing the SELECT COMMUNITY locking key A or B. Each SP has two lamps: the STOP lamp lights when the SP has been stopped and the POWER lamp remains lighted as long as the power is on.

4. Traffic Control

(a) Emergency transfer: The EMERGENCY TRANSFER key, when operated, causes certain high-priority customers to be connected to the DSA or toll switchboard via previously assigned outgoing trunks. When the transfer of lines is carried out by the operation of appropriate relays, the EMERGENCY TRANSFER lamp is lighted and a major alarm is given.

(b) Line load control: During an extremely busy service period, the system may find itself running out of time and unable to handle the traffic. Under such conditions, the system lights the MAIN OVERLOAD lamp and sounds the minor alarm. By depressing the LINE LOAD CONTROL key, the operating personnel can request the system to institute line load control, whereby some nonpriority customers are denied service. The number of customers to be denied service increases with the degree of overload.

The system carries out the request for line load control only if an overload condition does exist. The LINE LOAD CONTROL lamp is lighted and a major alarm is given.

(c) Toll network control: By depressing the TOLL NET. CONTROL key, the operating personnel can request the system to deprive all but high-priority customers of access to selected toll trunk groups. Regardless of the load, the system carries out the request for toll network control, lights the TOLL NET. CONTROL lamp, and gives a major alarm. In addition, if an over load exists, line load control is automatically instituted.

5. Status

This group contains miscellaneous displays as follows:

(a) MULT TBL - This lamp lights whenever the system detects that:

    (1) A trouble exists in the active CC and the standby CC is already in trouble,

    (2) A complete copy of program and translation information is not available, or

    (3) A complete copy of CS information is not available.

(b) DIAGNOSIS IN PROGRESS - This lamp lights when-ever an automatic diagnosis of some system unit has been started.

(c) SYS OFF NOR - This lamp lights when any key or switch on any other frame control panel is not in the normal position.

(d) PERIPHERAL CONTROL - This lamp indicates parrial or total loss of control of the peripheral bus system.

(e) MISC TBL - This lamp refers the operating personnel to the teletypewriter for a report on a miscellaneous alarm. Miscellaneous alarms include power crosses on customer lines, false cross and ground failures, etc.

6. Bay Control

The PWR ALARM lamp indicates a power failure at the alarm display and control frame. Depressing the PWR OFF key removes power from the frame. A lighted OFF NOR lamp indicates an operated key or switch on the alarm display and control panel.

7. Emergency Action

By depressing the SELECT ACTIVE key for CC0 or CC1, the operating personnel can force the selected CC to acquire active status. By depressing the SELECT PS BUS key for bus 0 or 1, the operating personnel can force the specified PS bus to work with the active CC. By means of the PROGRAM STORE STATE CONTROL rotary switch, the operating personnel can select one of eight states or configurations of PS to work with the active CC and the selected PS bus. In each of the eight states, one or more PS's are forced out of service. The remaining stores still contain a complete copy of program and translation information.

8. Repeated Time-Outs

An emergency action (EA) circuit in CC guards against trouble conditions that impair the system's ability to remove from service one or more faulty units and to assemble the remaining units in a workable combination. The EA circuit forces, in sequence, different combinations of buses, PS's and CC's to restore normal system operation. If the EA fails to assemble a workable combination, a signal is sent to the MCC; this signal:

(a) Opens the fail-safe loop to the remote maintenance teletypewriter.

(b) Lights the red REPEATED TIME-OUT lamp.

(c) Activates the MAJOR ALARM.

The EA circuit can be disabled by operating the DISABLE TIME-OUT key.

9. Error Detection

There are two modes of error detection, join and disjoin, in CC. In the join mode, both CC's perform an error correction or a reread of store information when either CC detects an error. In the disjoin mode, each CC performs an error correction or a reread as required by its own error detection circuits. The DISJOIN lamp is lighted when the active CC is in the disjoin mode. The DISJOIN and JOIN keys can be used to force the active CC into the disjoin or join mode, respectively.

10. Central Control and Bus Isolation Control

The lamps in this group display how the CC's are associated with the duplicated buses for PS's, CS's, peripheral units, and central pulse distributors (CPD). For each CC and each PS or CS bus, the SEND lamp lights when CC is connected to send information on the bus. Similarly, the RCV lamp lights when CC is connected to receive information from the bus. For each CC, the PWR lamp is on as long as CC has power applied to the cable pulsers associated with the bus.

11. Answer Bus

The two lamps indicate whether the active CC is using scanner answer bus 0 or bus 1. By setting the rotary switch to the BUS 0 or BUS 1 position and by depressing the SET MAN. key under EMERGENCY ACTION, the operating personnel can force both CCs to use bus 0 or 1.

12. Store Display

By setting the rotary switch to one of the position PS0 to PS5, the operating personnel can request that the association of a specified program store with CC-PS buses 0 and 1 can be displayed on the eight lamps. When lighted, the four lamps for bus 0 have the following meanings:

(a) TBL - Sending and receiving operations over bus 0 for the specified store are inhibited.

(b) H OUT - The specified store transmits any word read from its H half to bus 0.

(c) IN. - The specified store receives information from bus 0.

(d) G OUT - The specified store transmits any word read from its G half to bus 0.

The four lamps for bus 1 have similar meanings. By setting the rotary switch to the CALL STORES position, the operating personnel can request a display for a CS whose identity is specified by means of a teletypewriter input message.

13. Peripheral Mode

In the normal mode of operation, only one of the peripheral address buses is used, as selected by the F_{14} bit of the F register in CC. Two other modes are available for testing purposes. In mode A, the active CC transmits over both buses. In mode B, the active CC transmits over the bus selected by the F_{14} flip-flop, and the standby central control transmits over the other bus.

14. Central Pulse Distributor Mode

In the normal mode of operationg, only one of the two buses between CC and the CPD is used, as selected by a CPD B flip-flop in CC. The state of this flip-flop can be changed under program control. Two other modes of operation are available for testing purposes. In mode A, the active CC transmits over both buses. In mode B, the active CC transmits over the bus designated by the CPD B flip-flop; the standby CC transmits over the other bus.

15. Program Interrupt Control

The operating personnel can request that a program interrupt take place and that some action be carried out as selected by one of six INTERRUPT REQUEST keys labeled A to F. Key A, for instance, requests system reinitialization.

16. Program Display

24 lamps can be used to display the contents of memory locations and scanner readouts. The display is requested by means of a teletypewriter message specifying the location of the desired information and under what conditions the information is to be displayed.

C. LINE AND TRUNK TEST PANEL

GENERAL

The line and trunk test panel contains the facilities for (a) the removal from service and the testing of outgoing trunks, service circuits, and customer lines and (b) the disposition of permanent signals.

A TOUCH-TONE set is associated with the master test line. This line has an appearance at the line link network and requests service in the same manner as a customer line. Using the TOUCH-TONE set, the operating personnel keys into the system the equipment number of the circuit to be tested. Instructions for various tests are specified by the operation of the locking keys of the type previously described for the alarm, display, and control panel. These keys are observed by the system via the MS. The status of the circuit under test and the results of the tests are displayed by lamps controlled via a CPD or an SD. Meters and associated lamps and keys are provided for voltmeter and transmission tests.

Through the network, the master test line can be connected to any trunk or service circuit to be tested. Thus, it is not necessary to provide OGT (outgoing trunk) jacks for every trunk in the office at some test and control panel, as for existing central offices. An outgoing trunk can be marked busy in temporary memory by depressing a MAKE-BUSY key at the test panel. An audible alarm alerts the operating personnel if customer service will be adversely affected by the number of circuits removed from service. Through the network and an access trunk, any trunk or service circuit can be connected to the voltmeter or transmission test facilities. Likewise any customer line can be connected through the network and access trunk to the voltmeter test facilities.

D. TELETYPEWRITERS

GENERAL

Teletypewriters are used as the primary means of communication between the operating personnel and the No. 1 ESS. Through them, the operating personnel can request specific system actions, and the system can report back on these actions or on various internal conditions.

A number of teletypewriter channels are provided for an office. Each channel includes a tip and ring loop and the hardware needed for transmitting serially teletype signals. Each channel is equipped with a Teletype Corporation Model 35

teletypewriter. One maintenance teletypewriter is always
located at the MCC. The other maintenance teletypewriter may
be located at another place within the office or at a remote
maintenance center if the office is to be unattended. The
number of channels in a system depends on the needs of the
operating company.

A typical teletypewriter system with five channels is
shown in Figure 9-77. Teletypewriter No. 1 is located at the
MCC; teletypewriter No. 2 is located at the remote maintenance
center. When the office is unattended, the relaying of ESS
alarms is accomplished via this teletypewriter channel. A
special sequence of signals over the channel activates the
alarm system at the remote maintenance center. The operating
personnel retires the alarm, consults the teletypewriter print-
out for the nature of the trouble, and takes the necessary
action. Should the No. 1 ESS office become unable to communi-
cate with the remote center, a fail-safe relay releases,
opening the teletypewriter loop. An open loop activates a
major alarm at the remote center indicating that immediate
attention is required. Another channel is provided for recent
changes with a teletypewriter at an assignment bureau or at
an electronic data processing center. A fourth channel termi-
nates at a test bureau. It is a one-way channel used to
report automatic line insulation test (ALIT) results and
permanent signal data. The maintenance channel may be used
for this purpose, if the test bureau is in the electronic
office. Teletypewriter No. 5 is used to transmit traffic
information to a traffic data center. The No. 1 ESS can also
communicate with remote teletypewriters via the toll voice
networks (mechanized TWX service).

1. TTY Transmit and Receive Unit

A buffer, called a transmit-receive (TR) unit, is
inserted between CC and the teletypewriter. The
TR unit operates in two modes: transmit and receive.
In the transmit mode, the CC sends seven bits (1
character) in parallel via the peripheral address
bus to the TR unit every 100 msec. With an average
of six characters per word, information is trans-
mitted at the rate of 100 words per minute. The
TR unit converts the information received in par-
alel for each character into serial form and closes
and opens the teletypewriter loop in the required
sequence during 11 consecutive intervals; these are
called marking or spacing intervals depending on
whether the loop is closed or open, respectively.

In the receive mode, the TR unit detects the mark-
ing and spacing intervals in the teletypewriter
loop and assembles them into a single character of
seven data bits. The seven bits are detected by CC
in parallel via seven master scanner points.

Several signaling techniques can be used for serial
transmission over the teletypewriter loop. Whenever
feasible, private line communication employs 20-ma
dc signaling with marking and spacing intervals.
If signaling to a remote point is not feasible on a
dc loop basis, two 105A data sets are inserted in
the loop: one at the TR unit and the other at the
remote teletypewriter. The 105A data sets convert
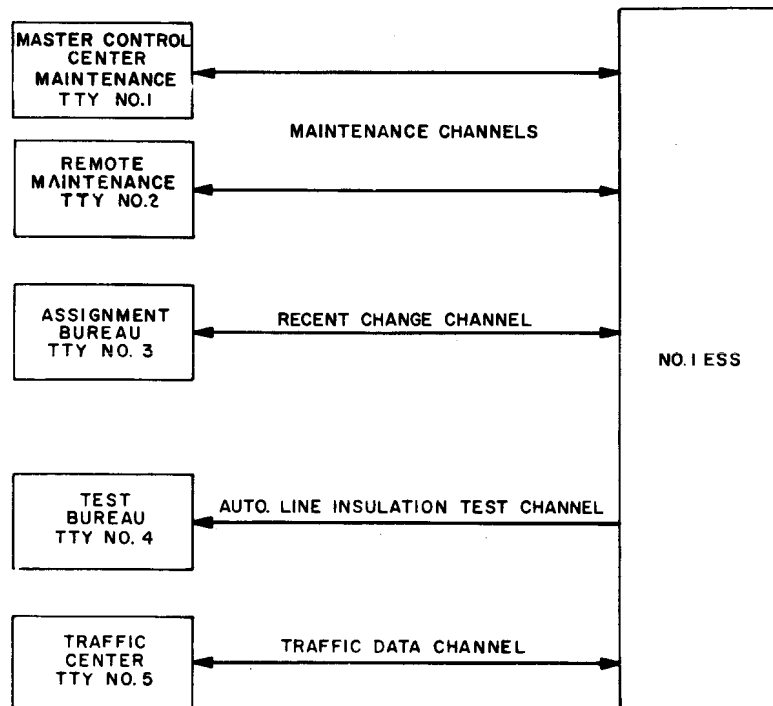the dc signals to frequency shift signals or vice
versa.

Figure 9-77   Typical Teletypewriter Channels

E. AUTOMATIC MESSAGE ACCOUNTING RECORDER

GENERAL

The automatic message accounting (AMA) recorder is used to store customer charging information on magnetic tapes. These tapes are then forwarded to a data processing accounting center where they are used to compute customer charges. Usually a single 2400-foot reel of tape is sufficient to store all the charging information for one day. A duplicate AMA unit is provided for reliability and continuity of recording. Additional recorders can be installed when necessary.

1. Apparatus Elements

Each recorder consists of a tape transport and an associated controller. The tape transport is mounted on a standard 25-inch relay rack. The front hinged dust cover is of plexiglass for veiwing of the control buttons, tape loop, and reels. Separate write and read heads are used for writing and reading the information on the half-inch 9-channel tape.

2. General Handling of Information

The system assembles all the charging data pertaining to a call into a single entry which is stored temporarily in a tape buffer area in a CS. A typical entry requires nine CS words. In some instances, an entry may require as many as 16 words. The tape buffer area consists of a 100-word block. When enough entries have been accumulated to fill this block, the information is transferred to the AMA recorder.

The AMA information is duplicated in two physically distinct CS's. Thus, there are two complete copies of the data accumulated in the 100-word block. The CC has the ability to obtain data from either copy and send it to either AMA recorder over either peripheral unit bus.

F. MEMORY CARD WRITER

1. General

In addition to program instructions, the Program Stores (PS's) contain various types of translation information. Any changes that supersede part of this translation information are entered initially in a call store (CS) area called the recent change memory. Whenever the system requires a particular item of translation information, it searches for it through the recent change memory. If the system does not find the desired item in the temporary memory, it refers to the translation section of the semipermanent memory.

When enough entries have been accumulated to fill the recent change memory, the memory card writer (MCW) is used to prepare, under program control, a new set of twistor cards that incorporate the changes. The recent change memory becomes available to accommodate subsequent changes until it is again necessary to prepare a new set of cards.

2. Apparatus Elements

Card Loader

Each PS contains 16 modules. Each module, in turn, contains 128 twistor cards, each with 64 rows of 44 small magnets. The cards of a module are handled as a unit. All 128 cards are inserted into, or withdrawn from, a module by a motor-driven magazine or loader. The loader is used to transport the cards between the card writer and the PS's. After the appropriate information has been written on a full module of spare cards, the latter is substituted for a module in a PS. A card loader weighs about 35 pounds when full and about 18 pounds when empty.

The cards in a module are divided into two groups: 64 left-hand cards and 64 right-hand cards. The cards are alternately right-hand and left-hand with the magnet sides facing each other. When a full loader is clamped to the MCW, one half of the cards have their magnets faced up and one half faced down. In order for either the left- or right-hand cards to be mounted with their magnets faced up,

two mounting positions, PASS A and PASS B are provided. In the PASS A position, 64 cards are processed. The loader is then manually inverted to the PASS B position and the remaining cards are processed.

3. Card Writing Unit

The MCW includes the card writing unit. This mechanism withdraws one card at a time from the loader. It writes information on the card one word at a time, by passing a 45-section writing head across the surface, and returns the card to the loader. The latter is automatically moved up and a new card is withdrawn. It takes about four seconds to withdraw a card, write the information, and reinsert the card. The time required for one pass of all right-hand or left-hand cards is about 4.5 minutes.

4. Method of Operation

The MCW is capable of sequentially handling and writing a full module of 128 cards in two passes of 64 cards each. Before writing a word, the card writer requests the necessary information from the system and stores it in a 44-bit register. Operation is automatic during each pass. Local audible and visual alarms indicate when attention is required.

The MCW is operated from a control panel which contains a number of lamps and pushbuttons.

The operating personnel initiates a card writing operation by typing a message at the teletypewriter. The system responds with a message listing all the translation modules for which there are entries in the recent change area. The system will still accept recent changes during card writing. Via a teletypewriter message, central control is informed of the identity of the module to be written. A loader containing spare cards is clamped on the card writer. The spare cards just processed are now used to replace an associated module of cards in some program store.

The operator removes the module of cards from the PS using an empty loader. He then inserts the newly written cards using the same loader that transported them to the card writer. Their information content is verified before the PS is restored to service.

If the verification is not successful, the new cards must be replaced by the old set. The teletypewriter is then consulted for a printout of the verification errors. Depending on the nature of the results, several procedures may be followed: (a) the entire set of cards may be rewritten, (b) maintenance procedures may be instituted to locate the cause of a gross failure, or (c) the corrections for the errors found during verification may be entered as recent changes in temporary memory.

9.13 METHOD OF OPERATION - NO SIGNAL PROCESSOR

Whenever it is stated that central control (or the system) performs some function, it must be understood that this function is carried out by central control (CC) under the direction of the program. It should also be remembered that the network map, the path memory, the busy-idle bits, the various call registers (originating, ringing etc), the peripheral order buffers (POB's), the hoppers, etc, are all areas in call store (CS) memory.

A. DIAL TONE CONNECTION

Assume that a call is originated by an individual line (L_0) that transmits dial pulses to the central office. During the 100-msec supervisory scan of lines, when central control (CC) requests a reading of the row containing the scanpoint of L_0, it detects a mismatch between the scanner reading and the associated line busy-idle word on the call store (CS). This word contains the previous scanner reading for the row containing L_0. Since the line scan supervises for originations only, the mismatch indicates that at least one line has gone off-hook. (Assume that L_0 is only one.) Dial tone must now be given to the customer via a customer digit receiver to indicate that he can start dialing. To request this, the CC enters in the line-service-request-hopper of the CS a line scanner number (LSN) which completely identifies the scanpoint associated with L_0.

Milliseconds later, CC unloads the LSN from the line-service-request-hopper and converts it into a line equipment number (LEN) which completely identifies the terminal appearance of L_o at the switching network. Then, CC hunts for and seizes an idle senior originating register (ØR) and records in it the LEN.

Next, CC converts the line equipment number into the program store address of the LEN translation information for the calling line (L_o). This information gives the line class, the directory number (DN), and the type of digit receiver to be connected to the line. It also indicates whether the line has special originating features, such as abbreviated dialing. CC stores the translation information in the ØR.

Knowing from the translation that line L_o transmits dial pulses, CC hunts for an idle customer dial pulse receiver (CDPR). Having seized a CDPR, CC searches the network map and selects a path from the orignating line to the dial pulse receiver. (See Figure 9-78 - Network Connection.)

CC loads a peripheral order buffer (POB) with the information needed to establish the connection. In addition, the POB is used to store the orders for all subsequent peripheral actions associated with giving dial tone. At 25-msec intervals, the POB is unloaded.

Before the paths are closed through the LLN and TLN, a false cross and ground (FCG) test is performed. After the paths are closed, a power-cross test is performed; if L_o is a party line, a party test is performed.

Via the signal distributor (SD), CC operates the dial tone relay in the CDPR to give dial tone to the calling customer. The transfer of supervision from the line scanner to the trunk scanner is checked by verifying that L_o appears off-hook at the CDPR.

Finally, the junior originating register (JØR) associated with the CDPR is made ready to count pulses. The address of the ØR is stored in this JØR.

The dial tone connection job is now complete. In addition to the LEN of the calling line, the originating register holds the identity of the junctor and the CDPR used in the connection. This information makes it possible to take down the connection if the call is abandoned. It usually takes less than 300 msec to return dial tone to the calling customer. Figure 9-78 summarizes the description of the dial tone connection.

When CC detects an origination during a 100-msec line scan, it enters the **LEN** of the originating line (L_O) into the line-service-request-hopper.

CC unloads entry from line-service-request-hopper.

CC hunts for $ØR$.

LEN is translated to class information which is stored in $ØR$.

CC hunts for a CDPR.

CC hunts for path in network map.

POB is loaded with;

(a) Link address for line-to-CDPR connection.

(b) SD and scanner addresses for FCG test.

(c) SD and scanner addresses for power-cross test.

(d) SD address to operate dial tone relay.

(e) Scanner address to check transfer of supervision.

Network path information is recorded in $ØR$ for a possible abandonment.

$JØR$ is initialized.

Dialing connection is completed. Dial pulse scanning starts.
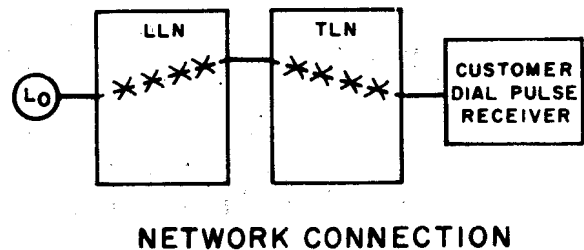

NETWORK CONNECTION

Figure 9-78   Summary of Dial Tone Connection Including Network Connection

B. INTRAOFFICE CALL

This description covers a call between two individual lines served by the same CC. The calling line L_0 is assumed to transmit dial pulses to the CC.

The actions to give dial tone to the calling customer are completed as previously described. Dial tone is removed after the first pulse of the first dialed digit. Dial pulses are counted and recorded in the $JØR$. As each digit is completed, it is transferred to the $ØR$ via the dial pulse digit hopper.

When the first digit is completed, CC determines that it is neither a 0 nor a 1. Next, the second and third digits are detected and recorded. A translation of the dialed office code informs CC that an intraoffice call is in progress and that seven digits are expected. This information is recorded in the ØR.

Upon completion of the seventh digit, CC converts the directory number of the called customer line (L_0) to a program store address. Here it finds the LEN and the terminating class features of the called line.

CC converts the LEN of the called line to the location of the line's busy-idle bit in the CS. This bit tells CC that the called line is idle; the bit is marked now to indicate that the line is busy.

CC seizes a ringing register (RR) in the CS to record the information it needs during the ringing phase of the call.

From the network map, paths are selected between L_0 and an audible ringing tone circuit and between L_0 and a ringing circuit Figure 9-79A. The appropriate orders are loaded into a POB. Also, a path from the calling to the called line is selected, reserved, and recorded in the RR.

The customer dial pulse receiver is released; the network path, the OR, and the JOR are marked idle in memory. The CC records in the ringing register the junctor network number of the junctor reserved for the talking connection. It also records the network location, or trunk network number (TNN), of the ringing and audible ring circuits.

While ordering the setting up of the ringing connection, CC also requests that the following checks be made:

(a) Power cross

(b) Continuity

(c) Pretrip

(d) Ringing

Every 100 msec, the ringing circuit is scanned for answers; the audible ringing circuit is scanned for a possible abandonment.

When the called line answers, ringing is automatically tripped by a relay in the ringing circuit. The ringing and audible ringing tone circuits are released and the temporary memory is brought up to date by CC.

A RINGING CONNECTION
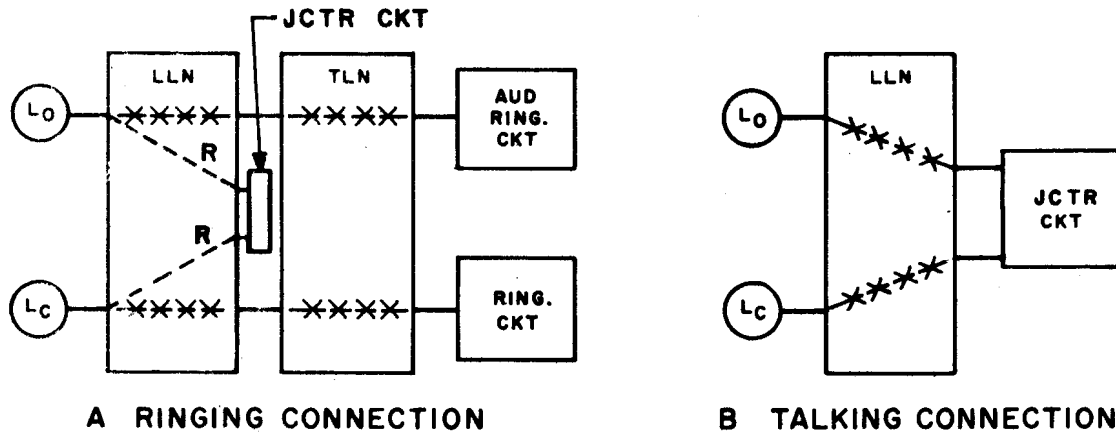
Dial tone is connected.

Dial tone is released after first pulse of first digit.

After the third digit, the office code translation indicates that the call is intraoffice and seven digits are expected.

The seventh digit is recognized by CC.

Dialed directory number is translated to LEN.

LEN is converted to the location of called line's busy-idle bit. Line is found idle.

CC seizes RR.

CC hunts through network map for paths between (a) L_O and audible

B TALKING CONNECTION

ring circuit, (b) L_c and ringing circuit, and (c) L_O and L_c.

CDPR J.ØR and ØR are released.

CC loads a POB with orders to connect audible ring to L_O and ringing to L_c - Talking path from L_O to L_c is reserved.

Power Cross Test, Continuity Test, and Pre Trip Test are made. Then ringing is applied.

When answer is detected, the ringing and audible ring circuits are released.

Reserved path from L_O to L_c is set up.

RR is released. 100-msec junctor scan supervises for disconnect.

C CALL SUMMARY

Figure 9-79   Summary of Intraoffice Call Including
Network Connection

The reserved talking path between L_O and L_c is now established. (See Figure 9-79B.) The transfer of supervision to the junctor scanner is verified.

CC releases the ringing register (RR), and brings the path memory up to date.

When the 100-msec junctor supervisory scan detects a change to on-hook by either the calling or called customer, an interval of 200 to 300 msec is timed. This is done as a safeguard against momentary on-hook conditions, or "hits", which would cause disconnect actions to be performed prematurely. When this hit timing is completed, a disconnect register is seized.

The call is under calling party control but a timed-release feature is provided in order to prevent the calling customer from holding the called line out of service indefinitely by failing to hang up the receiver. After the 200 to 300 msec time-out for the called line, the system times an interval of 10 to 11 seconds if the calling line remains off-hook. During this interval, if the called customer returns to off-hook, the network path is left established. If an on-hook is detected from the calling line or if the time-out occurs, the connection and the disconnect register are released.

C. OUTGOING CALL

This description covers a call from a No. 1 ESS customer to a line in a distant office. The calling customer is assumed to have an individual line that transmits dial pulses to the central office. The pulsing required between the No. 1 ESS and the distant office is assumed to be multifrequency (mf).

The actions to give dial tone to the calling customer are completed as previously described. Dial tone is removed after the first pulse of the first dialed digit. Dial pulses are counted and recorded in the JØR. As each digit is completed, it is recorded in the ØR.

When the first digit is completed, CC determines that it is neither a 0 nor a 1. Next, the second and third digits are detected and recorded.

The office code translation indicates than an outgoing call is being dialed and that outpulsing shall start after all seven digits have been received. (This is true, because of the assumed mf signaling. In the case of dp or rv signaling, outpulsing is usually started after the fifth digit has been received.) The office code translation provides also a route index number which is stored in the ØR and is used to derive routing, alternate routing, and signaling information.

When the last digit is received, CC hunts for and seizes an outpulsing register. Another hunt seizes an outgoing trunk (OGT). The identity of this trunk, the type of supervision, and the number of digits to be transmitted are recorded in the outpulsing register. An mf transmitter is

seized and its identity recorded in the outpulsing register. This register contains also the identity of the originating register that holds the digits to be outpulsed.

The calling line is still being supervised via the trunk scanner at the CDPR. Should this receiver be needed for another origination, the calling line's ferrod would be restored and supervision would be via the line scanner.

The CC loads a POB with the orders to establish the path between the OGT and the mf transmitter Figure 9-80A. The information that identifies a reserved path between the calling line L_0 and the OGT is stored in the outpulsing register. The OGT circuit is put in a bypass state and a seizure signal is sent to the distant office. Trunk continuity to the distant office is checked at the mf transmitter. If the check is successful, a "wink" is returned from the distant office. The digits in the $\emptyset R$ are transferred to the junior outpulsing register associated with the mf transmitter. Bursts of tones are then transmitted to identify the called line in the distant office. The CPD is used to operate and release relays that control the tone signals.

At the completion of outpulsing, CC releases the transmitter. The supervision of the outgoing trunk is transferred from the transmitter to the trunk circuit. The previously reserved network path between the originating line and the OGT is established and checked. (Figure 9-80B).

The CDPR, the $\emptyset R$, the J$\emptyset R$, and the outpulsing register are all released. Every 100 msec via the trunk scanner, the OGT is scanned for answer.

When the called customer answers, the trunk busy-idle bits are marked to the talking state.

When the 100-msec trunk supervisory scan detects a change to on-hook on the OGT, the system starts timing an interval of 200 to 300 msec as a safeguard against a hit. When hit timing is completed, a disconnect register is seized. If the calling line went on-hook first, the connection is released and disconnect supervision is sent to the far end. The trunk is not idled until distant office returns on-hook supervision. If the called line went on-hook first, a timed-release period of 10 to 11 seconds is initiated. If the calling line goes on-hook during the 10 to 11 seconds or if a time-out occurs, the connection is released.

The disconnect register is released after timing a guard interval of 750 msec during which the outgoing trunk cannot be reseized. This allows enough time for all the relays in the distant office to release.

A. SIGNALING PHASE

B. TALKING
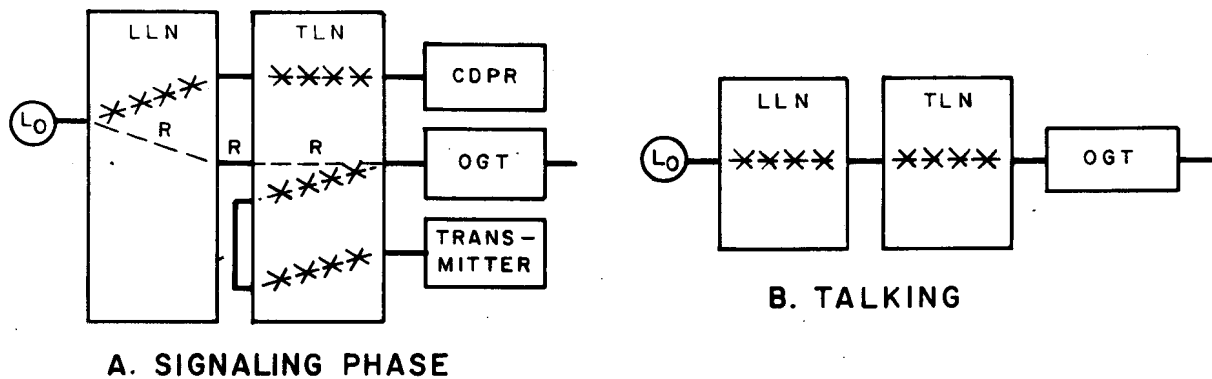
Dial tone is connected.

After the third digit, the office code translation indicates that the call is interoffice and supplies the route index number.

Completion of dialing is recognized.

CC hunts for:
    (a) outpulsing register.
    (b) outgoing trunk (OGT).
    (c) transmitter.
    (d) path from transmitter to outgoing trunk.

CC loads a POB with information (a) to connect transmitter to OGT and (b) to perform FCG test.

Outpulsing register is loaded with information identifying reserved path.

Outpulsing takes place.

CC loads a POB with orders (a) to release the CDPR, the transmitter and the associated paths, and (b) to establish the reserved path between L_0 and OGT.

The senior and junior originating and outpulsing registers are released.

When answer is detected, the busy idle bits of trunk are marked to indicate talking.

100-msec trunk scan supervises for disconnect.

Figure 9-80   Summary of Outgoing Call
Including Network Connections

D. INCOMING CALL

    It is assumed that the system is processing an incoming call to an individual line.

    During the 100-msec supervisory scan of trunks, when CC reads the row containing the scanpoint of the incoming trunk, it detects a mismatch between the scanner reading and the associated trunk Busy-idle word. The latter records the

previous scanner reading for that row. Among other things, the trunk scan supervises for incoming trunk seizures as well as outgoing trunk answers. Thus, CC cannot conclude from the mismatch whether a seizure or an answer has been detected. The trunk scanner number (TSN) of the trunk causing the mismatch is recorded in the trunk-service-request hopper because the trunk change is from on-hook to off-hook.

Milliseconds later, the TSN is taken from the hopper and converted to a unique program store address. The translation information stored there indicates that the trunk is incoming (which means that a seizure has been detected). It also specifies the TNN which identifies the network location of the trunk.

The CC seizes an incoming register (IR) and records in it the TNN. The CC converts the TNN into the program store address of the translation information for the trunk. This information is used by CC to determine the type of digit receiver (mf, dp, etc.) to be connected to the trunk, the number of digits to be received, and the type of supervision required. This information is recorded in the incoming register.

Knowing the type of digit receiver to be used, CC seizes an idle receiver and searches the network map for a path between the incoming trunk and the receiver. It loads a POB with the orders for the network controllers, the signal distributor, and the scanner to effect and check the connection. The path information is recorded into the IR.

The junior incoming register associated with the digit receiver is prepared to store the pulse count. The trunk circuit is put in the by-pass state and the start-dialing signal is transmitted to the distant office, which in turn transmits the last four digits of the called line's directory number (Figure 9-81A).

Upon completion of each digit, the pulse count is taken from the junior incoming register and via a digit hopper, is recorded in the IR that is administering the call. When the last digit is completed, the digits received are converted to the program store address of the directory number translation for the called line. A part of the translation is the line equipment number for the called line. The CC converts this LEN to the location of the line's busy-idle bit in the CS. This bit tells CC that the called line is idle. The ringing phase of the call starts as CC seizes a ringing register (RR) and then a POB. The incoming register is released.

A search of the network map results in the selection of a path from the incoming trunk to an audible ring tone circuit and from a ringing circuit to the called line; also a talking path between the incoming trunk and the called line is reserved. The information for all these paths is stored in the ringing register. The orders for the ringing connections are loaded into the POB (Figure 9-81B) with the signal distributor and scanner orders for a power cross test and a pretrip test.

Every 100-msec, the ringing circuit is scanned for answer. The incoming trunk is scanned for a possible abandonment.

When the called customer answers, ringing is automatically tripped by the ringing circuit. The ringing connections and the ringing register are released by CC. Answer supervision is returned to the originating office. The previously reserved talking path is established (Figure 9-81C); the temporary memory is brought up to date. The connection is now supervised via the trunk scanner for disconnect.

When the 100-msec trunk supervisory scan detects a change to on-hook on either the line or trunk side of the incoming trunk, the system starts hit timing (200 to 300 msec).

After the hit timing period, a disconnect register is seized. If the distant end has disconnected first, the trunk is made available for reseizure and a timed-release period of 10 to 11 seconds is started. During this time, the No. 1 ESS customer is being scanned at the trunk every 100 msec for disconnect. The connection is released when the No. 1 ESS customer disconnects or the timed-release period ends. Should the trunk be reseized in the meantime, the connection would be released immediately and the line would be supervised via the line scanner. If the No. 1 ESS customer remains off-hook beyond the timed-release period, the off-hook is treated as a new origination.

If the No. 1 ESS customer has disconnected first, when hit timing is completed, the distant office is notified of the disconnect. Then the No. 1 ESS starts timing a period of 35 to 45 seconds, waiting for the disconnect signal from the distant office. When the No. 1 ESS receives the disconnect signal or when the timing period ends, the connection is released. Figure 9-81 summarizes the description of an incoming call.

A. DIGIT RECEPTION PHASE

C. TALKING PHASE

B. RINGING PHASE
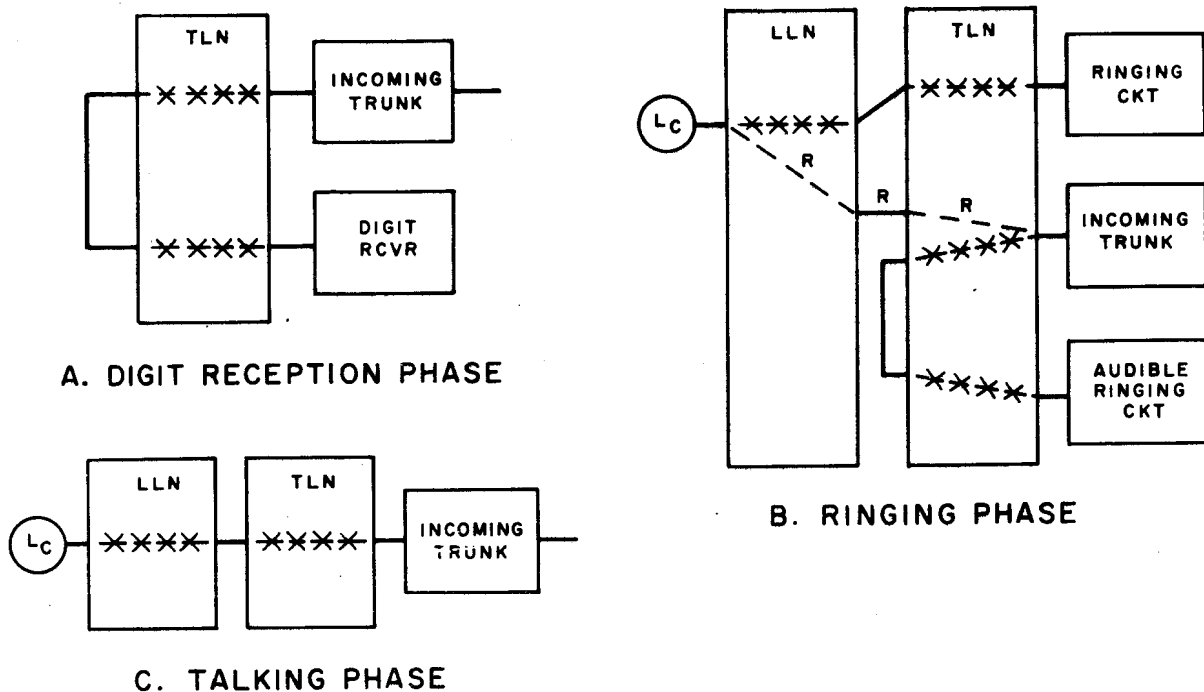
Translation of TSN identifies trunk as incoming, specifies its TNN.

CC hunts for and seizes an idle IR.

TNN is translated to the type of digit receiver (DR) and the number of digits to be expected

CC hunts for and seizes an idle digit receiver.

CC hunts for a path in network map from incoming trunk to DR.

CC requests the connection of the path by loading a POB with the necessary orders (Fig. A).

CC stores the TNN translation in IR.

Start-dialing signal is sent to distant office.

Junior IR is initialized

After the fourth digit is detected, the four digits are used to determine the LEN of the called line L_c.

CC finds that L_c is idle from its busy-idle bit and seizes a RR. The junior and senior IR's are released.

CC loads a POB with orders to connect ringing and reserve a talking path (Fig. B).

When answer is detected, talking connection is established, (Fig. C).

The RR is released

Figure 9-81   Incoming Call Including Network Connection

E. REVERTING CALL

A reverting call is a call between two customers who share the same line. Thus, both customers have the same line equipment number.

The system processes the call as a regular intraoffice call until it receives all seven digits and finds that the calling and called LEN's are the same. It knows then that a reverting call is in progress. Thereafter, the call is handled in one of the following ways, depending upon the option selected by the telephone company.

1. Operator Assistance

For flat or message rate customers, the call is routed to an operator over a recording-completing trunk. The operator recognizes that she must assist in the completion of a reverting call from the trunk group or from the reception of identification tone. She then requests the called number from the calling customer and instructs him to hang up, to wait long enough for the called party to answer, and then to go off-hook again. In the meantime, she dials the called number over a local toll switching trunk and when the ringing connection is set up, ringing is applied under her control. She makes sure that the call is terminated properly before making out the message rate ticket or leaving the call. Throughout the conversation, the call is supervised via the local toll switching trunk. After both parties disconnect, the connection is taken down and the trunk is released.

a. 2-Party Selective, 4-Party Semiselective, Divided Code Ringing

The system returns busy tone until the calling customer hangs up. The busy tone is removed and reverting ringing is connected. When any customer on the party line removes his receiver from the switchhook, ringing is removed and a talking connection is established to a holding trunk. When both customers hang up and the disconnect is detected at the holding trunk, disconnect timing is completed and the connection is released.

b. **2-Party Selective, 4-Party Full Selective, 8-Party Semiselective Ringing**

The system returns special high tone to the calling customer as a request to dial an additional digit that will identify his station and therefore his ringing code.

Having received the eighth digit, the system removes the high tone and returns busy tone to the calling customer. When the calling customer hangs up, the system removes the busy tone and connects ringing to the calling and called stations. If the calling and called stations are on the same side of the line and have the same polarity, only the called line's ringing code is applied. In other cases reverting ringing is returned to the calling station.

F. ASSISTANCE, SERVICE CODE, AND DIRECT DISTANCE DIALING CALLS

Assistance, service code, and direct distance dialing (DDD) calls are handled like outgoing calls. A translation of the dialed digit(s) tells CC:

(a) The type of trunk required to complete the call.

(b) The kind of supervision the trunk requires.

(c) Whether or not outpulsing is required.

Outpulsing is required for DDD calls and when operator switchboard positions are reached through another office.

1. Assistance Calls

After the first digit is translated and CC knows that the customer has dialed a zero, an operator trunk is seized. Audible ringing tone is sent to the customer until the operator answers. When the operator answers, a talking connection is established. Both the operator and the customer must disconnect before the connection is released.

2. Service Code Calls

Calls to a service code operator (long distance, repair service, etc.) follow a pattern similar to that of assistance calls. A translation of the dialed digits informs CC how to terminate the call. Audible ringing tone is sent to the customer and a lamp signal to the operator. The audible ringing connection is released and the talking connection is established when the operator answers. The talking connection is released when the customer disconnects.

3. Direct Distance Dialed Calls

A translation of the area code digits plus the office code if necessary, tells CC how to terminate the call. CC selects the proper trunk and outpulses the proper digits.

4. Manual Calls

A dial office may serve manual customers who require the assistance of an operator on all originating calls. When a manual customer goes off-hook, the LEN translation informs CC that this is a manual service line. A digit receiver is connected to the line but dial tone is not applied. The transfer of supervision is checked and the FCG and power-cross tests are made in the usual manner. The digit receiver is then released. Via an operator trunk, a connection is established to an operator as though the customer had dialed "0". The operator completes the call as requested by the customer.

G. SPECIAL SERVICES

Some of the special services available to No. 1 ESS customers are:

1. Abbreviated dialing

2. Add-on

3. Dial conference

4. Variable transfer

5. Preset transfer

Two of the special services - dial conference and add-on - use a flash of the switch-hook while a conversation is in progress as an alert to the system to prepare for a customer request. The system detects the flash as part of the normal supervisory scan for disconnect. After hit timing has been completed and CC has determined from a bit in the path memory that the customer has the "flash privilege," CC times an interval ranging from 200 msec to 1.2 seconds. If the on-hook signal is longer than 1.2 seconds, it is treated as a disconnect signal. If it is shorter than 1.2 seconds, the proper service actions are taken.

1. Abbreviated Dialing

This service allows a customer to place calls to frequently called numbers by dialing an abbreviated code instead of the usual seven or more digits.

The customer goes off-hook, receives dial tone, and dials or keys the prefix 11. (Customers with TOUCH-TONE Calling may have an eleventh button to obviate the need for the 11 prefix.) The LEN translation tells CC which special services the customer is entitled to. The 11 prefix tells CC that the customer is going to use his abbreviated dial service and that only one or two more digits are to be expected. A list of directory numbers assigned by the subscribing customer is stored in the PS memory. CC uses the dialed digits(s) to determine from the list the directory number of the called line. The maximum number of abbreviated codes for a list is 32. Customers are assigned 1-digit abbreviations for repertories of up to ten numbers; 2-digit abbreviations for repertories of 11 to 32 numbers. A customer wishing to add, delete, or change his abbreviated dial list must contact the telephone company business office to arrange for the changes.

2. Add-On Service

This service allows a No. 1 ESS customer A who is talking to customer B to add another party, C, to the call. Customer A alerts the system by a flash of his switchhook. The established connection is released but party B is still supervised by the junctor or trunk to which he was connected. Customer A is connected to a digit receiver. He receives a special dial tone and then dials the add-on digit 2, followed by the directory number or, if he has abbreviated dial service, the abbreviated dial code

of the line to be added. Customers A and B are then
connected to a conference circuit (see Figure 9-82).
Both parties hear audible ring, busy, or reorder
tone depending upon the state of the line to be ad-
ded. When customer C answers, all three customers
can converse via the conference circuit. Only one
toll connection is permitted to a conference circuit.

To remove the third party from the connection,
whether or not he has answered, customer A alerts the
system by a switchhook flash, receives dial tone, and
dials the cancel digit 3. The system tries to set
up a regular talking path after having released the
conference circuit. Customers A and B remain con-
nected together via the conference circuit, if traf-
fic conditions do not permit the establishment of a
new talking path. A new party may be added as pre-
viously described. The conference connection is re-
leased when customer A hangs up. An AMA record is
kept for each usage of the conference circuit, and
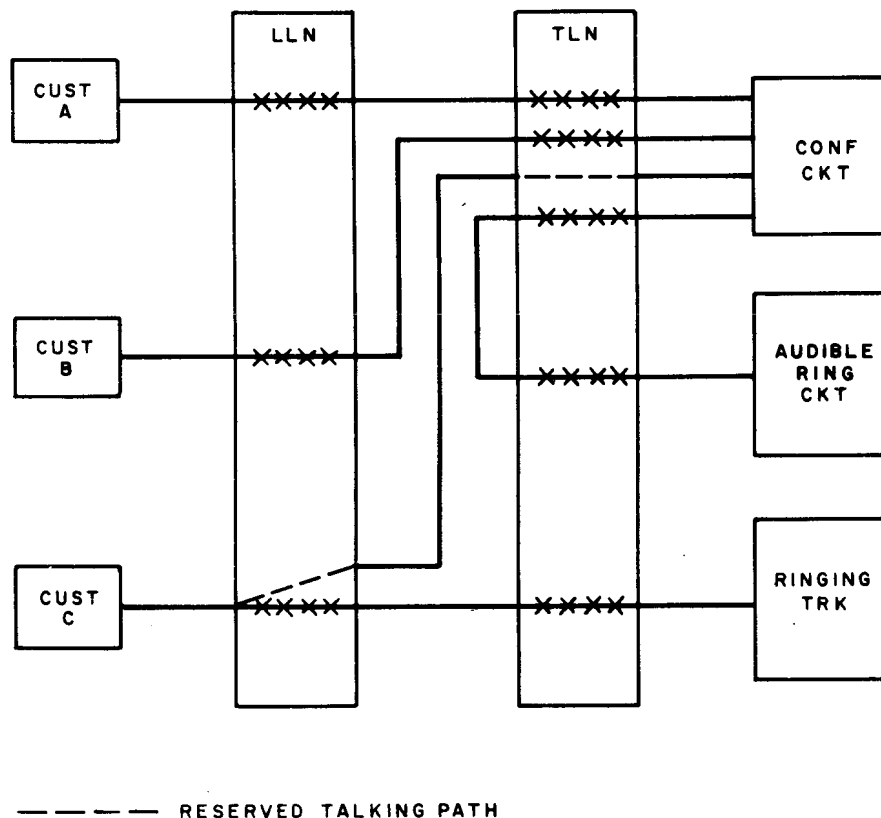for each leg of the conference circuit that is used.

Figure 9-82   Network Connections for Add-On Service
              Connections

3. Dial Conference Circuit

This service allows a customer to establish a conference call without operator assistance. He initiates this service by dialing the conference service access code, which is an abbreviated code. The conference service code tells the system to reserve a conference circuit for the customer. The customer remains connected to the digit receiver, receives dial tone, and dials the add-on digit 2, followed by the directory number of the first conferee. A connection is established between the originating customer and the first conferee via a conference circuit. To add an additional conferee, the customer alerts the system with a switchhook flash, receives dial tone, and dials 2 and the directory number. The dial conference circuit is limited to one originating customer and three conferees (see Figure 9-83). Only one leg of a conference circuit can be connected to toll facilities. To remove the last leg added to the call, the customer alerts the system with a switchhook flash, receives dial tone, and dials the cancel digit 3. Parties previously connected cannot be released by the originating station. All connections are released when the originating customer hangs up. The AMA record includes the time and directory number for each chargeable leg, the total conference circuit usage time, and the maximum number of legs used.
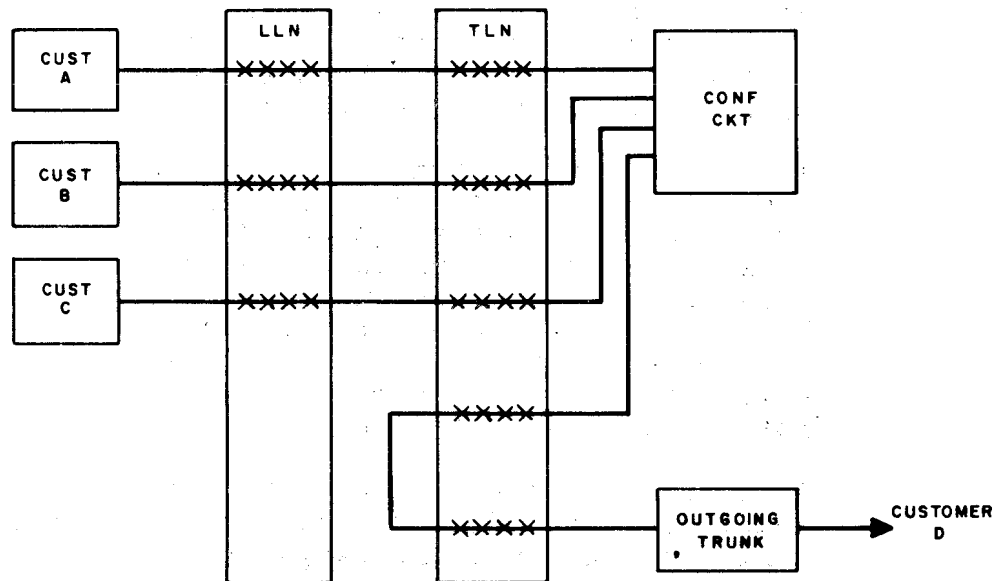
Figure 9-83   Network Connections for Dial Conference Call

4. Variable Transfer

This service allows a customer to have all incoming calls to his base station transferred to a remote station designated by him. To initiate this service, the customer goes off-hook, receives dial tone, and dials an activate code. He receives dial tone again and dials the directory number of the remote station. The customer hears a confirmation tone. The call is then completed to the remote station in the normal manner. The service is activated when the remote station answers. The system, however, can activate the service even though the remote station does not answer, if the program for that office includes this feature. The base station is still able to originate calls regardless of the state of the remote station.

To deactivate this service, the customer dials the deactivate code from the base station, receives the confirmation tone, and hangs up. Subsequent incoming calls will ring only the base station.

5. Preset Transfer

This service allows a customer to have all incoming calls to his base station transferred to any one of eight previously selected remote stations. The restrictions on the location of the remote station are the same as for the variable transfer service. Any additions, deletions, or changes in the list of remote stations are handled through the telephone company business office.

To initiate the service, the customer goes off-hook, receives dial tone, and dials an activate code. He receives dial tone again and dials one digit to designate the station to which he wants his calls transferred. The customer hears a confirmation tone. The call is then completed to the remote station in the normal manner. The service is activated upon completion of dialing regardless of whether the remote station has answered.

To deactivate the service, the customer dials a deactivate code from the base station, receives the confirmation tone, and hangs up.

H. TRAFFIC, ADMINISTRATION AND TEST FEATURES

1. Service Observing

Service observations of customer lines are used to determine the quality of service given by a telephone office. A service observing "shoe" is placed on a customer line at the MDF to connect the line to service observing equipment. A temporary translation is typed in at the maintenance teletypewriter to indicate that the line is to be service observed. The operator releases her connection after she has determined how well the office has performed on the call. Service observations of PBX lines are made to appraise the actions of attendants on terminating calls. In this case the operator connection is made to the attendant's PBX trunk after the directory number translation is made.

2. Call Tracing

Calls are traced by the No. 1 ESS for one of two reasons:

(a) The directory number translation indicates that all calls to a line should be traced.

(b) A request has been made via the teletypewriter to trace a call in progress to a specified line.

For each call to a line whose DN translation specifies call tracing, the system gives a printout that identifies either the local directory number or the incoming trunk from which the call was originaged. For a trace requested via the teletypewriter, the system determines from the path memory in the CS the line or trunk at the other end of the connection. The system prints out the identity of the line or trunk connected to the line being traced.

3. Traffic Measurements

Many items of traffic data are gathered by the No. 1 ESS in the form of counts which are kept in CS traffic registers. These counts are obtained through the joint actions of call processing programs and a traffic measurement program. The call processing programs increment or otherwise update

appropriate counters as events occur during call processing. The traffic measurement program uses the counters of the traffic registers to prepare the traffic data for final output. Most traffic data reflect the busy-hour use of the office equipment. Counts in this category are collected on a regular busy-hour schedule five days a week. Some counts are used to indicate overload conditions and are collected only when an overload exists. Data that are required only occasionally are collected only upon request by teletypewriter. Traffic data will be transmitted upon request to a traffic data processing center via DTWX and/or printed at local or remote traffic teletypewriter installations.

4. Emergency Manual Service

Even when the system is partially or completely inoperative, certain important customers must be provided with originating and terminating service. Each of these customer lines is terminated at an emergency manual line circuit which normally connects the line to a line switch frame. Under abnormal conditions, this circuit connects the line to a distant or local switchboard. This office feature is controlled by a guarded key at the MCC and, if required, by keys at a remote location.

5. Service Order Facilities

Recent change registers in the temporary memory are used to record service order changes, additions and deletions for lines and trunks. The service order number and the associated data are transmitted to the system via a teletypewriter. The data is recorded in a recent change register and is indexed by the service order number. To make a service order effective, an operating company employee dials an appropriate code followed by the service order number.