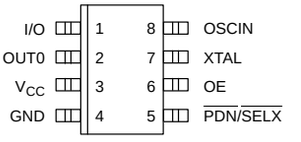
DALLAS SEMICONDUCTOR

DS1073
3–Volt EconOscillator/Divider

FEATURES

- Dual Fixed frequency outputs (30 KHz – 100 MHz)
- User–programmable on–chip dividers (from 1 – 513)
- User–programmable on–chip prescaler (1, 2, 4)
- No external components
- ±0.5% Initial tolerance
- ±1% variation over temperature and voltage
- Internal clock, External clock or crystal reference options
- 2.7 – 3.6V supply
- Power–down mode
- Synchronous output gating

PIN ASSIGNMENT



DS1073Z 150–MIL SOIC
DS1073M 300–MIL DIP

FREQUENCY OPTIONS

Part No.	Max O/P freq.
DS1073–100	100 MHz
DS1073–80	80 MHz
DS1073–66	66 MHz
DS1073–60	60 MHz

DESCRIPTION

The DS1073 is a fixed frequency oscillator requiring no external components for operation. Numerous operating frequencies are possible in the range 30 KHz to 100 MHz through the use of an on–chip programmable prescaler and divider.

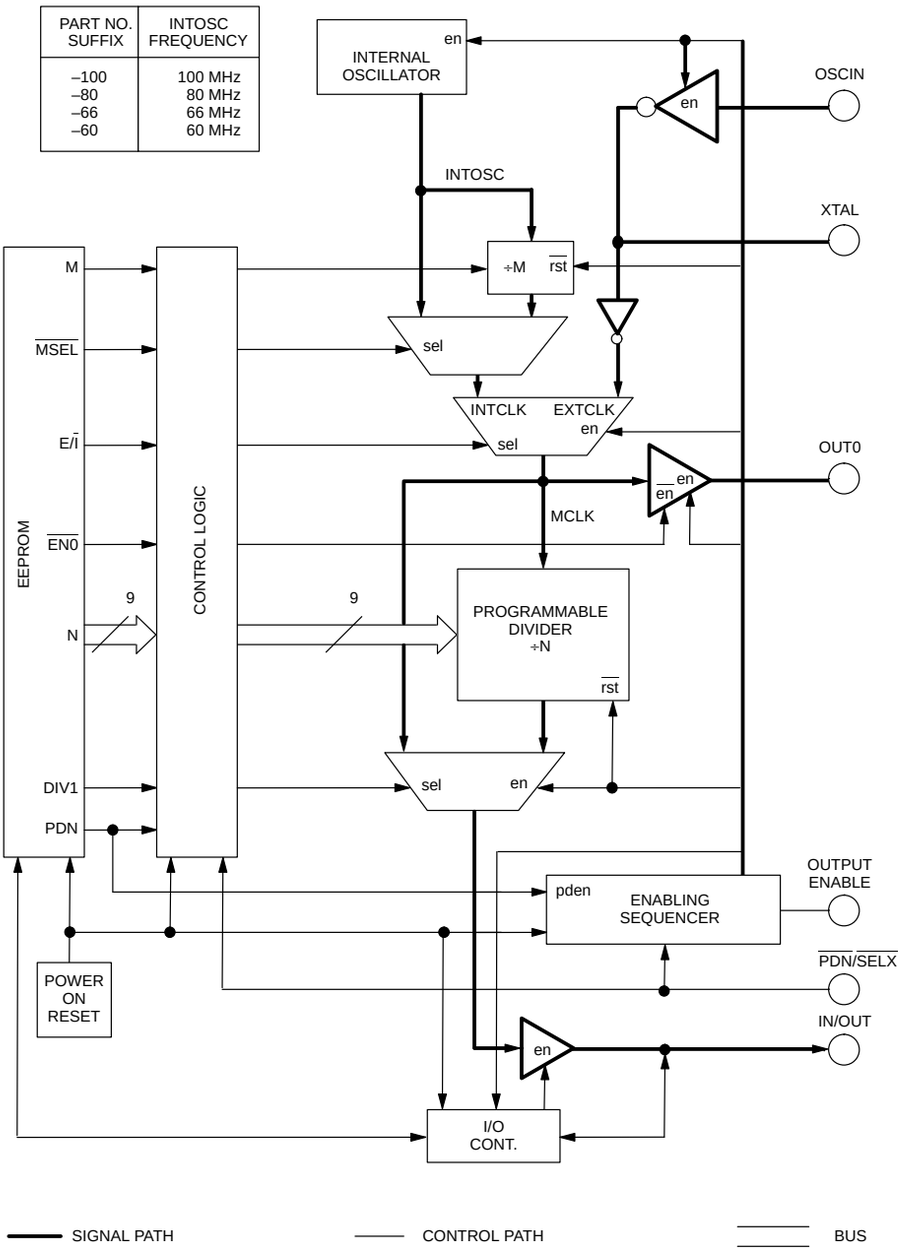
The DS1073 features a master oscillator followed by a prescaler and then a programmable divider. The prescaler and programmable divider are user–programmable with the desired values being stored in non–volatile memory. This allows the user to buy an off the shelf component and program it on site prior to board production. Design changes can be accommodated on the fly by simply programming different values into the device (or reprogramming previously programmed devices).

The DS1073 is shipped from the factory configured for half the maximum operating frequency. Pre–programmed devices can be ordered on a custom basis as DS1073C–xxx. As alternatives to the on–board oscillator an external clock signal or a crystal may be used as a reference. The choice of reference source (internal or external) is user–selectable at the time of programming (or on the fly if the SEL mode is chosen).

The DS1073 features a dual–purpose Input/Output pin. If the device is powered up in Program mode this pin can be used to input serial data to the on chip registers. After a Write command this data is stored in non–volatile memory. When the chip is subsequently powered up in operating mode these values are automatically restored to the on–chip registers and the Input/Output pin becomes the oscillator output.

The DS1073 is available in 8–pin DIP or SOIC packages, allowing the generation of a clock signal easily, economically and using minimal board area.

BLOCK DIAGRAM Figure 1



PIN DESCRIPTIONS

Input/Output Pin (IN/OUT): This pin is the main oscillator output, with a frequency determined by clock reference, M and N dividers. Except in programming mode this pin is always an output and will be referred to as "OUT". In programming mode this pin will be referred to as "IN".

External Oscillator Input (OSCIN): This pin can be used to supply an external reference frequency to the device.

Crystal Oscillator Connection (XTAL): A crystal can be connected between this pin and OSCIN to provide an alternative frequency reference. The crystal must be used in fundamental mode. If a crystal is not used this pin should be left open.

Output Enable Function (OE pin): The DS1073 also features a "synchronous" output enable. When OE is at a high logic level the oscillator free runs. When this pin is taken low OUT is held low, immediately if OUT is already low, or at it's next high–to–low transition if OUT is high. This prevents any possible truncation of the output pulse width when the enable is used. While the output is disabled the master oscillator continues to run (producing an output at OUT0, if the $\overline{EN0}$ bit = 0) but the internal counters (/N) are reset. This results in a constant phase relationship between OE's return to a high level and the resulting OUT signal. When the enable is released OUT will make its first transition within one to two clock periods of the master clock.

Power–Down/Select Function ($\overline{PDN}$/$\overline{SELX}$ pin): The Power–Down/Select ($\overline{PDN}$/$\overline{SELX}$) pin has a user–selectable function determined by one bit (PDN bit) of the user–programmable memory. According to which function is selected, this pin will be referred to as $\overline{PDN}$ or $\overline{SELX}$.

If the Power–Down function is selected (PDN bit = 1) a low logic level on this pin can be used to make the device stop oscillating (active low) and go into a reduced power consumption state. The "Enabling Sequencer" circuitry will first disable OUT in the same way as when OE is used. Next OUT0 will be disabled in a similar fashion. Finally the oscillator circuitry will be disabled. In this mode both outputs will go into a high impedance state. The power consumption in the power–down state is much less than if OE is used because the internal oscillator (if used) is completely powered down. Even if an external reference or a crystal is used all of the on–chip buffers are powered down to minimize current drain. Consequently the device will take considerably longer to recover (i.e., achieve stable oscillation) from a power–down condition than if the OE is used.

If the Select function is chosen (PDN bit = 0) this pin can be used to switch between the internal oscillator and an external reference (or crystal) on the fly. When this mode is chosen the E/$\overline{I}$ select bit is overridden, a high logic level on $\overline{SELX}$ will select the internal oscillator, a low logic level will select the external reference (or crystal oscillator).

Reference Output (OUT0 pin): A reference output, OUT0, is also available from the output of the reference select mux. This output is especially useful as a buffered output of a crystal defined master frequency. OUT0 is unaffected by the OE pin, but is disabled in a glitchless fashion if the device is powered down. If this output is not required it can be permanently disabled by setting the $\overline{EN0}$ bit to one, and there will be a corresponding reduction in overall power consumption.

USER–PROGRAMMABLE REGISTERS

The following registers can be programmed by the user to determine operating frequency and mode of operation. Details of how these registers are programmed can be found in a later section, in this section the function of the registers are described. The register settings are non–volatile, the values being stored automatically in EEPROM when the registers are programmed.

Note: The register bits cannot be used to make mode or frequency changes on the fly. Changes can only be made by powering the device up in "Programming" mode. For them to be become effective the device must then be powered down and powered up again in "Operation" mode.

For programming purposes the register bits are divided into two 9–bit words, the "MUX" word determines mode of operation and prescaler values. The "DIV" word sets the value of the programmable divider.

MUX WORD Figure 2

(MSB)								(LSB)
0*	0*	0*	$\overline{EN0}$	PDN	M	$\overline{MSEL}$	DIV1	E/$\bar{I}$

* These bits must be set to zero

E/$\bar{I}$

This bit selects either the internal oscillator or the external/crystal reference.

1=External/Crystal

0=Internal Oscillator

however, if the PDN bit is set to zero the E/$\bar{I}$ bit will be overridden by the logic level on the $\overline{PDN}$/$\overline{SELX}$ pin.

Table 1

PDN BIT	E/$\bar{I}$	$\overline{PDN}$/$\overline{SELX}$ PIN	OSCILLATOR MODE
0	X	0	EXTERNAL/CRYSTAL
0	X	1	INTERNAL
1	X	0	POWER–DOWN
1	0	1	INTERNAL
1	1	1	EXTERNAL/CRYSTAL

DIV1

This bit allows the master clock to be routed directly to the output (DIV1=1). The N programmable divider is bypassed so the programmed value of N is ignored. The frequency of the output (f_{OUT}) will be INTCLK or EXTCLK depending on which reference has been selected. If the Internal clock is selected the M prescaler may still be used, so in this case f_{OUT}=INTOSC/M (which also equals MCLK and INTCLK) . If DIV1=0 the programmable divider functions normally.

$\overline{MSEL}$

This bit determines whether or not the M prescaler is bypassed. $\overline{MSEL}$=1 will bypass the prescaler. $\overline{MSEL}$=0 will switch in the prescaler (unless overridden by DIV1=1), with a divide–by number determined by the M bit.

M

This bit sets the divide–by number for the prescaler. M=0 results in divide–by–4, M=1 results in divide–by–2. The setting of this bit is irrelevant if either DIV1=1 or $\overline{MSEL}$=1.

Table 2

DIV1 BIT	E/$\bar{I}$ BIT*	$\overline{MSEL}$ BIT	M BIT	OPERATION
0	0	0	0	INTERNAL OSCILLATOR DIVIDED BY 4*N
0	0	0	1	INTERNAL OSCILLATOR DIVIDED BY 2*N
0	0	1	X	INTERNAL OSCILLATOR DIVIDED BY N
0	1	X	X	EXTERNAL OSCILLATOR DIVIDED BY N
1	0	X	X	INTERNAL OSCILLATOR DIVIDED BY 1
1	1	X	X	EXTERNAL OSCILLATOR DIVIDED BY 1

*Assuming PDN bit = 1, otherwise internal/external selection will be controlled by the $\overline{PDN}$/$\overline{SELX}$ pin.

DIV WORD Figure 3

(MSB)	(LSB)
N (9–BITS)	

PDN
This bit is used to determine the function of the $\overline{PDN}$/$\overline{SELX}$ pin. If PDN=0, the $\overline{PDN}$/$\overline{SELX}$ pin can be used to determine the timing reference (either the internal oscillator or an external reference/crystal). If PDN=1, the $\overline{PDN}$/$\overline{SELX}$ pin is used to put the device into power–down mode.

$\overline{EN0}$
This bit is used to determine whether the OUT0 pin is active or not. If $\overline{EN0}$ =1, OUT0 is disabled (High–impedance). If $\overline{EN0}$=0, the internal reference clock (MCLK) is output from OUT0. The OE pin has no effect on OUT0, but OUT0 is disabled as part of the power–down sequence.

N
These nine bits determine the value of the programmable divider. The range of divisor values is from 2 to 513, and is equal to the programmed value of N plus 2:

Table 3

BIT VALUES	DIVISOR (N) VALUE
000000000	2
000000001	3
.	.
.	.
.	.
.	.
.	.
111111111	513

NOTE:
The maximum value of N is constrained by the minimum output frequency. If the internal clock is selected, INTOSC/(M*N) must be greater than f_{OUTmin}; if the external clock is selected, EXTCLK/N must be greater than f_{OUTmin}. (If DIV1=1, then INTOSC or EXTCLK, as applicable, must exceed f_{OUTmin}).

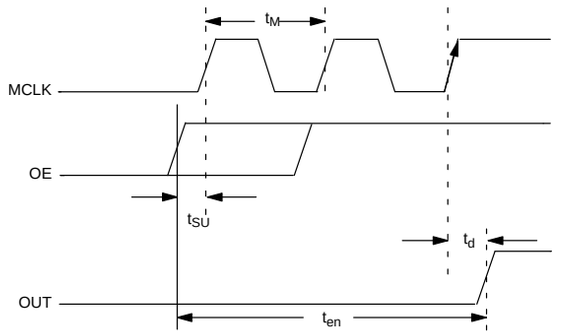
OPERATION OF OUTPUT ENABLE

Since the output enable, internal master oscillator and/or external master oscillator are likely all asynchronous there is the possibility of timing difficulties in the application. To minimize these difficulties the DS1073 features an “enabling sequencer” to produce predictable results when the device is enabled and disabled. In particular the output gating is configured so that truncated output pulses can never be produced.

Enable timing

The output enable function is produced by sampling the OE input with the output from the prescaler mux (MCLK) and gating this with the output from the programmable divider. The exact behavior of the device is therefore dependent on the setup time (t_{SU}) from a transition on the OE input to the rising edge of MCLK. If the actual setup time is less than t_{SUEM} then one more complete cycle of MCLK will be required to complete the enable or disable operation (see diagrams). This is unlikely to be of any consequence in most applications, and then only if the value for N is small. In general, the output will make its first positive transition between approximately one and two clock periods of MCLK after the rising edge of OE.

FIGURE 4



t_M = PERIOD OF MCLK
t_d = PROP DELAY FROM MCLK ↑ TO OUT ↑

MAX VALUE OF $t_{en} = t_{SUEM} + 2\ t_M + t_d$
MIN VALUE OF $t_{en} = t_{SUEM} + t_M + t_d$

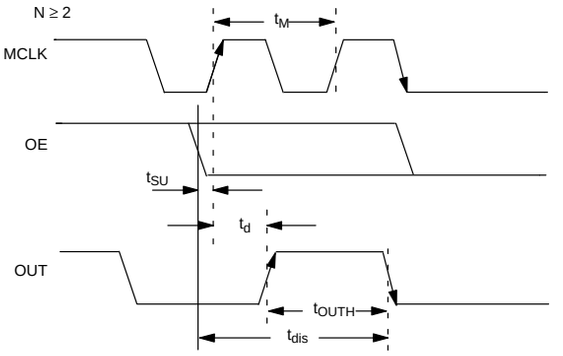
Disable Timing

If OE goes low while OUT is high, the output will be disabled on the completion of the output pulse. If OUT is low, the disabling behavior will be dependent on the setup time between the falling edge of OE and the rising edge of MCLK. If $t_{SU} < t_{SUEM}$ the result will be one additional pulse appearing on the output before disabling occurs.

If the device is in divide–by–one mode, the disabling occurs slightly differently. In this case if $t_{SU} > t_{SUEM}$ one additional output pulse will appear, if $t_{SU} < t_{SUEM}$ then two additional output pulses will appear.

The following diagrams illustrate the timing in each of these cases.

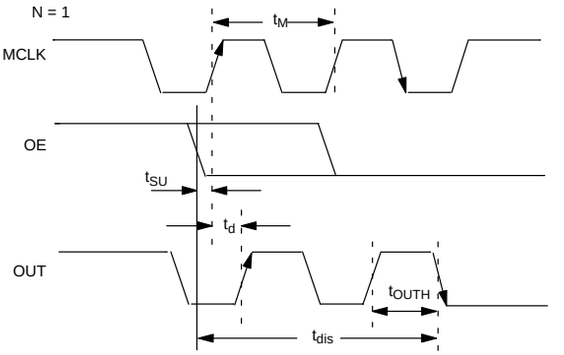
Figure 5



t_M = PERIOD OF MCLK
t_d = PROP DELAY FROM MCLK ↑ TO OUT ↑
t_{OUTH} = WIDTH OF OUTPUT PULSE

MAX VALUE OF $t_{dis} = t_{SUEM} + t_d + t_{OUTH}$
MIN VALUE OF $t_{dis} = 0$

Figure 6



t_M = PERIOD OF MCLK
t_d = PROP DELAY FROM MCLK ↑ TO OUT ↑
t_{OUTH} = WIDTH OF OUTPUT PULSE

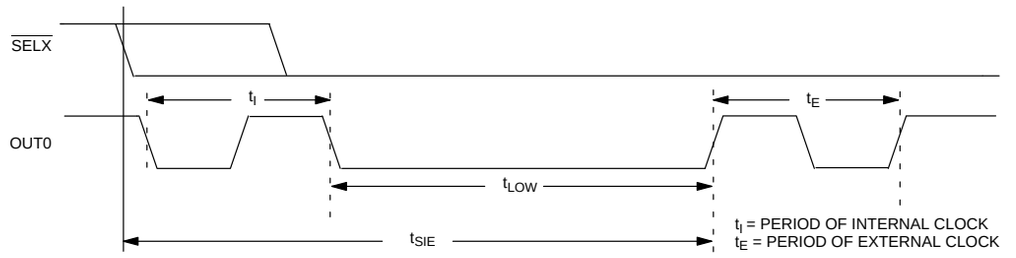
MAX VALUE OF $t_{dis} = t_{SUEM} + t_d + t_{OUTH} + t_M$
MIN VALUE OF $t_{dis} = t_{SUEM} + t_d + t_{OUTH}$

SELECT TIMING

If the PDN bit is set to “0”, the $\overline{PDN}/\overline{SELX}$ pin can be used to switch between the internal oscillator and an external or crystal reference. The “Enabling Sequencer” is again employed to ensure this transition occurs in a glitch–free fashion. Two asynchronous clock signals are involved, INTCLK is the internal reference oscillator divided by one or whatever value of M is selected. EXTCLK is the clock signal fed into the OSCIN pin, or the clock resulting from a crystal connected between OSCIN and XTAL. The behavior of OUT0 is described in the following paragraphs, the OUT pin will behavior similarly but will be divided by N.

From Internal to External clock
This is accomplished by a high to low transition on the $\overline{SELX}$ pin. This transition is detected on the falling edge of INTCLK. The output OUT0 will be held low for a minimum of half the period of INTCLK ($t_I/2$), then if EXTCLK is low it will be routed through to OUT0. If EXTCLK is high the switching will not occur until EXTCLK returns to a low level.

Figure 7



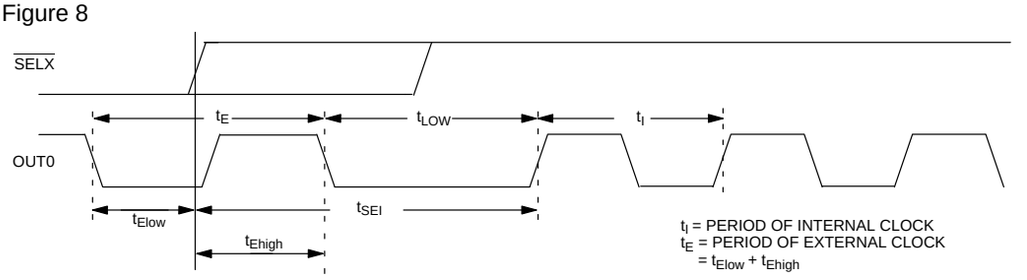
Depending on the relative timing of the $\overline{SELX}$ signal and the internal clock, there may be up to one full cycle of t_I on the output after the falling edge of $\overline{SELX}$. Then, the "low" time (t_{LOW}) between output pulses will be dependent on the relative timing between t_I and t_E. The time interval between the falling edge of $\overline{SELX}$ and the first rising edge of the externally derived clock is t_{SIE}. Approximate maximum and minimum values of these parameters are:

t_{LOW} (min) = $t_I/2$
t_{LOW} (max) = $t_I/2 + t_E$
t_{SIE} (min) = $t_I/2$
t_{SIE} (max) = $3t_I/2 + t_E$

NOTE:
In each case there will be a small additional delay due to internal propagation delays.

From External to Internal clock
This is accomplished by a low to high transition on the $\overline{SELX}$ pin. In this case the switch is level triggered, to allow for the possibility of a clock signal not being present at OSCIN. Note therefore, that if a constant high–level signal is applied to OSCIN it will not be possible to switch over to the internal reference. (Level triggering was not employed for the switch from internal to external reference as this approach is slower and the internal clock may be running at a much higher frequency than the maximum allowed external clock rate). When $\overline{SELX}$ is high and a low level is sensed on EXTCLK, OUT0 will be held low until a falling edge occurs on INTCLK, then the next rising edge of INTCLK will be routed through to OUT0.

Figure 8



Depending on the relative timing of the $\overline{SELX}$ signal and the external clock, there may be up to one full t_{Ehigh} period on the output after the rising edge of $\overline{SELX}$. Then, the "low" time (t_{LOW}) between output pulses will be dependent on the relative timing between t_I and t_E. The time interval between the falling edge of $\overline{SELX}$ and the first rising edge of the externally derived clock is t_{SIE}. Approximate maximum and minimum values of these parameters are:

t_{LOW} (min) = $t_I/2$
t_{LOW} (max) = $3t_I/2 + t_{Elow}$
t_{SEI} (min) = $t_I/2$
t_{SEI} (max) = $3t_I/2 + t_{Ehigh}$

NOTE:
In each case there will be a small additional delay due to internal propagation delays.

POWER–DOWN CONTROL

If the PDN bit is set to “1”, the $\overline{PDN}$/$\overline{SELX}$ pin can be used to power–down the device. If $\overline{PDN}$ is high the device will run normally.

Power–Down
If $\overline{PDN}$ is taken low a power–down sequence is initiated. The “Enabling Sequencer” is used to execute events in the following sequence:

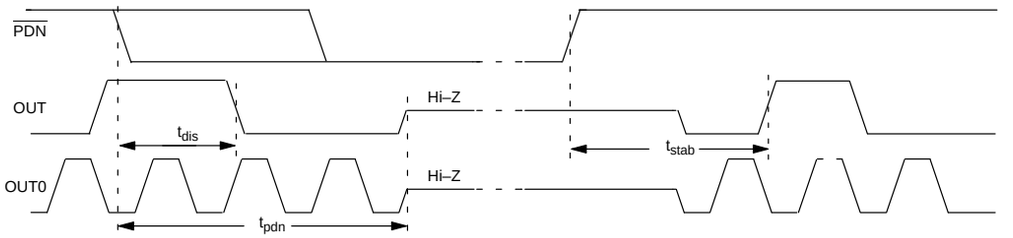
1. Disable OUT (same sequence as when OE is used) and reset N counters.
2. When OUT is low, switch OUT to high–impedance state.
3. Disable MCLK (and OUT0 if $\overline{EN0}$ bit = 0), switch OUT0 to high impedance state.
4. Disable internal oscillator and OSCIN buffer.

Power–UP
When $\overline{PDN}$ is taken to a high level the following power–up sequence occurs:

1. Enable internal oscillator and/or OSCIN buffer.
2. Set M and N to maximum values.
3. Wait approximately 256 cycles of MCLK for it to stabilize.
4. Reset M and N to programmed values.
5. Enable OUT0 (assuming $\overline{EN0}$ bit = 0).
6. Enable OUT.

Steps 2 through 4 exist to allow the oscillator to stabilize before enabling the outputs.

Figure 9

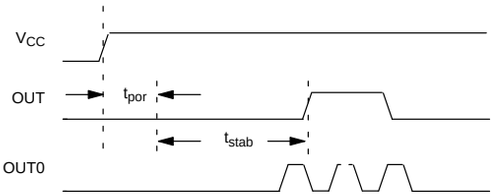


POWER–ON RESET

When power is initially applied to the device supply pin, a power–on reset sequence is executed, similar to that which occurs when the device is restored from a power–down condition. This sequence comprises two stages, first a conventional POR to initialize all on–chip circuitry, followed by a stabilization period to allow the oscillator to reach a stable frequency before enabling the outputs:

1. Initialize internal circuitry.
2. Enable internal oscillator and/or OSCIN buffer.
3. Set M and N to maximum values.
4. Wait approximately 256 cycles of MCLK for the oscillator to stabilize.
5. Load M and N programmed values from EEPROM.
6. Enable OUT0 (assuming EN0=0).
7. Enable OUT.

Figure 10



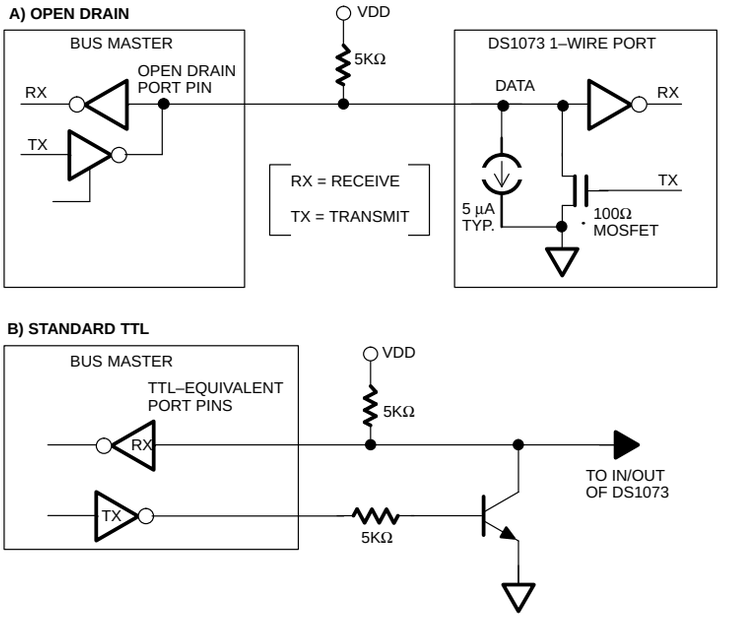
PROGRAMMING

Normally when power is applied to the supply voltage pin the device will enter its normal operating mode following the power–on reset sequence. However the device can be made to enter a programming mode if a pull–up resistor is connected between IN/OUT and the supply voltage pin, prior to power–up. The method used for programming is a variant of the 1–Wire™ protocol used on a number of Dallas Semiconductor products.

HARDWARE

The hardware configuration is shown in the diagram. A bus master is used to read and write data to the DS1073's internal registers. The bus master may have either an open–drain or TTL–type architecture.

Figure 11

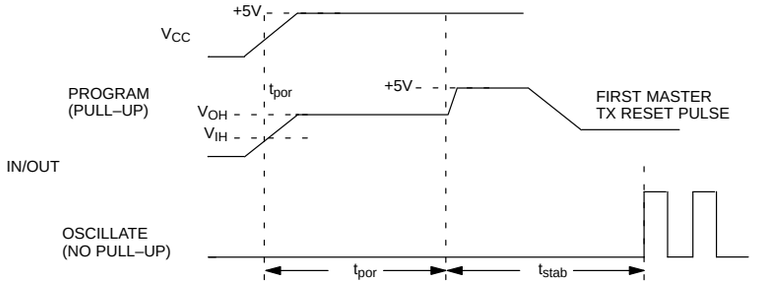


Programming mode is entered by simply powering up the DS1073 with a pull–up of approximately 5KΩ. This will pull the IN/OUT pin above V_{IH} on power–up and initiate the programming mode, causing the DS1073 to internally release the IN/OUT pin (after t_{POR}), and allow the pullup resistor to pull the pin to the supply rail and await the Master Tx Reset pulse (see diagram).

NOTE:

To ensure normal operation any external pull–up applied to IN/OUT must be greater than 20KΩ in value. This will cause the IN/OUT pin to remain below V_{IH} on power–up, resulting in normal operation at the end of t_{STAB}.

Figure 12



TRANSACTION SEQUENCE

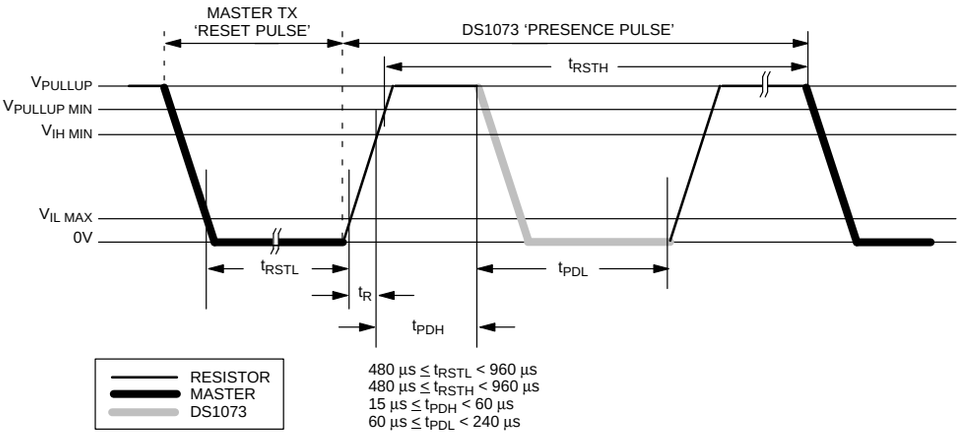
The sequence for accessing the DS1073 via the 1–Wire port is as follows:

Initialization
Function Command
Transaction/Data

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the DS1073. The presence pulse lets the bus master know that the DS1073 is present and is ready to operate.

Figure 13



FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four function commands. All Function Commands are eight bits long, and are written lsb first. A list of these commands follows:

Write DIV Register [01H]

This command allows the bus master to write to the DS1073's DIV register.

Read DIV Register [A1H]

This command allows the bus master to read the DS1073's DIV register.

Write MUX Register [02H]

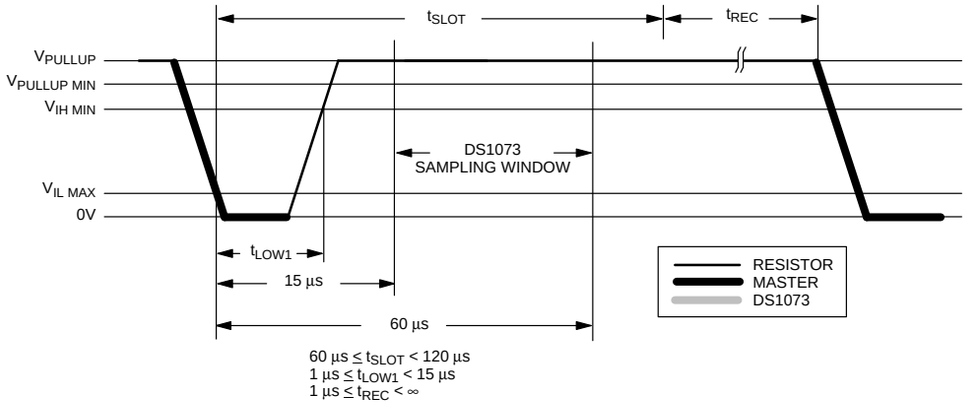
This command allows the bus master to write to the DS1073's MUX register.

Read MUX Register [A2H]
This command allows the bus master to read the DS1073's MUX register.

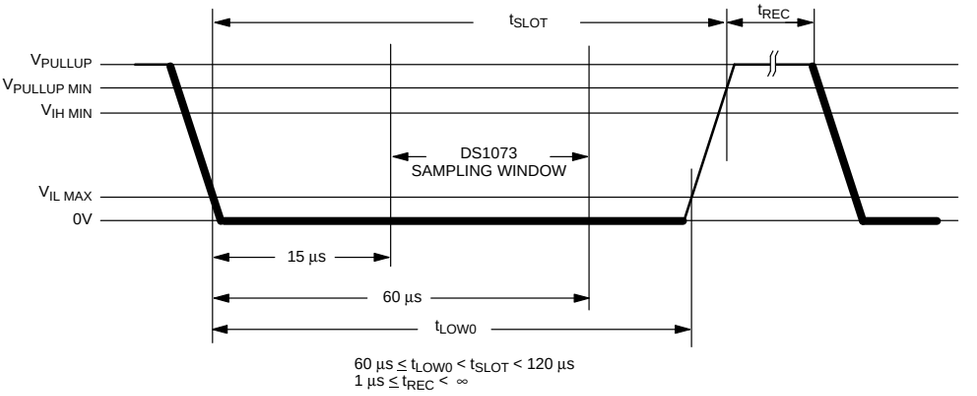
TRANSACTION/DATA
Immediately following the Function Command, the nine data bits are written to or read from the DS1073. This data is written/read lsb first. The following diagrams illustrate the timing. Once data transfer is complete a new transaction sequence can be started by re–initializing the device. Therefore to program both the DIV and MUX registers two complete transaction sequences are required.

READ/WRITE TIME SLOTS
The definitions of write and read time slots are illustrated below. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS1073 to the master by triggering a delay circuit in the DS1073. During write time slots, the delay circuit determines when the DS1073 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS1073 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the DS1073 will leave the read data time slot unchanged.

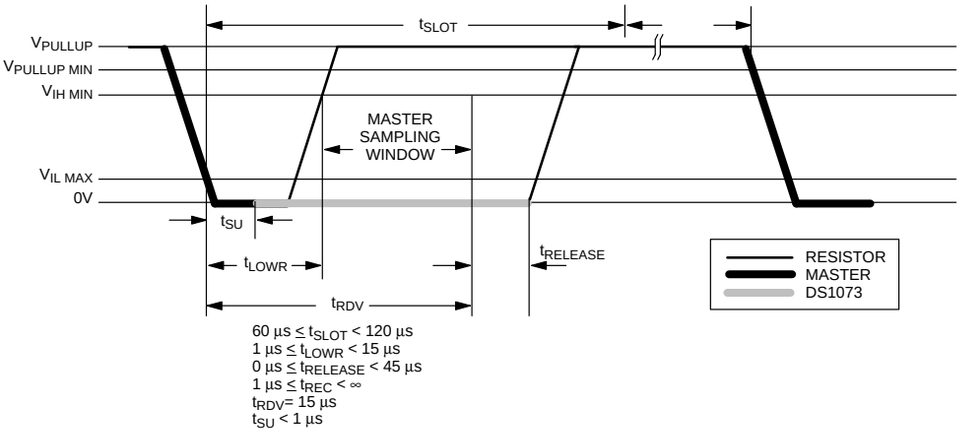
WRITE "1" TIME SLOT Figure 14



WRITE "0" TIME SLOT Figure 15



READ DATA TIME SLOT Figure 16



RETURN TO NORMAL OPERATION

When programming is complete the DS1073 should be powered down. If the pull–up resistor on the IN/OUT pin is removed, normal device operation will be restored next time power is applied.

DEFAULT REGISTER VALUES

Unless ordered from the factory with specific register program values, the DS1073 is shipped with the following default register values:

DIV = 0 0000 0000 (Programmable divider will divide by two)
MUX = 0 0011 0100
OUT0 Disabled
Power–Down Enabled, Select Disabled
M = 4 (Ignored, see $\overline{\text{MSEL}}$)
$\overline{\text{MSEL}}$ = 1 (M prescaler bypassed)
DIV1 = 0 (N Dividers enabled)
E/$\bar{\text{I}}$ = 0 (Internal oscillator selected)

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(t_A = 0°C to 70°C) (V_{CC}=2.7V to 3.6V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		2.7		3.6	V	
High–level Output Voltage (IN/OUT, OUT0)	V_{OH}	I_{OH} = –2 mA, V_{CC} = MIN	2.4			V	
Low–level Output Voltage (IN/OUT, OUT0)	V_{OL}	I_{OL} = 2 mA			0.4	V	
High–level Input Voltage	V_{IH}		2			V	
Low–level Input Voltage	V_{IL}				0.8	V	
High–level Input Current ($\overline{PDN}$/$\overline{SELX}$, OE) (OSCIN)	I_{IH} I_{IH}	V_{IH}=2.4V, V_{CC}= 3.6V V_{IH}=V_{CC} =3.6V			1 10	uA uA	
Low–level Input Current ($\overline{PDN}$/$\overline{SELX}$, OE) (OSCIN)	I_{IL} I_{IL}	V_{IL}=0,V_{CC}=3.6V V_{IL}=0,V_{CC}=3.6V	–1 –10			uA uA	
Supply Current (Active) DS1073–100 DS1073–80 DS1073–66 DS1073–60	I_{CC}	C_L = 15 pF (both outputs)		25	40	mA	
Standby Current (power–down)	I_{CCQ}	Power–Down Mode		0.8		uA	

AC ELECTRICAL CHARACTERISTICS

(t_A = 0°C to 70°C) (V_{CC}=2.7V to 3.6V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Output Frequency Accuracy	f_O	V_{CC} = 3.15V, T_A = 25°C	–0.5	0	+0.5	%	
Combined Freq. Variation	Δf_O	Over temp and voltage	–1		+1	%	
Maximum Input Frequency	f_{OSCIN}	External clock			50	MHz	1
		Crystal reference			25	MHz	
Minimum Output Frequency	f_{OUT}		30			KHz	2
Power–Up Time	$t_{por} + t_{stab}$			0.1	1	ms	3, 4
Enable OUT from $\overline{PDN}$ ↑	t_{stab}			0.1	1	ms	4
Enable OUT0 from $\overline{PDN}$ ↑	t_{stab}			0.1	1	ms	4, 5
OUT Hi–Z from $\overline{PDN}$ ↓	t_{pdn}				1	ms	
OUT0 Hi–Z from $\overline{PDN}$ ↓	t_{pdn}				1	ms	
Load Capacitance (IN/OUT, OUT0)	C_L			15		pF	6
Output Duty Cycle IN/OUT OUT0			 40 40		 60 60	 % %	

NOTES:

1. This is the maximum frequency which can be applied to OSCIN, or, the maximum crystal frequency that can be used. If a crystal is used it must be operated in fundamental mode.
2. The values of M, N and the frequency of OSCIN (if used) must be chosen so that this spec is met
3. This is the time from when V_{CC} is applied until the output starts oscillating
4. When the device is initially powered up, or restored from the power–down mode, OE should be asserted (high). Otherwise the start of the t_{stab} interval will be delayed until OE goes high. OE can subsequently be returned to a low level during the t_{stab} interval to force out low after the t_{stab} interval. If the external mode is selected t_{stab} will be a function of the OSCIN period, i.e., external clock frequency. See “Calculated Parameters” to determine the value of t_{stab} in this case.
5. Although OE does not normally affect OUT0 operation, if OE is held low during power–up the start of the t_{stab} period will be delayed until OE is asserted. If OE remains low, OUT0 will not start.
6. Operation with higher capacitive loads is possible but may impair output voltage swing and maximum operation frequency.

AC ELECTRICAL CHARACTERISTICS – CALCULATED PARAMETERS

The following characteristic are derived from various device operating parameters (frequency, mode etc.). They are not specifically tested or guaranteed and may differ from the min and max limits shown by a small amount due to internal device setup times and propagation delays. However, these equations can be used to derive a more accurate idea of typical device performance than the guaranteed values.

PARAMETER	SYMBOL	CONDITION	MIN	MAX
OUT ↑ from OE ↑	t_{en}		t_M	$2t_M$
OUT ↓ from OE ↓ N = 1 N ≥ 2	 t_{dis} t_{dis}		 t_{OUTH} 0	 $t_{OUTH} + t_M$ t_{OUTH}
$\overline{SELX}$ ↓ to OUT0 ↑ – Internal to External – External to Internal	 t_{SIE} t_{SEI}		 $t_I/2$ $t_I/2$	 $3t_I/2 + t_E$ $3t_I/2 + t_{Ehigh}$
Break during SEL switch – Internal to External – External to Internal	 t_{LOW} t_{LOW}		 $t_I/2$ $t_I/2$	 $t_I/2 + t_E$ $3t_I/2 + t_{Elow}$
$\overline{PDN}$ ↓ to IN/OUT Hi–Z N = 1 N ≥ 2	 t_{pdn} t_{pdn}		 t_{OUTH} 0	 $t_{OUTH} + t_M$ t_{OUTH}
$\overline{PDN}$ ↓ to OUT0 Hi–Z N = 1 N ≥ 2	 t_{pdn} t_{pdn}		 t_{OUTH} 0	 $t_{OUTH} + t_M$ t_{OUTH}
$\overline{PDN}$ ↑ to OUT ↑	t_{stab}			$256t_M$
$\overline{PDN}$ ↑ to OUT0 ↑	t_{stab}			$256t_M$
OUT ↑ after Power–Up				$256t_M$
OUT0 ↑ after Power–Up				$256t_M$