NOT RECOMMENDED FOR NEW DESIGNS. SEE DS1245Y/AB DATA SHEET.

FEATURES

• 10 years minimum data retention in the absence of external power
• Data is automatically protected during power loss
• Unlimited write cycles
• Low–power CMOS
• Read and write access times as fast as 70 ns
• Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
• Full ±10% VCC operating range (DS1245YL)
• Optional ±5% VCC operating range DS1245BL)
• Optional industrial temperature range of –40°C to +85°C, designated IND
• Low Profile Module (LPM) package
  – Fits into standard 68–pin PLCC surface–mountable sockets
  – 250 mil package height

PIN DESCRIPTION

A0 – A16 – Address Inputs
DQ0 – DQ7 – Data In/Data Out
CE – Chip Enable
WE – Write Enable
OE – Output Enable
VCC – Power (+5V)
GND – Ground
NC – No Connect

DESCRIPTION

The DS1245 1024K Nonvolatile SRAMs are 1,048,576–bit, fully static, nonvolatile SRAMs organized as 131,072 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors VCC for an out–of–tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interfacing.
READ MODE
The DS1245 devices execute a read cycle whenever WE (Write Enable) is inactive (high) and CE (Chip Enable) and OE (Output Enable) are active (low). The unique address specified by the 17 address inputs (A0 - A16) defines which of the 131,072 bytes of data is accessed. Valid data will be available to the eight data output drivers within tACC (Access Time) after the last address input signal is stable, providing that CE and OE access times are also satisfied. If CE and OE access times are not satisfied, then data access must be measured from the later occurring signal (CE or OE) and the limiting parameter is either tCO for CE or tOE for OE rather than address access.

WRITE MODE
The DS1245 devices execute a write cycle whenever the WE and CE signals are active (low) after address inputs are stable. The later occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (tWR) before another cycle can be initiated. The CE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled (CE and OE active) then WE will disable the outputs in tODW from its falling edge.

DATA RETENTION MODE
The DS1245BL provides full functional capability for VCC greater than 4.75 volts and write protects by 4.5 volts. The DS1245YL provides full functional capability for VCC greater than 4.5V and write protects by 4.25 volts. Data is maintained in the absence of VCC without any additional support circuitry. The nonvolatile static RAMs constantly monitor VCC. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become “don’t care,” and all outputs become high impedance. As VCC falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when VCC rises above approximately 3.0 volts, the power switching circuit connects external VCC to RAM and disconnects the lithium energy source. Normal RAM operation can resume after VCC exceeds 4.75 volts for the DS1245BL and 4.5 volts for the DS1245YL.

FRESHNESS SEAL
Each DS1245 device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When VCC is first applied at a level greater than VTP, the lithium energy source is enabled for battery backup operation.
ABSOLUTE MAXIMUM RATINGS*
Voltage on Any Pin Relative to Ground –0.3V to +7.0V
Operating Temperature 0°C to 70°C, –40°C to +85°C for Ind parts
Storage Temperature –40°C to +70°C, –40°C to +85°C for Ind parts
Soldering Temperature 260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (t A: See Note 10)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS1245BL Power Supply Voltage</td>
<td>V CC</td>
<td>4.75</td>
<td>5.0</td>
<td>5.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>DS1245YL Power Supply Voltage</td>
<td>V CC</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Logic 1</td>
<td>V IH</td>
<td>2.2</td>
<td></td>
<td>V CC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Logic 0</td>
<td>V IL</td>
<td>0.0</td>
<td></td>
<td>+0.8</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

DC ELECTRICAL CHARACTERISTICS (t A: See Note 10) (V CC=5V ± 5% for DS1245BL)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Leakage Current</td>
<td>I IL</td>
<td>–1.0</td>
<td></td>
<td>+1.0</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>I/O Leakage Current</td>
<td>I IO</td>
<td>–1.0</td>
<td></td>
<td>+1.0</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Output Current @ 2.4V</td>
<td>I O H</td>
<td>–1.0</td>
<td></td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Output Current @ 0.4V</td>
<td>I O L</td>
<td>2.0</td>
<td></td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Standby Current CE=2.2V</td>
<td>I CCS1</td>
<td>5.0</td>
<td></td>
<td>10.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Standby Current CE=V CC–0.5V</td>
<td>I CCS2</td>
<td>3.0</td>
<td></td>
<td>5.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Operating Current</td>
<td>I CCD1</td>
<td></td>
<td></td>
<td>85</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Write Protection Voltage (DS1245BL)</td>
<td>V TP</td>
<td>4.50</td>
<td></td>
<td>4.62</td>
<td>4.75</td>
<td>V</td>
</tr>
<tr>
<td>Write Protection Voltage (DS1245YL)</td>
<td>V TP</td>
<td>4.25</td>
<td></td>
<td>4.37</td>
<td>4.5</td>
<td>V</td>
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</table>

CAPACITANCE (t A = 25°C)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Capacitance</td>
<td>C IN</td>
<td>5</td>
<td></td>
<td>10</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Input/Output Capacitance</td>
<td>C IO</td>
<td>5</td>
<td></td>
<td>10</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>
AC ELECTRICAL CHARACTERISTICS

\( V_{CC} = 5V \pm 5\% \) for DS1245BL

\( (t_A: \text{See Note 10}) \ (V_{CC} = 5V \pm 10\% \) for DS1245YL

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>DS1245BL–70</th>
<th>DS1245BL–70</th>
<th>DS1245YL–70</th>
<th>DS1245YL–100</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read Cycle Time</td>
<td>( t_{RC} )</td>
<td>70</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Access Time</td>
<td>( t_{ACC} )</td>
<td>70</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OE to Output Valid</td>
<td>( t_{OE} )</td>
<td>35</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CE to Output Valid</td>
<td>( t_{CO} )</td>
<td>70</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OE or CE to Output Active</td>
<td>( t_{COE} )</td>
<td>5</td>
<td>5</td>
<td>ns</td>
<td></td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>Output High Z from Deselection</td>
<td>( t_{OD} )</td>
<td>25</td>
<td>35</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Output Hold from Address Change</td>
<td>( t_{OH} )</td>
<td>5</td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Write Cycle Time</td>
<td>( t_{WC} )</td>
<td>70</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Write Pulse Width</td>
<td>( t_{WP} )</td>
<td>55</td>
<td>75</td>
<td></td>
<td></td>
<td>ns</td>
<td>3</td>
</tr>
<tr>
<td>Address Setup time</td>
<td>( t_{AW} )</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Write Recovery Time</td>
<td>( t_{WR1} )</td>
<td>5</td>
<td>5</td>
<td>ns</td>
<td></td>
<td></td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>( t_{WR2} )</td>
<td>15</td>
<td>15</td>
<td>ns</td>
<td></td>
<td></td>
<td>13</td>
</tr>
<tr>
<td>Output High Z from ( WE )</td>
<td>( t_{OW} )</td>
<td>25</td>
<td>35</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Output Active from ( WE )</td>
<td>( t_{OEW} )</td>
<td>5</td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Data Setup Time</td>
<td>( t_{DS} )</td>
<td>30</td>
<td>40</td>
<td></td>
<td></td>
<td>ns</td>
<td>4</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>( t_{DH1} )</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
<td></td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>( t_{DH2} )</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
<td>13</td>
</tr>
</tbody>
</table>
READ CYCLE

WRITE CYCLE 1

SEE NOTE 1

SEE NOTES 2, 3, 4, 6, 7, 8 and 12
WRITE CYCLE 2

ADDRESS

CE

WE

DOUT

DN

DATA IN STABLE

SEE NOTES 2, 3, 4, 6, 7, 8 and 13

POWER–DOWN/POWER–UP CONDITION

VCC

VTP

3.2V

WE, CE

LEAKAGE CURRENT $I_L$ SUPPLIED FROM LITHIUM CELL

DATA RETENTION TIME $t_{DR}$

SEE NOTE 11
POWER–DOWN/POWER–UP TIMING

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>CE, WE at $V_{IH}$ before Power–Down</td>
<td>$t_{PD}$</td>
<td>0 µs</td>
<td>11 µs</td>
<td>11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$ slew from $V_{TP}$ to 0V</td>
<td>$t_F$</td>
<td>300 µs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$ slew from 0V to $V_{TP}$</td>
<td>$t_R$</td>
<td>300 µs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CE, WE at $V_{IH}$ after Power–Up</td>
<td>$t_{REC}$</td>
<td>2 ms</td>
<td>125 ms</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

($T_A$: See Note 10)

$T_A = 25^\circ C$

**WARNING:**
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES:**
1. WE is high for a Read Cycle.
2. $OE = V_{IH} = V_{IL}$. If $OE = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. $t_{WP}$ is specified as the logical AND of CE and WE. $t_{WP}$ is measured from the latter of CE or WE going low to the earlier of CE or WE going high.
4. $t_{DS}$ is measured from the earlier of CE or WE going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the CE low transition occurs simultaneously with or latter than the WE low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in high impedance state during this period.
8. If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1245 has a built–in switch that disconnects the lithium source until $V_{CC}$ is first applied by the user. The expected $t_{DR}$ is defined as accumulative time in the absence of $V_{CC}$ starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on $V_{CC}$.
12. $t_{WR1, WR2}$ are measured from WE going high.
13. $t_{DH1, DH2}$ are measured from CE going high.
DC TEST CONDITIONS
Outputs Open
Cycle = 200 ns for operating current
All voltages are referenced to ground

AC TEST CONDITIONS
Output Load: 100 pF + 1 TTL Gate
Input Pulse Levels: 0 – 3.0V
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION

DS1245 TT SSS III
Operating Temperature Range
Blank: 0°C to 70°C
IND: –40°C to +85°C
Access Speed
70: 70 ns
100: 100 ns
VCC Tolerance
BL: ±5%
YL: ±10%
Dallas Semiconductor Low Profile Modules must be inserted into 68-pin PLCC sockets for proper operation. Direct surface-mounting of these products by reflow soldering will destroy internal lithium batteries.

For recommended PLCC sockets, contact the Dallas Semiconductor factory.