DALLAS
SEMICONDUCTOR

DS1280
3-Wire to Bytewide Converter Chip

FEATURES

- Adapts JEDEC bytewide memory to a 3-wire serial port
- Supports 512K bytes of memory
- 68-pin version provides arbitration mechanisms for dual port operation
- CMOS circuitry design for battery backup and battery operate applications
- Cyclic redundancy check monitors serial data transmission for error
- Available in 44- or 80-pin quad flat pack for high density requirements

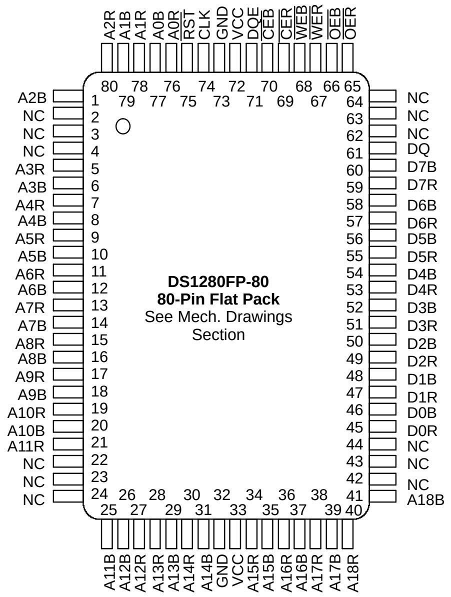
ORDERING INFORMATION

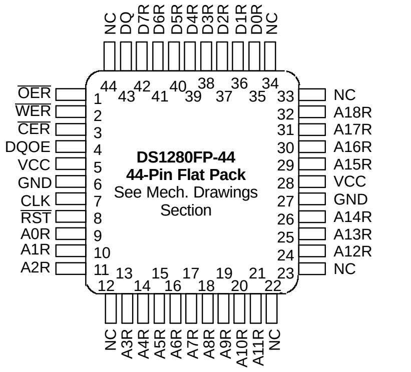
DS1280FP-XX	-80	80-pin Flat Pack
	-44	44-pin Flat Pack

PIN DESCRIPTION

$\overline{\text{RST}}$	–	Reset For Serial Port
DQ	–	Data Input/Output For Serial Port
CLK	–	Clock Input For Serial Port
$\overline{\text{DQE}}$	–	Serial Port Active Output
$\overline{\text{CEB}}$	–	System Bus Enable
$\overline{\text{OEB}}$	–	System Bus Read Enable
$\overline{\text{WEB}}$	–	System Bus Write Enable
A0B-A18B	–	System Address Bus
D0B-D7B	–	System Data Bus
$\overline{\text{CER}}$	–	RAM Chip Enable
$\overline{\text{WER}}$	–	RAM Write Enable
$\overline{\text{OER}}$	–	RAM Output Enable
A0R-A18R	–	RAM Address Bus
D0R-D7R	–	RAM Data Bus
GND	–	Ground
V_{CC}	–	+5 Volts

PIN ASSIGNMENT


A2R A1B A1R A0B A0R RST CLK GND VCC DQE CEB CER WEB WER OEB OER
A2B NC NC NC A3R A3B A4R A4B A5R A5B A6R A6B A7R A7B A8R A8B A9R A9B A10R A10B A11R NC NC NC
NC NC NC DQ D7B D7R D6B D6R D5B D5R D4B D4R D3B D3R D2B D2R D1B D1R D0B D0R NC NC NC A18B
A11B A12B A12R A13R A13B A14R A14B GND VCC A15R A15B A16R A16B A17R A17B A18R
DS1280FP-80
80-Pin Flat Pack
See Mech. Drawings
Section


NC DQ D7R D6R D5R D4R D3R D2R D1R D0R NC
OER WER CER DQOE VCC GND CLK RST A0R A1R A2R
NC A18R A17R A16R A15R VCC GND A14R A13R A12R NC
NC A3R A4R A5R A6R A7R A8R A9R A10R A11R NC
DS1280FP-44
44-Pin Flat Pack
See Mech. Drawings
Section

DESCRIPTION

The DS1280 adds a 3-wire serial port to a bytewide static RAM yet maintains the existing bytewide port. Memory capacity of up to 512K bytes can be addressed directly. Arbitration between the serial and bytewide port is accomplished by handshaking or using predictable idle time as an access window. The serial port requires a 6-byte protocol to set up memory transfers. Cyclic redundancy check circuitry is included to monitor serial data transmission for error.

PIN DESCRIPTION

$\overline{\mathrm{RST}}$ – The 3-wire serial port selection signal input. When RST is low, all communications to the serial port are inhibited. When high, data is clocked into or out of the serial port.

CLK – The clock input signal is used to input or extract data from the 3-wire serial port. A clock cycle is defined as a falling edge followed by a rising edge. Data is driven out onto the 3-wire bus after a falling edge during read cycles and latched into the port on the rising edge during write cycles.

DQ – The DQ signal is the bidirectional data signal for the 3-wire serial port. Byte 0 bit 0 is the first bit input/output.

DQE – The DQE output signal is active (high level) whenever the 3-wire serial port is driving the DQ line. Therefore, this pin will be high whenever data is being read. Otherwise it will be low and the DQ line will be an input. This signal can be used as a means of tri-stating the DQ driver on the other end.

$\overline{\mathrm{CER}}$ – Chip enable output to RAM. This signal is asserted active (low) during RAM read or write cycles. This signal is either derived from the system bus chip enable ($\overline{\mathrm{CEB}}$) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

$\overline{\mathrm{WER}}$ – Write enable output to RAM. This signal is asserted active (low) during RAM write cycles. This signal is either derived from the system bus write enable ($\overline{\mathrm{WEB}}$) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

$\overline{\mathrm{OER}}$ – Output enable to RAM. This signal is asserted active (low) during RAM read cycles. This signal is either derived from the system bus read enable ($\overline{\mathrm{OEB}}$) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

A0R-A18R – Addresses supplied to RAM. These signals allow access to up to 512K bytes of RAM controlled by the DS1280. The addresses are either derived from the system address bus (A0B-A18B) or from the protocol and internal binary counter provided by the 3-wire serial port and associated timing circuits.

D0R–D7R – Data bus supplied to RAM. These eight signals comprise the bidirectional data bus between external bytewide RAM and the DS1280. This data bus is either derived from the system data bus (D0B-D7B) or from the protocol and data stream provided by the 3-wire serial port and associated timing circuits.

$\overline{\mathrm{CEB}}$ – System bus chip enable to the DS1280. This signal is used to generate the RAM chip enable for transfer of data to and from the parallel system bus to RAM (68-pin package only).

$\overline{\mathrm{OEB}}$ – System bus output enable (read) for transfer of data from RAM to the parallel system bus (68-pin package only).

$\overline{\mathrm{WEB}}$ – System bus write enable to the DS1280. This signal is used to generate the RAM write enable for transfer of data from the parallel system bus to the RAM (68-pin package only).

A0B-A18B – System bus addresses to the DS1280. These signals are used to specify the address location for data transfer to and from RAM (68-pin package only).

D0B-D7B – System data bus to and from the DS1280. This bidirectional bus is used to carry data to and from the parallel system bus and RAM (68-pin package only).

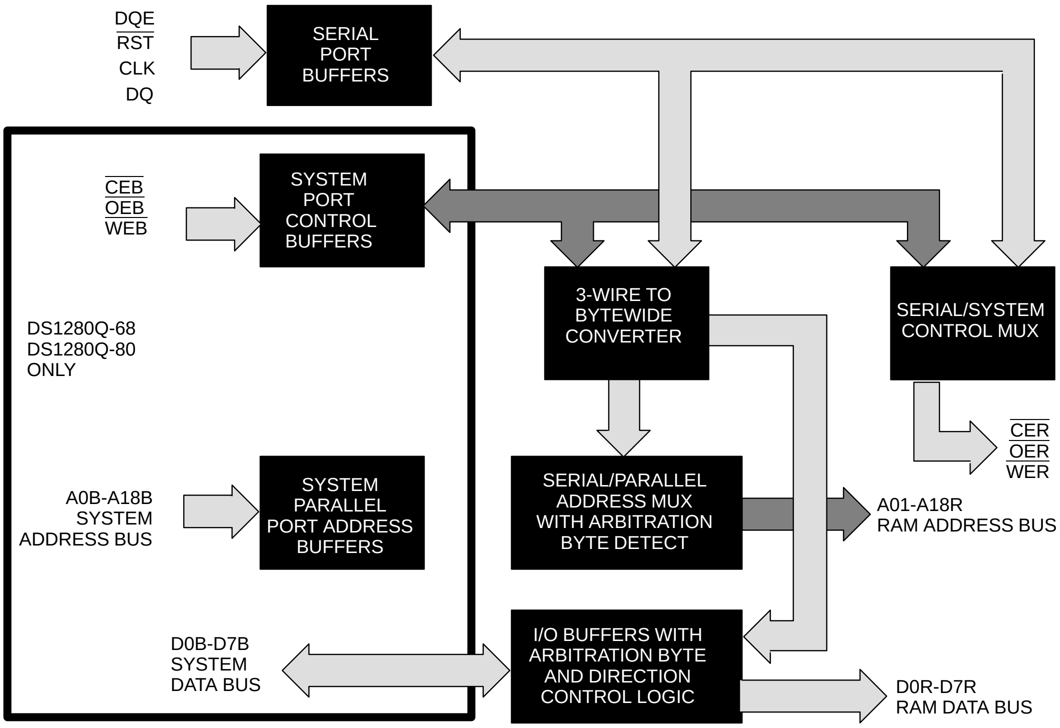
Vcc – +5volt power from the DS1280 (2 pins).

GND – Ground for the DS1280 (2 pins).

OPERATION

Figure 1 illustrates the main elements of the DS1280. As shown, the DS1280 has two major sections: a 3-wire to bytewide converter and a serial/parallel multiplexer. The source of the serial/parallel multiplexer is either a 3–wire serial port or a bytewide system bus. Arbitration of the serial/parallel multiplexer is controlled by signals from the 3-wire to bytewide converter. The 3-wire serial port, therefore, has priority in accessing the RAM and the methods used to avoid collisions are primarily directed by the 3-wire to bytewide converter.

DS1280 BLOCK DIAGRAM Figure 1



SYSTEM BYTEWIDE PARALLEL BUS

If the $\overline{RST}$ signal for the 3-wire serial port is low (inactive), the bytewide parallel port can access associated RAM directly. The bytewide parallel bus addresses (A0B-A18B) and control signals ($\overline{CEB}$, $\overline{OEB}$ and $\overline{WEB}$) are buffered by the DS1280 and become outputs A0R-A18R, $\overline{CER}$, $\overline{OER}$, and $\overline{WER}$ respectively, which are connected directly to RAM. The data input/output signals (D0B-D7B) are internally buffered and sent to RAM on the data input/output signals D0R-D7R. The buffering is designed to handle bidirectional data transfer. Data will be written from the bytewide parallel bus to RAM when $\overline{CEB}$ and $\overline{WEB}$ inputs are both active (low). The $\overline{OEB}$ signal is a ''don't care" signal during a write cycle. Data is read from RAM via the byte wide parallel port when $\overline{CEB}$ and $\overline{OEB}$ signals are both low and $\overline{WEB}$ is high.

3-WIRE SERIAL BUS

If the RST signal for the 3-wire serial port is active (high), the 3-wire to bytewide converter controls the RAM through the control/address/data multiplexers. The 3-wire to bytewide converter uses a 56-bit protocol written serially using $\overline{RST}$, DQ, and CLK to determine the action required and also the starting address location in the RAM to be used. Data is entered into the 3-wire while $\overline{RST}$ is high on the low-to-high transition of the CLK signal provided the data is stable on the DQ line with the proper setup and hold times. The last eight bits of the 56-bit protocol are a cyclic redundancy check byte (CRC) that ensures that all bits of the protocol have been received correctly. If the 56 bits of protocol have not been received correctly, further action will be aborted. The CRC check byte can catch up to three single bit errors within the 56-bit protocol and can also be used on incoming and outgoing serial data streams to check the integrity of data being read or written. More discussion on CRC use and CRC generation will follow later in this text.

PROTOCOL: 3-WIRE SERIAL BUS

The 3-wire serial bus protocol can cause eight different actions to occur as shown in Table 1.

The organization of the 56-bit protocol is shown in Figure 2. As defined, the first byte of the protocol determines whether the action which is to occur involves a read or write. A read function is defined by the binary pattern 11101000. This pattern, therefore, applies to commands 1, 3, 5, and 6 of Table 1. A write function is defined by the binary pattern 00010111. This pattern, therefore, applies to commands 2, 4, 7, and 8 of Table 1. Any other pattern which is entered into the read/write field will cause further action to terminate. Additional differentiation as to which read or write command is determined by the last five bits of the third byte of the protocol called the command field. The control field bits are defined in Table 2 .

A burst read uses a 19-bit address field which consists of the second, third, and bits 0, 1, and 2 of the fourth byte of the protocol to determine the starting address of information to be read from RAM. The byte of data resident in that location is loaded into an 8-bit shift register within the DS1280. The byte of data is then transferred from the shift register to the 3-wire bus by driving the DQ line on the falling edge of the next eight clocks with the LSB first. A burst write uses the same 19-bit address field to determine the starting address of information to be written into RAM. Data is shifted from the DQ line of the 3-wire bus into an 8-bit shift register within the DS1280 on the next eight rising clock edges. After a byte is loaded, the data is written into the RAM location immediately after the rising edge of the eighth clock. Burst reads and writes will continue on a byte-by-byte basis, automatically incrementing the selected address by one location for each successive byte.

PROTOCOL COMMANDS Table 1

1. Burst read
2. Burst write
3. Read protocol select bits
4. Write protocol select bits
5. Burst read masking portions of the protocol select bits
6. Read CRC register
7. Set the address arbitration byte location
8. Poll arbitration byte for status and control

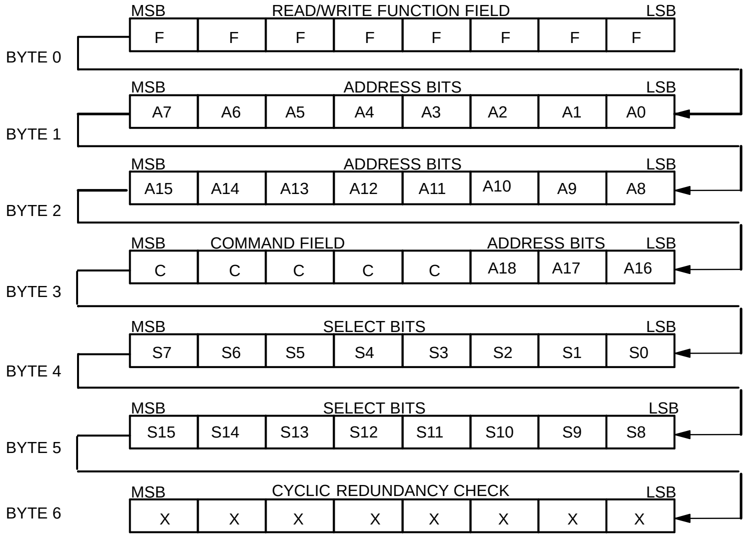
Termination of a current operation will occur at any time when $\overline{RST}$ is taken low. If a byte of data has been loaded into the shift register, a write cycle is allowed to finish, so corrupted data is not written into the RAM. If a full byte of data has not been loaded into the shift register when $\overline{RST}$ goes low, no writing occurs. Reads can be terminated at any point since there is no potential for corruption of data. The read CRC command provides a method for checking the integrity of data sent over the 3-wire bus. The CRC byte resides in the last byte (byte 6) of the protocol. The 8-bit CRC byte not only operates on the protocol bits as they are written in, but also on all data that is written or read from RAM.

After a burst read or write has finished and $\overline{RST}$ has gone low, the final value of the CRC is stored in the DS1280. If a read CRC register command is issued, the stored CRC value is driven onto the DQ line by the first eight clock cycles after the protocol is received. The CRC value generated by the DS1280 should match exactly with the value generated in the host system which is transmitting or receiving data on the other end of the 3-wire bus. If it does not, data has been corrupted and a retransmission should occur. It should be noted that the CRC for the previous transaction can only be obtained if a read CRC command is issued immediately after $\overline{RST}$ goes low to reset the DS1280, then high to accept a read CRC command. If any other sequence is followed, an intermediate CRC will be generated and stored whenever $\overline{RST}$ goes low again, destroying the CRC value of interest. Generation of the CRC byte by the external unit on the 3-wire bus will be covered later in this data sheet.

COMMAND FIELD Table 2

00110	Burst read
10001	Burst write
00011	Read CRC register
10110	Set arbitration byte address to 00000 or 7FFFF
01001	Poll arbitration byte for access to RAM
00101	Read protocol select bits
01110	Write protocol select bits
11XXX	Burst read masking portions of the select bits

PROTOCOL Figure 2



		MSB		READ/WRITE FUNCTION FIELD					LSB
BYTE 0		F	F	F	F	F	F	F	F
		MSB		ADDRESS BITS					LSB
BYTE 1		A7	A6	A5	A4	A3	A2	A1	A0
		MSB		ADDRESS BITS					LSB
BYTE 2		A15	A14	A13	A12	A11	A10	A9	A8
		MSB	COMMAND FIELD				ADDRESS BITS		LSB
BYTE 3		C	C	C	C	C	A18	A17	A16
		MSB		SELECT BITS					LSB
BYTE 4		S7	S6	S5	S4	S3	S2	S1	S0
		MSB		SELECT BITS					LSB
BYTE 5		S15	S14	S13	S12	S11	S10	S9	S8
		MSB		CYCLIC REDUNDANCY CHECK					LSB
BYTE 6		X	X	X	X	X	X	X	X

In any 2-port system there is a potential for access collisions. To solve this problem, an arbitration byte is provided so that the serial and parallel ports of the DS1280 can determine the status of the other port. A special byte in RAM address space is reserved to allow for handshaking between the two ports. This arbitration byte has a special attribute in that it is simultaneously accessible by both ports.

Two commands are used by the 3-wire serial port protocol to manage the arbitration byte. First, since this byte will create a hole in RAM address space for the parallel bytewide port, a command is added to move the arbitration byte to either address location ‘‘00000” or address location “7FFFF.” When setting the arbitration byte address location, the correct read/write field and command field must be entered along with all zeroes or all ones in the address field. It is important to note that the arbitration byte is located in the parallel memory location assigned by the serial port using the appropriate commands. However, the physical byte of RAM is located within the DS1280. The existence of this physical byte is transparent to the bytewide parallel port and looks like normal RAM space with some read/write restriction. However, the serial port can still address the actual RAM location at either 00000 or 7FFFF in addition to accessing the arbitration byte.

The second command used by the 3-wire serial port provides for polling of the arbitration byte to determine the status of the parallel port. In addition, the arbitration byte can be set to indicate to the parallel port that the serial port is taking over the RAM. The second command protocol allows the serial port to do a compressed read-write-read operation that causes the arbitration byte to be read by the first eight clocks following the protocol. The next eight clocks cause data to be written into the arbitration byte, and the last eight clock cycles allow for a second read of the data for verification. The 24 cycles occur by entering the 56-bit protocol only once. The protocol pattern entered is a write function in the read/write field (00010111) and the correct command field.

SELECT BITS

Three other commands are used to set the select bits in the protocol. Once the select bits are set to a binary value they must be matched exactly when protocol is sent or further activity is prevented. The bits allow for 65,536 different binary combinations. Therefore, multiple DS1280s can be connected on the same serial bus and only the appropriate device will respond. To write the select bits, a write function in the read/write field is required along with the appropriate command in the command field.

To read the select bits, a read cycle in the read/write field is required along with the appropriate command in the command field. The arrangement of reading and writing select bits allows the user to have multiple DS1280s in use and uniquely identify each. A read can occur successfully without knowing the select bits but a write cannot occur without matching the current select field.

A third command masking specific select bits provides a means for determining the identity of a specific DS1280 when more than one is used. A read in the read/write field and a "11000" in the command field will execute a mask read that ignores all select bits to determine the presence of one or more DS1280s. With the detection of at least one device, a search can begin by masking all but a single pair of DS1280 select bits. A read in the read/write field and a "11001" in the command field will unmask the first two LSBs of byte 4 of the select bits (see Figure 3). With these two select bits unmasked, only an exact match of four possible combinations of these two select bits will allow access through the 3-wire port to RAM. The combinations are 00, 01, 10, and 11. Therefore, repeating the unmasking of the first two bits of the select field up to four times will give the binary value of these select bits.

Having determined the first two select bits, the next two select bits can be unmasked, and the process of matching one of four combinations can proceed as before. Repetition of unmasking select bit pairs will yield an exact match of 65,536 possible DS1280s in no more than 32 attempts.

ARBITRATION

As mentioned earlier, one byte of RAM has been reserved for arbitration between the 3-wire port and the bytewide parallel bus. The location of this byte within the memory map will be at address 00000 or at address 7FFFF as determined by the protocol input from the 3-wire serial port. The arbitration byte has special restrictions and disciplines so that the 3-wire serial bus and the bytewide parallel bus are never in contention for RAM access. This byte is shown in Figure 4.

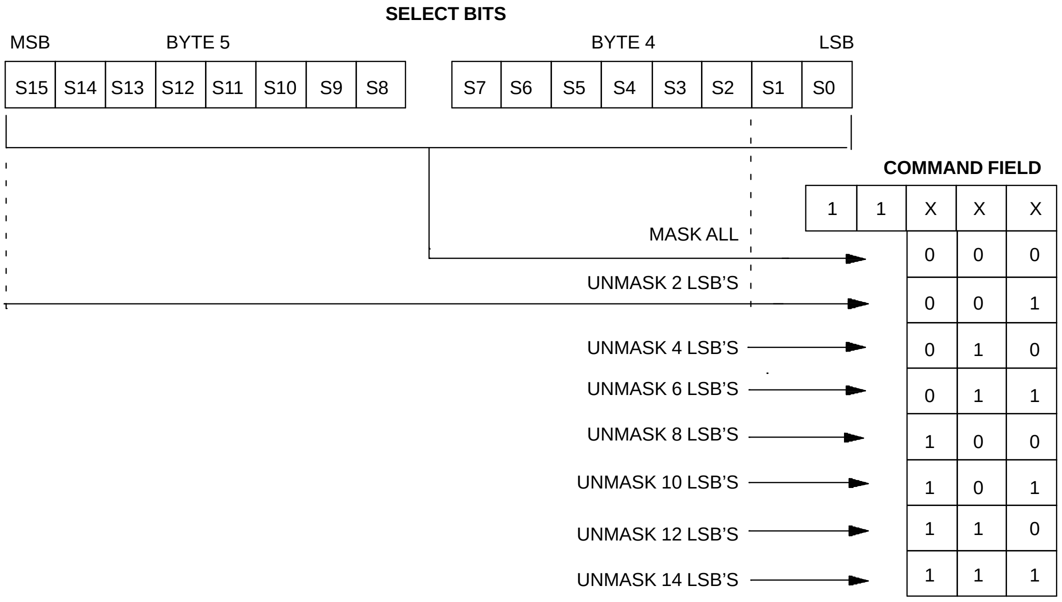
As defined, the 3-wire serial port can read the whole byte but can only write bits S2-S0. The bytewide parallel port can read the whole byte but can only write bits B1-B0. An internal counter controls bits C2-C0 that cannot be written by either port. Arbitration is accomplished when the status bits are read and written by the respective ports. If the 3-wire serial port wants to access RAM, the arbitration byte should be polled by the serial port until bit B1 equals zero. If B1 equals zero, the 3-wire serial port should then write a one into bit S2. After the write of bit S2, the 3-wire serial port should then read the arbitration byte to confirm that B1=0 and S2=1. This operation must be executed with the protocol for the compressed read/write/read sequence which minimizes overhead.

The 3-wire serial port should always abort any attempt to access RAM if B1 equals one. When the 3-wire serial port completes any transfer of data to or from RAM, bit S2 should be written back to zero so that the bytewide parallel port will know that the 3-wire serial port is not using the RAM. The bytewide serial bus can gain access to RAM by polling the arbitration byte until S2 bit equals zero. When S2 equals zero, the bytewide parallel port then writes a one into bit B1. A read cycle verifying that S2 equals zero and B1 equals one confirms that the bytewide parallel port has access to RAM. The bytewide parallel port can then read or write RAM as required. When the entire transaction is complete, the bytewide parallel port should write the B1 bit to zero, signaling the 3-wire serial port that the RAM is not in use.

The bits B0, S1, and S0 can be defined by the user to pass additional arbitration information, making possible more elaborate handshaking schemes between the two ports. Some typical uses for these bits could be an indication that a port desires access to RAM or the amount of RAM written. Another method of arbitration between the 3-wire serial port and the bytewide parallel bus is the use of the count bits C0-C2. The 3-wire port reads or writes from RAM only once every eight clock cycles. This action occurs when the internal byte counter transitions from a "111" state to a "000" state. The access occurs regardless of the arbitration byte status bits. C0-C2 are updated as the internal serial bit counter is incremented. The bytewide port can execute reads or writes depending on the status of C0-C2. These bits indicate the number of bits the 3-wire serial port has loaded and, therefore, indicate when a read or write will occur from the 3-wire port.

Since the 3-wire port always reads or writes at the ends of a byte (C0-C2 = 1) the bytewide parallel bus should never access RAM if the count bits read all ones. The bytewide parallel port can determine the minimum time left before the 3-wire serial port will access the memory from the count bits and the minimum clock cycle applied to the 3-wire clock input. Essentially the 3-wire serial port is given priority on access to RAM and the bytewide parallel port determines when it can access the RAM to avoid colliding with the 3-wire serial port.

SELECT BITS MASK Figure 3



ARBITRATION BYTE Figure 4

MSB							LSB
P1	P0	S2	S1	S0	C2	C1	C0
PARALLEL BUS STATUS BITS	NOT USED	SERIAL PORT STATUS BITS	NOT USED	NOT USED	COUNT BIT	COUNT BIT	COUNT BIT

CRC GENERATION

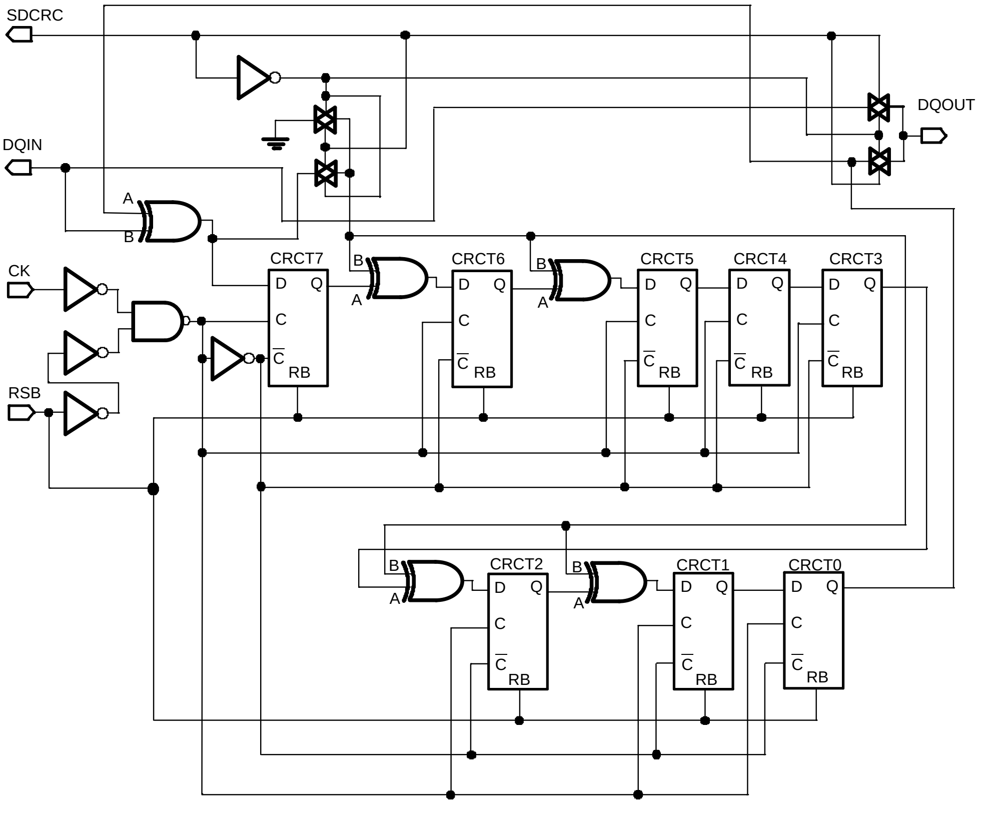
The logic involved in CRC generation is shown in Figure 5. It is comprised of an 8-bit shift register, four exclusive OR gates, and two sets of transmission gates. The transmission gates serve to divert data from DQIN to the CRC generator while each byte is being assembled and, at the same time, output data to the output (DQ OUT). When input select CRC (SDCRC) is driven to an active level (high), data is output at DQOUT from the CRC generator using the clock input (CK) in the same manner as described earlier for operation of the 3-wire serial bus.

The reset signal (RSB) must be high while the CRC generator is being used, as an inactive state will disable the 8-bit shift register. This signal is the same as the reset described for the 3-wire serial bus. A CRC generator for serial port communications can be constructed as described above to satisfy the DS1280 CRC requirements. However, another approach is to generate the CRC using software. An example of how this is accomplished using assembly language follows. This assembly language code is written for the DS5000 Soft Microcontroller. The assembly language procedure DO CRC given below calculates the cumulative CRC of all the bytes passed to it in the accumulator. Before it is used to calculate the CRC of a data stream, it should be initialized by setting the variable CRC to zero. Each byte of the data is then placed in the accumulator and DO CRC is called to update the CRC. After all the data has been passed to DO CRC, the variable CRC will contain the result.

CRC GENERATION LOGIC Table 3

```
DO_CRC:
          PUSH      ACC                     ; Save the Accumulator
          PUSH      B                       ; Save the B register
          PUSH      ACC                     ; Save bits to be shifted
          MOV       B,          #8          ; Set to shift eight bits
CRC_LOOP:
          XRL       A,          CRC         ; Calculate DQIN xor CRCTO
          RRC       A                       ; Move it to the last
          MOV       A,          CRC         ; Get the last CRC value
          JNC       ZERO                    ; Skip if DQIN xor CRCTO = 0
          XRL       A,          #0CCH       ; Update the CRC value
ZERO:
          RRC       A                       ; Position the new CRC
          MOV       CRC,        A           : Store the new CRC
          POP       ACC                     : Get the remaining bits
     ,    RR        A                       ; Position next bit in LSB
          PUSH      ACC                     ; Save the remaining bits
          DJNZ      B,          CRC_LOOP    ; Repeat for eight bits
          POP       ACC                     ; Clean up the stack
          POP       B                       ; Restore the B register
          POP       ACC                     ; Restore the Accumulator
          RET                               ; Return
```

CRC GENERATION Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to+125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (t_A=0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply	V_{CC}	3.25	5.0	6.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3V	V	
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS (t_A=0°C to 70°C ; V_{CC}=+5V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1		+1	µA	9
Output Leakage	I_{LO}			1	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}	+2			mA	
Supply Current	I_{CC1}			15	mA	2
Supply Current	I_{CC2}			50	mA	3

AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%; 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	4
Data to CLK Hold	t_{CDH}	40			ns	4
Data to CLK Delay	t_{CDD}			125	ns	4,5,6
CLK Low Time	t_{CL}	500			ns	4
CLK High Time	t_{CH}	500			ns	4
CLK Frequency	f_{CLK}	DC		1	MHz	4,10
CLK Rise & Fall Time	$t_R t_F$			100	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	4
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	4
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	4
$\overline{RST}$ to D/Q High Z	t_{CDZ}			50	ns	4,6
Serial Port Active	t_{DI}			25	ns	4,6
Serial Port Inactive	t_{DI}			25	ns	4,6
Parallel Port Propagation	t_{PD}		12	20	ns	4,6,8

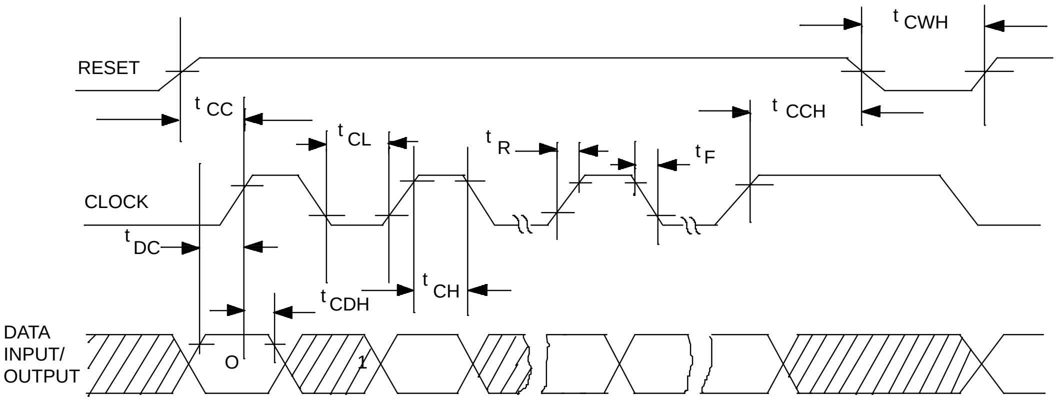
CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			15	pF	

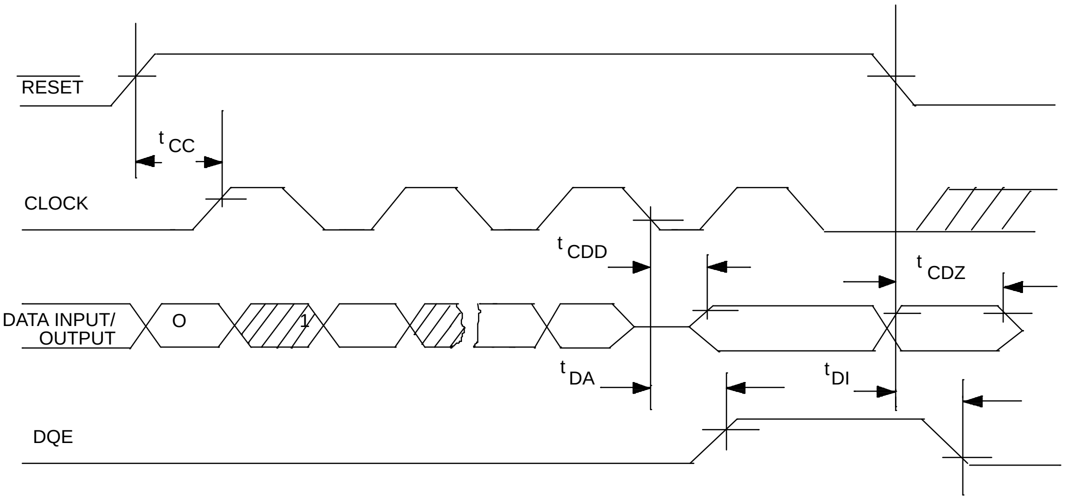
NOTES:

1. All voltages are referenced to ground.
2. I_{CC1} is measured with all outputs open and both the 3-wire serial port or the bytewide parallel port inactive.
3. I_{CC2} is measured with all outputs open.
4. Measured at V_{IH} = 2.0 V or V_{IL} = 0.8V and 10ns maximum rise and fall time.
5. Measured at V_{OH}= 2.4 V and V_{OL} = 0.4V.
6. Measured with a load capacitance of 50 pF.
7. The 3-wire serial port will correctly read and write any static RAM with an effective access time of 200ns.
8. Propagation delay is the same for data going either way on the bytewide parallel bus.
9. Pins A0B through A18B, $\overline{RST}$, DQ, $\overline{CEB}$ have pulldown resistors which will leak approximately 50 µA.
10. Arbitration byte must be accessed at a maximum clock frequency of 500 KHz with a symmetrical waveform.

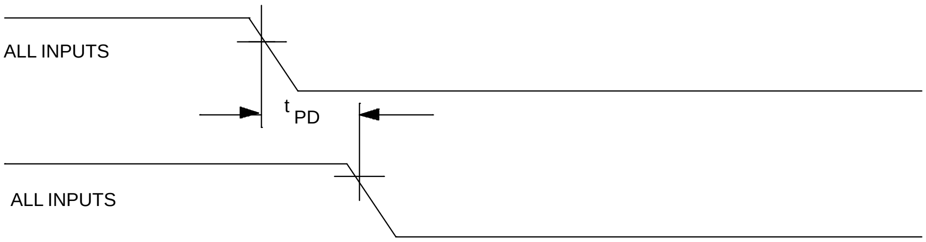
TIMING DIAGRAM: WRITE DATA TRANSFER 3-WIRE SERIAL PORT (7)



TIMING DIAGRAM: READ DATA TRANSFER 3-WIRE SERIAL PORT (7)



PROPAGATION DELAY: DATA TRANSFER: BYTEWIDE PARALLEL DATA BUS (8)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