DS1321 Flexible Nonvolatile Controller with Lithium Battery Monitor

FEATURES

- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write–protects SRAM when VCC is out of tolerance
- Automatically switches to battery backup supply when VCC power failure occurs
- Flexible memory organization
  - Mode 0: 4 banks with 1 SRAM each
  - Mode 1: 2 banks with 2 SRAMs each
  - Mode 2: 1 bank with 4 SRAMs each
- Monitors voltage of a lithium cell and provides advanced warning of impending battery failure
- Signals low–battery condition on active low Battery Warning output signal
- Resets processor when power failure occurs and holds processor in reset during system power–up
- Optional –5% or –10% power fail detection
- 16–pin DIP, 16–pin SOIC and 20–pin TSSOP packages
- Industrial temperature range of –40°C to +85°C.

PIN DESCRIPTION

VCCI – +5V Power Supply Input
VCCO – SRAM Power Supply Output
VBAT – Backup Battery Input
A, B – Address Inputs
CE0 – CE4 – Chip Enable Inputs
CEO1 – CEO4 – Chip Enable Outputs
TOL – VCC Tolerance Select
BW – Battery Warning Output (Open Drain)
RST – Reset Output (Open Drain)
MODE – Mode Input
GND – Ground
NC – No Connection

PIN ASSIGNMENT

DS1321 16–PIN DIP (300 MIL)

DS1321S 16–PIN SOIC (150 MIL)

DS1321E 20–PIN TSSOP
DESCRIPTION
The DS1321 Flexible Nonvolatile Controller with Lithium Battery Monitor is a CMOS circuit which solves the application problem of converting CMOS SRAMs into nonvolatile memory. Incoming power is monitored for an out–of–tolerance condition. When such a condition is detected, chip enable outputs are inhibited to accomplish write protection and the battery is switched on to supply the SRAMs with uninterrupted power. Special circuitry uses a low–leakage CMOS process which affords precise voltage detection at extremely low battery consumption. One DS1321 can support as many as four SRAMs arranged in any of three memory configurations.

In addition to battery–backup support, the DS1321 performs the important function of monitoring the remaining capacity of the lithium battery and providing a warning before the battery reaches end–of–life. Because the open–circuit voltage of a lithium backup battery remains relatively constant over the majority of its life, accurate battery monitoring requires loaded–battery voltage measurement. The DS1321 performs such measurement by periodically comparing the voltage of the battery, as it supports an internal resistive load, with a carefully selected reference voltage. If the battery voltage falls below the reference voltage under such conditions, the battery will soon reach end–of–life. As a result, the Battery Warning pin is activated to signal the need for battery replacement.

MEMORY BACKUP
The DS1321 performs all the circuit functions required to provide battery–backup for as many as four SRAMs. First, the device provides a switch to direct power from the battery or the system power supply (VCC). Whenever VCC is less than the VCC trip point and VCC is less than the battery voltage VBAT, the battery is switched in to provide backup power to the SRAM. This switch has voltage drop of less than 0.2 volts.

Second, the DS1321 handles power failure detection and SRAM write–protection. VCC is constantly monitored, and when the supply goes out of tolerance, a precision comparator detects power failure and inhibits the four chip enable outputs in order to write–protect the SRAMs. This is accomplished by holding CE0 through CE3 to within 0.2 volts of VCCO when VCC is out of tolerance. If any CE is active (low) at the time that power failure is detected, the corresponding CE signal is kept low until the CE signal is brought high again. Once the CE signal is brought high, the CBO signal is taken high and held high until after VCC has returned to its nominal voltage level. If the CE signal is not brought high by 1.5 µs after power failure is detected, the corresponding CBO is forced high at that time. This specific scheme for delaying write protection for up to 1.5 µs guarantees that any memory access in progress when power failure occurs will complete properly. Power failure detection occurs in the range of 4.75 to 4.5 volts (5% tolerance) when the TOL pin is wired to GND or in the range of 4.5 to 4.25 volts (10% tolerance) when TOL is connected to VCCO.
MEMORY CONFIGURATIONS

The DS1321 can be configured via the MODE pin for three different arrangements of the four attached SRAMs. The state of the MODE pin is latched at $V_{CCI} = V_{CCTP}$ on power up. See Figure 1 for details.

**MEMORY CONFIGURATIONS Figure 1**

- **MODE = GND (4 BANKS WITH 1 SRAM EACH):**

- **MODE = $V_{CCO}$ (2 BANKS WITH 2 SRAM EACH):**

- **MODE FLOATING (1 BANK WITH 4 SRAMs):**
BATTERY VOLTAGE MONITORING

The DS1321 automatically performs periodic battery voltage monitoring at a factory-programmed time interval of 24 hours. Such monitoring begins within $t_{REC}$ after $V_{CCI}$ rises above $V_{CCTP}$ and is suspended when power failure occurs.

After each 24 hour period ($t_{BTCN}$) has elapsed, the DS1321 connects $V_{BAT}$ to an internal $1\Omega$ test resistor ($R_{INT}$) for one second ($t_{BTPW}$). During this one second, if $V_{BAT}$ falls below the factory-programmed battery voltage trip point ($V_{BTP}$), the battery warning output $BW$ is asserted. While $BW$ is active, battery testing will be performed with period $t_{TCW}$ to detect battery removal and replacement. Once asserted, $BW$ remains active until the battery is physically removed and replaced by a fresh cell. The battery is still retested after each $V_{CC}$ power-up, however, even if $BW$ was active on power-down. If the battery is found to be higher than $V_{BTP}$ during such testing, $BW$ is deasserted and regular 24-hour testing resumes. $BW$ has an open-drain output driver.

Battery replacement following $BW$ activation is normally done with $V_{CCI}$ nominal so that SRAM data is not lost. During battery replacement, the minimum time duration between old battery detachment and new battery attachment ($t_{BDBA}$) must be met or $BW$ will not deactivate following attachment of the new battery. Should $BW$ not deactivate for this reason, the new battery can be detached for $t_{BDBA}$ and then re-attached to clear $BW$.

NOTE: Battery monitoring is only a useful technique when testing can be done regularly over the entire life of a lithium battery. Because the DS1321 only performs battery monitoring when $V_{CC}$ is nominal, systems which are powered-down for excessively long periods can completely drain their lithium cells without receiving any advanced warning. To prevent such an occurrence, systems using the DS1321 battery monitoring feature should be powered-up periodically (at least once every few months) in order to perform battery testing. Furthermore, anytime $BW$ is activated on the first battery test after a power-up, data integrity should be checked via checksum or other technique.

POWER MONITORING

The DS1321 automatically detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When $V_{CCI}$ falls below the trip point level defined by the TOL pin ($V_{CCTP}$), the $V_{CCI}$ comparator activates the reset signal $RST$. Reset occurs in the range of 4.75 to 4.5 volts (5% tolerance) when the TOL pin is connected to GND or in the range of 4.5 to 4.25 volts (10% tolerance) when TOL is connected to $V_{CCO}$.

$RST$ also serves as a power-on reset during power-up. After $V_{CCI}$ exceeds $V_{CCTP}$, $RST$ will be held active for 200 ms nominal ($t_{RPU}$). This reset period is sufficiently long to prevent system operation during power-on transients and to allow $t_{REC}$ to expire. $RST$ has an open-drain output driver.

FRESHNESS SEAL MODE

When the battery is first attached to the DS1321 without $V_{CC}$ power applied, the device does not immediately provide battery-backup power on $V_{CCO}$. Only after $V_{CCI}$ exceeds $V_{CCTP}$ and later falls below both $V_{CCTP}$ and $V_{BAT}$ will the DS1321 leave Freshness Seal Mode and provide battery-backup power. This mode allows a battery to be attached during manufacturing but not used until after the system has been activated for the first time. As a result, no battery energy is drained during storage and shipping.
FUNCTIONAL BLOCK DIAGRAM Figure 2

- MODE
- CEIT
- CEO1
- CEO2
- CEO3
- CEO4
- RST

- V CCI
- 1.2 MΩ
- +
- –
- V CCTP REF
- TOL

- V CCO
- –
- +
- V BTP REF
- V BAT

- CURRENT-LIMITING RESISTOR
- REDUNDANT SERIES FET
- BATTERY CHARGING/SHORTING PROTECTION CIRCUITRY

- B/CEI4
- A/CEI3
- CEI2
- CEI1

- BATTERY WARNING CONTROL CIRCUITRY
ABSOLUTE MAXIMUM RATINGS*
Voltage on Any Pin Relative to Ground -0.5V to +7.0V
Operating Temperature -40°C to +85°C
Storage Temperature -55°C to +125°C
Soldering Temperature 260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS
(–40°C to +85°C)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage TOL=GND</td>
<td>V CCI</td>
<td>4.75</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Supply Voltage TOL=V CCO</td>
<td>V CCI</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Battery Supply Voltage</td>
<td>V BAT</td>
<td>2.0</td>
<td>3.0</td>
<td>6.0</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Logic 1 Input</td>
<td>V IH</td>
<td>2.0</td>
<td></td>
<td>V CCI+0.3</td>
<td>V</td>
<td>1, 12</td>
</tr>
<tr>
<td>Logic 0 Input</td>
<td>V IL</td>
<td>-0.3</td>
<td></td>
<td>+0.8</td>
<td>V</td>
<td>1, 12</td>
</tr>
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</table>

DC ELECTRICAL CHARACTERISTICS
(–40°C to +85°C; V CCI ≥ V CCTP)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
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<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Current (TTL inputs)</td>
<td>ICC1</td>
<td></td>
<td>1.5</td>
<td>mA</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>Operating Current (CMOS inputs)</td>
<td>ICC2</td>
<td>100</td>
<td>150</td>
<td>µA</td>
<td>2, 5</td>
<td></td>
</tr>
<tr>
<td>RAM Supply Voltage</td>
<td>V CCO</td>
<td>V CCI–0.2</td>
<td></td>
<td>V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>RAM Supply Current</td>
<td>ICCO1</td>
<td>185</td>
<td>mA</td>
<td></td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Supply Current</td>
<td>ICCO2</td>
<td>260</td>
<td>mA</td>
<td></td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>V CC Trip Point (TOL=GND)</td>
<td>V CCTP</td>
<td>4.50</td>
<td>4.62</td>
<td>4.75</td>
<td>V</td>
<td>1</td>
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<tr>
<td>V CC Trip Point (TOL=V CCO)</td>
<td>V CCTP</td>
<td>4.25</td>
<td>4.37</td>
<td>4.50</td>
<td>V</td>
<td>1</td>
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<tr>
<td>V BAT Trip Point</td>
<td>V BTP</td>
<td>2.50</td>
<td>2.6</td>
<td>2.70</td>
<td>V</td>
<td>1</td>
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<tr>
<td>Output Current @ 2.4V</td>
<td>I OH</td>
<td>-1</td>
<td></td>
<td>mA</td>
<td>7, 10</td>
<td></td>
</tr>
<tr>
<td>Output Current @ 0.4V</td>
<td>I OL</td>
<td>4</td>
<td></td>
<td>mA</td>
<td>7, 10</td>
<td></td>
</tr>
<tr>
<td>Input Leakage</td>
<td>I IL</td>
<td>-1.0</td>
<td>+1.0</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Leakage</td>
<td>I LO</td>
<td>-1.0</td>
<td>+1.0</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Battery Monitoring Test Load</td>
<td>R INT</td>
<td>0.8</td>
<td>1.2</td>
<td>1.5</td>
<td>MΩ</td>
<td></td>
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</table>
### DC Electrical Characteristics

(-40°C to +85°C; \( V_{CCI} < V_{BAT}, V_{CCI} < V_{CCTP} \))

<table>
<thead>
<tr>
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<th>MAX</th>
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<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Battery Current</td>
<td>( I_{BAT} )</td>
<td>100</td>
<td>nA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Battery Backup Current</td>
<td>( I_{CCO3} )</td>
<td>500</td>
<td>( \mu )A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>( V_{CCO} )</td>
<td>( V_{BAT} - 0.2 )</td>
<td>V</td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>CEO Output</td>
<td>( V_{OHL} )</td>
<td>( V_{BAT} - 0.2 )</td>
<td>V</td>
<td></td>
<td></td>
<td>1, 8</td>
</tr>
</tbody>
</table>

### Capacitance

\((t_A=25°C)\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Capacitance</td>
<td>( C_{IN} )</td>
<td>7</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>( C_{OUT} )</td>
<td>7</td>
<td>pF</td>
<td></td>
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</table>

### AC Electrical Characteristics

(-40°C to +85°C; \( V_{CCI} > V_{CCTP} \))

<table>
<thead>
<tr>
<th>PARAMETER</th>
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<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
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</thead>
<tbody>
<tr>
<td>CEI to CEO Propagation Delay</td>
<td>( t_{PD} )</td>
<td>12</td>
<td>20</td>
<td>ns</td>
<td></td>
<td>11</td>
</tr>
<tr>
<td>CE Pulse Width</td>
<td>( t_{CE} )</td>
<td>1.5</td>
<td>( \mu )s</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC Valid to End of Write Protection</td>
<td>( t_{REC} )</td>
<td>125</td>
<td>ms</td>
<td></td>
<td></td>
<td>9</td>
</tr>
<tr>
<td>VCC Valid to CEI Inactive</td>
<td>( t_{IR} )</td>
<td>2</td>
<td>ms</td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>VCC Valid to RST Inactive</td>
<td>( t_{IRF} )</td>
<td>150</td>
<td>200</td>
<td>350</td>
<td>ms</td>
<td>10</td>
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</table>

### AC Electrical Characteristics

(-40°C to +85°C; \( V_{CCI} < V_{CCTP} \))

<table>
<thead>
<tr>
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<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC Slew Rate</td>
<td>( t_{F} )</td>
<td>150</td>
<td>( \mu )s</td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>VCC Fail Detect to RST Active</td>
<td>( t_{RPD} )</td>
<td>15</td>
<td>( \mu )s</td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>VCC Slew Rate</td>
<td>( t_{R} )</td>
<td>15</td>
<td>( \mu )s</td>
<td></td>
<td></td>
<td>10</td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

(-40°C to +85°C; \( V_{CCI} \geq V_{CCTP} \))

<table>
<thead>
<tr>
<th>PARAMETER</th>
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<th>MAX</th>
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<th>NOTES</th>
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</thead>
<tbody>
<tr>
<td>Battery Test to BW Active</td>
<td>( t_{BW} )</td>
<td>1</td>
<td>s</td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>Battery Test Cycle–Normal</td>
<td>( t_{BTCN} )</td>
<td>24</td>
<td>hr</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Battery Test Cycle–Warning</td>
<td>( t_{BTCW} )</td>
<td>5</td>
<td>s</td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>Battery Test Pulse Width</td>
<td>( t_{BTPW} )</td>
<td>1</td>
<td>s</td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>Battery Detach to Battery Attach</td>
<td>( t_{DBA} )</td>
<td>7</td>
<td>s</td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>Battery Attach to BW Inactive</td>
<td>( t_{BABW} )</td>
<td>1</td>
<td>s</td>
<td></td>
<td></td>
<td>10</td>
</tr>
</tbody>
</table>
NOTE:
If $V_{BAT} > V_{CTP}$, $V_{CCO}$ will begin to slew with $V_{CCI}$ when $V_{CCI} = V_{CTP}$. 
TIMING DIAGRAM: POWER DOWN

NOTE:
If $V_{BAT} > V_{CCTP}$, $V_{CCO}$ will slew down with $V_{CCI}$ until $V_{CCI} = V_{CCTP}$. 

NOTE:
\( t_{BW} \) is measured from the expiration of the internal timer to the activation of the battery warning output BW.

TIMING DIAGRAM: BATTERY REPLACEMENT
NOTES:
1. All voltages referenced to ground.
3. $I_{CCO1}$ is the maximum average load which the DS1321 can supply to attached memories at $V_{CCO} \geq V_{CCI} - 0.2V$.
4. $I_{CCO2}$ is the maximum average load which the DS1321 can supply to attached memories at $V_{CCO} \geq V_{CCI} - 0.3V$.
5. All inputs within 0.3V of ground or $V_{CCI}$.
6. $I_{CCO3}$ is the maximum average load current which the DS1321 can supply to the memories in the battery backup mode at $V_{CCO} \geq V_{BAT} - 0.2V$.
7. Measured with a load as shown in Figure 1.
8. Chip Enable Outputs CEO1 – CEO4 can only sustain leakage current in the battery backup mode.
9. CEO1 through CEO4 will be held high for a time equal to $t_{REC}$ after $V_{CCI}$ crosses $V_{CCTP}$ on power–up.
10. BW and RST are open drain outputs and, as such, cannot source current. External pull–up resistors should be connected to these pins for proper operation. Both BW and RST can sink 10 mA.
11. $t_{CE}$ maximum must be met to ensure data integrity on power down.
12. In battery backup mode, inputs must never be below ground or above $V_{CCO}$.

DC TEST CONDITIONS
Output Load: See below
All voltages are referenced to ground

AC TEST CONDITIONS
Output Load: See below
Input Pulse Levels: 0 – 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

OUTPUT LOAD Figure 3

*INCLUDING SCOPE AND JIG CAPACITANCE
DATA SHEET REVISION SUMMARY
The following represent the key differences between 03/26/96 and 06/12/97 version of the DS1321 data sheet. Please review this summary carefully.

1. Changed I_{CCO1} from 200 to 185 mA max
2. Changed I_{CCO2} from 350 to 260 mA max
3. Changed V_{TP} from 2.55 – 2.65V to 2.50 – 2.70V
4. Changed R_{IM} from 1.0 typ to 1.2 MΩ and 1.4 max to 1.5 MΩ
5. Changed t_{PD} from 5 typ, 15 max to 12 typ, 20 max
6. Changed t_{RP} units from ns to µs
7. Changed block diagram to show U.L. compliance

The following represent the key differences between 06/12/97 and 09/29/97 version of the DS1321 data sheet. Please review this summary carefully.

1. Changed AC test conditions

The following represent the key differences between 09/29/97 and 12/12/97 version of the DS1321 data sheet. Please review this summary carefully.

1. Removed preliminary from title bar.
2. Specified which inputs and outputs are relevant for C_{IN} and C_{OUT} specs. This is not a change, just a clarification.