DALLAS SEMICONDUCTOR

DS1395/DS1397
RAMified Real Time Clock

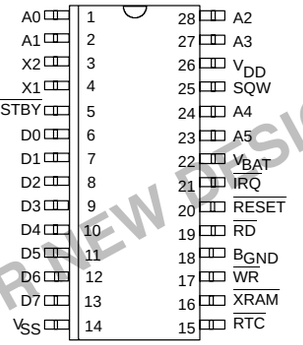
FEATURES

- Ideal for EISA bus PCs
- Functionally compatible with MC146818 in 32 KHz mode
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Binary or BCD representations of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Interfaced with software as 64 register/RAM locations plus 4K x 8 of static RAM
  - 14 bytes of clock and control registers
  - 50 bytes of general and control registers
  - Separate 4K x 8 nonvolatile SRAM
- Programmable square wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable:
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End-of-clock update cycle
- 28-pin JEDEC footprint
- Available as chip (DS1395/DS1395S) or stand alone module with embedded lithium battery and crystal (DS1397)

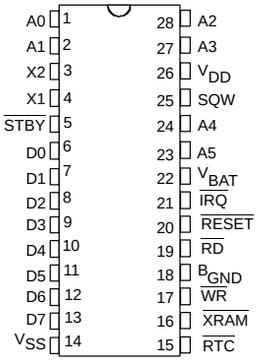
ORDERING INFORMATION

DS1395	RTC Chip; 28–pin DIP
DS1395S	RTC Chip; 28–pin SOIC
DS1397	RTC Module; 28–pin DIP

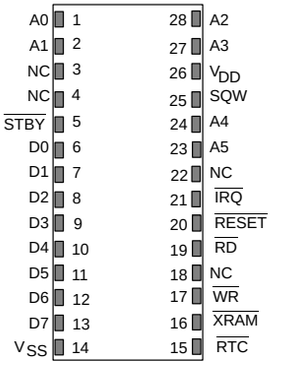
PIN ASSIGNMENT



DS1395S 28-Pin SOIC (330 mil)



DS1395 28-Pin DIP (600 mil)



DS1397 28-Pin Encapsulated Package (720 mil)

PIN DESCRIPTIONS

V_{DD}, V_{SS} – Bus operational power is supplied to the part via these pins. The voltage level present on these pins should be monitored to transition between operational power and battery power.

D0-D7 – Data Bus (bidirectional): Data is written into the device from the data bus if either $\overline{XRAM}$ or $\overline{RTC}$ is asserted during a write cycle at the rising edge of a $\overline{WR}$ pulse. Data is read from the device and driven onto the data bus if either $\overline{XRAM}$ or $\overline{RTC}$ is asserted during a read cycle when the $\overline{RD}$ signal is low.

A0-A5 – Address Bus (input): Various internal registers of the device are selected by these lines. When $\overline{RTC}$ is asserted, A0 selects between the indirect address register and RTC data register. When the $\overline{XRAM}$ is asserted, A0-A5 addresses a 32–byte page of RAM. When A5 is high, the RAM page register is accessible. When A5 is low, A0-A4 address the 32-byte page of RAM.

$\overline{RD}$ - Read Strobe (input): Data is read from the selected register and driven onto the data bus by the device when this line is low and either $\overline{RTC}$ or $\overline{XRAM}$ is asserted.

$\overline{WR}$ - Write Strobe (input): Data is written into the device from the data bus on the rising edge after a low pulse on this line when the device has been selected by either the $\overline{XRAM}$ or $\overline{RTC}$ signals.

$\overline{STBY}$ - Standby (input): Accesses to the device are inhibited and outputs are tri-stated to a high impedance state when this signal is asserted low. All data in RAM of the device is preserved. The real time clock continues to keep time.

If a read or write cycle is in progress when the $\overline{STBY}$ signal is asserted low, the internal cycle will be terminated when either the external cycle completes or when the internal chip enable condition (V_{DD} is 4.25 volts, typical) is negated, whichever occurs first.

$\overline{RTC}$ - Real Time Clock Select (input): When this signal is asserted low, the real time clock registers are accessible. Registers are selected by the A0 line. Data is driven onto the data bus when $\overline{RD}$ is low. Data is received from the bus when $\overline{WR}$ is pulsed low and then high.

SQW - Square Wave (output): Frequency selectable output. Frequency is selected by setting register A bits RS0-RS3. See Table 2 for frequencies that can be selected.

$\overline{XRAM}$ - Extended RAM Select (input): When this signal is asserted low, the extended RAM bytes are accessible. The XRAM page register is selected when the A5 address line is high. A 32-byte page of RAM is accessible when A5 is low. A0-A4 select the bytes within the page of RAM pointed to by the page register. Data is driven onto the data bus when $\overline{RD}$ is low. Data is received from the bus when $\overline{WR}$ is pulsed low and then high.

$\overline{IRQ}$ - Interrupt Request (output): The $\overline{IRQ}$ signal is an active low, open drain output that is used as a processor interrupt request. The $\overline{IRQ}$ output follows the state of the IRQF bit (bit 7) in status register C. $\overline{IRQ}$ can be asserted by the alarm, update ended, or periodic interrupt functions depending on the configuration of register B.

$\overline{RESET}$ - Reset (input): The reset signal is used to initialize certain registers to allow proper operation of the RTC module. When $\overline{RESET}$ is low, the following occurs.

1. The following register bits are cleared:
   a. Periodic interrupt (PIE)
   b. Alarm interrupt enable (AIE)
   c. Update ended interrupt (UF)
   d. Interrupt request flag (IRQF)
   e. Periodic interrupt flag (PF)
   f. Alarm interrupt flag (AF)
   g. Square wave output enable (SQWE)
   h. Update ended interrupt enable (UIE)
2. The $\overline{IRQ}$ pin is in the high impedance state.
3. The RTC is not processor accessible.

ADDITIONAL PIN DESCRIPTION
(FOR DS1395, DS1395S)

X1, X2 – Connections for a standard 32.768 KHz quartz crystal, Daiwa part number DT-26S or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6 pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, “Crystal Considerations with Dallas Real Time Clocks”.

V_{BAT} – Battery input for any standard +3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.5 volts for proper operation. The nominal write protect trip point voltage at which access to the real time clock and user RAM is denied is set by the internal circuitry as 1.26 x V_{BAT}. A maximum load of 1 µA at 25°C and 3.0V on V_{BAT} in the absence of power should be used to size the external energy source.

The battery should be connected directly to the V_{BAT} pin. A diode must not be placed in series with the battery to the V_{BAT} pin. Furthermore, a diode is not necessary because reverse charging current protection circuitry is provided internal to the device and has passed the requirements of Underwriters Laboratories for UL listing.

B_{GND} – Battery ground: This pin or pin 14 can be used for the battery ground return.

OPERATION
Power-Down/Power-Up: The real time clock will continue to operate and all of the RAM, time, and calendar and alarm memory locations will remain non-volatile regardless of the voltage level of V_{DD}. When the voltage level applied to the V_{DD} input is greater than 4.25 volts (typical), the module becomes accessible after 200 ms provided that the oscillator and countdown chain have been programmed to be running. This time period allows the module to stabilize after power is applied.

When V_{DD} falls below the CE_{THR} (4.25 volts typical), the chip select inputs $\overline{RTC}$ and $\overline{XRAM}$ are forced to an inactive state regardless of the state of the pin signals. This puts the module into a write protected mode in which all inputs are ignored and all outputs are in a high impedance state. When V_{DD} falls below 3.2 volts (typical), the module is switched over to an internal power source in the case of the DS1397, or to an external battery connected to the V_{BAT} and BGND pins in the case of the DS1395 and DS1395S, so that power is not interrupted to timekeeping and nonvolatile RAM functions.

Address Map: The registers of the device appear in two distinct address ranges. One set of registers is active when $\overline{RTC}$ is asserted low and represents the real time clock. The second set of registers is active when $\overline{XRAM}$ is asserted low and represents the extended RAM.

RTC Address Map: The address map of the RTC module is shown in Figure 2. The address map consists of 50 bytes of general purpose RAM, 10 bytes of RTC/calendar information, and 4 bytes of status and control information. All 64 bytes can be accessed as read/write registers except for the following:

1. Registers C and D are Read Only (status information)
2. Bit 7 of register A is Read Only
3. Bit 7 of the ”Seconds” byte (00) is Read Only

The first byte of the real time clock address map is the RTC indirect address register, accessible when A0 is low. The second byte is the RTC data register, accessible when A0 is high. The function of the RTC indirect address register is to point to one of the 64 RTC registers that are indirectly accessible through the RTC data register.

Extended RAM Address Map: The first 32 bytes of the extended RAM represent one of 128 pages of general purpose nonvolatile memory. These 32 bytes on a page are addressed by A0 through A4 when A5 is low. When A5 is high, the XRAM page register is accessible. The value in the XRAM page register points to one of 128 pages of nonvolatile memory available. The address of the XRAM page register is dependent only on A5 being high; thus, there are 31 aliases of this register in I/0 spaces. (See Figure 3.)

TIME, CALENDAR AND ALARM LOCATIONS

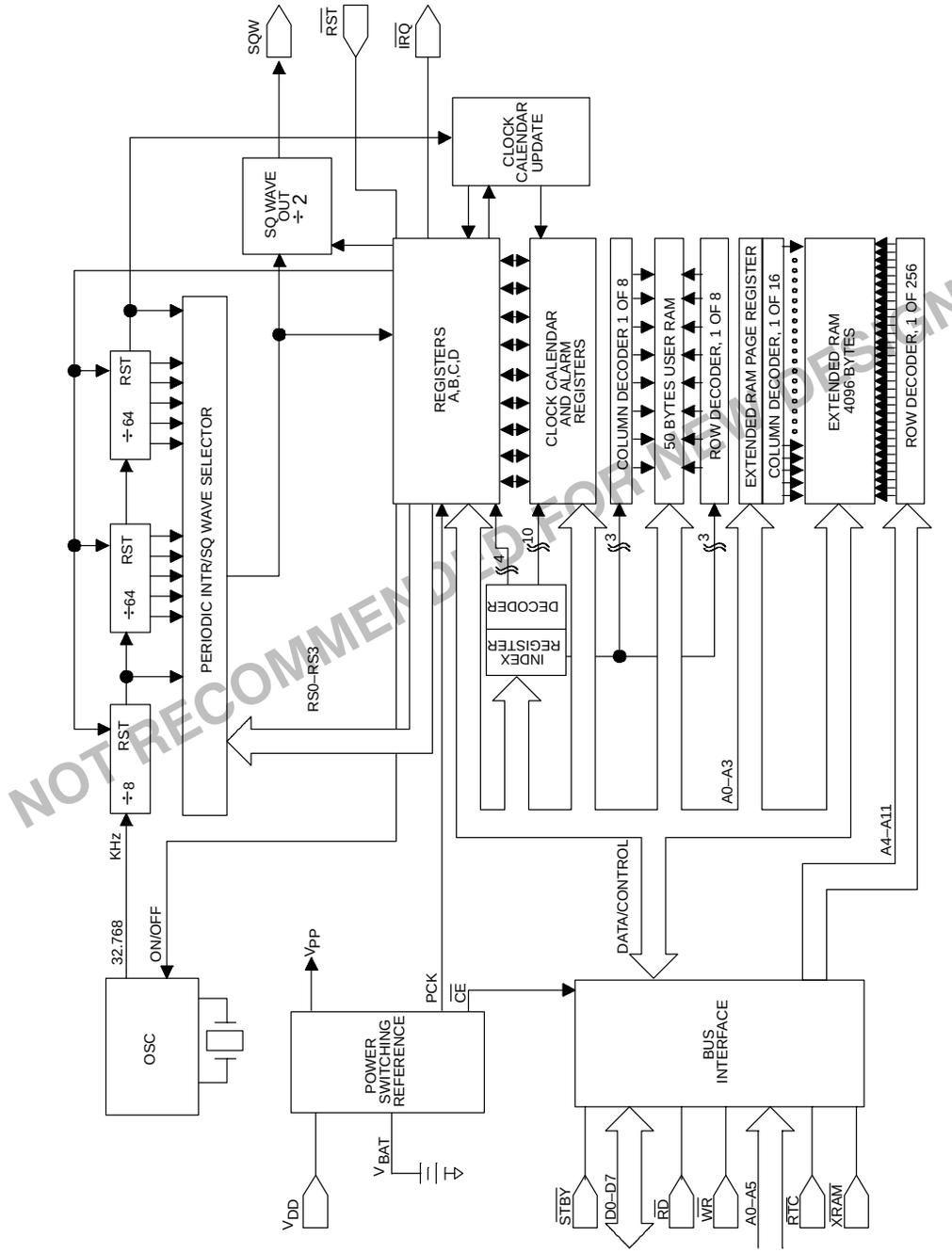
The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations.

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

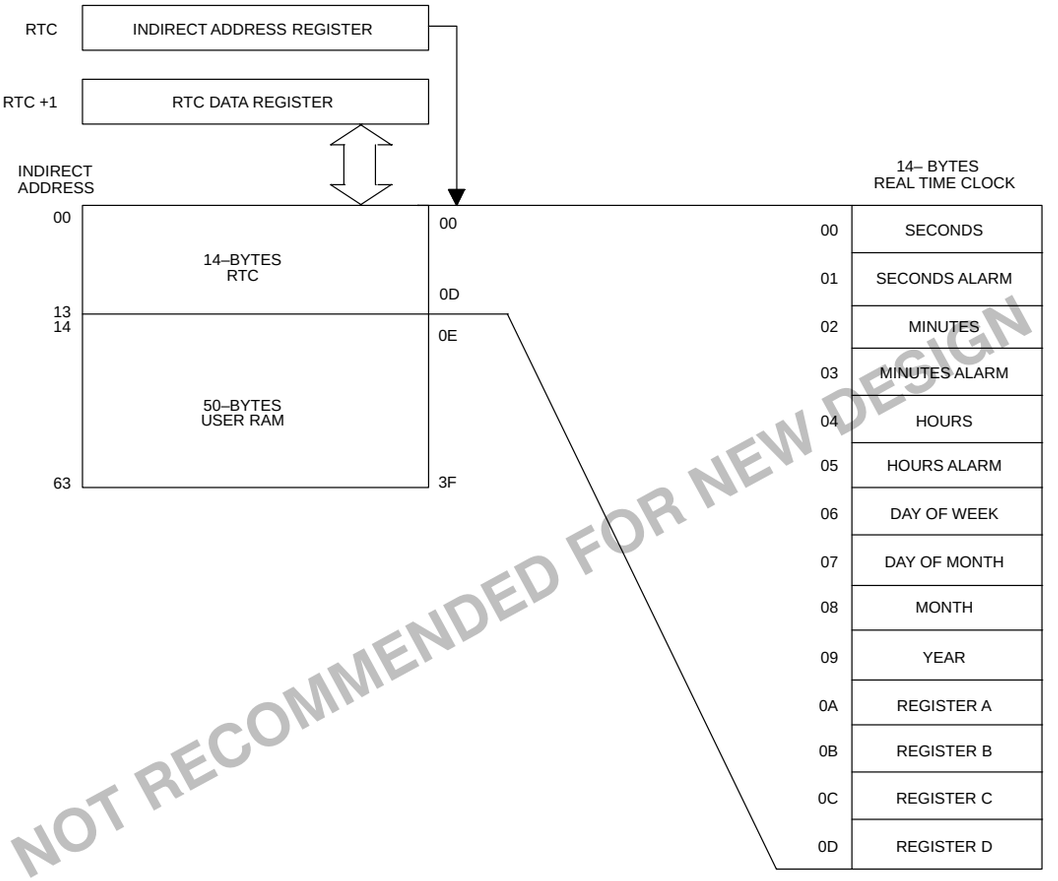
Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second method is to insert a “don’t care” state in one or more of the three alarm bytes. The “don’t care” code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the “don’t care” condition when at logic 1. An alarm will be generated each hour when the “don’t care” bits are set in the hours byte. Similarly, an alarm is generated every minute with “don’t care” codes in the hours and minute alarm bytes. The “don’t care” codes in all three alarm bytes create an interrupt every second.

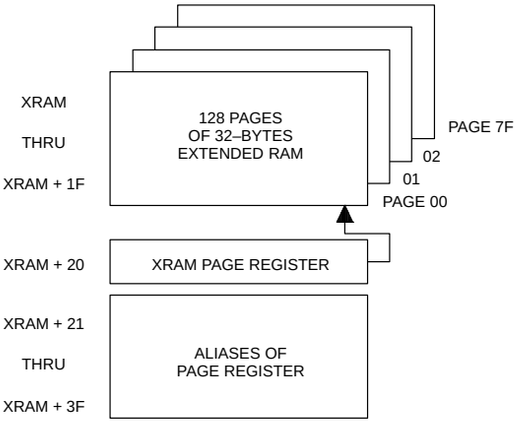
DS139X BLOCK DIAGRAM Figure 1



REAL TIME CLOCK RAM MAP Figure 2



EXTENDED RAM ADDRESS MAP Figure 3



TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

USER NONVOLATILE RAM - RTC

The 50 user nonvolatile RAM bytes are not dedicated to any special function within the DS1395/DS1397. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible in the RTC section.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The application program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read. However, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The alternative flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that

the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1395/DS1397. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS1395/DS1397 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 2. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 KHz
0	1	0	0	244.141 µs	4.096 KHz
0	1	0	1	488.281 µs	2.048 KHz
0	1	1	0	976.5625 µs	1.024 KHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

UPDATE CYCLE

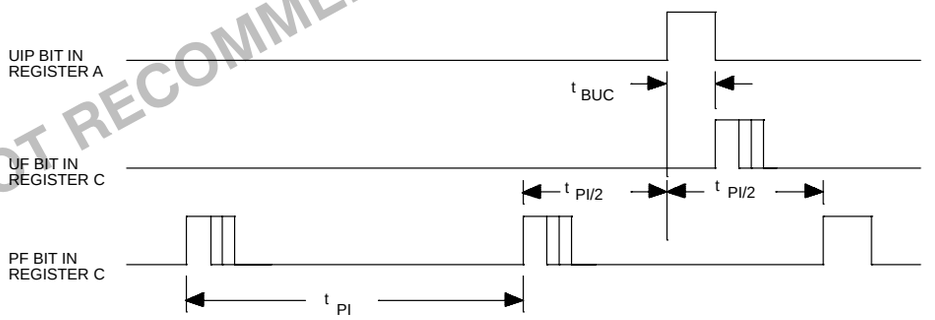
The DS1395/DS1397 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a “don’t care” code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($t_{PI}/2+t_{BUC}$) to ensure that data is not read during the update cycle.

UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 4



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS1395/DS1397 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1395/DS1397.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1395/DS1397 functions but is cleared by the hardware $\overline{RESET}$ signal.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS1395/DS1397 do not affect the AIE bit but is cleared by $\overline{RESET}$.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update Ended Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high or the $\overline{RESET}$ pin going low clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit and is cleared by $\overline{RESET}$.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1
i.e., IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE)

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{RESET}$ pin is low.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C or by $\overline{RESET}$.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C or a $\overline{RESET}$ will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C or by $\overline{RESET}$.

BIT 0 THROUGH BIT 3 - These are reserved bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor Corporation prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are reserved and not usable. They cannot be written and, when read, they will always read zero.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} Pin Potential to Ground Pin	-0.3V to +7.0V
Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3V
Power Dissipation	500 mW
Storage Temperature	DS1397: –40°C to +70°C DS1395: –55°C to +125°C
Ambient Temperature	0°C to 70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High Voltage	Recognized as a High Signal Over Recommended V_{DD} and t_A Range	V_{IH}	2.2	V_{DD}+ 0.3	V V	
Input Low Voltage	Recognized as a Low Signal Over Recommended V_{DD} and t_A Range	V_{IL}	-0.3	0.8	V	
Battery Voltage		V_{BAT}	2.5	3.5	V	

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0V ± 10%, V_{SS} = 0V, t_A = 0° C to 70°C)

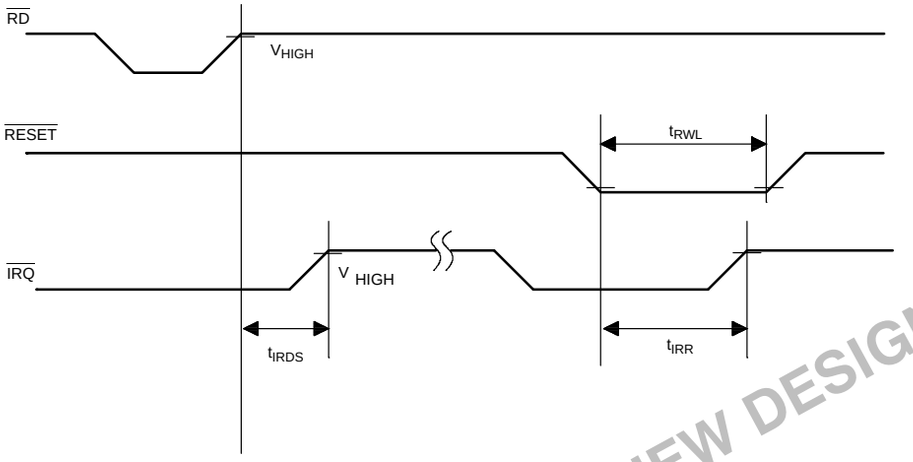
CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNIT	NOTES
Input Leakage V_{IL}=0V, V_{IH}=V_{DD}	For any Single Pin: D0-7, $\overline{RD}$, $\overline{WR}$, A0-5, XRAM, $\overline{RTC}$, $\overline{RESET}$	I_I		±1	µA	
Output High Voltage	V_{DD}=5.0V I_{LOAD} =1 mA	V_{OH}	2.4		V	
Output Low Voltage	V_{DD} = 5.0V I_{LOAD} = 2 mA	V_{OL}		0.4	V	
Power Supply Current	Outputs Unloaded	I_{DD}		50	mA	
$\overline{STBY}$ pin Input Current	$\overline{STBY}$=V_{DD}	I_{STBY}		+500	µA	
$\overline{STBY}$ pin Input Current	$\overline{STBY}$=V_{SS}	I_{STBY}		–1	µA	

AC SWITCHING CHARACTERISTICS

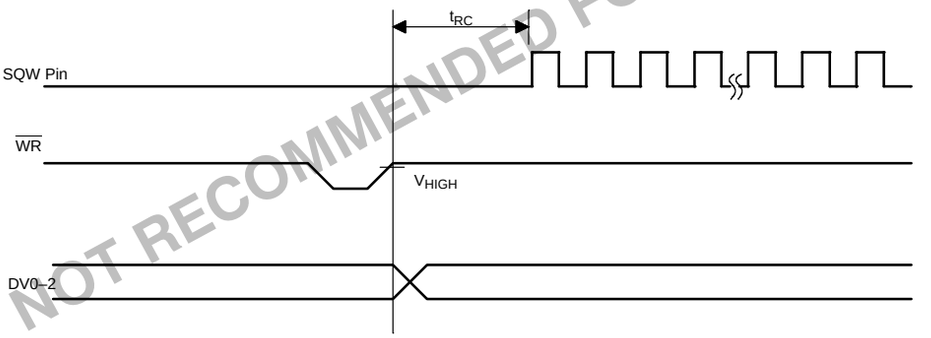
(0°C to 70°C; V_{DD} = 4.5V to 5.5V)

CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNIT	NOTES
Reset Pulse Width		t_{RWL}	5		µs	
Oscillator Startup	From Software Enable Via DV Bits	t_{RC}		1	s	
IRQ Release from $\overline{RD}$ High		t_{IRDS}		2	µs	
IRQ Release from $\overline{RESET}$ Low		t_{IRR}		2	µs	

IRQ RELEASE DELAY



OSCILLATOR START-UP



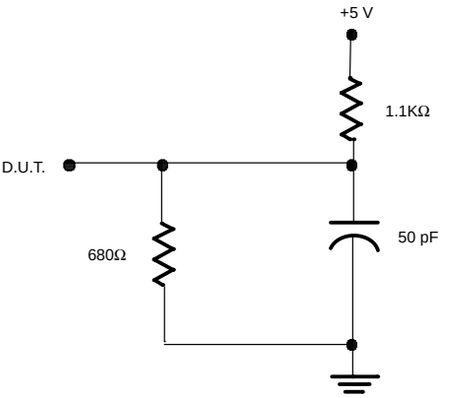
NOTE:
Timing assumes RS3-0 Bits = 0011, minimum t_{PI}.

BUS TIMING

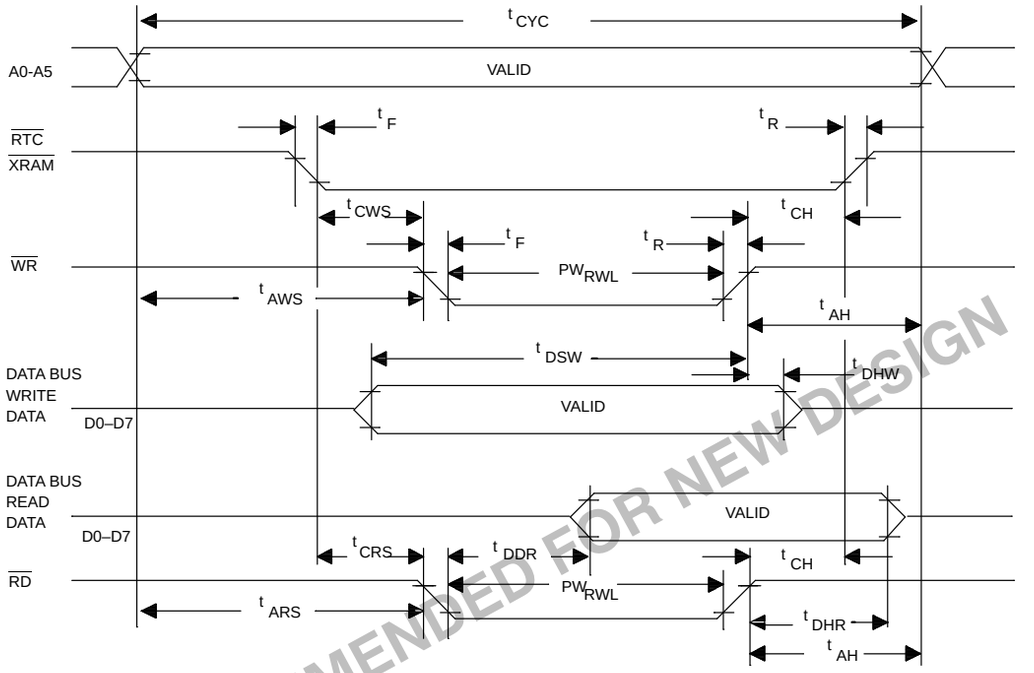
(0°C to 70°C; V_{DD} = 4.5V to 5.5V)

PARAMETER	SYM	MIN	TYP	MAX	UNIT	NOTES
Cycle Time	t_{CYC}	395		DC	ns	
Pulse Width, RD/WR Low	PW_{RWL}	200			ns	
Signal Rise and Fall Time, $\overline{RTC}$, $\overline{XRAM}$, $\overline{RD}$, $\overline{WR}$	t_R, t_F			30	ns	
Address Hold Time	t_{AH}	20			ns	
Address Setup Time Before $\overline{RD}$	t_{ARS}	30			ns	
Address Setup Time Before $\overline{WR}$	t_{AWS}	0			ns	
$\overline{RTC}$/$\overline{XRAM}$ Select Setup Time Before $\overline{RD}$	t_{CRS}	30			ns	
$\overline{RTC}$/$\overline{XRAM}$ Select Setup Time Before $\overline{WR}$	t_{CWS}	0			ns	
$\overline{RTC}$/$\overline{XRAM}$ Select Hold Time After $\overline{RD}$ or $\overline{WR}$	t_{CH}	20			ns	
Read Data Hold Time	t_{DHR}	10		100	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Output Data Delay Time from RD	t_{DDR}	20		200	ns	
Write Data Setup Time	t_{DSW}	200			ns	

OUTPUT LOAD



BUS READ/WRITE TIMING



POWER-DOWN/ POWER-UP TIMING

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F 4.0 ≤V_{CC} ≤ 4.5V	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} 3.0 ≤V_{CC}≤ 4.0V	10			µs	
V_{CC} Slew Rate Power Up	t_R 4.5V≥V_{CC}≥4.0V	0			µs	
Expected Data Retention	t_{DR}	10			years	

NOTE:
$\overline{CE}$ is chip enabled for access, an internal signal which is defined by ($\overline{RD}$ + $\overline{WR}$) ($\overline{XRAM}$ + $\overline{RTC}$).

CAPACITANCE

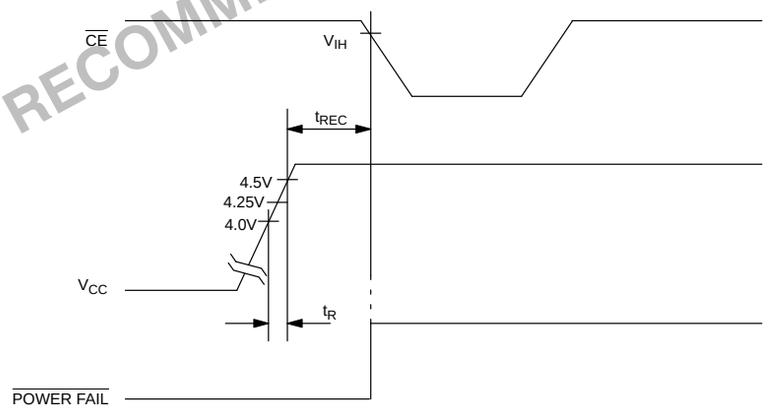
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

GENERAL INFORMATION

PARAMETER	SYM	MIN	TYP	MAX	UNIT	NOTES
Expected Data Retention @ 25°C (DS1397 only)	t_{DR}	10			Years	
Clock Accuracy for t_{DR} @ 25°C (DS1397 only)	C_Q	±1			Min/Mo	
Clock Accuracy Temperature Coefficient (DS1397)	K			.050	ppm/°C²	
Clock Temperature Coefficient Turnover Temperature (DS1397 only)	t_O	20		30	0°C	
Chip Enable Threshold (DS1397 only)	CE_{THR}			4.5	V	

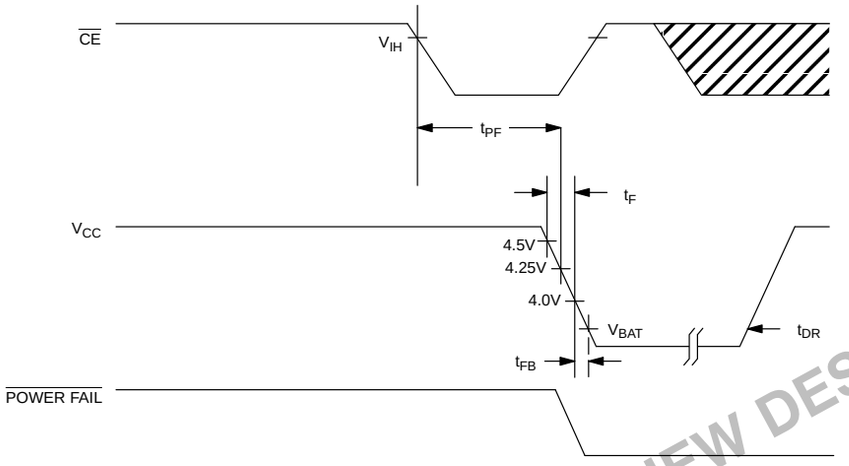
POWER–UP CONDITION



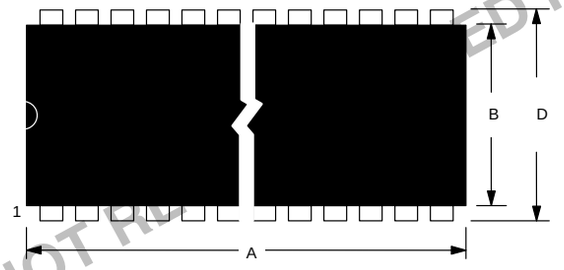
NOTE:

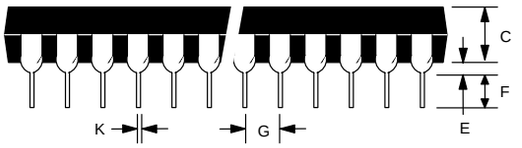
$\overline{CE}$ is an internal signal generated by the power switching reference in the DS139X products.

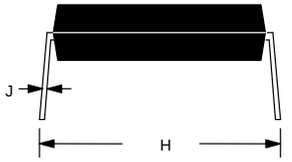
POWER–DOWN CONDITION



DS1395 28–PIN DIP

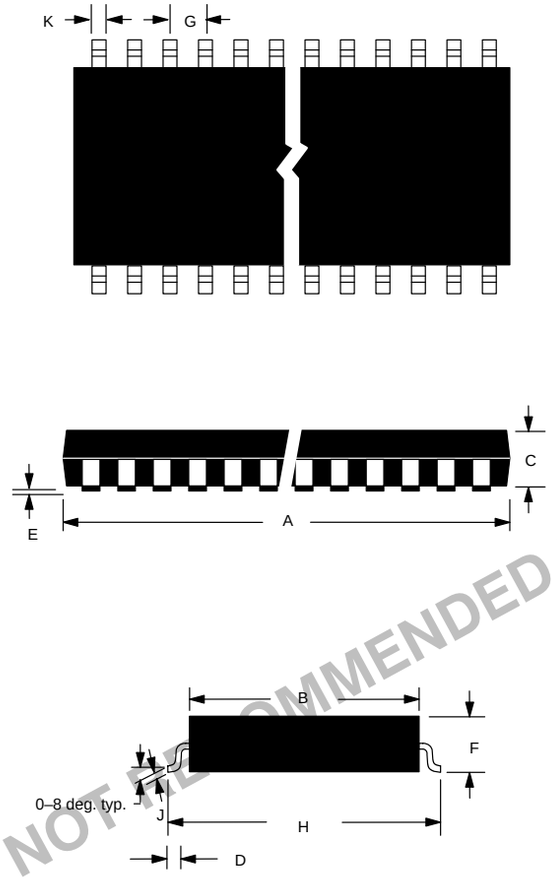






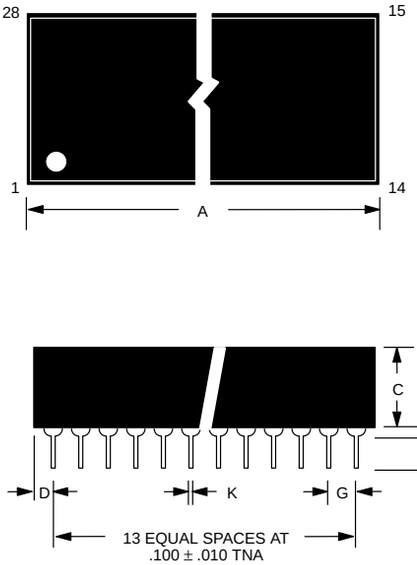
PKG	28–PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.445 36.70	1.470 37.34
B IN. MM	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.625 15.88	0.675 17.15
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56

DS1395S 28–PIN SOIC



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.706 17.93	0.728 18.49
B IN. MM	0.338 8.58	0.350 8.89
C IN. MM	0.086 2.18	0.110 2.79
D IN. MM	0.020 0.58	0.050 1.27
E IN. MM	0.002 0.05	0.014 0.36
F IN. MM	0.090 2.29	0.124 3.15
G IN. MM	0.050 1.27	BSC
H IN. MM	0.460 11.68	0.480 12.19
J IN. MM	0.006 0.15	0.013 0.33
K IN. MM	0.014 0.36	0.020 0.51

DS1397 28–PIN 720 MIL FLUSH ENCAPSULATED



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.350	0.375
MM	8.89	9.52
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

NOTE: PINS 3, 4, 18 AND 22 ARE MISSING BY DESIGN.