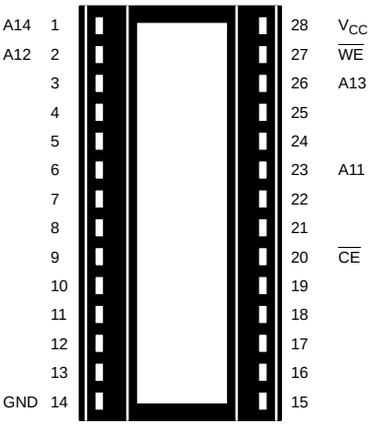
DALLAS SEMICONDUCTOR

DS1613C
Partitionable 256K SmartSocket

FEATURES

- Accepts standard 32K x 8, CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Unconditionally write protects all of memory when V_{CC} is out of tolerance
- Write protects selected blocks of memory when programmed
- Automatically switches to battery backup supply when power fail occurs
- Data retention time is greater than 10 years with the proper RAM selection
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN ASSIGNMENT



28–PIN INTELLIGENT SOCKET

PIN DESCRIPTION

A11–A14	–	Address Lines
$\overline{CE}$	–	Conditioned Chip Enable
$\overline{WE}$	–	Conditioned Write Enable
V_{CC}	–	Switched V_{CC}
GND	–	Ground

All pins pass through except 20, 28, and 27.

DESCRIPTION

The DS1613C SmartSocket is a 28–pin, 600 mil DIP socket with a built–in CMOS controller circuit and an embedded lithium energy source. It accepts a 32K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out–of–tolerance condition. When such a condition occurs, on internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt programs important data.

Using the SmartSocket saves printed circuit board space since the SRAM/SmartSocket combination occupies no more area than the SRAM alone. The SmartSocket modifies only pins 20, 27 and 28 to nonvolatize the RAM. All other pins are passed straight through. Pins 1, 2, 23, and 26 are address inputs used to program memory partitions.

OPERATION

The DS1613C SmartSocket performs five circuit functions required to battery back up a CMOS memory. The first function involves switching between the battery and the V_{CC} supply, depending on which is greater. The switch has a voltage drop of less than 0.2 volts.

The second function is power–fail detection. The DS161C constantly monitors the V_{CC} supply. When V_{CC} falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable.

The third function, write protection, is accomplished by holding the RAM chip enable signal to within 0.2 volts of V_{CC} or the battery supply whichever is greater. If the incoming chip enable signal is active at the time power fail detection occurs, write protection is delayed until after the current memory cycle is complete to avoid corruption of data. Power fail detection occurs in the range of 4.75 to 4.5 volts. During nominal power supply conditions the chip enable signal will be passed through from the socket pin to the socket contact with a maximum propagation delay of 20 ns.

The fourth function the DS1613C performs is to check battery status to warn of potential data loss. Each time that V_{CC} power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory access to the SmartSocket is inhibited. Battery status can, therefore, be determined by a three–step process. First, a read cycle is performed to any location in the memory, in order to save the contents of that location. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, then the battery voltage is less than 2.0 V and data is in danger of being corrupted.

The fifth function the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to ensure reliability. The DS1613C SmartSocket provides two batteries and an internal isolation switch to select between them. During battery back up, the battery with the highest voltage is selected for use. If one battery fails, the other automatically takes over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. Each of the two internal lithium cells has a 45 mAh capacity.

NOTE: As shipped from Dallas Semiconductor, battery voltage cannot be measured on the V_{CC} socket contact. Only after V_{CC} has been applied to the device for the first time and then removed will the battery voltage be present on socket contacts 28, 26 and 20.

PARTITION PROGRAMMING MODE

The register controlling the partitioning logic switch is selected by recognition of a specific binary pattern which is sent on address lines A11–A14. These address lines are normally the four upper–order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycles will load the partition register. Since there are 16 protectable partitions, the size of each partition is 32K/16 or 2K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A11 through A14 and shown in Table 2. A logical 1 in a bit location write protects the corresponding partition. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A12 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1613C to internally inhibit $\overline{WE}$ whenever A14 A13 A12 A11=0101. Note that while programming the partition register, data which is being accessed from the RAM should be ignored, since the purpose of the 16 read cycles is to program the partition switch, not to access data from RAM.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A11	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A12	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A13	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A14	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST BITS ENTERED

PARTITION REGISTER MAPPING Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{14} A_{13} A_{12} A_{11})
A11	BIT 21	PARTITION 0	0000
A12	BIT 21	PARTITION 1	0001
A13	BIT 21	PARTITION 2	0010
A14	BIT 21	PARTITION 3	0011
A11	BIT 22	PARTITION 4	0100
A12	BIT 22	PARTITION 5	0101
A13	BIT 22	PARTITION 6	0110
A14	BIT 22	PARTITION 7	0111
A11	BIT 23	PARTITION 8	1000
A12	BIT 23	PARTITION 9	1001
A13	BIT 23	PARTITION 10	1010
A14	BIT 23	PARTITION 11	1011
A11	BIT 24	PARTITION 12	1100
A12	BIT 24	PARTITION 13	1101
A13	BIT 24	PARTITION 14	1110
A14	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28 L Supply Voltage	V_{CC}	4.75	5.0	5.5	V	1, 3
Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	1, 3
Logic 0	V_{IL}	-0.3		+0.8	V	1, 3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28 L Supply Current	I_{CC}			5	mA	3, 4, 5
Pin 28 U Supply Voltage	V_{CCO}	V_{CC}-0.2			V	1, 3, 7
Pin 28 U Supply Current	I_{CCO}			150	mA	3, 7
Pin 20 L $\overline{CE}$, Pin 27 L $\overline{WE}$ Input Leakage Address A11-A14	I_{IL}	–1.0		+1.0	µA	3, 4
Pin 20 U $\overline{CE}$, Pin 27 U $\overline{WE}$ Output @ 2.4V	I_{OH}	–1.0			mA	2, 3
Pin 20 U $\overline{CE}$, Pin 27 U $\overline{WE}$ Output @ 0.4V	I_{OL}			4.0	mA	2, 3

DC ELECTRICAL CHARACTERISTICS

0° to 70°C; V_{CC} < 4.5V

Pin 20 U Output Pin 27 U Output	V_{OLH}	V_{CC}–0.2 V_{BAT}–0.2			V	1, 3
Pin 28 U Battery Current	I_{BAT}			1	µA	3
Pin 28 U Battery Voltage	V_{BAT}	2	3	3.6	V	1, 3

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	3
Output Capacitance Pin 27 U, Pin 20 U	C_{OUT}			7	pF	3

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.75 to 5.5V)

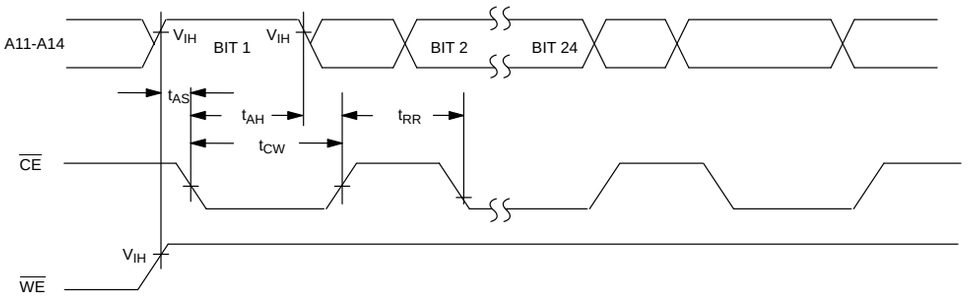
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{WE}$, $\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2, 8
$\overline{WE}$, $\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	10			ns	
$\overline{CE}$ Pulse Width	t_{CW}	75			ns	

AC ELECTRICAL CHARACTERISTICS

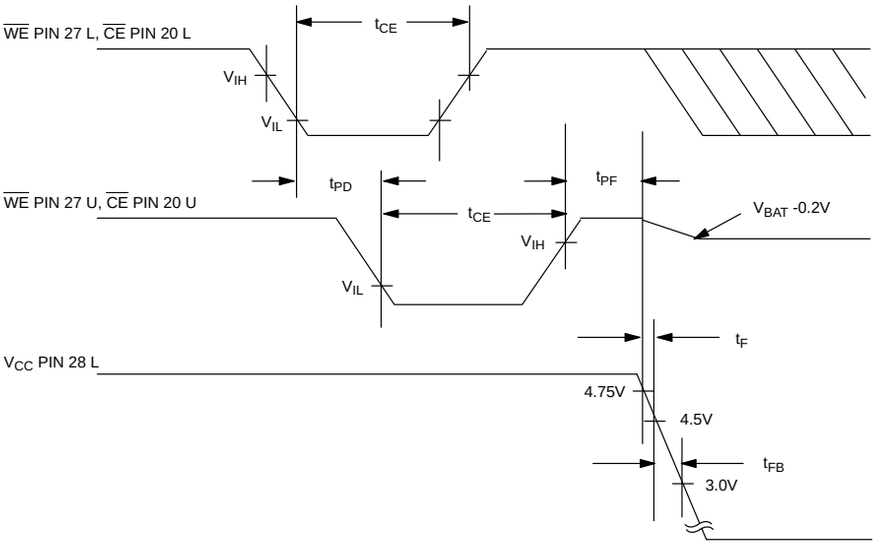
(0°C to 70°C; V_{CCI} < 4.75V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-up	t_{REC}	25	80	125	ms	
V_{CC} Slew Rate 4.75 – 4.5V	t_F	300			µs	
V_{CC} Slew Rate 4.5 – 3V	t_{FB}	10			µs	
V_{CC} Slew Rate 4.5 – 4.75V	t_R	0			µs	
$\overline{WE}$, $\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	6

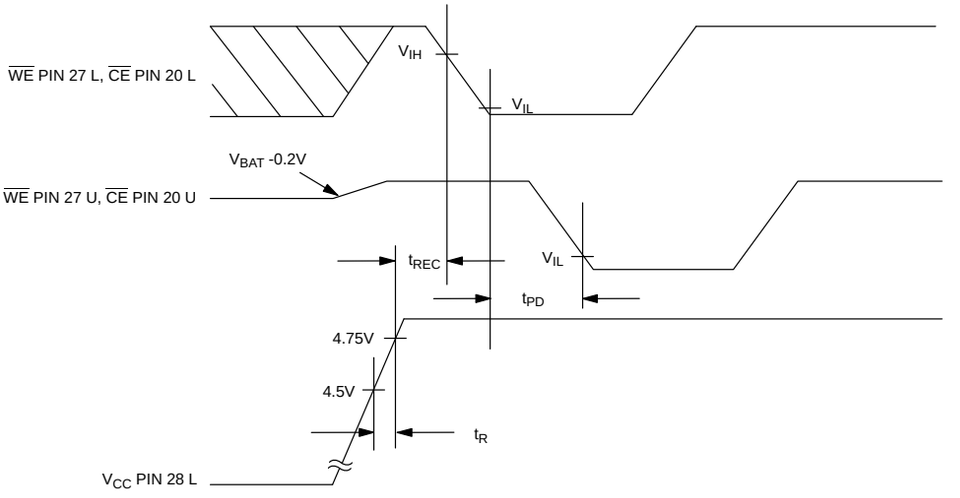
TIMING DIAGRAM: LOADING PARTITION REGISTER



TIMING DIAGRAM: POWER DOWN



TIMING DIAGRAM: POWER UP



WARNINGS:

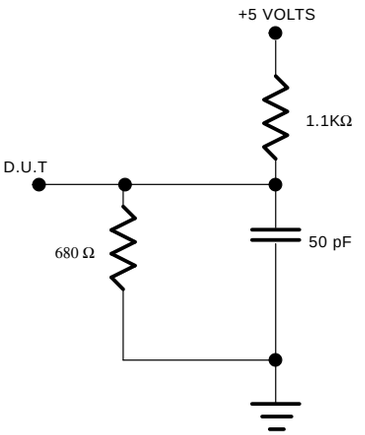
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal will discharge internal lithium source because exposed voltage pins are present.

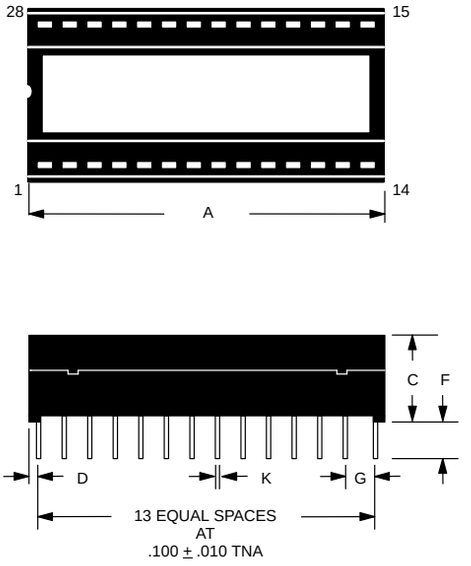
NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.
3. Pin locations are designated “U” (for upper) when a parameter definition refers to the socket receptacle and “L” (for lower) when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. I_{BAT} is the maximum load current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
6. t_{CE} maximum must be met to ensure data integrity on power loss.
7. V_{CC} is within nominal limits and a memory is installed in the socket.
8. Input pulse rise and fall times equal 10 ns.

OUTPUT LOAD Figure 1



DS1613C INTELLIGENT SOCKET 28–PIN (600 MIL DIP)



PKG	28–PIN	
DIM	**MIN**	**MAX**
A IN.	1.380	1.420
MM	35.05	36.07
B IN.	0.690	0.720
MM	17.53	18.29
C IN.	0.370	0.420
MM	9.39	10.67
D IN.	0.035	0.065
MM	0.89	1.65
E IN.	0.015	0.035
MM	0.39	0.89
F IN.	0.120	0.160
MM	3.04	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53