# DALLAS
SEMICONDUCTOR

DS1613D
Partitionable 1024K SmartSocket

FEATURES

- Accepts standard 128K x 8, CMOS static RAM

- Embedded lithium energy cell retains RAM data

- Unconditionally write protects all of memory when V_{CC} is out of tolerance

- Write protects selected blocks of memory regardless of V_{CC} status when programmed

- Automatically switches to battery backup supply when power fail occurs

- Data retention time is greater than 10 years with the proper RAM selection

- Proven gas-tight socket contacts

- Operating temperature range 0°C to 70°C

PIN ASSIGNMENT

	1		32	V_{CC}
A16	2		31	A15
A14	3		30	
			29	$\overline{WE}$
			28	A13
			22	$\overline{CE}$
GND	16		17	
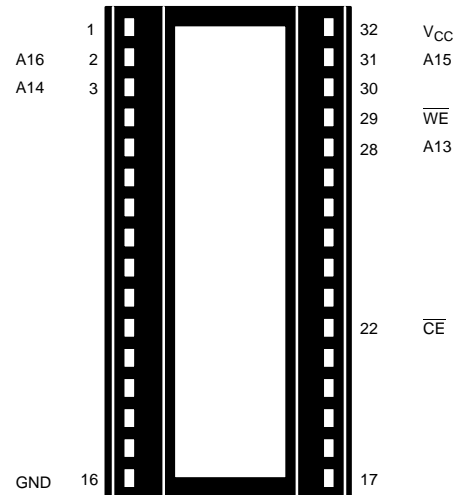
32-PIN SOCKET (600 MIL)

PIN DESCRIPTION

A13–A16	– Address Lines
$\overline{CE}$	– Conditioned Chip Enable
$\overline{WE}$	– Conditioned Write Enable
V_{CC}	– Switched V_{CC}
GND	– Ground

All pins pass through except 22, 29, 30 and 32.

DESCRIPTION

The DS1613D SmartSocket is a 32-pin, 600 mil DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts 128K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt programs and important data.

Using the SmartSocket saves printed circuit board pacing since the SRAM/SmartSocket combination occupies no more area than the SRAM alone. The SmartSocket modifies only pins 22, 29, 30, and 32 to nonvolatize the RAM. All other pins are passed straight through. Pins 2, 3, 28, and 31 are address inputs used to program memory partitions.

The DS1613D is exactly the same as the DS1613C except that the DS1613D has 32 pins instead of 28 and the address and control signals are on different pin numbers and locations. The upper order address lines used to program the memory partitions also differ because a different RAM size is used. Tables 1 and 2 illustrate the pattern match required for partitioning of the DS1613D. See the DS1613C data sheet for all additional technical details and specifications.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 1

|	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A13	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A14	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A15	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A16	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED   LAST BITS ENTERED

PARTITION REGISTER MAPPING Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected $(A_{16}\ A_{15}\ A_{14}\ A_{13})$
A13	BIT 21	PARTITION 0	0000
A14	BIT 21	PARTITION 1	0001
A15	BIT 21	PARTITION 2	0010
A16	BIT 21	PARTITION 3	0011
A13	BIT 22	PARTITION 4	0100
A14	BIT 22	PARTITION 5	0101
A15	BIT 22	PARTITION 6	0110
A16	BIT 22	PARTITION 7	0111
A13	BIT 23	PARTITION 8	1000
A14	BIT 23	PARTITION 9	1001
A15	BIT 23	PARTITION 10	1010
A16	BIT 23	PARTITION 11	1011
A13	BIT 24	PARTITION 12	1100
A14	BIT 24	PARTITION 13	1101
A15	BIT 24	PARTITION 14	1110
A16	BIT 24	PARTITION 15	1111

DS1613D INTELLIGENT SOCKET 32 PIN (FOR 600 MIL DIP)
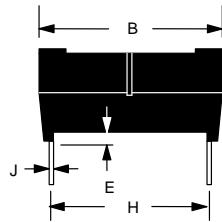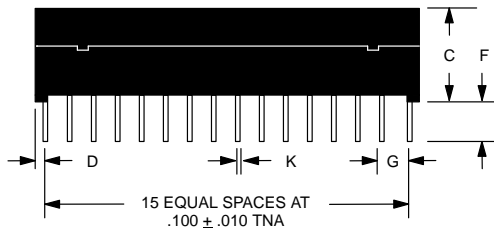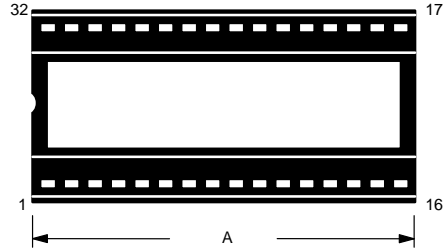
PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN.	1.580	1.620
MM	40.13	41.15
B IN.	0.690	0.720
MM	17.53	18.29
C IN.	0.350	0.410
MM	8.89	10.40
D IN.	0.035	0.065
MM	0.89	1.65
E IN.	0.015	0.035
MM	0.39	0.89
F IN.	0.120	0.160
MM	3.04	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53