# DALLAS
## SEMICONDUCTOR

# DS1643AL
## Nonvolatile Timekeeping RAM

## FEATURES

- Integrated NV SRAM, real time clock, crystal, power–fail control circuit and lithium energy source

- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.

- Totally nonvolatile with over 10 years of operation in the absence of power

- Access times of 120 ns and 150 ns

- Quartz accuracy ±1 minute a month @ 25°C, factory calibrated

- BCD coded year, month, date, day, hours, minutes, and seconds with leap year compensation valid up to 2100

- Power–fail write protection allows for ±10% $V_{CC}$ power supply tolerance

- Low Profile socketable module
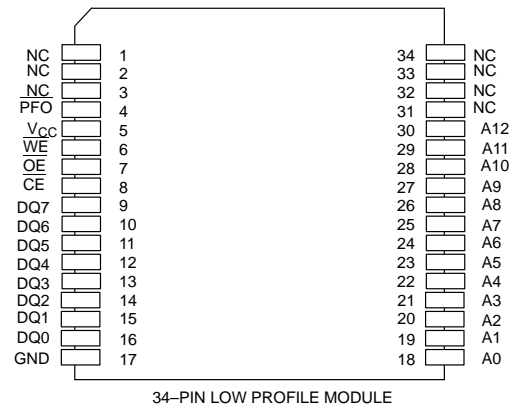  - 255 mil package height

## ORDERING INFORMATION

DS1643AL–XX   34–pin low profile module

└──► –12 = 120 ns access
     –15 = 150 ns access

## PIN ASSIGNMENT

| | | | | |
|---|---|---|---|---|
| NC | 1 | | 34 | NC |
| NC | 2 | | 33 | NC |
| NC | 3 | | 32 | NC |
| PFO | 4 | | 31 | NC |
| $V_{CC}$ | 5 | | 30 | A12 |
| WE | 6 | | 29 | A11 |
| OE | 7 | | 28 | A10 |
| CE | 8 | | 27 | A9 |
| DQ7 | 9 | | 26 | A8 |
| DQ6 | 10 | | 25 | A7 |
| DQ5 | 11 | | 24 | A6 |
| DQ4 | 12 | | 23 | A5 |
| DQ3 | 13 | | 22 | A4 |
| DQ2 | 14 | | 21 | A3 |
| DQ1 | 15 | | 20 | A2 |
| DQ0 | 16 | | 19 | A1 |
| GND | 17 | | 18 | A0 |

34–PIN LOW PROFILE MODULE

## DESCRIPTION

The DS1643AL is an 8K x 8 nonvolatile static RAM with a full function real time clock which are both accessible in a bytewide format. The nonvolatile time keeping RAM is functionally equivalent to any JEDEC standard 8K x 8 SRAM. The DS1643AL is a Low Profile Module that requires a PLCC surface mountable socket and , except for the additional Power Fail Output ($\overline{PFO}$) signal, is functionally equivalent to the DS1643. The Real Time Clock (RTC) information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24 hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1643AL also contains its own power–fail circuitry which deselects the device when the $V_{CC}$ supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low $V_{CC}$ as errant access and update cycles are avoided.

## PIN DESCRIPTION

| | | |
|---|---|---|
| A0–A12 | – | Address Input |
| $\overline{CE}$ | – | Chip Enable |
| $\overline{OE}$ | – | Output Enable |
| $\overline{WE}$ | – | Write Enable |
| NC | – | No Connection |
| $V_{CC}$ | – | +5 Volts |
| GND | – | Ground |
| DQ0-DQ7 | – | Data Input/Output |
| $\overline{PFO}$ | – | Power–Fail Output |

## CLOCK OPERATIONS–READING THE CLOCK

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1643AL clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when an one is written into the read bit, the seventh most significant bit in the control register. As long as a one remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1643AL registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to zero.

**DS1643 BLOCK DIAGRAM** Figure 1
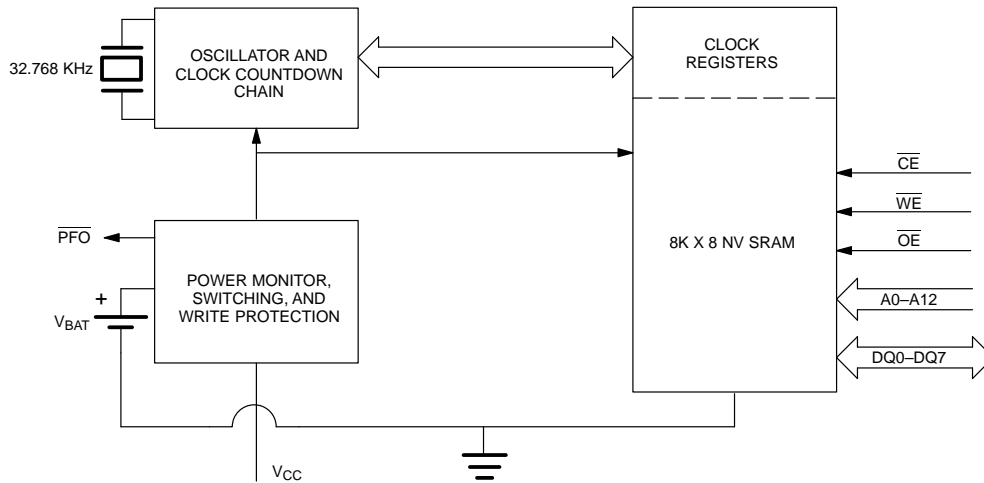
**DS1643AL TRUTH TABLE** Table 1

| V$_{CC}$ | $\overline{\text{CE}}$ | CE2 | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | MODE | DQ | POWER |
|---|---|---|---|---|---|---|---|
| 5 VOLTS ± 10% | V$_{IH}$ | X | X | X | DESELECT | HIGH–Z | STANDBY |
| | X | V$_{IL}$ | X | X | DESELECT | HIGH–Z | STANDBY |
| | V$_{IL}$ | V$_{IH}$ | X | V$_{IL}$ | WRITE | DATA IN | ACTIVE |
| | V$_{IL}$ | V$_{IH}$ | V$_{IL}$ | V$_{IH}$ | READ | DATA OUT | ACTIVE |
| | V$_{IL}$ | V$_{IH}$ | V$_{IH}$ | V$_{IH}$ | READ | HIGH–Z | ACTIVE |
| <4.5 VOLTS >V$_{BAT}$ | X | X | X | X | DESELECT | HIGH–Z | CMOS STANDBY |
| <V$_{BAT}$ | X | X | X | X | DESELECT | HIGH–Z | DATA RETENTION MODE |

## SETTING THE CLOCK

Bit 8 of the control register is the write bit. Setting the write bit to a one, like the read bit, halts updates to the DS1643AL registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a zero then transfers those values to the actual clock counters and allows normal operation to resume.

## STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{\text{OSC}}$ bit is the MSB for the seconds registers. Setting it to an one stops the oscillator.

## FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic "1" and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{\text{CE}}$ low, $\overline{\text{OE}}$ low, and address for seconds register remain valid and stable).

## CLOCK ACCURACY

The DS1643AL is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The clock is calibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. The DS1643AL does not require additional calibration and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary. Attempts to calibrate the clock that may be used with similar device types (MK48T08 family) will not have any effect even though the DS1643AL appears to accept calibration data.

**DS1643AL REGISTER MAP – BANK1** Table 2

| ADDRESS | DATA | | | | | | | | FUNCTION | |
|---------|------|------|------|------|------|------|------|------|----------|---|
| | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| 1FFF | – | – | – | – | – | – | – | – | YEAR | 00–99 |
| 1FFE | X | X | X | – | – | – | – | – | MONTH | 01–12 |
| 1FFD | X | X | – | – | – | – | – | – | DATE | 01–31 |
| 1FFC | X | FT | X | X | X | – | – | – | DAY | 01–07 |
| 1FFB | X | X | – | – | – | – | – | – | HOUR | 00–23 |
| 1FFA | X | – | – | – | – | – | – | – | MINUTES | 00–59 |
| 1FF9 | $\overline{OSC}$ | – | – | – | – | – | – | – | SECONDS | 00–59 |
| 1FF8 | W | R | X | X | X | X | X | X | CONTROL | A |

$\overline{OSC}$ = STOP BIT     R = READ BIT     FT = FREQUENCY TEST
W = WRITE BIT     X = SEE NOTE BELOW

## NOTE:

All indicated "X" bits are not dedicated to any particular function and can be used as normal RAM bits.

## RETRIEVING DATA FROM RAM OR CLOCK

The DS1643AL is in the read mode whenever $\overline{OE}$ (output enable) is low, $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within $t_{AA}$ after the last address input is stable, providing that the $\overline{CE}$, and $\overline{OE}$ access times are and states satisfied. If $\overline{CE}$, or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access ($t_{CEA}$) or at output enable access time ($t_{OEA}$). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$, and $\overline{OE}$. If the outputs are activated before $t_{AA}$, the data lines are driven to an intermediate state until $t_{AA}$. If the address inputs are changed while $\overline{CE}$, and $\overline{OE}$ remain valid, output data will remain valid for output data hold time ($t_{OH}$) but will then go indeterminate until the next address access.

## WRITING DATA TO RAM OR CLOCK

The DS1643 is in the write mode whenever $\overline{WE}$, and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$, on $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$, or $\overline{WE}$ must return inactive for a minimum of $t_{WR}$ prior to the initiation of another read or write cycle. Data in must be valid $t_{DS}$ prior to the end of write and remain valid for $t_{DH}$ afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs $t_{WEZ}$ after $\overline{WE}$ goes active.

## DATA RETENTION MODE

When $V_{CC}$ is within nominal limits ($V_{CC} > 4.5$ volts) the DS1643AL can be accessed as described above by read or write cycles. However, when $V_{CC}$ is below the power–fail point $V_{PF}$ (point at which write protection occurs) the internal clock registers and RAM is blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. At this time the Power–Fail Output signal ($\overline{PFO}$) will be driven active (logic 0) until $V_{CC}$ returns to nominal levels. When $V_{CC}$ falls below the level of the internal battery supply, power input is switched from the $V_{CC}$ pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until $V_{CC}$ is returned to nominal level.

**ABSOLUTE MAXIMUM RATINGS\***

| | |
|---|---|
| Voltage on Any Pin Relative to Ground | −0.3V to +7.0V |
| Operating Temperature | 0°C to 70°C |
| Storage Temperature | −20°C to +70°C |
| Soldering Temperature | 260°C for 10 seconds (See Note 7) |

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**                                           (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Logic 1 Voltage All Inputs | $V_{IH}$ | 2.2 | | $V_{CC}$+0.3 | V | |
| Logic 0 Voltage All Inputs | $V_{IL}$ | −0.3 | | 0.8 | V | |

**DC ELECTRICAL CHARACTERISTICS**                          (0°C $\leq t_A \leq$ 70°C; $V_{CC}$ = 5.0V $\pm$ 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Average $V_{CC}$ Power Supply Current | $I_{CC1}$ | | | 65 | mA | 2, 3 |
| TTL Standby Current ($\overline{CE}$ = $V_{IH}$) | $I_{CC2}$ | | 3 | 6 | mA | 2, 3 |
| CMOS Standby Current ($\overline{CE}$=$V_{CC}$−0.2V) | $I_{CC3}$ | | 2 | 4.0 | mA | 2, 3 |
| Input Leakage Current (any input) | $I_{IL}$ | −1 | | +1 | µA | |
| Output Leakage Current | $I_{OL}$ | −1 | | +1 | µA | |
| Output Logic 1 Voltage ($I_{OUT}$ = −1.0 mA) | $V_{OH}$ | 2.4 | | | V | |
| Output Logic 0 Voltage ($I_{OUT}$ = +2.1 mA) | $V_{OL}$ | | | 0.4 | V | |
| Write Protection Voltage | $V_{PF}$ | 4.0 | 4.25 | 4.5 | V | |

## AC ELECTRICAL CHARACTERISTICS  (0°C to 70°C; $V_{CC} = 5.0V \pm 10\%$)

| PARAMETER | SYMBOL | DS1643AL–12 120 ns Access MIN | MAX | DS1643AL–15 150 ns Access MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 120 | | 150 | | ns | |
| Address Access Time | $t_{AA}$ | | 120 | | 150 | ns | |
| $\overline{CE}$ Access Time | $t_{CEA}$ | | 120 | | 150 | ns | |
| $\overline{CE}$ Data Off Time | $t_{CEZ}$ | | 40 | | 50 | ns | |
| Output Enable Access Time | $t_{OEA}$ | | 100 | | 120 | ns | |
| Output Enable Data Off Time | $t_{OEZ}$ | | 35 | | 45 | ns | |
| Output Enable to DQ Low–Z | $t_{OEL}$ | 5 | | 5 | | ns | |
| $\overline{CE}$ to DQ Low–Z | $t_{CEL}$ | 5 | | 5 | | ns | |
| Output Hold from Address | $t_{OH}$ | 5 | | 5 | | ns | |
| Write Cycle Time | $t_{WC}$ | 120 | | 150 | | ns | |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | ns | |
| $\overline{CE}$ Pulse Width | $t_{CEW}$ | 100 | | 120 | | ns | |
| Address Hold from End of Write | $t_{AH1}$ $t_{AH2}$ | 5 30 | | 5 30 | | ns ns | 5 6 |
| Write Pulse Width | $t_{WEW}$ | 75 | | 90 | | ns | |
| $\overline{WE}$ Data Off Time | $t_{WEZ}$ | | 40 | | 50 | ns | |
| $\overline{WE}$ or $\overline{CE}$ Inactive Time | $t_{WR}$ | 10 | | 10 | | ns | |
| Data Setup Time | $t_{DS}$ | 85 | | 110 | | ns | |
| Data Hold Time High | $t_{DH1}$ $t_{DH2}$ | 0 15 | | 0 15 | | ns ns | 5 6 |

## AC TEST CONDITIONS
Input Levels:         0V to 3V
Transition Times:     5 ns

## CAPACITANCE  ($t_A = 25°C$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Capacitance on all pins (except DQ) | $C_I$ | | | 7 | pF | |
| Capacitance on DQ pins | $C_{DQ}$ | | | 10 | pF | |

## AC ELECTRICAL CHARACTERISTICS (POWER–UP/DOWN TIMING)  (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ or $\overline{WE}$ at $V_{IH}$ before Power Down | $t_{PD}$ | 0 | | | µs | |
| $V_{PF}$ (Max) to $V_{PF}$ (Min) $V_{CC}$ Fall Time | $t_F$ | 300 | | | µs | |
| $V_{PF}$ (Min) to $V_{SO}$ $V_{CC}$ Fall Time | $t_{FB}$ | 10 | | | µs | |
| $V_{SO}$ to $V_{PF}$ (Min) $V_{CC}$ Rise Time | $t_{RB}$ | 1 | | | µs | |
| $V_{PF}$ (Min) to $V_{PF}$ (Max) $V_{CC}$ Rise Time | $t_R$ | 0 | | | µs | |
| Power–Up | $t_{REC}$ | 15 | 25 | 35 | ms | |
| Expected Data Retention Time (Oscillator On) | $t_{DR}$ | 10 | | | years | 4 |

## DS1643AL READ CYCLE TIMING
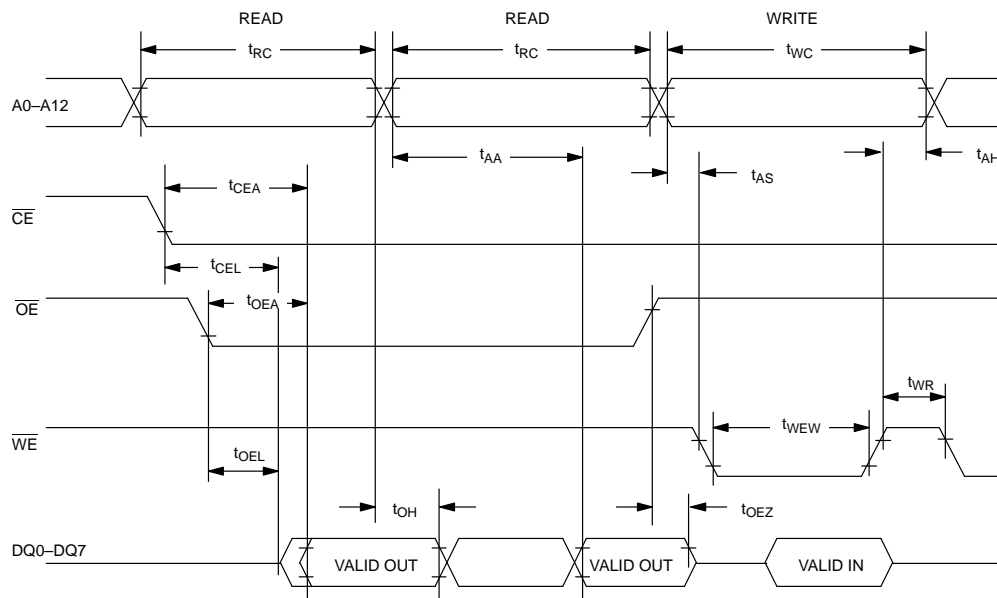
## DS1643AL WRITE CYCLE TIMING
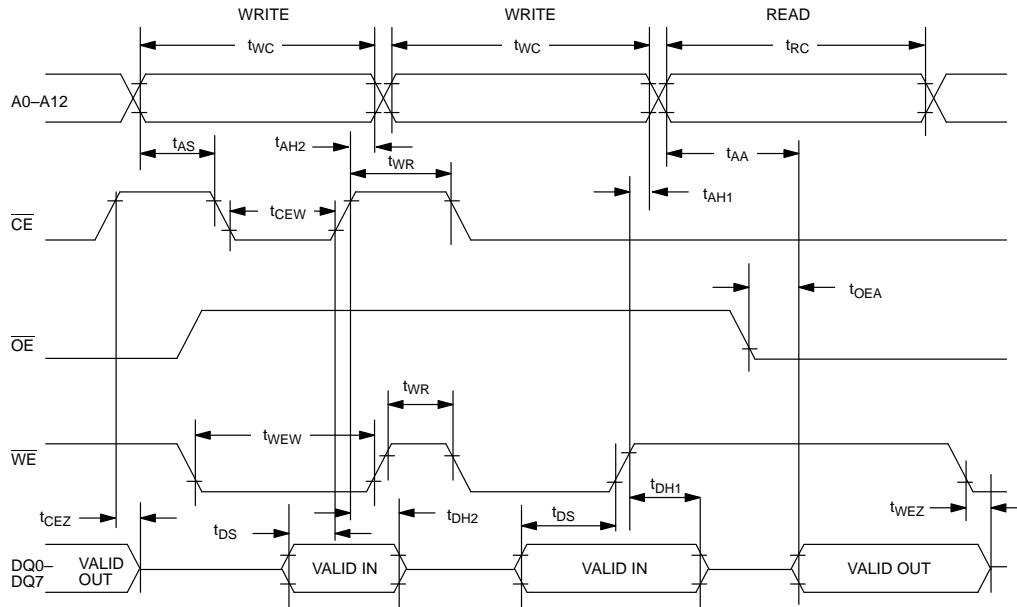


## POWER–DOWN/POWER–UP TIMING
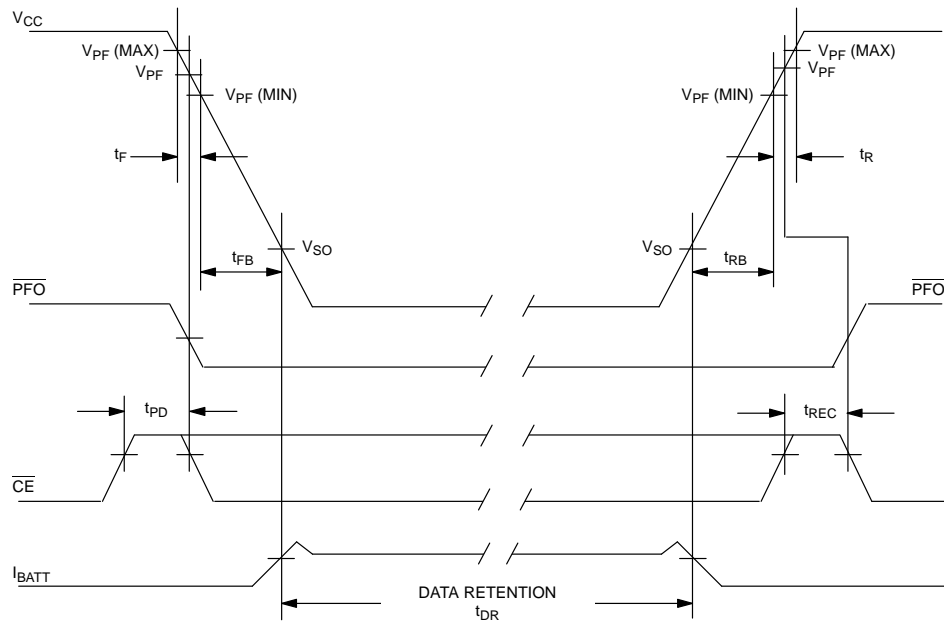
## NOTES:

1. All voltages are referenced to ground.

2. Typical values are at 25°C and nominal supplies.

3. Outputs are open.

4. Data retention time is at 25°C and is calculated from the date code on the device package. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225, would mean the 25th week of 1992.

5. $t_{AH1}$, $t_{DH1}$ are measured from $\overline{WE}$ going high.

6. $t_{AH2}$, $t_{DH2}$ are measured from $\overline{CE}$ going high.

7. Unencapsulated Low Profile Modules are not recommended for processing through conventional wavesoldering techniques. The use of a PLCC socket is recommended for production proposes.

## OUTPUT LOAD

+5 VOLTS

1.8KΩ

D.U.T.

1KΩ
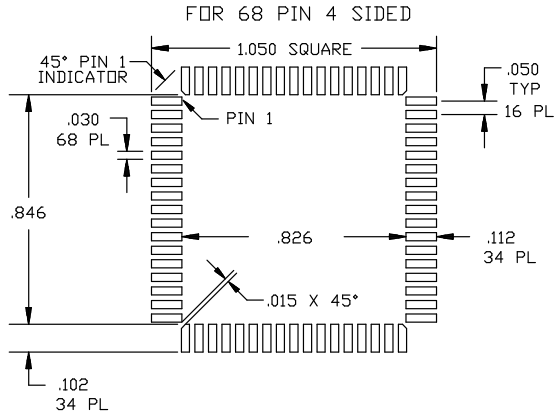
100 pF
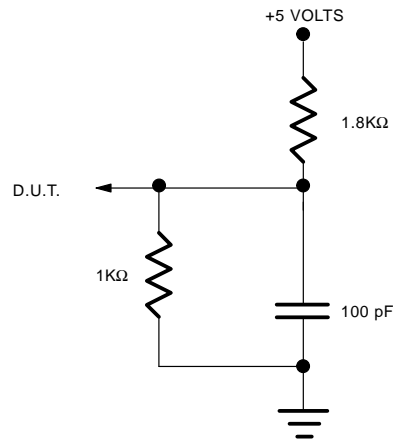
## DS1643AL 34–PIN LOW PROFILE MODULE
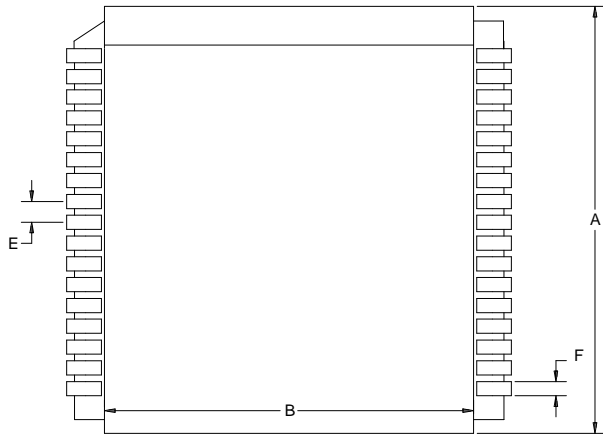
| PKG | INCHES | |
|-----|--------|--------|
| DIM | MIN | MAX |
| A | 0.955 | 0.980 |
| B | 0.840 | 0.855 |
| C | 0.230 | 0.250 |
| D | 0.975 | 0.995 |
| E | 0.047 | 0.053 |
| F | 0.015 | 0.025 |
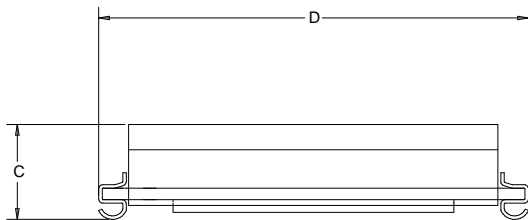
**NOTE:**
Dallas Semiconductor recommends the AMP PLCC socket, P/N 822453–1, Revision A (date code 9810 or later), for use with our 34–pin LPM device.

## RECOMMENDED DS1643AL MODULE SOCKET LAND PATTERNS

FOR 68 PIN 4 SIDED

45° PIN 1 INDICATOR

1.050 SQUARE

.050 TYP 16 PL

.030 68 PL

PIN 1

.846

.826

.112 34 PL

.015 X 45°

.102 34 PL

EITHER A TWO OR FOUR SIDED SOCKET MAY BE
UTILIZED FOR DS1643AL INSTALLATION.

FOR 68 PIN 2 SIDED (34 LEADS)

.030

1.050

.050 TYP 16 PL

.826

.112