**FEATURES**

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5%, 10% or 20% resets for 3.3 systems and 5% or 10% resets for 5.0 volt systems
- Eliminates the need for discrete components
- 3.3 volt 20% tolerance for use with 3.0 volt systems
- Pin compatible with the MAXIM MAX705/MAX706 in 8-pin DIP and 8-pin SOIC
- 8-pin DIP, 8-pin SOIC and 8-pin µ-SOP packages
- Industrial temperature range –40°C to +85°C

**PIN ASSIGNMENT**

- **PBRST** – Pushbutton Reset Input
- **VCC** – Power Supply
- **GND** – Ground
- **IN** – Input
- **NMI** – Non-maskable Interrupt
- **ST** – Strobe Input
- **RST** – Active Low Reset Output
- ***RST** – Active High Reset Output
- **WDS** – Watchdog Status Output

**DESCRIPTION**

The DS1705/DS1706 3.3 or 5.0 Volt MicroMonitor monitors three vital conditions for a microprocessor: power supply, software execution, and external override. A precision temperature compensated reference and comparator circuit monitors the status of VCC at the device and at an upstream point for maximum protection. When the sense input detects an out-of-tolerance condition a non-maskable interrupt is generated. As the voltage at the device degrades an internal power fail signal is generated which forces the reset to an active state. When VCC returns to an in-tolerance condition, the reset signal is kept in the active state for a minimum of 130 ms to allow the power supply and processor to stabilize.
The second function the DS1705/DS1706 performs is pushbutton reset control. The DS1705/DS1706 debounces the pushbutton input and guarantees an active reset pulse width of 130 ms minimum.

The third function is a watchdog timer. The DS1705/DS1706 has an internal timer that forces the WDO signal to the active state if the strobe input is not driven low prior to time-out.

**OPERATION**

**Power Monitor**
The DS1705/DS1706 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V\text{CC} falls below the minimum V\text{CC} tolerance, a comparator outputs the RST (or RST) signal. RST (or RST) is an excellent control signal for a microprocessor, as processing is stopped at the last possible moment of valid V\text{CC}. On power-up, RST (or RST) are kept active for a minimum of 130 ms to allow the power supply and processor to stabilize.

**Pushbutton Reset**
The DS1705/DS1706 provides an input pin for direct connection to a push-button reset (see Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that a RST (or RST) signal of at least 130 ms minimum will be generated. The 130 ms delay commences as the pushbutton reset input is released from the low level. The push–button can be initiated by connecting the WDS or NMI outputs to the PBRST input as shown in Figure 3.

**Non–Maskable Interrupt**
The DS1705/DS1706 generates a non–maskable interrupt (NMI) for early warning of a power failure. A precision comparator monitors the voltage level at the IN pin relative to an on–chip reference generated by an internal band gap. The IN pin is a high impedance input allowing for a user–defined sense point. An external resistor voltage divider network (Figure 5) is used to interface with high voltage signals. This sense point may be derived from a regulated supply or from a higher DC voltage level closer to the main system power input. Since the IN trip point V\text{TP} is 1.25 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 5. Proper operation of the DS1705/DS1706 requires that the voltage at the IN pin be limited to V\text{CC}. Therefore, the maximum allowable voltage at the supply being monitored (V\text{MAX}) can also be derived as shown in Figure 5. A simple approach to solving the equation is to select a value for R2 high enough to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for system shutdown between NMI and RST (or RST).

When the supply being monitored decays to the voltage sense point, the DS1705/DS1706 pulses the NMI output to the active state for a minimum 200 $\mu$s. The NMI power fail detection circuitry also has built–in hysteresis of 100 $\mu$V. The supply must be below the voltage sense point for approximately 5 $\mu$s before a low NMI will be generated. In this way, power supply noise is removed from the monitoring function, preventing false interrupts. During a power–up, any detected IN pin levels below V\text{TP} by the comparator are disabled from generating an interrupt until V\text{CC} rises to V\text{CC}\text{TP}. As a result, any potential NMI pulse will not be initiated until V\text{CC} reaches V\text{CC}\text{TP}.

Connecting NMI to PBRST would allow non–maskable interrupt to generate an automatic reset when an out–of–tolerance condition occurred in a monitored supply. An example is shown in Figure 3.

**Watchdog Timer**
The watchdog timer function forces WDS signals active when the ST input is not clocked within the 1 second time out period. Timeout of the watchdog starts when RST (or RST) becomes inactive. If a high–to–low transition occurs on the ST input pin prior to time–out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time out, the WDS signal is driven active (low) for a minimum of 130 ms. The ST input can be derived from many microprocessor outputs. The typical signals used are the microprocessors address signals, data signals, or control signals. When the microprocessor functions normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time–out. To guarantee that the watchdog timer does not time–out, a high–to–low transition must occur at or less than the minimum watchdog time–out of 1 second. A typical circuit example is shown in Figure 6.
MICROMONITOR BLOCK DIAGRAM

**Figure 1**

```
+ T.C. REFERENCE
- +
- +
VCC
```

```
DIGITAL SAMPLER
DIGITAL SAMPLER
```

```
LEVEL SENSE AND DEBOUNCE
```

```
DIGITAL DELAY
WATCHDOG STATUS LATCH
```

```
DS1706_/A/R/S/T
DS1706L/DS1706P
```

**PUSH-BUTTON RESET**

**Figure 2**

```
DS1706P
```

```
8051 µP
```

```
RST
ALE
```

**PUSH-BUTTON RESET CONTROLLED BY NMI AND WDS**

**Figure 3**

```
UPSTREAM SUPPLY VOLTAGE
```

```
DS1706
```

```
µP
```

```
RST
ALE
```
TIMING DIAGRAM: PUSHBUTTON RESET  Figure 4

NON–MASKABLE INTERRUPT CIRCUIT EXAMPLE  Figure 5

\[ V_{\text{SENSE}} = \frac{R_1 + R_2}{R_2} \times 1.25 \]
\[ V_{\text{MAX}} = \frac{V_{\text{SENSE}}}{V_{\text{TP}}} \times V_{\text{CC}} \]

Example:  
\[ V_{\text{SENSE}} = 4.50 \text{ volts at the trip point} \]
\[ V_{\text{CC}} = 3.3 \text{ volts} \]
\[ 10\text{K}\Omega = R_2 \]

Therefore:  
\[ 4.50 \times 3.3 = 12.4 \text{ volts maximum} \]

\[ 4.5 = \frac{R_1 + 10\text{K}}{10\text{K}} \times 1.25 \quad R_1 = 26\text{K}\Omega \]
WATCHDOG TIMER  Figure 6

TIMING DIAGRAM: STROBE INPUT  Figure 7

TIMING DIAGRAM: NON–MASKABLE INTERRUPT  Figure 8
TIMING DIAGRAM: POWER DOWN  Figure 9

- **VCC**
- **VCCP(MAX)**
- **VCCP(MIN)**
- **RST**
  (DS1705 AND DS1706_/R/S/T)
- **WDS**
  (DS1706L AND DS1706P ONLY)
- **tRPD**
- **tF**
- **VOL**
- **VCCS**
- **RST SLEWS WITH VCC**
- **WDS SLEWS WITH VCC**
TIMING DIAGRAM: POWER UP  Figure 10

- $V_{CC}$
- $V_{OH}$
- $V_{OL}$
- $t_{RPU}$
- $V_{CCTP}$
- $V_{CCTP(MIN)}$
- $V_{CCTP(MAX)}$
- RST

(DS1705 AND DS1706, RST)

(DS1706L AND DS1706P ONLY)

WUBS
ABSOLUTE MAXIMUM RATINGS*
- Voltage on VCC Pin Relative to Ground: −0.5V to +7.0V
- Voltage on I/O Relative to Ground**: −0.5V to VCC + 0.5V
- Operating Temperature: −40°C to +85°C
- Storage Temperature: −55°C to +125°C
- Soldering Temperature: 260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**The voltage input on IN, ST, and PBRST can be exceeded if the input current is less than 10 mA.

RECOMMENDED DC OPERATING CONDITIONS
(−40°C to +85°C)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>VCC</td>
<td>1.0</td>
<td>5.5</td>
<td></td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>ST and PBRST Input High Level</td>
<td>VH</td>
<td>2.0</td>
<td></td>
<td>VCC+0.3</td>
<td>V</td>
<td>1, 3</td>
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<tr>
<td>ST and PBRST Input Low Level</td>
<td>VL</td>
<td>−0.03</td>
<td>+0.5</td>
<td>V</td>
<td>1</td>
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DC ELECTRICAL CHARACTERISTICS
(−40°C to +85°C; VCC=1.2V to 5.5V)

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<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
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<tbody>
<tr>
<td>VCC Trip Point DS1705/DS1706L</td>
<td>VCTP</td>
<td>4.50</td>
<td>4.65</td>
<td>4.75</td>
<td>V</td>
<td>1</td>
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<td>VCC Trip Point DS1706</td>
<td>VCTP</td>
<td>4.25</td>
<td>4.40</td>
<td>4.50</td>
<td>V</td>
<td>1</td>
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<td>VCC Trip Point DS1706T</td>
<td>VCTP</td>
<td>3.00</td>
<td>3.08</td>
<td>3.15</td>
<td>V</td>
<td>1</td>
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<td>VCC Trip Point DS1706S</td>
<td>VCTP</td>
<td>2.85</td>
<td>2.93</td>
<td>3.00</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>VCC Trip Point DS1706P or R</td>
<td>VCTP</td>
<td>2.55</td>
<td>2.63</td>
<td>2.70</td>
<td>V</td>
<td>1</td>
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<tr>
<td>Input Leakage</td>
<td>IL</td>
<td>−1.0</td>
<td>+1.0</td>
<td>µA</td>
<td>2</td>
<td></td>
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<tr>
<td>Output Current @ 2.4 volts</td>
<td>IOH</td>
<td>350</td>
<td>µA</td>
<td>3</td>
<td></td>
<td></td>
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<tr>
<td>Output Current @ 0.4 volts</td>
<td>IOL</td>
<td>10</td>
<td>mA</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage @ −500 µA</td>
<td>VOH</td>
<td>VCC+−0.3</td>
<td>VCC−0.1</td>
<td>V</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Operating Current @ VCC &lt; 5.5 volts</td>
<td>ICC</td>
<td>60</td>
<td>µA</td>
<td>5</td>
<td></td>
<td></td>
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<tr>
<td>Operating Current @ VCC &lt; 3.8 volts</td>
<td>ICC</td>
<td>50</td>
<td>µA</td>
<td>5</td>
<td></td>
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<tr>
<td>IN Input Trip Point</td>
<td>VTP</td>
<td>1.20</td>
<td>1.25</td>
<td>1.30</td>
<td>V</td>
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CAPACITANCE
(tA=25°C)

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<th>PARAMETER</th>
<th>SYMBOL</th>
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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Capacitance</td>
<td>Cin</td>
<td>5</td>
<td></td>
<td></td>
<td>pF</td>
<td></td>
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<tr>
<td>Output Capacitance</td>
<td>Cout</td>
<td>7</td>
<td></td>
<td></td>
<td>pF</td>
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</tbody>
</table>
### AC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; V\(_{CC}\) = 1.2V to 5.5V)

<table>
<thead>
<tr>
<th>PARAMETER</th>
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<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>PBRST = V(_{IL})</td>
<td>(t_{PB})</td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Reset Active Time</td>
<td>(t_{RST})</td>
<td>130</td>
<td>205</td>
<td>285</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>ST Pulse Width</td>
<td>(t_{ST})</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
<td>6</td>
</tr>
<tr>
<td>V(_{CC}) Detect to RST and RST</td>
<td>(t_{RPD})</td>
<td>5</td>
<td>8</td>
<td></td>
<td>(\mu)s</td>
<td>9</td>
</tr>
<tr>
<td>V(_{CC}) Slew Rate</td>
<td>(t_{F})</td>
<td>20</td>
<td></td>
<td></td>
<td>(\mu)s</td>
<td></td>
</tr>
<tr>
<td>V(_{CC}) Detect to RST and RST</td>
<td>(t_{RPU})</td>
<td>130</td>
<td>205</td>
<td>285</td>
<td>ms</td>
<td>7</td>
</tr>
<tr>
<td>V(_{CC}) Slew Rate</td>
<td>(t_{R})</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>PBRST Stable Low to RST and RST</td>
<td>(t_{PDLY})</td>
<td></td>
<td></td>
<td>250</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Watchdog Timeout</td>
<td>(t_{TD})</td>
<td>1.0</td>
<td>1.6</td>
<td>2.2</td>
<td>s</td>
<td>8</td>
</tr>
<tr>
<td>VIN Detect to NMI</td>
<td>(t_{IPD})</td>
<td>5</td>
<td>8</td>
<td></td>
<td>(\mu)s</td>
<td>9</td>
</tr>
</tbody>
</table>

**NOTES:**

1. All voltages are referenced to ground.
2. PBRST is internally pulled up to V\(_{CC}\) with an internal impedance of 40K\(\Omega\) typical and the ST input is internally pulled up to V\(_{CC}\) with an internal impedance of 180K\(\Omega\) typical.
3. V\(_{CC}\) \(\geq\) 2.4 volts
4. V\(_{CC}\) < 2.4 volts
5. Measured with outputs open and all inputs at V\(_{CC}\) or ground.
6. Must not exceed \(t_{TD}\) minimum.
7. \(t_{R}\) = 5 \(\mu\)s
8. Minimum watchdog timeout tested at 2.7 volts for the 3.3 volt devices and 4.5 volts for the 5.0 volt devices.
9. Noise immunity – pulses < 2 \(\mu\)s at V\(_{CC}\) minimum will not cause a reset.
PART MARKING CODES

A, B, C and D represents the device type and tolerance.

ABCD
705_ = DS1705
706_ = DS1706
706L = DS1706L
706P = DS1706P
706R = DS1706R
706S = DS1706S
706T = DS1706T

WWY represents the device manufacturing Work Week, Year.
DATA SHEET REVISION SUMMARY
The following represent the key differences between 01/12/96 and 06/17/97 version of the DS1705/06 data sheet. Please review this summary carefully.

1. Page 8 add the following statement to the "Absolute Maximum Ratings"
   The voltage input limits on IN, ST, and PBREST can be exceeded if the input current is less than 10 mA.