DALLAS SEMICONDUCTOR

DS1710
Partitioned NV Controller

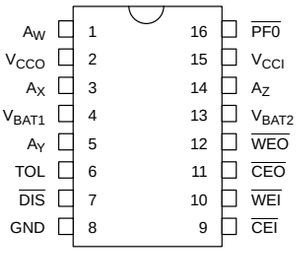
FEATURES

- Converts CMOS RAMs into nonvolatile memories
- Automatically selects +3.0V or +5.0V operation
- SOIC version is pin compatible with the Dallas Semiconductor DS1210S and DS1610S NV Controllers
- Unconditionally write protects all of memory when V_{cc} is out of tolerance
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Automatically switches to battery backup supply when power fail occurs
- Provides for multiple batteries
- Consumes less than 100 nA of battery current
- Tests battery on power up by inhibiting the second memory cycle
- Optional 5% or 10% Power Fail Detection
- 16-pin DIP or 16-pin SOIC surface mount package or 20–pin TSSOP package
- Low forward voltage drop on the V_{CC} switch with currents of up to 150 mA
- Optional industrial temperature range of -40°C to +85°C

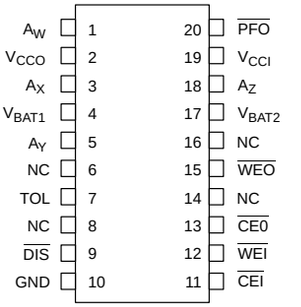
DESCRIPTION

The DS1710 is a low power CMOS circuit which solves the application problems of converting CMOS RAMS into nonvolatile memories. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The incoming power supply voltage at the V_{CCI} input pin is constantly monitored for an out of tolerance condition. When such a condition is detected, both the chip enable and write enable outputs are inhibited to protect stored data. The battery inputs are used to supply V_{CCO} with power when

PIN ASSIGNMENT



16-Pin DIP and 16-Pin SOIC



20–Pin TSSOP

PIN DESCRIPTION

V_{CCI}	–	Input 2.7 to 5.5 Volt Supply
V_{BAT1}	–	+ Battery 1 Input
V_{BAT2}	–	+ Battery 2 Input
V_{CCO}	–	RAM Power (V_{CC}) Supply
GND	–	Ground
$\overline{CEI}$	–	Chip Enable Input
$\overline{CEO}$	–	Chip Enable Output
$\overline{WEI}$	–	Write Enable Input
$\overline{WEO}$	–	Write Enable Output
TOL	–	Power Supply Tolerance Select
A_W - A_Z	–	Address Inputs
$\overline{DIS}$	–	Memory Partition Disable
$\overline{PF0}$	–	Power Fail Output
NC	–	No Connect

V_{CCI} is less than the battery input voltages. Special circuitry uses a low leakage CMOS process which affords precise voltage detection at extremely low current consumption. By combining the DS1710 Partitioned NV Controller chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

The DS1710 Partitioned NV Controller incorporates all the functions of the DS1610 with the additional feature of either +3.0V or +5.0V operation. The DS1710 functions like the Dallas Semiconductor DS1210 NV controller when the ($\overline{DIS}$) disable pin is grounded and also incorporates the power–up auto sensing. An internal pull–down resistor to ground on the $\overline{DIS}$ pin of the DS1710S allows it to retrofit into DS1210S applications. When the $\overline{DIS}$ pin is grounded the address inputs A_W - A_Z and the write enable input $\overline{WEI}$ are ignored. Also the power fail output $\overline{PFO}$ and the write enable output $\overline{WEO}$ are tristated.

POWER–UP AUTO SENSING

V_{CCI} will accept either +3.0V or +5.0V input. Selection of 3V operation is automatically invoked when V_{CC} rises and remains between V_{CCTP2} and V_{CCTP1} for t_{REC}. 5V operation is automatically selected if V_{CC} rises and remains above both V_{CCTP2} and V_{CCTP1} for t_{REC}. In either case, t_{REC} is measured from the time V_{CC} first rises above V_{CCTP2}. The DS1710 will not change modes until V_{CC} falls below V_{CCTP2}.

OPERATION – DISABLE PIN CONNECTED TO V_{CCO}

The DS1710 performs five circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming power supply (V_{CCI}) depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function provided by the DS1710 is power fail detection. The incoming supply (V_{CCI}) is constantly monitored. When the supply goes out of tolerance a precision comparator detects power failure and inhibits both the chip enable output ($\overline{CEO}$) and the write enable output ($\overline{WEO}$). A third function of write protection is accomplished by holding both the chip enable output $\overline{CEO}$ and write enable output $\overline{WEO}$ to within 0.2 volts of V_{CCO} when V_{CCI} is out of tolerance. If $\overline{CEI}$ is low at the time that power fail detection occurs the $\overline{CEO}$ signal is kept low until $\overline{CEI}$ is brought high again. However, $\overline{CEO}$ is forced high after 1.5 µsec regardless of the state of $\overline{CEI}$. Similarly, if $\overline{WEI}$ is low at the time that power fail detection occurs, the $\overline{WEO}$ is signal will remain low until $\overline{WEI}$ is brought high or 1.5 µsec elapses. The delay of write protection until the current memory cycle is complete prevents corrupted data. Power fail detection occurs in the range of 4.75 to 4.5 volts with the tolerance pin TOL grounded and in 5 volt mode. If the tolerance pin is connected to V_{CCO} while in 5 volt mode, then power fail detection occurs in the range of 4.5 volts to 4.25 volts. If in 3 volt mode, the power fail detection will occur in the range of 2.7 to 2.5 volts. The $\overline{PF0}$ signal is driven low and remains low until V_{CCI} returns to nominal conditions. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ and $\overline{WEO}$ will follow $\overline{WEI}$. The fourth function which the DS1710 performs is a battery status warning so that potential data loss is avoided. Each time V_{CCI} is applied to the device battery status is checked with a precision comparator. If during battery backup, no switch occurred from one battery to the other, the voltage of the battery supplying power when V_{CCI} is applied is checked. If this voltage is less than 2.0 volts the second chip enable cycle after power is applied is inhibited. If any switch from one battery to another did occur the voltage of both batteries is checked. If either voltage is less than 2.0 volts the second chip enable cycle will be inhibited. Battery status can therefore be determined by performing a read cycle after power up to any location in memory, verifying that memory location's contents. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data then the data is in danger of being corrupted. The fifth function of the DS1710 provides for battery redundancy. When data integrity is extremely important it is wise to use two batteries to insure reliability. The DS1710 controller provides an internal isolation switch which allows the connection of two batteries. When entering battery backup operation, the battery with the highest voltage is selected for use. If one battery should fail, the other would then supply energy to the connected load. The switch to a redundant battery is transparent to circuit operation and to the user. In applications where battery redundancy is not a major concern a single battery should be connected to the BAT1 pin. The BAT2 battery pin must be grounded. When batteries are first connected to one or both of the V_{BAT} pins V_{CCO} will not show the battery potential until V_{CCI} is applied and removed for the first time.

OPERATION – WRITE PROTECTION PROGRAMMING MODE

When the disable pin is connected to V_{CCI} or V_{CCO}, the DS1710 performs all of the functions described earlier with the addition of a partition switch which selectively write protects blocks of memory. The state of the $\overline{DIS}$ pin is strobed and latched as V_{CCI} crosses the power fail trip point so that the DS1710 maintains its configuration during power loss. If the strobed value of $\overline{DIS}$ is high, the internal pull–down resistor on the $\overline{DIS}$ pin will be disconnected in the power fail state to eliminate the possibility of battery discharge. The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A_W-A_Z. These address lines are normally the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions, the size of each partition is determined by the size of the memory. For example, a 128K X 8 memory would be divided into 16 partitions of 128K/16 or 8K X 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A_W through A_Z and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A_X was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1710 to inhibit $\overline{WEO}$ from going low as $\overline{WEI}$ goes low whenever $A_Z A_Y A_X A_W$=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM. Also note that on initial battery attach the partition register can power up in any state.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A_W	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A_X	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A_Y	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A_Z	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

PARTITION REGISTER MAPPING Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_Z A_Y A_X A_W)
A_W	BIT 21	PARTITION 0	0000
A_X	BIT 21	PARTITION 1	0001
A_Y	BIT 21	PARTITION 2	0010
A_Z	BIT 21	PARTITION 3	0011
A_W	BIT 22	PARTITION 4	0100
A_X	BIT 22	PARTITION 5	0101
A_Y	BIT 22	PARTITION 6	0110
A_Z	BIT 22	PARTITION 7	0111
A_W	BIT 23	PARTITION 8	1000
A_X	BIT 23	PARTITION 9	1001
A_Y	BIT 23	PARTITION 10	1010
A_Z	BIT 23	PARTITION 11	1011
A_W	BIT 24	PARTITION 12	1100
A_X	BIT 24	PARTITION 13	1101
A_Y	BIT 24	PARTITION 14	1110
A_Z	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 6=GND Supply Voltage (5V Operation)	V_{CCI}	4.75	5.0	5.5	V	1
Pin 6 = V_{CCO} Supply Voltage (5V Operation)	V_{CCI}	4.5	5.0	5.5	V	1
Pin 6=GND Supply Voltage (3V Operation)	V_{CCI}	2.7	3.0	4.0	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC} + 0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1} V_{BAT2}	2.0		4.0	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}<V_{BAT}, V_{CCI}<V_{CCTP2})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	
$\overline{WEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			100	nA	2, 3
Battery Backup Current @ V_{CCO} = V_{BAT} -0.2V	I_{CCO2}			150	µA	6, 8

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{CC1}			5	mA	3, 14
Standby Current	I_{CC2}			200	µA	3, 15
Supply Voltage	V_{CCO}	V_{CC} -0.2			V	1
Supply Current	I_{CCO1}			150	mA	4
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
$\overline{PFO}$, $\overline{WEO}$ Output @ 2.4V	I_{OH}	–1.0			mA	10, 16
$\overline{PFO}$, $\overline{WEO}$ Output @ 0.4V	I_{OL}			4.0	mA	10, 16
V_{CC} Trip Point (TOL=GND)	V_{CCTP1}	4.50	4.62	4.75	V	1, 16
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP1}	4.25	4.37	4.50	V	1, 16
V_{CC} Trip Point	V_{CCTP2}	2.50	2.60	2.70	V	1, 16
$\overline{CEI}$ to $\overline{CEO}$ Impedance	Z_{CE}			30	Ω	5
$\overline{DIS}$ Pull–down Resistance	R_{DIS}	50K		250K	Ω	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=4.75V to 5.50V, TOL=GND
V_{CCI}=4.50V to 5.50V, TOL=V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	20			ns	9
$\overline{CEI}$, $\overline{WEI}$ Pulse Width	t_{CW}	75			ns	
$\overline{CEI}$ to $\overline{CEO}$ Falling Propagation Delay	t_{PDF}			5	ns	10
Later of $\overline{CEI}$, $\overline{WEI}$ to $\overline{WEO}$ Falling Propagation Delay	t_{PDF}			20	ns	10, 11
$\overline{CEI}$ to $\overline{CEO}$ Rising Propagation Delay	t_{PDR}			5	ns	10
Earlier of $\overline{CEI}$, $\overline{WEI}$ to $\overline{WEO}$ Rising Propagation Delay	t_{PDR}			5	ns	10, 11
Write Recovery	t_{WR}	10			ns	11

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; 5V Operation)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t_{REC}	100		200	ms	12
V_{CC} Slew Rate Power Down	t_F	300			µs	
V_{CC} Slew Rate Power Down	t_{FB}	10			µs	
V_{CC} Slew Rate Power Up	t_R	0			µs	13
$\overline{CEI}$ Pulse Width	t_{CE}			1.5	µs	7, 8
$\overline{WEI}$ Pulse Width	t_{CE}			1.5	µs	7, 8

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=2.7V to 4.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{CC1}			3	mA	3, 14
Standby Current	I_{CC2}			200	µA	3, 15
Supply Voltage	V_{CCO}	V_{CC} -0.2			V	1
Supply Current	I_{CCO1}			100	mA	4
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
$\overline{PFO}$, $\overline{WEO}$ Output @ 2.4V	I_{OH}	–1.0			mA	10, 16
$\overline{PFO}$, $\overline{WEO}$ Output @ 0.4V	I_{OL}			4.0	mA	10, 16
V_{CC} Trip Point	V_{CCTP}2	2.50	2.60	2.70	V	1, 16
$\overline{CEI}$ to $\overline{CEO}$ Impedance	Z_{CE}			60	Ω	5
$\overline{DIS}$ Pull–down Resistance	R_{DIS}	50K		250K	Ω	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=2.7V to 4.0V)

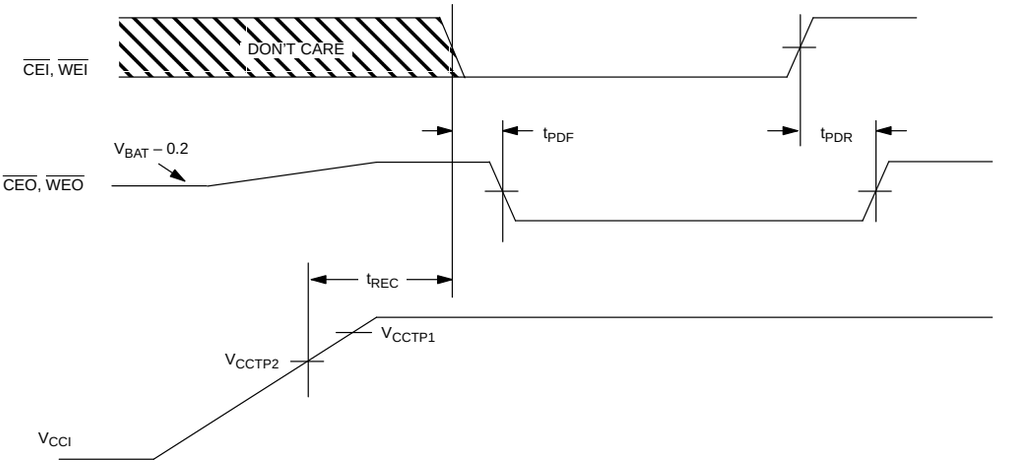
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	20			ns	9
$\overline{CEI}$, $\overline{WEI}$ Pulse Width	t_{CW}	75			ns	
$\overline{CEI}$ to $\overline{CEO}$ Falling Propagation Delay	t_{PDF}			5	ns	10
Later of $\overline{CEI}$, $\overline{WEI}$ to $\overline{WEO}$ Falling Propagation Delay	t_{PDF}			50	ns	10, 11
$\overline{CEI}$ to $\overline{CEO}$ Rising Propagation Delay	t_{PDR}			5	ns	10
Earlier of $\overline{CEI}$, $\overline{WEI}$ to $\overline{WEO}$ Rising Propagation Delay	t_{PDR}			20	ns	10, 11
Write Recovery	t_{WR}	10			ns	11

AC ELECTRICAL CHARACTERISTICS

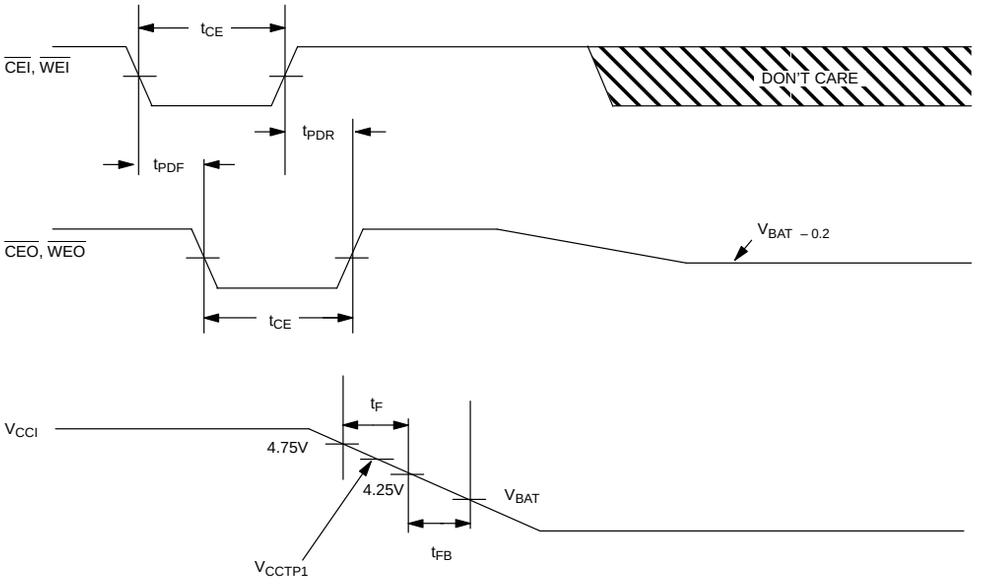
(0°C to 70°C; 3V Operation)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t_{REC}	100		200	ms	12
V_{CC} Slew Rate Power Down	t_F	300			µs	
V_{CC} Slew Rate Power Up	t_R	0			µs	13
$\overline{CEI}$ Pulse Width	t_{CE}			1.5	µs	7, 8
$\overline{WEI}$ Pulse Width	t_{CE}			1.5	µs	7, 8

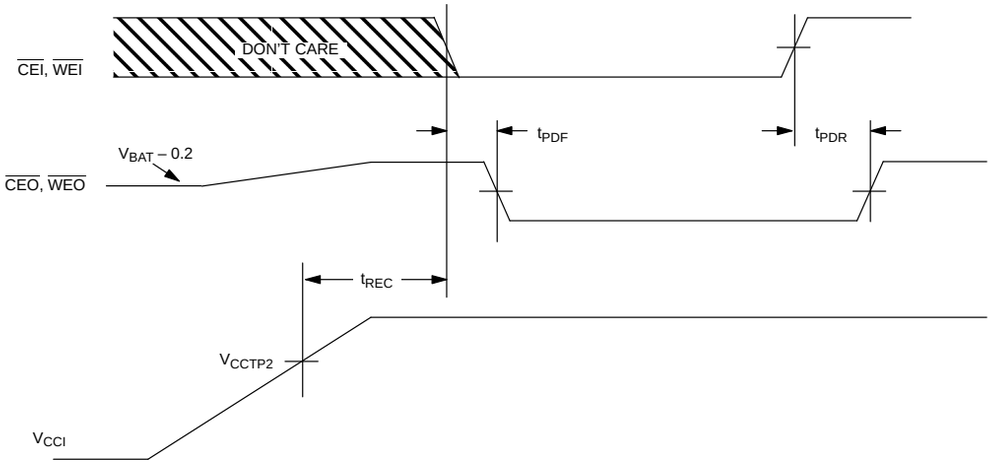
TIMING DIAGRAM: POWER UP (5 VOLT)



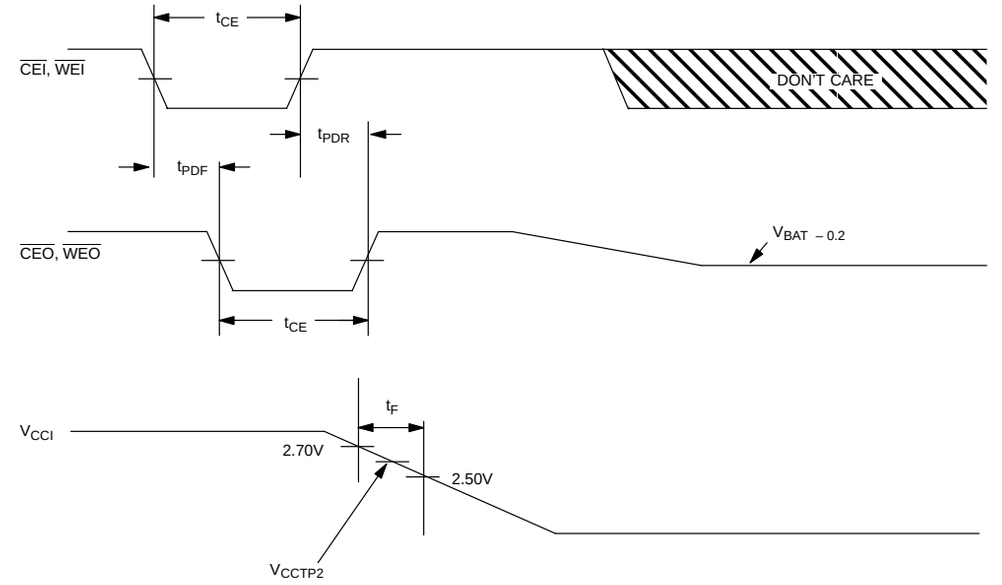
TIMING DIAGRAM: POWER DOWN (5 VOLT)



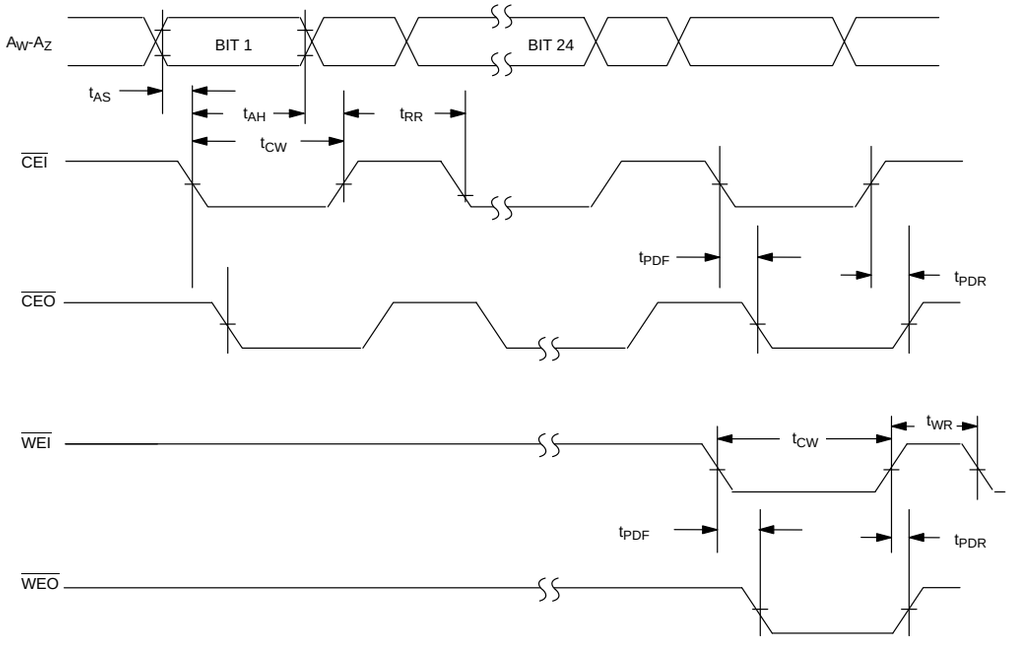
TIMING DIAGRAM: POWER UP (3 VOLT)



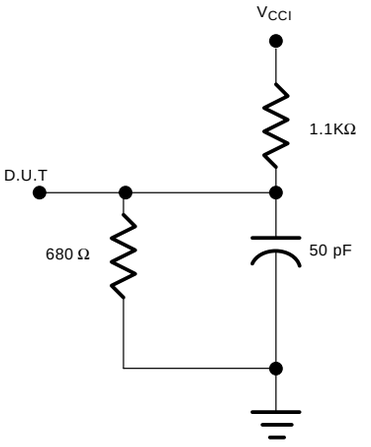
TIMING DIAGRAM: POWER DOWN (3 VOLT)



TIMING DIAGRAM: LOADING PARTITION REGISTER



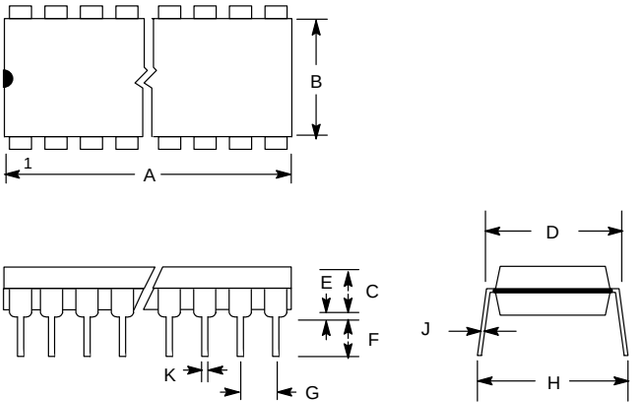
OUTPUT LOAD Figure 1



NOTES:

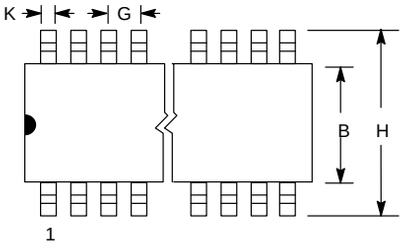
1. All voltages are reference to ground
2. Only one battery input is required.
3. Measured with outputs open circuited.
4. I_{CC01} is the maximum average load which the DS1710 can supply to the memories.
5. Z_{CE} is an average input-to-output impedance as the input is swept from ground to V_{CCI} and less than 4 mA is forced through Z_{CE}.
6. I_{CC02} is the maximum average load current which the DS1710 can supply to the memories in the battery backup mode.
7. t_{CE} max must be met to insure data integrity on power loss.
8. Chip Enable Output $\overline{CEO}$ can only sustain leakage current in the battery mode.
9. Applies only when loading partition switch.
10. Measured with a load as shown in Figure 1.
11. Measured with $\overline{DIS}$ at a logic high level.
12. $\overline{CEO}$ and $\overline{WEO}$ will be held high for a time equal to t_{REC} after V_{CCI} crosses V_{CCTP2}.
13. t_R is the slew rate of V_{CCI} from 4.25V to 4.75V or 2.50 to +2.70 volts.
14. $\overline{CEI}$, $\overline{WEI}$, A_W - A_Z run at minimum timing set and at voltage levels of 0V to 3V.
15. All inputs within 0.3V of ground or V_{CCI} and $\overline{CEI}$ within 0.3V of V_{CCI}.
16. The power fail output signal ($\overline{PFO}$) is driven active (V_{OL} = 0.4V) when the V_{CC} trip point occurs. While active, the $\overline{PFO}$ pin can sink 4 mA and will maintain a maximum output voltage of 0.4 volts. When inactive, the voltage output of $\overline{PFO}$ is 2.4 volts minimum and will source a current of 1 mA.

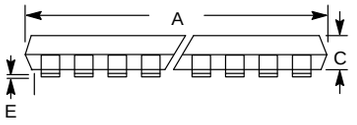
DS1710 16–PIN DIP (300 MIL)

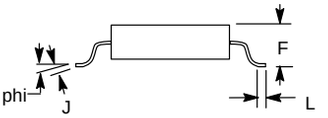


PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.740 18.80	0.780 19.81
B IN. MM	0.240 6.10	0.260 6.60
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.04	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN MM	0.320 8.13	0.370 9.40
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

DS1710 16–PIN SOIC (300 MIL)

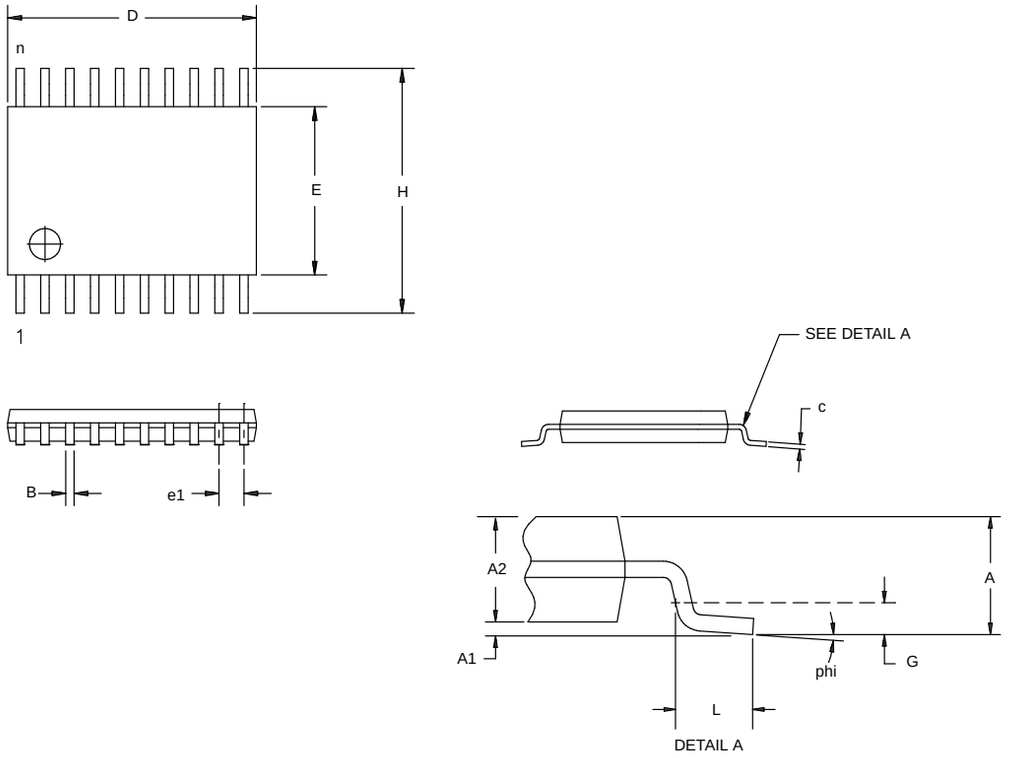






PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.402 10.21	0.412 10.46
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	.050 BSC 1.27 BSC	
H IN MM	0.398 10.11	0.416 10.57
J IN MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN MM	.016 .40	.040 1.02
PHI	0°	8°

DS1710 20-PIN TSSOP



DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°