**PRELIMINARY**

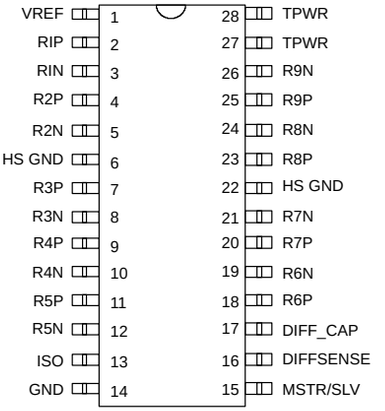
DALLAS SEMICONDUCTOR

# DS2119M
## Ultra2 LVD/SE SCSI Terminator

### FEATURES

- Fully compliant with Ultra2 SCSI
- Provides Multimode Low Voltage Differential/Single–Ended (LVD/SE) termination for 9 signal line pairs
- Auto–selection of LVD or SE termination
- 5% tolerance on SE and LVD termination resistance
- Low power down capacitance of 3 pF
- Onboard thermal shutdown circuitry
- SCSI bus hot plug compatible
- Fully supports actively negated SE SCSI signals

### PIN ASSIGNMENT




DS2119MB 28–PIN TSSOP

### DESCRIPTION

The DS2119M Ultra2 LVD/SE SCSI Terminator is both a Low Voltage Differential (LVD) and Single–Ended (SE) terminator. The multimode operation enables the designer to implement LVD in current products while allowing the end–user SE backward compatibility with legacy devices. If the device is connected in an LVD only bus, the DS2119M will use LVD termination. If any SE devices are connected to the bus, the DS2119M will use SE termination. This is accomplished automatically inside the part by sensing the voltage on the SCSI bus DIFFSENS line.

For the LVD termination, the DS2119M integrates two current sources with nine precision resistor strings. For the SE termination, one regulator and nine precision 110 Ohm resistors are used. Three DS2119M terminators are needed for a Wide SCSI bus.

## REFERENCE DOCUMENTS

SCSI Parallel Interface 2 (SPI–2) {X310/1142D}
SCSI–3 Parallel Interface (SPI) {X3T10/855D}
SCSI–3 Fast–20 {X3T10/1071D}
SCSI–2 {X3.131–1994}

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## FUNCTIONAL DESCRIPTION

The DS2119 combines LVD and SE termination with DIFFSENSE sourcing and detection.

A bandgap reference is fed into two amplifiers, which create a 1.25V reference voltage and a 2.85V reference voltage. The control logic determines which of these references will be applied to the termination resistors. If the SCSI bus is in LVD mode, then the 1.25V reference will be used. If the SCSI bus is in SE mode, then the 2.85V reference will be used. That same control logic will switch in/out parallel resistors to change the total termination resistance accordingly. Finally, in SE mode, the Rn pins will be switched to ground.

The DIFFSENSE circuitry decodes trinary logic. There will be one of three voltages on the SCSI control line called DIFFSENS. Two comparators and a NAND gate determine if the voltage is above V, below V, or in between. That indicates the mode of the bus to be HVD, SE, or LVD, respectively.

The DS2119M's DIFF_CAP pin monitors the DIFFSENS line to determine the proper operating mode of the device. The DIFFSENSE pin can also drive the SCSI DIFFSENS line (when MSTR/SLV = 1) to determine the SCSI bus operating mode. The DS2119M switches to the termination mode that is appropriate for the bus based on the value of the DIFFSENS voltage. These modes are:

**LVD mode** LVD termination is provided by a precision laser trimmed resistor string with two current sources. This configuration yields a 105Ω differential and 150Ω common mode impedance. A fail–safe bias of 112 mV is maintained when no drivers are connected to the SCSI bus.

**SE mode** When the external driver for a given signal line turns off, the active terminator will pull that signal line to 2.85 volts (quiescent state). When used with an active negation driver, the power amp can sink 22 mA per line while keeping the voltage reference in regulation. The terminating resistors maintain their 110Ω value.

**HVD Isolation Mode** The DS2119M identifies that there is an HVD (high voltage differential) device on the SCSI bus and isolates the termination pins from the bus.

When ISO = 1, the termination pins are isolated from the SCSI bus, Vref remains active. During thermal shutdown, the termination pins are isolated from the SCSI bus and Vref becomes high impedance. The diffsense driver is shut down during either of these two events.

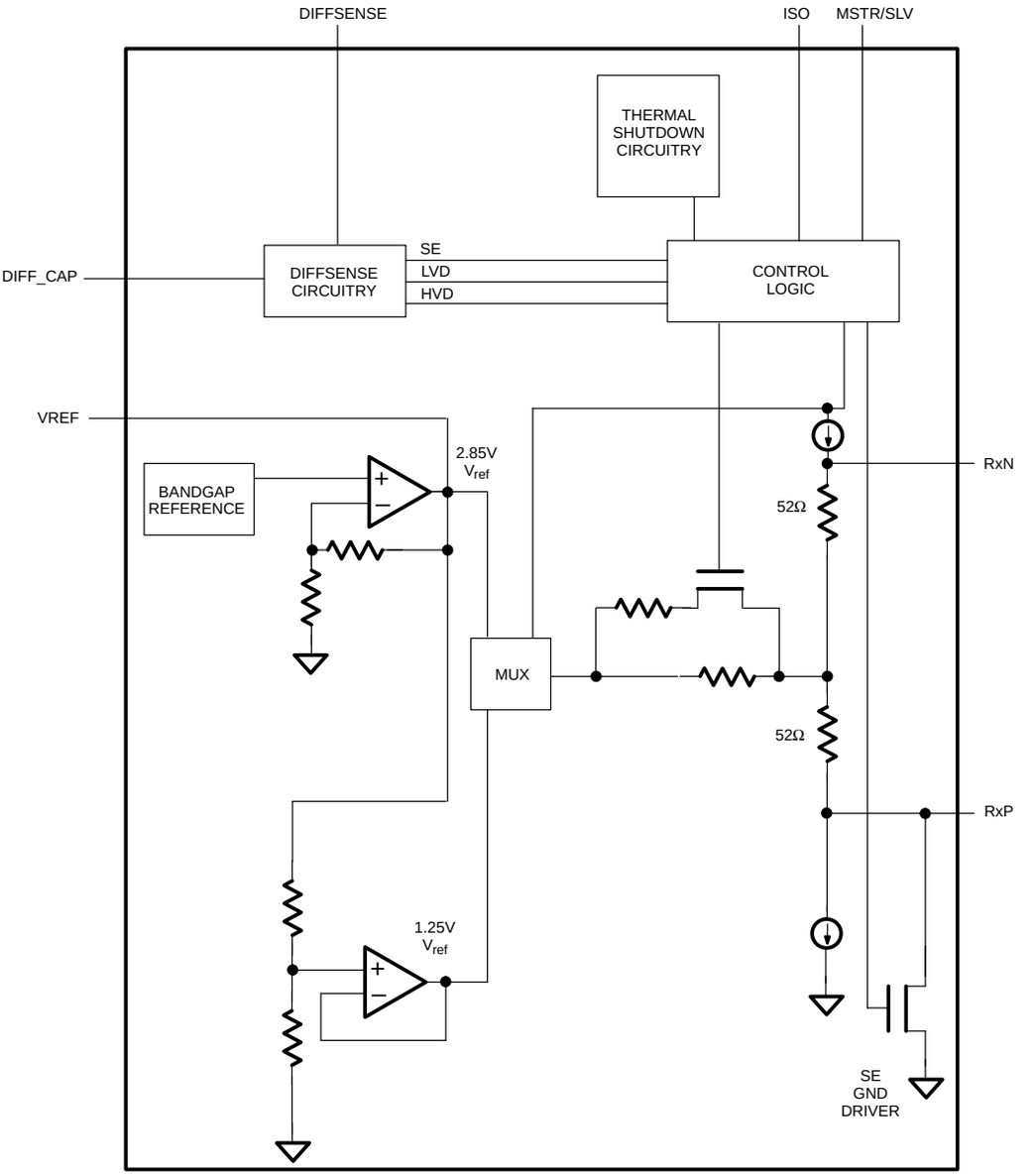
To ensure proper operation, the TPWR pin should be connected to the SCSI bus TERMPWR line. As with all analog circuitry, the TERMPWR and VDD lines should be bypassed locally. A 2.2 µF capacitor and a 0.01 µF high frequency capacitor is recommended between TPWR and ground and placed as close as possible to the DS2119M. The DS2119M should be placed as close as possible to the SCSI connector to minimize signal and power trace length, thereby resulting in less input capacitance and reflections which can degrade the bus signals.

To maintain the specified regulation, a 4.7 µF capacitor is required between the Vref pin (VREF) and ground of each DS2119M. A high frequency cap (0.1 µF ceramic recommended) can also be placed on the Vref pin in applications that use fast rise/fall time drivers. A typical SCSI bus configuration is shown in Figure 2.

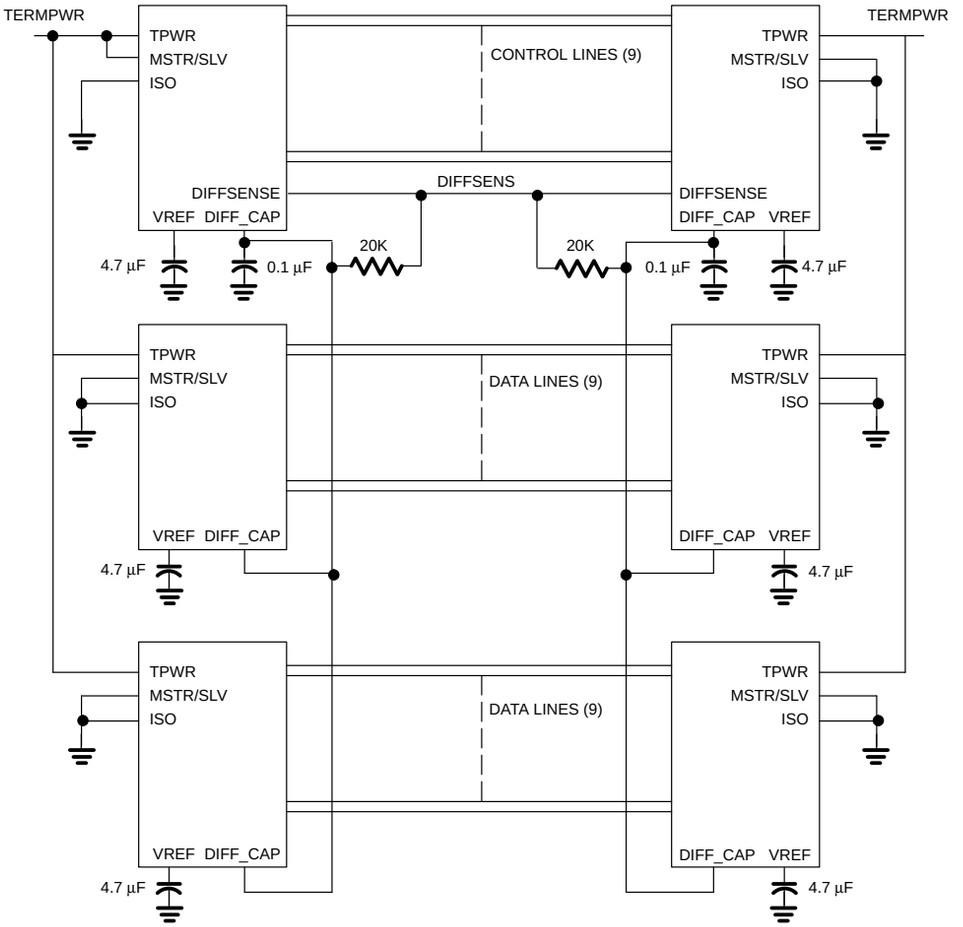
### NOTE:

DIFFSENS – Refers to the SCSI bus signal.
DIFFSENSE – Refers to the Dallas Semiconductor pin name and internal circuitry relating to differential sensing.

**DS2119M BLOCK DIAGRAM** Figure 1



**SCSI BUS CONFIGURATION** Figure 2



**PIN DESCRIPTION** Table 1

| PIN | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | VREF | **Reference Voltage.** 2.85 volt reference; must be decoupled with a 4.7 µF cap. |
| 2, 3 | NC | **No Connect.** Do not connect these pins. |
| 4–7, 11–16, 22–25, 29–32 | RxP, RxN | **Signal Termination.** Connect to SCSI bus signal lines. |
| 8, 10, 26, 9, 28, 27 | HS GND | **Heat Sink Ground.** Internally connected to the mounting pad. Should be either grounded. |
| 17 | ISO | **Isolation.** When pulled high, the DS2119M isolates it's bus pins (RxP, FxP) from the SCSI bus. |
| 18 | GND | **Ground.** Signal ground; 0.0 volts. |
| 19 | MSTR/SLV | **Master/slave.** Mode select for the non–controlling terminator. MSTR enables the DIFFSENSE driver. |
| 20 | DIFFSENSE | **DIFFSENSE.** Output to drive the SCSI bus DIFFSENS line. |
| 21 | DIFF_CAP | **DIFFSENSE CAPACITOR.** Connect 0.1 µF capacitor for DIFFSENSE filter. Input to detect the type of device (differential or single–ended) on the SCSI bus. |
| 36 | TPWR | **Terminator Power.** Connect to SCSI bus TERMPWR line and decouple with 2.2 µF capacitor. |

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Termpower Voltage | $V_{tpwr}$ | 4.0 | | 5.50 | V | |
| Logic 0 | $V_{il}$ | –0.3 | | +0.8 | V | |
| Logic 1 | $V_{ih}$ | 2.0 | | $V_{tpwr}$ + 0.3 | V | |
| Operating Temperature | $V_{amb}$ | 0 | | 70 | °C | |

## SINGLE ENDED CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| SE Termination Resistance | Rse | 104.5 | 110 | 115.5 | Ohms | 1 |
| SE Voltage Reference | Vref | 2.79 | | 2.91 | Volts | |
| SE Output Current | Iose | | | 25.4 | mA | 2 |
| Output Capacitance | Cout | | | 3 | pF | 3 |

## LOW VOLTAGE DIFFERENTIAL CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Differential Mode Termination Resistance | Rdm | 100 | | 110 | Ohms | |
| Common Mode Termination Resistance | Rcm | 110 | | 190 | Ohms | |
| Differential Mode Bias | Vdm | 100 | | 125 | mV | 4 |
| Common Mode Bias | Vcm | 1.125 | | 1.375 | V | |

## DC CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Termpower Current | $I_{tpmr}$ | | 35 | | mA | 4 |
| Input Leakage High | $I_{ih}$ | –1.0 | | | uA | |
| Input Leakage Low | $I_{il}$ | | | 1.0 | uA | |
| Output Current High | $I_{oh}$ | –1.0 | | | mA | 5, 7 |
| Output Current Low | $I_{ol}$ | 4.0 | | | mA | 6, 7 |
| DIFFSENS SE Operating Range | $V_{seor}$ | –0.3 | | 0.5 | V | |
| DIFFSENS LVD Operating Range | $V_{lvdor}$ | 0.7 | | 1.9 | V | |
| DIFFSENS HVD Operating Range | $V_{hvdor}$ | 2.4 | | $V_{tpwr}$ + 0.3 | V | |
| Diffsense Driver Output Voltage | $V_{dso}$ | 1.2 | | 1.4 | V | 8, 9 |
| Diffsense Driver Source Current | $I_{dsh}$ | | 5 | 15 | mA | 8, 10 |
| Diffsense Driver Sink Current | $I_{dsl}$ | 20 | | 200 | uA | 8, 11 |

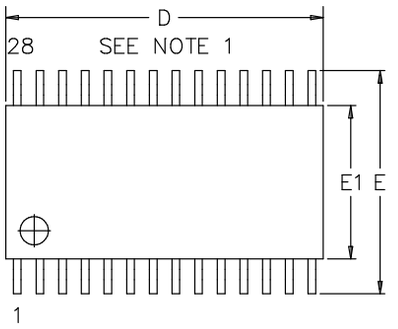
**REGULATOR CHARACTERISTICS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Line Regulation | $LI_{REG}$ | | 1.0 | 2.0 | % | |
| Load Regulation | $LO_{REG}$ | | 1.3 | 3.0 | % | |
| Current Limit | $I_{LIM}$ | | 350 | | mA | |
| Sink Current | $I_{SINK}$ | 200 | | | mA | |

**NOTES:**

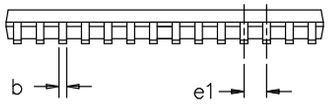
1. Vline = 0–3.0 volts.
2. Vline = 0.2 volts.
3. Guaranteed by design.
4. All lines open.
5. $V_{OUT}$ = 2.4 volts.
6. $V_{OUT}$ = 0.4 volts.
7. SE/LVD/HUD pins only.
8. MSTR/SLV = 1.
9. $I_{ds}$ = 0–5 mA.
10. $V_{dso}$ = 0.0 volts.
11. $V_{dso}$ = 2.75 volts.

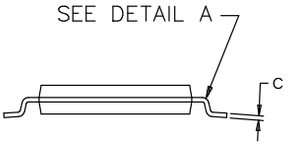
## DS2119M 28–PIN SSOP PACKAGE



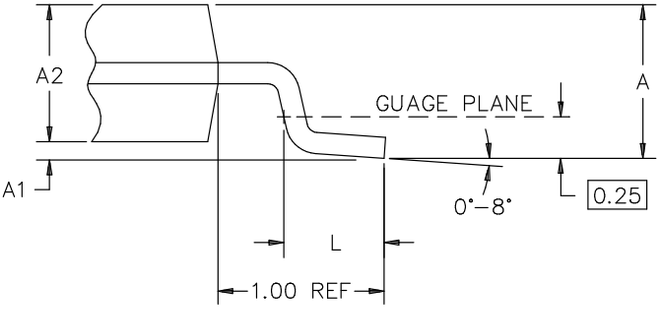

NOTES:

1. DIMENSION "D" DOES NOT INCLUDE MOLD MISSMATCH, FLASH OR PROTRUSIONS. MOLD MISSMATCH, FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.15 PER SIDE.
2. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.




| DIM | MIN | MAX |
|---|---|---|
| A | – | 1.10 |
| A1 | 0.05 | – |
| A2 | 0.75 | 1.05 |
| c | 0.09 | 0.20 |
| L | 0.50 | 0.75 |
| e1 | 0.65 BSC | |
| b | 0.18 | 0.30 |
| D | 9.60 | 9.80 |
| E1 | 4.40 BSC | |
| E | 6.20 | 6.60 |




DETAIL A