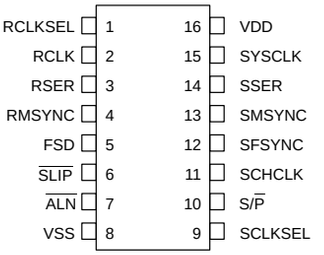
DALLAS SEMICONDUCTOR

DS2175
T1/CEPT Elastic Store

FEATURES

- Rate buffer for T1 and CEPT transmission systems
- Synchronizes loop–timed and system timed data streams on frame boundaries
- Ideal for T1 (1.544 MHz) to CEPT (2.048 MHz), CEPT to T1 interfaces
- Supports parallel and serial backplanes
- Buffer depth is 2 frames
- Comprehensive on–chip “slip” control logic
  - Slips occur only on frame boundaries
  - Outputs report slip occurrences and direction
  - Align feature allows buffer to be recentered at any time
  - Buffer depth easily monitored
- Compatible with DS2180A T1 and DS2181A CEPT Transceivers
- Industrial temperature range of –40°C to +85°C available, designated DS2175N

PIN ASSIGNMENT

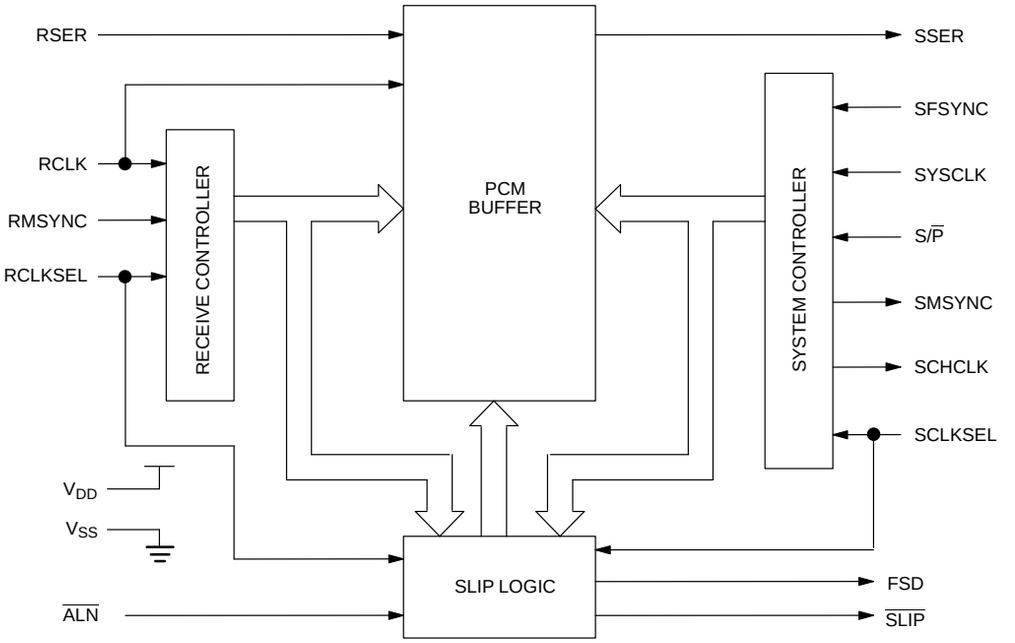


16–PIN DIP (300 MIL)
16–PIN SOIC (300 MIL)

DESCRIPTION

The DS2175 is a low–power CMOS elastic–store memory optimized for use in primary rate telecommunications transmission equipment. The device serves as a synchronizing element between async data streams and is compatible with North American (T1–1.544 MHz) and European (CEPT–2.048 MHz) rate networks. The chip has several flexible operating modes which eliminate support logic and hardware currently required to interconnect parallel or serial TDM backplanes. Application areas include digital trunks, drop and insert equipment, digital cross–connects (DACS), private network equipment and PABX–to–computer interfaces such as DMI and CPI.

DS2175 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	RCLKSEL	I	**Receive Clock Select**. Tie to V_{SS} for 1.544 MHz applications, to V_{DD} for 2.048 MHz.
2	RCLK	I	**Receive Clock**. 1.544 or 2.048 MHz data clock.
3	RSER	I	**Receive Serial Data**. Sampled on falling edge of RCLK.
4	RMSYNC	I	**Receive Multifram Sync**. Rising edge establishes receive side frame and multiframe boundaries.
5	FSD	O	**Frame Slip Direction**. State indicates direction of last slip; latched on slip occurrence.
6	$\overline{SLIP}$	O	**Frame Slip**. Active low, open collector output. Held low for 65 SYSCLK cycles when a slip occurs.
7	$\overline{ALN}$	I	**Align**. Recenters buffer on next system side frame boundary when forced low; negative edge–triggered.
8	V_{SS}	–	**Signal Ground**. 0.0 volts
9	SCLKSEL	I	**System Clock Select**. Tie to V_{SS} for 1.544 MHz applications, to V_{DD} for 2.048 MHz.
10	S/$\overline{P}$	I	**Serial/Parallel Select**. Tie to V_{SS} for parallel backplane applications, to V_{DD} for serial.
11	SCHCLK	O	**System Channel Clock**. Transitions high on channel boundaries; useful for serial to parallel conversion of channel data.
12	SFSYNC	I	**System Frame Sync**. Rising edge establishes system side frame boundaries.
13	SMSYNC	O	**System Multiframe Sync**. Slip–compensated multiframe output; used with RMSYNC to monitor depth of store real time.
14	SSER	O	**System Serial Data**. Updated on rising edge of SYSCLK.
15	SYSCLK	I	**System Clock**. 1.544 or 2.048 MHz data clock.
16	V_{DD}	–	**Positive Supply**. 5.0 volts.

PCM BUFFER

The DS2175 utilizes a 2–frame buffer to synchronize incoming PCM data to the system backplane clock. Buffer depth is mode–dependent; 2.048 MHz to 2.048 MHz applications utilize 64 bytes of buffer memory, while all other modes are supported by 48 bytes. The buffer samples data at RSER on the falling edge of RCLK. Output data appears at SSER and is updated on the rising edge of SYSCLK. The buffer depth is constantly monitored by onboard contention logic; a “slip” occurs when the buffer is completely emptied or filled. Slips automatically recenter the buffer to a one–frame depth and always occur on frame boundaries.

DATA FORMAT

Data is presented to, and output from, the elastic store in a “framed” format. A rising edge at RMSYNC and SFSYNC establishes frame boundaries for the receive and system sides. North American (T1) frames contain 24 data channels of 8 bits each and an F–bit (193 bits total). European (CEPT) frames contain 32 data channels (256 bits). The frame rate of both systems is 8 KHz. RMSYNC and SFSYNC do not require a pulse at every frame boundary; if desired, they may be pulsed once to establish frame alignment. Internal counters will then maintain the frame alignment and may be reinforced by the next rising edge at RMSYNC and/or SFSYNC.

SLIP CORRECTION CAPABILITY

The 2–frame buffer depth is adequate for T–carrier and CEPT applications where short term jitter synchronization, rather than correction of significant frequency differences, is required. The DS2175 provides an ideal balance between total delay (less than 250 microseconds at its full depth) and slip correction capability.

BUFFER RECENTERING

Many applications require that the buffer be recentered during system power–up and/or initialization. Forcing $\overline{\text{ALN}}$ low recenters the buffer on the occurrence of the next frame sync boundary. A slip will occur during this recentering if the buffer depth is adjusted. If the depth is presently optimum, no adjustment (slip) occurs.

SLIP REPORTING

$\overline{\text{SLIP}}$ is held low for 65 SYSCLK cycles when a slip occurs. $\overline{\text{SLIP}}$ is an active–low, open collector output. FSD indicates slip direction. When low (buffer empty) a frame of data was “repeated” at SSER during the previous slip. When high (buffer full), a frame of data was “deleted”. FSD is updated at every slip occurrence.

BUFFER DEPTH MONITORING

SMSYNC is a system side output pulse which indicates system side multiframe boundaries. The distance between rising edges of RMSYNC and SMSYNC indicates the current buffer depth. Impending slip conditions may be determined by monitoring RMSYNC and SMSYNC real time. SMSYNC is held high for 65 SYSCLK periods.

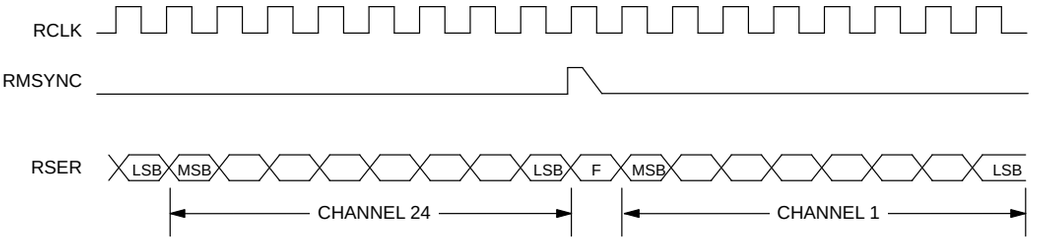
CLOCK SELECT

Receive and system side clock frequencies are independently selectable by inputs RCLKSEL and SCLKSEL. 1.544 MHz is selected when RCLKSEL (SCLKSEL) = 0; 2.048 MHz is selected when RCLKSEL (SCLKSEL) = 1. In 1.544 MHz (receive) to 1.544 MHz (system) applications, the F–bit position is passed through the receive buffer and presented at SSER immediately after the rising edge of the system side frame sync. The F–bit position is forced to 1 in 2.048 MHz to 1.544 MHz applications. No F–bit position exists in 2.048 MHz system side applications.

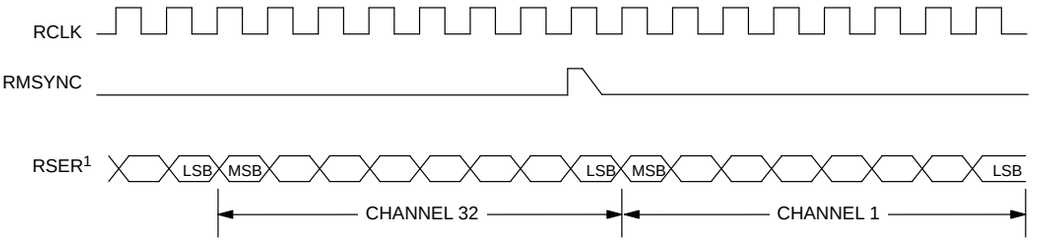
PARALLEL COMPATIBILITY

The DS2175 is compatible with parallel and serial backplanes. Channel 1 data appears at SSER after a rising edge at SFSYNC (serial applications, S/$\overline{\text{P}}$ = 1). The device utilizes a look–ahead circuit in parallel applications (S/$\overline{\text{P}}$ = 0), and presents data 8 clocks early as shown in Figures 4 and 5. Converting SSER to a parallel format requires an HC595 shift register.

RECEIVE SIDE TIMING (RCLK = 1.544 MHz) Figure 2



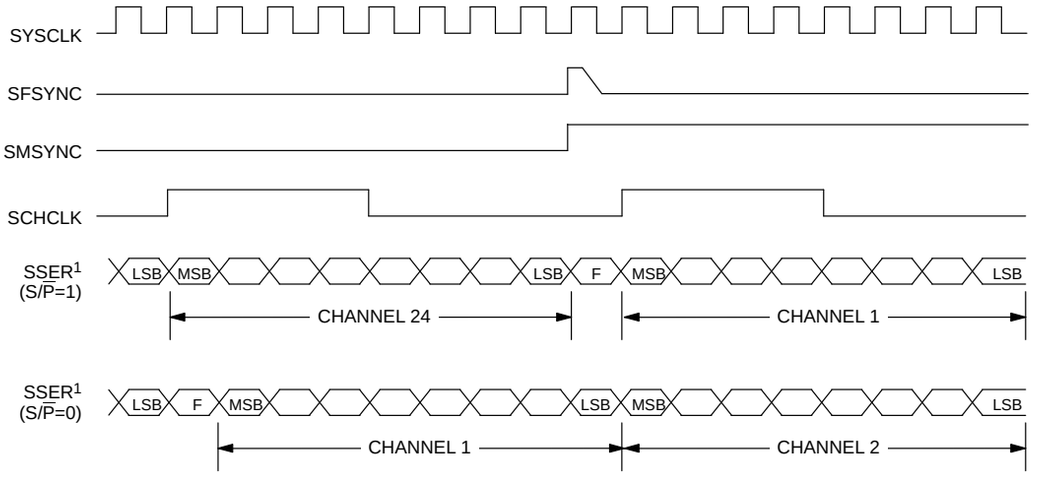
RECEIVE SIDE TIMING (RCLK = 2.048 MHz) Figure 3



NOTES:

1. All channel data is passed through the elastic store in 2.048 MHz system side applications (SCLKSEL = 1);
2. Data in channels >24 is ignored in 1.544 MHz system side applications (SCLKSEL = 0).

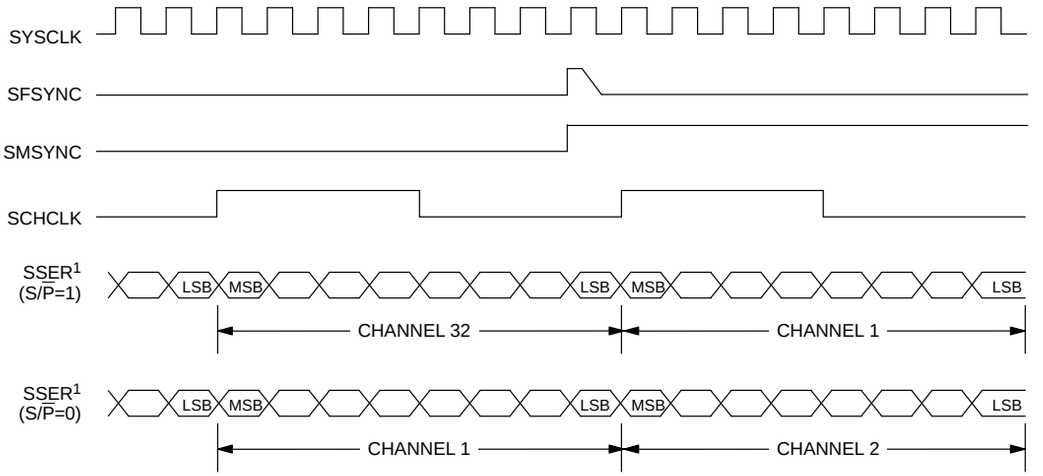
SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 1.544 MHz) Figure 4



NOTES:

1. In 1.544 MHz receive side applications (RCLKSEL=0), the F–bit position contains F–bit data extracted from the data stream at RSER. The F–bit position is forced to “1” in 2.048 MHz receive side applications (RCLKSEL=1).
2. In 2.048 MHz receive side applications (RCLKSEL=1), the E–bit position is forced to “1” and data in channels >24 is ignored.

SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 2.048 MHz) Figure 5



NOTES:

1. In 2.048 MHz receive side applications (RCLKSEL=1), all channel data is passed through the elastic store.
2. In 1.544 MHz receive side applications (RCLKSEL=0), all channel data is passed through the elastic store, except the F–bit position which is ignored. Data in channels >24 on the system side is forced to all ones.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD}+0.3	V	
Logic 0	V_{IL}	–0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		9	16	mA	1, 2
Input Leakage	I_{IL}	–1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	–1.0			mA	3
Output Current @ 0.4V	I_{OL}	+4.0			mA	4

NOTES:

1. SYSCLK = RCLK = 2.048 MHz
2. Outputs open
3. All outputs except $\overline{\text{SLIP}}$, which is open collector
4. All outputs

AC ELECTRICAL CHARACTERISTICS

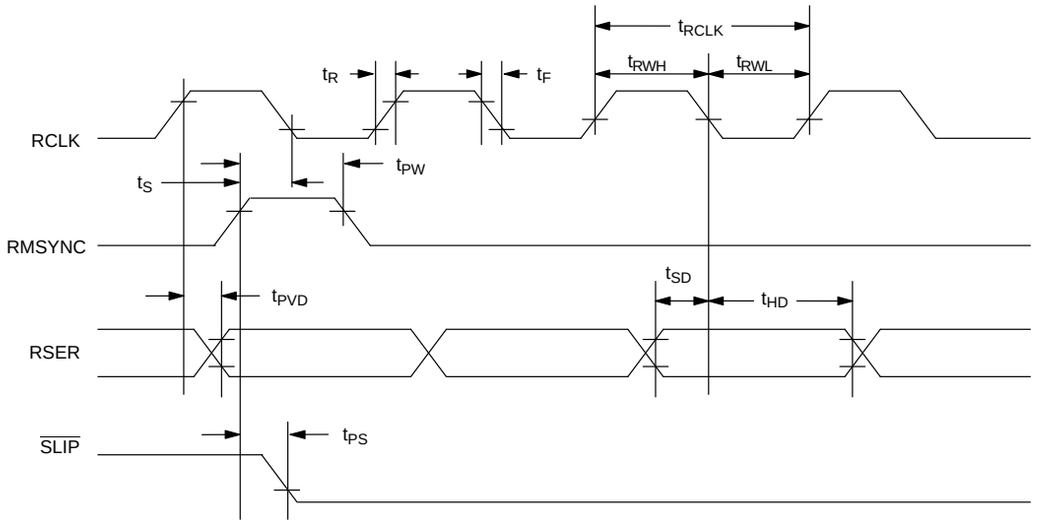
(0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{RCLK}	200			ns	
RCLK, SYSCLK Rise and Fall Times	t_R, t_F			20	ns	
RCLK Pulse Width	t_{RWH}, t_{RWL}	100			ns	
SYSCLK Pulse Width	t_{SWH}, t_{SWL}	100			ns	
SYSCLK Period	t_{SYSCLK}	200			ns	
RMSYNC Setup to RCLK Falling	t_{SC}	20		t_{RWH}–5	ns	
SFSYNC Setup to SYSCLK Falling	t_{SC}	20		t_{SWH}–5	ns	
RMSYNC, SFSYNC, $\overline{ALN}$ Pulse Width	t_{PW}	50			ns	
RSER Setup to RCLK Falling	t_{SD}	50			ns	
RSER Hold from RCLK Falling	t_{HD}	50			ns	
Propagation Delay SYSCLK to SSER	t_{PVD}			75	ns	
Propagation Delay SYSCLK to SMSYNC High	t_{PSS}			75	ns	
Propagation Delay SYSCLK or RCLK to $\overline{SLIP}$ Low, FSD Low/ High	t_{PS}			100	ns	
$\overline{ALN}$ Setup to SFSYNC Rising	t_{SR}	500			ns	

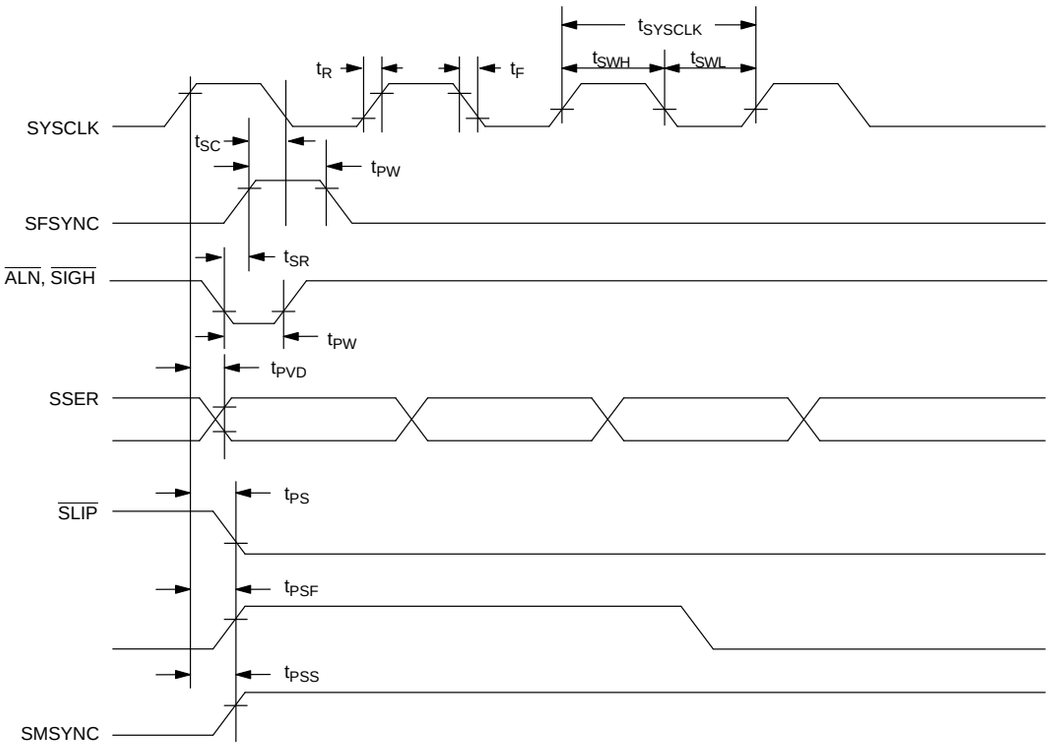
NOTES:

1. Measured at V_{IH}=2.0V, V_{IL}–0.8V, and 10 ns maximum rise and fall times.
2. Output load capacitance = 100 pF.

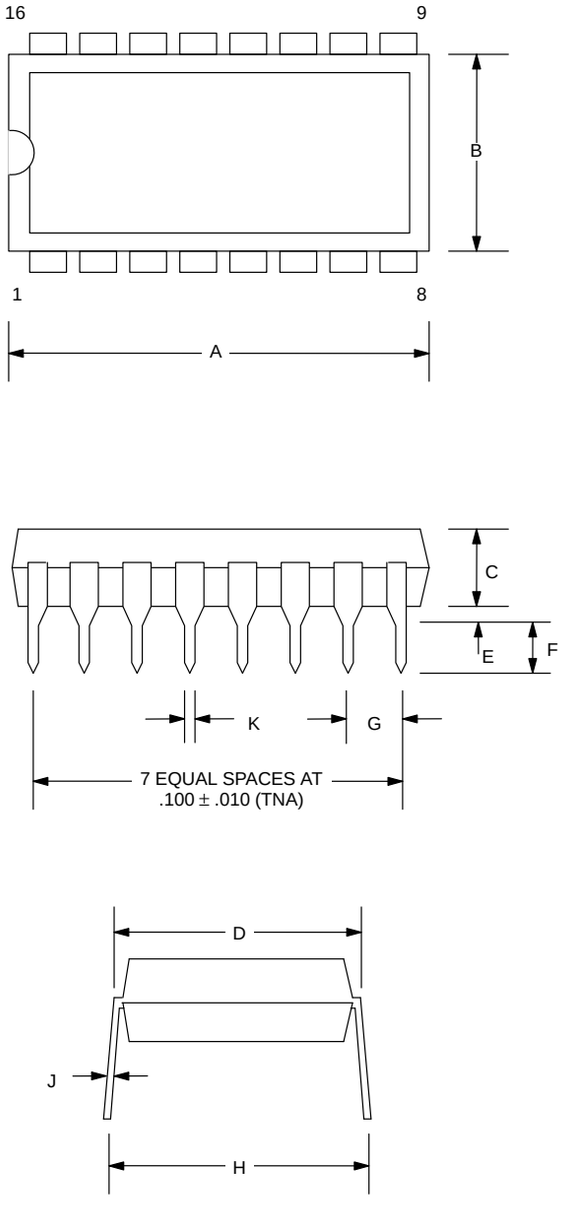
RECEIVE AC TIMING DIAGRAM Figure 6



SYSTEM AC TIMING DIAGRAM Figure 7

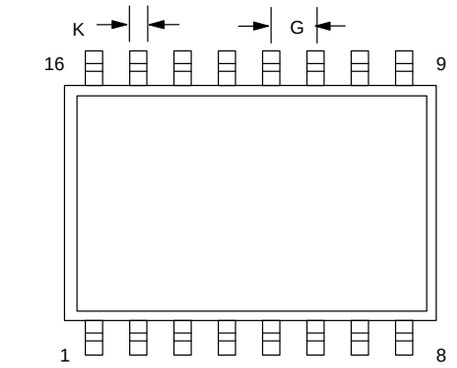


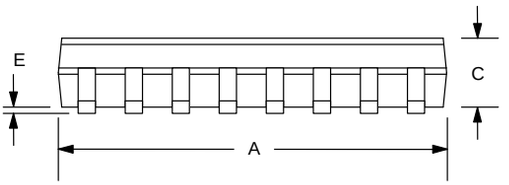
DS2175 T1/CEPT ELASTIC STORE

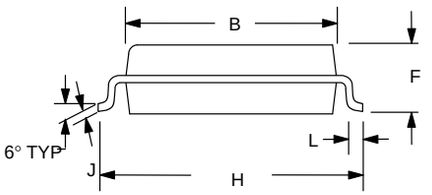


PKG	16–PIN	
DIM	MIN	MAX
A IN.	0.740	0.780
B IN.	0.240	0.260
C IN.	0.120	0.140
D IN.	0.300	0.325
E IN.	0.015	0.040
F IN.	0.120	0.140
G IN.	0.090	0.110
H IN	0.290	0.420
J IN.	0.008	0.012
K IN.	0.015	0.021

DS2175S T1/CEPT ELASTIC STORE







PKG	16–PIN	
DIM	MIN	MAX
A IN.	0.402	0.412
B IN.	0.290	0.300
C IN.	0.089	0.095
E IN.	0.004	0.012
F IN.	0.094	0.105
G IN.	0.050 BSC	
H IN	0.398	0.416
J IN.	0.009	0.013
K IN.	0.013	0.019
L IN.	0.016	0.040

DATA SHEET REVISION SUMMARY

The following represent the key differences between 04/19/95 and 06/13/97 version of the DS2175 data sheet. Please review this summary carefully.

1. SYNC/CLOCK Relationship in timing diagram