DALLAS SEMICONDUCTOR

DS2430A
256–Bit 1–Wire™ EEPROM

FEATURES

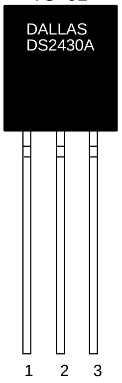
- 256–bit Electrically Erasable Programmable Read Only Memory (EEPROM) plus 64–bit one–time programmable application register
- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute identity because no two parts are alike
- Built–in multidrop controller ensures compatibility with other MicroLAN™ products
- EEPROM organized as one page of 32 bytes for random access
- Reduces control, address, data and power to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3k bits per second
- 8–bit family code specifies DS2430A communication requirements to reader
- Presence detector acknowledges when reader first applies voltage
- Low cost TO–92 or 6–pin TSOC surface mount package
- Reads and writes over a wide voltage range of 2.8V to 6.0V from –40°C to +85°C

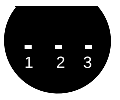
ORDERING INFORMATION

DS2430A	TO–92 package
DS2430AP	6–pin TSOC package
DS2430AT	Tape & Reel version of DS2430A
DS2430AV	Tape & Reel version of DS2430AP

PIN ASSIGNMENT

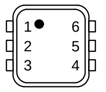
TO–92



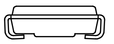


BOTTOM VIEW
See Mech. Drawings Section

TSOC PACKAGE



TOP VIEW
3.7 X 4.0 X 1.5 mm



SIDE VIEW
See Mech. Drawings Section

PIN DESCRIPTION

	TO–92	TSOC
Pin 1	Ground	Ground
Pin 2	Data	Data
Pin 3	NC	NC
Pin 4	——	NC
Pin 5	——	NC
Pin 6	——	NC

SILICON LABEL DESCRIPTION

The DS2430A 256–bit 1–Wire EEPROM identifies and stores relevant information about the product to which it is associated. This lot or product specific information can be accessed with minimal interface, for example a single port pin of a microcontroller. The DS2430A consists of a factory–lasered registration number that includes a unique 48–bit serial number, an 8–bit CRC, and an 8–bit Family Code (14h) plus 256 bits of user–programmable EEPROM and a 64–bit one–time programmable application register. The power to read and write the DS2430A is derived entirely from the 1–Wire communication line. Data is transferred serially via the

1–Wire protocol which requires only a single data lead and a ground return. The 48–bit serial number that is factory–lasered into each DS2430A provides a guaranteed unique identity which allows for absolute traceability. The TO–92 and TSOC packages provide a compact enclosure that allows standard assembly equipment to handle the device easily for attachment to printed circuit boards or wiring. Typical applications include storage of calibration constants, board identification and product revision status.

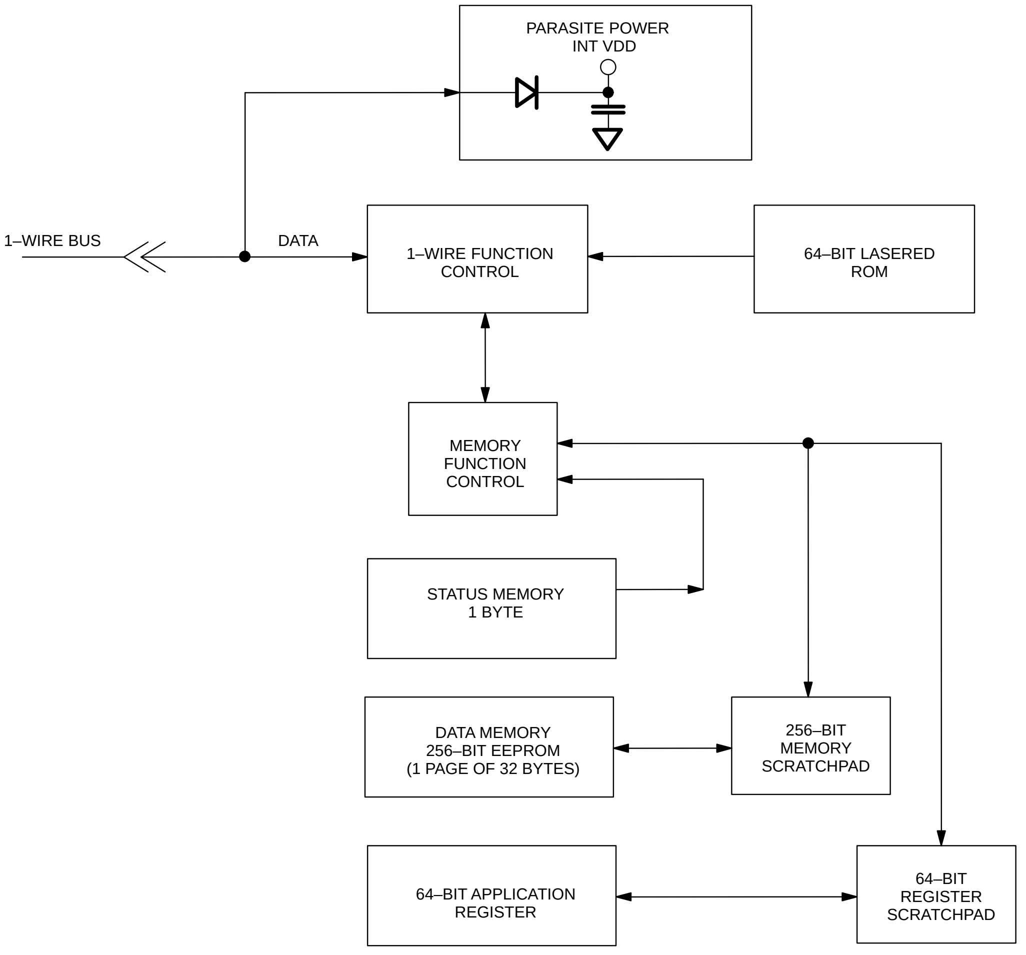
OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2430A. The DS2430A has four main data components: 1) 64–bit lasered ROM, 2) 256–bit EEPROM data memory with scratchpad, 3) 64–bit one–time programmable application register with scratchpad and 4) 8–bit Status Memory. The hierarchical structure of the 1–Wire protocol is shown in Figure 2. The bus master must first provide one of the four ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM. The protocol required for these ROM Function Commands is described in Figure 8. After a ROM Function Command is successfully executed, the memory functions become accessible and the master may provide any one of the four memory function commands. The protocol for these memory function commands is described in Figure 6. All data is read and written least significant bit first.

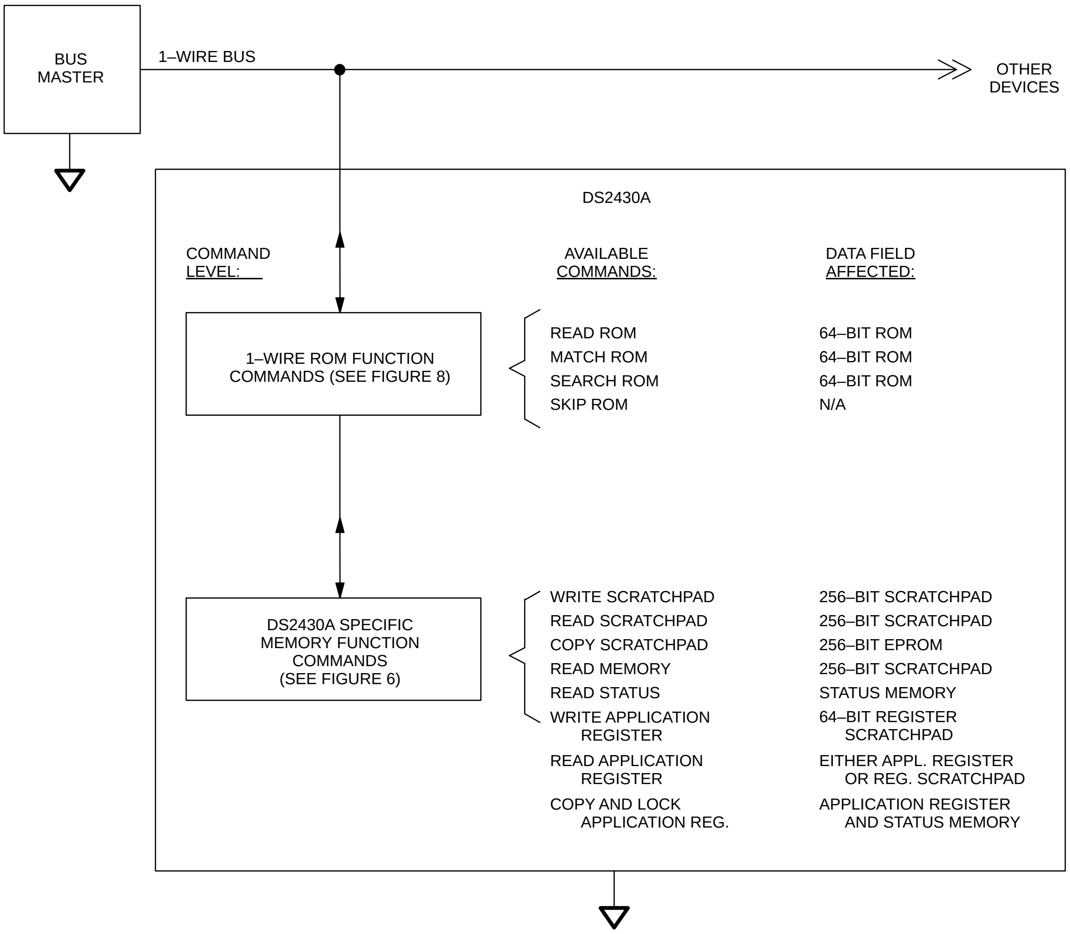
64–BIT LASERED ROM

Each DS2430A contains a unique ROM code that is 64 bits long. The first eight bits are a 1–Wire family code (14h). The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (Figure 3). The 1–Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1–Wire Cyclic Redundancy Check is available in the Book of DS19xx iButton Standards. The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

DS2430A BLOCK DIAGRAM Figure 1



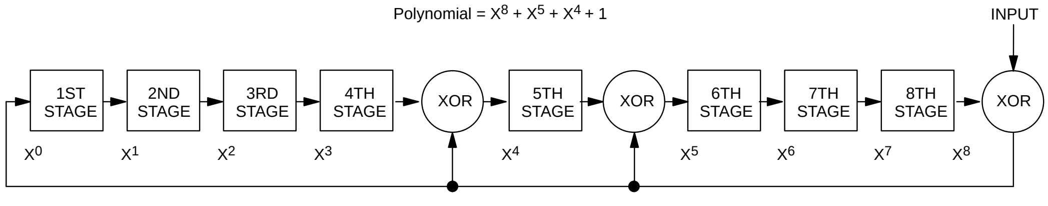
HIERARCHICAL STRUCTURE FOR 1–WIRE PROTOCOL Figure 2



64–BIT LASERED ROM Figure 3

8–Bit CRC Code	48–Bit Serial Number	8–Bit Family Code (14H)
MSB LSB	MSB LSB	MSB LSB

1–WIRE CRC GENERATOR Figure 4

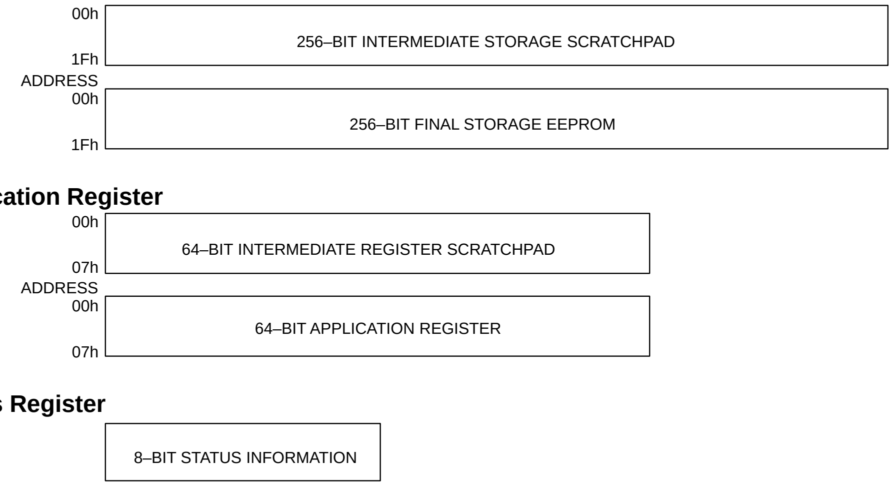


MEMORY

The memory of the DS2430A consists of three separate sections, called data memory, application register and status register (Figure 5). The data memory and the application register each has its own intermediate storage area called scratchpad that acts as a buffer when writing to the device. The data memory can be read and written as often as desired. The application register, however, is one–time programmable only. Once the application register is programmed, it is automatically write–protected. The status register will indicate if the application register is already locked or if it is still available for storing data. As long as the application register is unprogrammed, the status register will read FFh. Copying data from the register scratchpad to the application register will clear the two least significant bits of the status register, yielding a FCh the next time when one reads the status register.

DS2430A MEMORY MAP Figure 5

Data Memory



MEMORY FUNCTION COMMANDS

The “Memory Function Flow Chart” (Figure 6) describes the protocols necessary for accessing the different memory sections of the DS2430A. An example is shown later in this document.

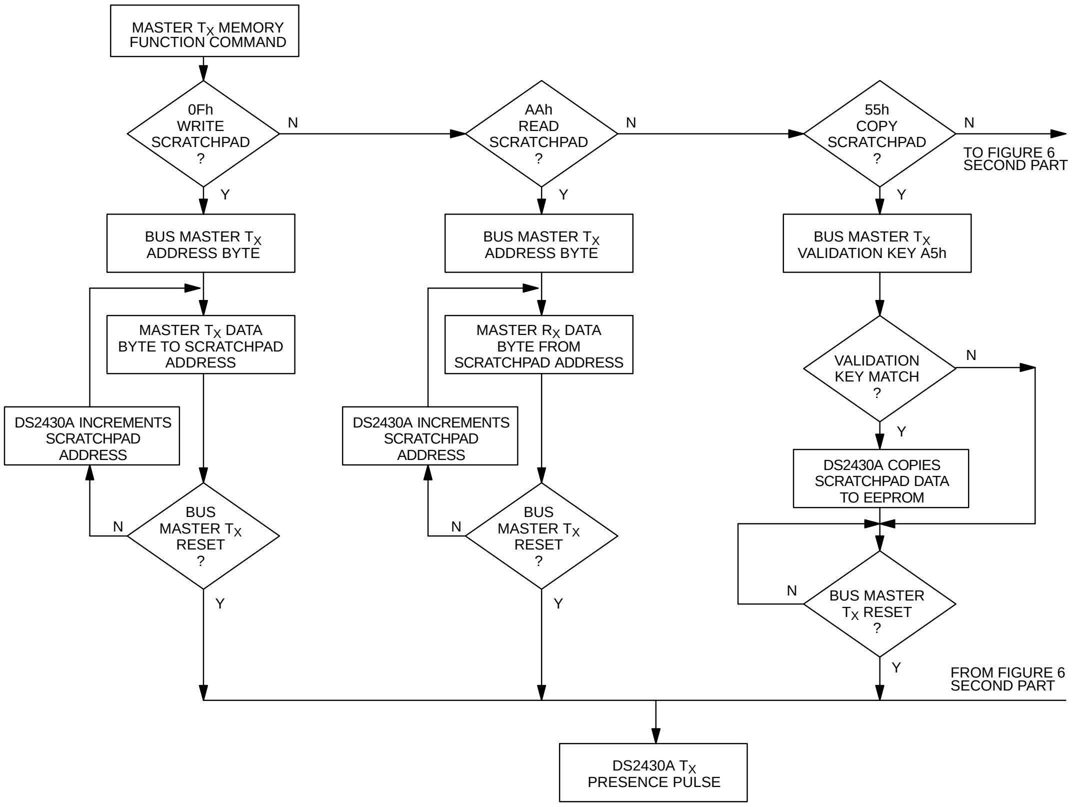
WRITE SCRATCHPAD [0Fh]

After issuing the write scratchpad command, the master must first provide a 1–byte address, followed by the data to be written to the scratchpad for the data memory. The DS2430A will automatically increment the address after every byte it received. After having received a data byte for address 1Fh, the address counter will wrap around to 00h for the next byte and writing continues until the master sends a reset pulse.

READ SCRATCHPAD [AAh]

This command is used to verify data previously written to the scratchpad before it is copied into the final storage EEPROM memory. After issuing the read scratchpad command, the master must provide the 1–byte starting address from where data is to be read. The DS2430A will automatically increment the address after every byte read by the master. After the data of address 1Fh has been read, the address counter will wrap around to 00h for the next byte and reading continues until the master sends a reset pulse.

MEMORY FUNCTION FLOW CHART Figure 6



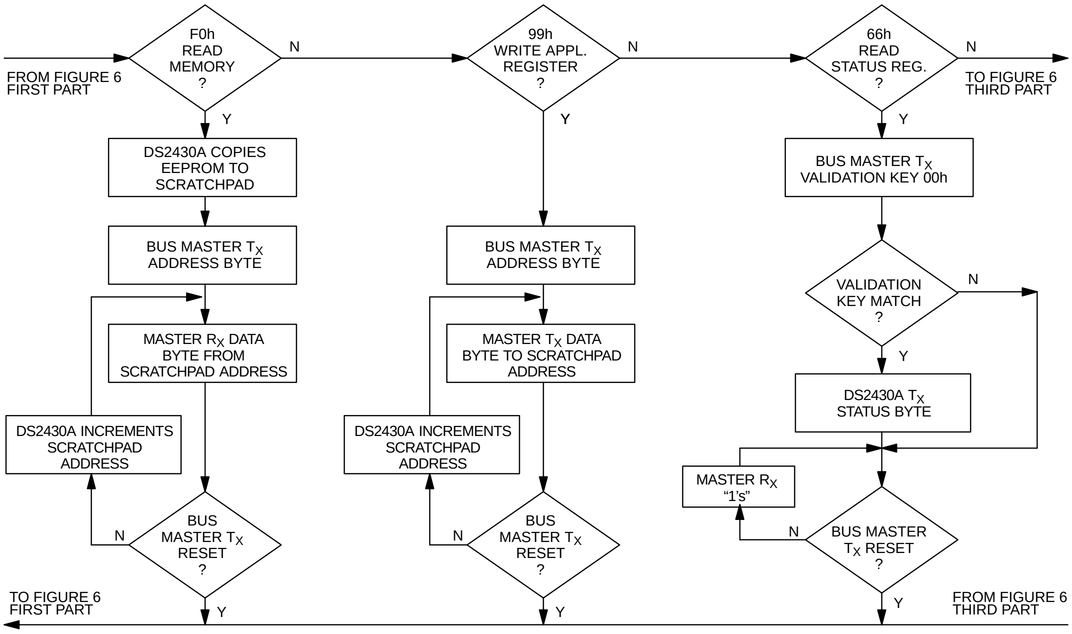
COPY SCRATCHPAD [55h]

After the data stored in the scratchpad has been verified the master may send the copy scratchpad command followed by a validation key of A5h to transfer data from the scratchpad to the EEPROM memory. This command will always copy the data of the entire scratchpad. Therefore, if one desires to change only a few bytes of the EEPROM data, the scratchpad should contain a copy of the latest EEPROM data before the write scratchpad and copy scratchpad commands are issued. After this command is issued, the data line must be held at logic high level for at least 100 ms.

READ MEMORY [F0h]

The read memory command is used to read a portion or all of the EEPROM data memory and to copy the entire data memory into the scratchpad to prepare for changing a few bytes. To copy data from the data memory to the scratchpad and to read it, the master must issue the read memory command followed by the 1–byte starting address from where data is to be read from the scratchpad. The DS2430A will automatically increment the address after every byte read by the master. After the data of address 1Fh has been read, the address counter will wrap around to 00h for the next byte and reading continues until the master sends a reset pulse. If one intends to copy the entire data memory to the scratchpad without reading data, a starting address is not required; the master may send a reset pulse immediately following the command code.

MEMORY FUNCTION FLOW CHART Figure 6 (cont'd)



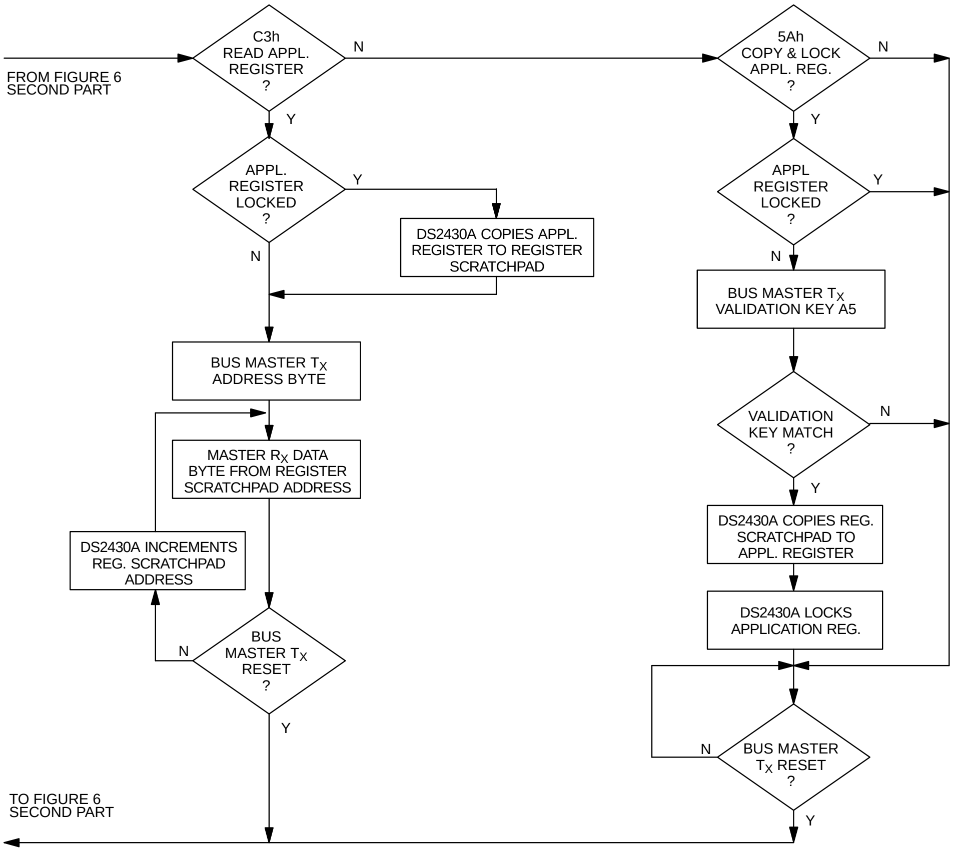
WRITE APPLICATION REGISTER [99h]

This command is essentially the same as the write scratchpad command, but it addresses the 64–bit register scratchpad. After issuing the command code, the master must provide a 1–byte address, followed by the data to be written. The DS2430A will automatically increment the address after every byte it received. After having received a data byte for address 07h, the address counter will wrap around to 00h for the next byte and writing continues until the master sends a reset pulse. The write application register command can be used as long as the application register has not yet been locked. If issued for a device with the application register locked, the data written to the register scratchpad will be lost.

READ STATUS REGISTER [66h]

The status register is a means for the master to find out if the application register has been programmed and locked. After issuing the read status register command, the master must provide the validation key 00h before receiving status information. The two least significant bits of the 8–bit status register will be 0 if the application register was programmed and locked; all other bits will always read 1. The master may finish the read status command by sending a reset pulse at any time.

MEMORY FUNCTION FLOW CHART Figure 6 (cont'd)



READ APPLICATION REGISTER [C3h]

This command is used to read the application register or the register scratchpad. As long as the application register is not yet locked, one will receive data from the register scratchpad. After the application register is locked the DS2430A will transmit data from the application register, making the register scratchpad inaccessible for reading. The contents of the status register indicates where the data received with this command came from. After issuing the read application register command, the master must provide the 1–byte starting address from where data is to be read. The DS2430A will automatically increment the address after every byte read by the master. After the data of address 07h has been read, the address counter will wrap around to 00h for the next byte and reading continues until the master sends a reset pulse.

COPY & LOCK APPLICATION REGISTER [5Ah]

After the data stored in the register scratchpad has been verified the master may send the copy & lock application register command followed by a validation key of A5h to transfer the contents of the entire register scratchpad to the application register and to simultaneously write–protect it. The master may cancel this command by sending a reset pulse instead of the validation key. After the validation key was transmitted, the application register will contain the data of the register scratchpad. Further write accesses to the application register will be denied. **The copy & lock application register command can only be executed once.**

1–WIRE BUS SYSTEM

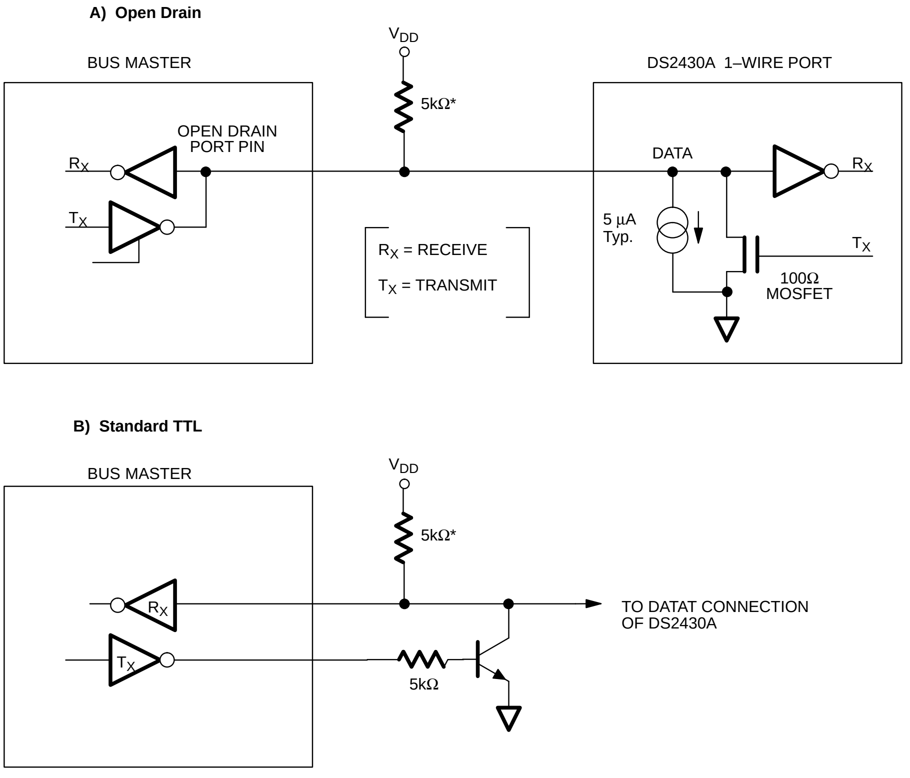
The 1–Wire bus is a system which has a single bus master and one or more slaves. In all instances, the DS2430A is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signaling (signal type and timing). A 1–Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx iButton Standards.

Hardware Configuration

The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have open drain connection or 3–state outputs. The 1–Wire port of the DS2430A is open drain with an internal circuit equivalent to that shown in Figure 7. A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus has a maximum data rate of 16.3k bits per second and requires a pull–up resistor of approximately 5kΩ.

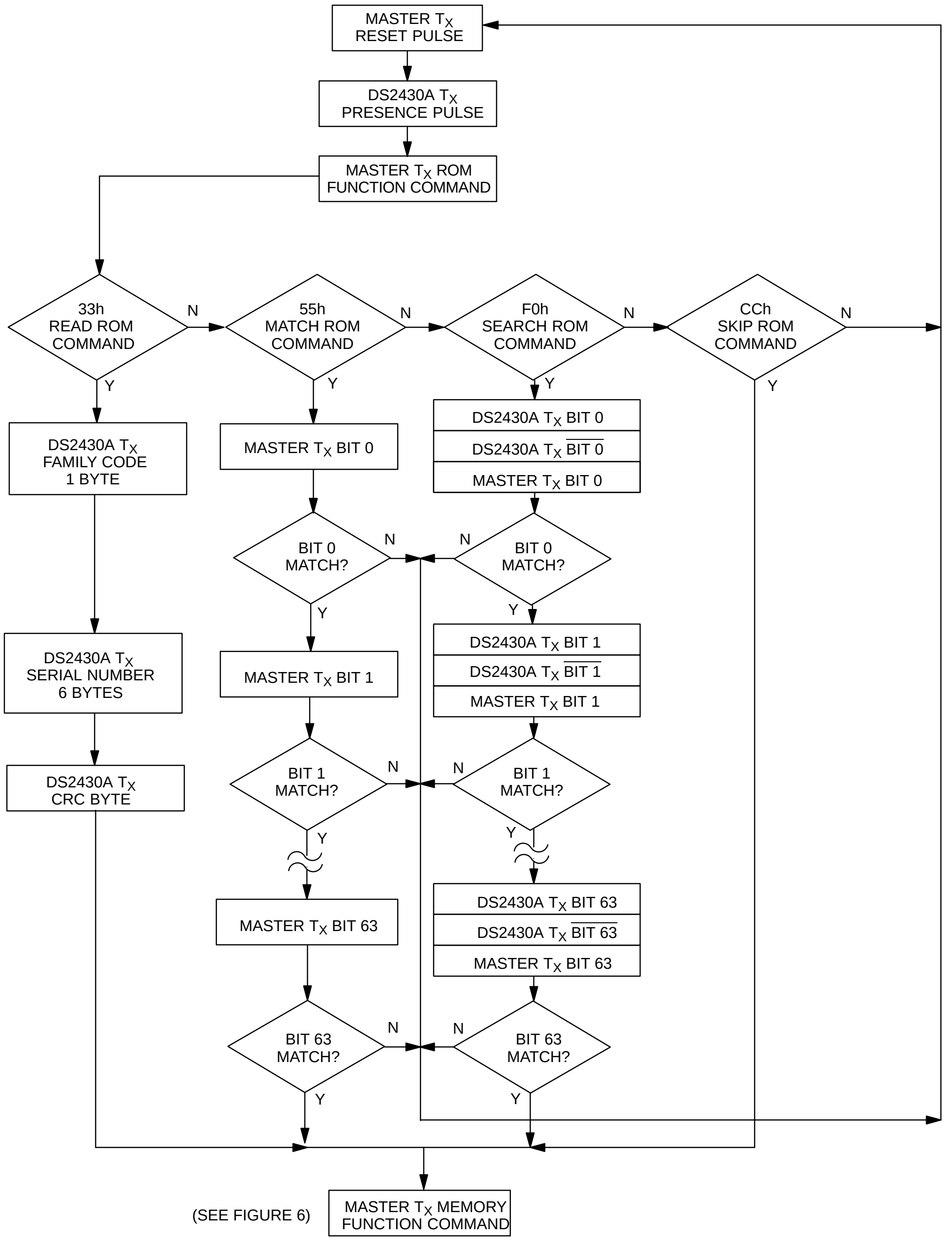
The idle state for the 1–Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 µs, one or more of the devices on the bus may be reset.

HARDWARE CONFIGURATION Figure 7



*5kΩ is adequate for reading the DS2430A. To write to a single device, a 2.2kΩ resistor and V_{DD} of at least 2.8V is sufficient. For writing multiple DS2430As simultaneously, the resistor should be bypassed by a low–impedance pullup to V_{DD} while the device copies the scratchpad to EEPROM.

ROM FUNCTIONS FLOW CHART Figure 8



Transaction Sequence

The sequence for accessing the DS2430A via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2430A is on the bus and is ready to operate. For more details, see the "1–Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 8):

Read ROM [33h]

This command allows the bus master to read the DS2430A's 8–bit family code, unique 48–bit serial number, and 8–bit CRC. This command can be used only if there is a single DS2430A on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired–AND result). The resultant family code and 48–bit serial number will usually result in a mis–match of the CRC.

Match ROM [55h]

The match ROM command, followed by a 64–bit ROM sequence, allows the bus master to address a specific DS2430A on a multidrop bus. Only the DS2430A that exactly matches the 64–bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64–bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64–bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull–downs will produce a wired–AND result).

Search ROM [F0h]

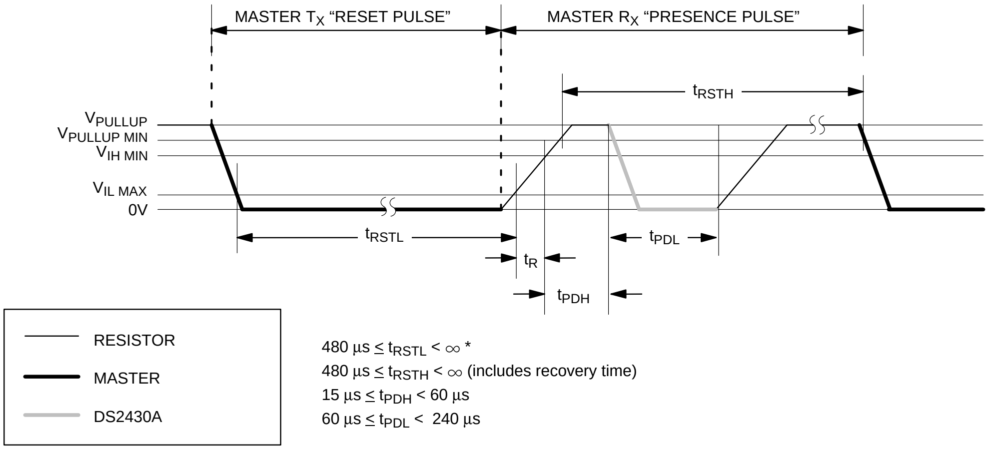
When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3–step routine on each bit of the ROM.

After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx iButton Standards for a comprehensive discussion of a search ROM, including an actual example.

1–Wire Signaling

The DS2430A requires strict protocols to insure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1 and Read Data. All these signals except presence pulse are initiated by the bus master. The initialization sequence required to begin any communication with the DS2430A is shown in Figure 9. A reset pulse followed by a presence pulse indicates the DS2430A is ready to accept a ROM command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs). The bus master then releases the line and goes into receive mode (RX). The 1–Wire bus is pulled to a high state via the pull–up resistor. After detecting the rising edge on the data pin, the DS2430A waits (t_{PDH}, 15–60 µs) and then transmits the presence pulse (t_{PDL}, 60–240 µs).

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 9



480 µs ≤ t_{RSTL} < ∞ *
480 µs ≤ t_{RSTH} < ∞ (includes recovery time)
15 µs ≤ t_{PDH} < 60 µs
60 µs ≤ t_{PDL} < 240 µs

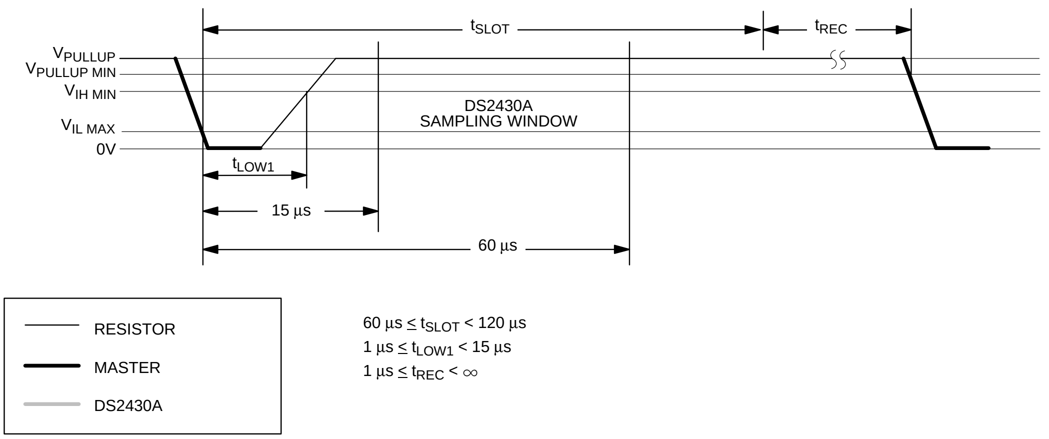
* In order not to mask interrupt signalling by other devices on the 1–Wire bus, t_{RSTL} + t_R should always be less than 960 µs.

Read/Write Time Slots

The definitions of write and read time slots are illustrated in Figure 10. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2430A to the master by triggering a delay circuit in the DS2430A. During write time slots, the delay circuit determines when the DS2430A will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2430A will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the DS2430A will leave the read data time slot unchanged.

READ/WRITE TIMING DIAGRAM Figure 10

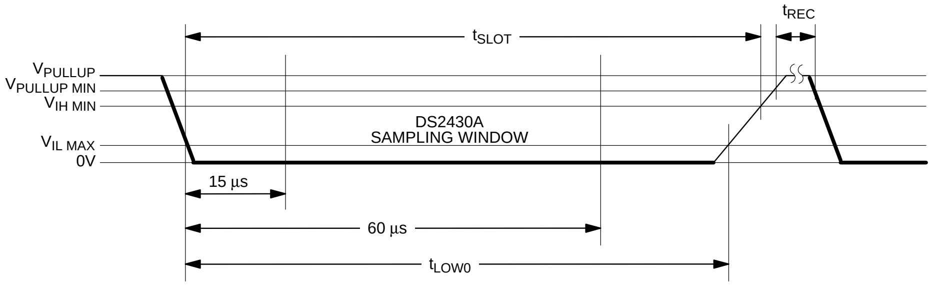
Write–one Time Slot



60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOW1} < 15 µs
1 µs ≤ t_{REC} < ∞

READ/WRITE TIMING DIAGRAM NO TAG (cont'd)

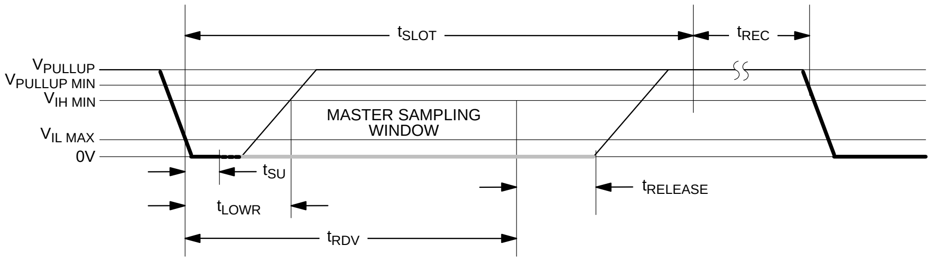
Write–zero Time Slot



$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

Read–data Time Slot



— (thin line)	RESISTOR
— (thick line)	MASTER
— (gray line)	DS2430A

$60\ \mu s \le t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{LOWR} < 15\ \mu s$

$0 \le t_{RELEASE} < 45\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

$t_{RDV} = 15\ \mu s$

$t_{SU} < 1\ \mu s$

MEMORY FUNCTION EXAMPLE

Example: Write two data bytes to data memory location 0006 and 0007. Read entire data memory.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 μs)
RX	Presence	Presence pulse
TX	CCh	Issue “Skip ROM” command
TX	F0h	Issue “Read Memory” command
TX	Reset	Reset pulse (480–960 μs)
RX	Presence	Presence pulse
TX	CCh	Issue “Skip ROM” command
TX	0Fh	Issue “Write Scratchpad” command
TX	06h	Start address = 06h
TX	<2 data bytes>	Write two bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “Skip ROM” command
TX	AAh	Issue “Read Scratchpad” command
TX	06h	Start address = 06h
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “Skip ROM” command
TX	55h	Issue “Copy Scratchpad” command
TX	A5h	Validation key
TX	<data line high>	Data line is held high for 100 ms by the bus master to provide energy for copying data from the scratchpad to EEPROM
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “Skip ROM” command
TX	F0h	Issue “Read Memory” command
TX	00h	Start address = 00h
RX	<32 bytes>	Read EEPROM data page
TX	Reset	Reset pulse
RX	Presence	Presence pulse

ABSOLUTE MAXIMUM RATINGS*

Voltage on DATA to Ground	–0.5V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{PUP}=2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2			V	1, 6
Logic 0	V_{IL}	–0.3		+0.8	V	1, 11
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current (DATA pin)	I_L		5		µA	3
Operating Charge	Q_{OP}			30	nC	7, 8
Programming Current	I_P			600	µA	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance DATA pin	C_D			800	pF	9

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{PUP}=2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Low Time	t_{LOWR}	1		15	µs	
Read Data Valid	t_{RDV}		exactly 15		µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480		5000	µs	10
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	
Programming Time	t_{PROG}			100	ms	

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP}=external pull–up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1–wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum (15 µs total from falling edge on 1–wire bus).
6. V_{IH} is a function of the external pull–up resistor and V_{PUP}.
7. 30 nanocoulombs per 72 time slots @ 5.0V.
8. At V_{CC}=5.0V with 5kΩ pullup to V_{CC} and a maximum time slot of 120 µs.
9. Capacitance on the data pin could be 800 pF when power is first applied. If a 5kΩ resistor is used to pull up the data line to V_{CC}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.
10. t_{RSTL} should be limited to maximum 5 ms. Otherwise the DS2430A may perform a power–on reset.
11. Under certain low voltage conditions V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a presence pulse.