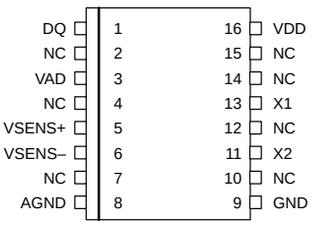
DALLAS SEMICONDUCTOR

DS2437
Smart Battery Monitor

FEATURES

- Unique 1–Wire™ interface requires only one port pin for communication
- Provides unique 64–bit serial number to battery packs
- Eliminates thermistors by sensing battery temperature on–chip
- On–board A/D converter allows monitoring of battery voltage for end–of–charge and end–of–discharge determination
- On–board integrated current accumulator facilitates gas gauging
- Real–time clock in binary format
- 40–byte nonvolatile user memory available for storage of user data such as gas gauge and manufacturing information
- Operating range –40°C to +85°C
- Applications include portable computers, portable/ cellular phones, consumer electronics, and handheld instrumentation

PIN ASSIGNMENT



16–PIN SSOP
See Mech. Drawings Section

PIN DESCRIPTION

DQ	–	Data In/Out
VAD	–	General A/D input
VSENS+	–	Battery current monitor input (+)
VSENS–	–	Battery current monitor input (–)
NC	–	No connect
GND	–	Digital Ground
AGND	–	Analog Ground
X2	–	Connection for 32.768 KHz XTAL
X1	–	Connection for 32.768 KHz XTAL
VDD	–	Power Supply (2.7V to 10.0V)

DESCRIPTION

The DS2437 Smart Battery Monitor provides several functions that are desirable to carry in a battery pack: a means of tagging a battery pack with a unique serial number, a direct–to–digital temperature sensor which eliminates the need for thermistors in the battery pack, an A/D converter which measures the battery voltage and current, an integrated current accumulator, which keeps a running total of all current going into and out of the battery, a real–time clock, and 40 bytes of nonvolatile EEPROM memory for storage of important parameters such as battery capacity, capacity remaining, and indication of battery cycling.

Information is sent to/from the DS2437 over a 1–Wire interface, so that only one wire (and ground) needs to be connected from a central microprocessor to a DS2437. This means that battery packs need only have three output connectors: battery power, ground, and the 1–Wire interface.

Because each DS2437 contains a unique silicon serial number, multiple DS2437s can exist on the same 1–Wire bus. This allows multiple battery packs to be charged or used in the system simultaneously.

Applications for the smart battery pack monitor include portable computers, portable/cellular telephones, and handheld instrumentation battery packs in which it is critical to monitor real–time battery performance. Used in conjunction with a microcontroller in the battery pack or host system, the DS2437 provides a complete smart battery pack solution that is fully chemistry–independent. The customization for a particular battery chemistry and capacity is realized in the code programmed into the microcontroller and DS2437 EEPROM, and only a software revision is necessary should a designer wish to change battery pack chemistry.

DETAILED PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	DQ	**Data Input/Out:** for 1–Wire operation: Open drain
3	VAD	**ADC Input:** input for general purpose A/D
5	VSENS+	**Battery Input:** connection for battery current to be monitored (see text)
6	VSENS–	**Battery Input:** connection for battery current to be monitored (see text)
8	AGND	**Analog Ground:** must be at the same potential as GND
9	GND	**Digital Ground:** must be at the same potential as AGND
11	X2	**Crystal Input:** connection for 32.768 KHz for RTC operation
13	X1	**Crystal Input:** connection for 32.768 KHz for RTC operation
16	V_{DD}	**V_{DD} Pin:** input supply voltage
2, 4, 7, 10, 12, 14, 15	NC	**No Connect**

OVERVIEW

The block diagram of Figure 1 shows the seven major components of the DS2437:

1. 64–bit lasered ROM
2. temperature sensor
3. battery voltage A/D
4. battery current A/D
5. current accumulators
6. real–time clock
7. 40–byte nonvolatile user–memory

Each DS2437 contains a unique 64–bit lasered ROM serial number so that several battery packs can be charged/monitored by the same host system. Furthermore, other Dallas products featuring the same 1–Wire bus architecture with a 64–bit ROM can reside on the same bus; refer to the Dallas Automatic Identification Data book for the specifications of these products.

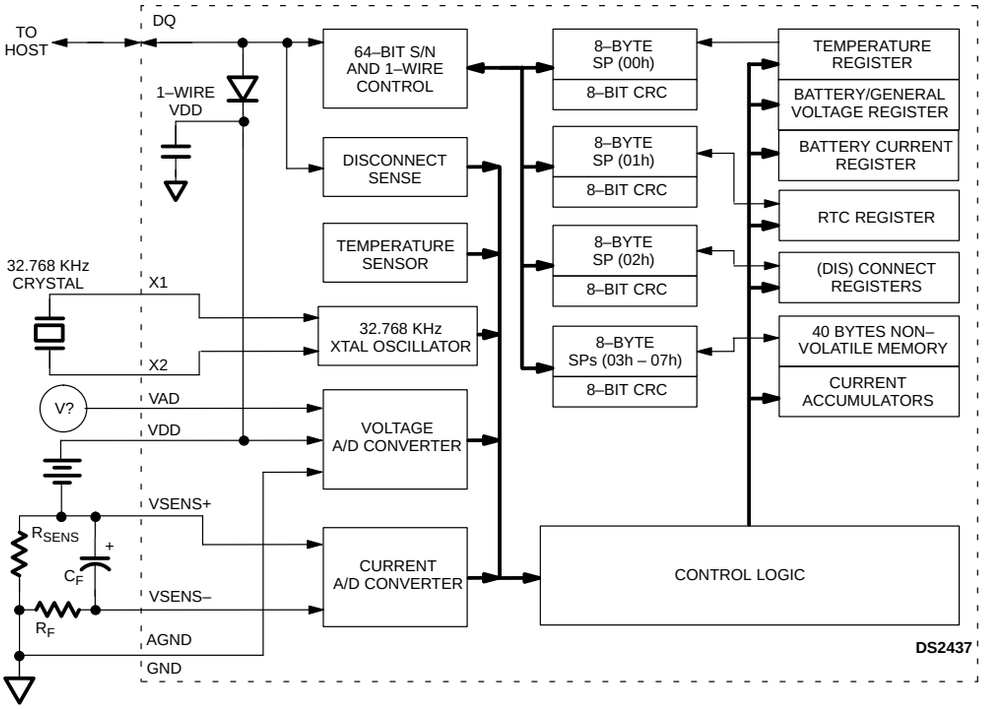
Communication to the DS2437 is via a 1–Wire port. With the 1–Wire port, the memory and control functions will not be available until the ROM function protocol has been established. The master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, or 4) Skip ROM. These commands operate on the 64–bit lasered ROM portion of each device and can singulate a specific device if many are present on the 1–Wire line as well as to indicate to the bus master how many and what types of devices are present. After a ROM function sequence has been successfully executed, the memory and control functions are accessible and the master may then provide any one of the six memory and control function commands.

Control function commands may be issued which instruct the DS2437 to perform a temperature measurement or battery voltage A/D conversion. The result of these measurements will be placed in the DS2437's memory map, and may be read by issuing a memory function command which reads the contents of the temperature and voltage registers. Additionally, the charging/discharging battery current is measured without user intervention, and again, the last completed result is stored in DS2437 memory space. The DS2437 uses these current measurements to update three current accumulators; one stores net charge for gas gauge calculations, the second accumulates the total charging current over the life of the battery, and the remaining accumulator tallies battery discharge current. The real time clock data, which can be used in calculating battery self–discharge or time–related charge termination limits, also resides in the DS2437 memory map and can be extracted with a control function command. The nonvolatile user memory of the DS2437 consists of forty bytes of EEPROM. These locations may be used to store any data the user wishes, and are written to using a memory function command. All data and commands are read and written least significant bit first.

PARASITE POWER

The block diagram (Figure 1) shows the parasite–powered circuitry. This circuitry "steals" power whenever the DQ pin is high. DQ will provide sufficient power as long as the specified timing and voltage requirements are met (see the section titled "1–Wire Bus System"). The advantage of parasite power is that the ROM may be read in absence of normal power, i.e., if the battery pack is completely discharged.

DS2437 BLOCK DIAGRAM Figure 1



OPERATION–MEASURING TEMPERATURE

The DS2437 measures temperatures through the use of an on–board proprietary temperature measurement technique.

The temperature reading is provided in a 13–bit, two's complement reading, which provides 0.03125°C of resolution. Table 1 describes the exact relationship of output data to measured temperature. The data is transmitted serially over the 1–Wire interface. The DS2437 can measure temperature over the range of –55°C to +125°C in 0.03125°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

Note that temperature is represented in the DS2437 in terms of a 0.03125°C LSb, yielding the following 13–bit format. The three least significant bits of the temperature register will always be zero. The remaining 13 bits contain the two's complement representation of the temperature in °C, with the MSb holding the sign (S) bit. See "Memory Map" section for the TEMPERATURE REGISTER address location.

Temperature/Data Relationships Table 1

2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	0 (set)	0 (set)	0 (set)	LSB
MSb				(unit = °C)			LSb	
S	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	MSB

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	01111101 00000000	7B00h
+25.0625°C	00011001 00010000	1910h
+1/2°C	00000000 10000000	0080h
0°C	00000000 00000000	0070
–1/2°C	11111111 10000000	FF80h
–25.0625°C	11100110 11110000	E6F0h
–55°C	11001001 00000000	C900h

OPERATION–MEASURING BATTERY VOLTAGE

The on–board analog–to–digital converter (ADC) has ten bits of resolution, and will perform a conversion when the DS2437 receives a command protocol (Convert V) instructing it to do so. The result of this measurement is placed in the two–byte VOLTAGE REGISTER. The range for the DS2437 ADC is 0V to 10V; this range is suitable for NiCd or NiMH battery packs up to six cells, and for lithium ion battery packs of two cells. The full–scale range of the ADC is scaled to 10.23V, resulting in a resolution of 10 mV.

While the ADC has a range that extends to 0V, it is important to note that the battery voltage can also be the supply voltage to the DS2437. As such, the accuracy of the ADC begins to degrade below battery voltages of 2.7V, and the ability to make conversions is limited by the operating voltage range of the DS2437.

Voltage is expressed in this register in scaled binary format, as outlined in Table 2. Note that while codes exist for values below 2.7V, accuracy of the ADC and the limitation on the DS2437's supply voltage make it unlikely that these values would be used in actual practice. See "Memory Map" section for the VOLTAGE REGISTER address location.

Voltage/Data Relationships Table 2

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LSB
MSb				(unit = 10 mV)			LSb	
0 (set)	0 (set)	0 (set)	0 (set)	0 (set)	0 (set)	2^9	2^8	MSB

BATTERY VOLTAGE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
0.01V	0000 0000 0000 0001	0001h
2.7	0000 0001 0000 1110	010Eh
3.6V	0000 0001 0110 1000	0168h
5V	0000 0001 1111 0100	01F4h
7.2V	0000 0010 1101 0000	02D0h
9.99V	0000 0011 1110 0111	03E7h
10V	0000 0011 1110 1000	03E8h

For applications requiring a general purpose voltage A/D converter, the DS2437 can be configured so that the result of a Convert V command will place the scaled binary representation of the voltage on the V_{AD} input (as opposed to the V_{DD} input) into the VOLTAGE REGISTER in the same format described in Table 2. Depending upon the state of the configuration register, either (but not both) the V_{DD} or V_{AD} voltage will be stored in the VOLTAGE REGISTER upon receipt of the Convert V command. Refer to the description of the Config-

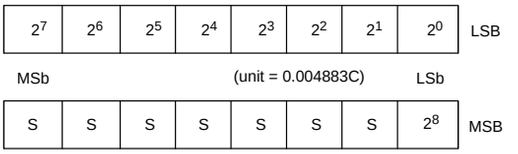
uration Register in the Memory Map section for details. If the V_{AD} input is used as the voltage input, the A/D will be accurate for $0V < V_{AD} < 2V_{DD}$ over the range $2.7V < V_{DD} < 5.0V$. Recall that the battery voltage A/D (V_{DD} input) loses accuracy as V_{DD} falls below 2.7V. This feature gives the user the ability to have a voltage A/D that meets spec accuracy for inputs over the entire range of $0V < V_{AD} < 10V$ for $V_{DD} = 5.0V$.

OPERATION – MEASURING BATTERY CURRENT

The DS2437 features a sigma–delta A/D converter that effectively measures the current flow into and out of the battery pack. It does so in the background at a rate of 32 measurements/sec; thus, no command is required to initiate current flow measurements. However, the DS2437 will only perform current A/D measurements if the IAD bit is set to “1” in the CONFIGURATION REGISTER. The DS2437 measures current flow in and out of the battery through the VSNS pins; the voltage from the VSNS+ pin to the VSNS– pin is considered to be the voltage across the current sense resistor, RSNS. While the VSNS– terminal may be tied directly to the low potential end of the RSNS resistor, we recommend to use a RC low pass filter between the hot side of RSNS and VSNST. Using a 47KΩ (max) resistor (R_F) and a 0.1 µF tantalum capacitor (CF), the filter cutoff is approximately 32Hz. The current A/D measures at a rate of 32 times per second, or once every 31.25 ms. This filter will capture the effect of many current spikes, and will thus allow the current accumulators to accurately reflect the total charge which has gone into or out of the battery.

The current is measured by the ADC with a signed 10–bit (0.004883C) resolution, and the last completed measurement is placed in the CURRENT REGISTER in a sign–extended 2’s complement format. This register is scaled such that a count of 205_{10} corresponds to a current level of 1C. This, the range of current flow that can be measured is from –2.0C (discharging) to +2.0C (charging). The sign (S) of the current measurement, indicating charge or discharge, resides in the seven most significant bits of the CURRENT REGISTER, as shown in Table 3. See “Memory Map” section for the CURRENT REGISTER address location.

Current/Data relationships Table 3



BATTERY CURRENT	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+2.495C	0000 0001 1111 1111	01FFh
+2.002C	0000 0001 1001 1010	019Ah
+1.25C	0000 0001 0000 0000	0100h
+1.001C	0000 0000 1100 1101	00CDh
0C	0000 0000 0000 0000	0000h
–1.001C	1111 1110 0011 0011	FF33h
–1.25C	1111 1111 0000 0000	FF00h
–2.002C	1111 1110 0110 0110	FE66h
–2.500C	1111 1110 0000 0000	FE00h

For the DS2437 to output current data scaled as in Table 3, the user is responsible for selecting an R_{SNS} that will provide a 100 mV drop across it at a 2C rate. However, this value could be changed to correspond to a different rate as long as this is comprehended by the user's software in interpreting the results from the DS2437.

OPERATION – CURRENT ACCUMULATORS

The DS2437 keeps track of the remaining capacity of a battery through the Integrated Current Accumulator (ICA). The ICA maintains a net accumulated total of current flowing into and out of the battery; therefore, the reading in this register is an indication of the remaining capacity in a battery, and may be used in performing gas gauge functions. In addition, the DS2437 has a register that accumulates battery charging (positive) current (CCA) and one that accumulates discharging (negative) current (DCA). This gives the smart battery system information needed to determine the end of life of a rechargeable battery, based on total charge/discharge current over its lifetime.

The current measurement described above yields a result of the instantaneous current measured at the 31.25 ms measurement times. This value is then used to increment or decrement the ICA register, increment the CCA (if current is positive), or increment the DCA (if current is negative).

The ICA is a scaled 8–bit (0.01C resolution) volatile binary counter which represents the amount of capacity remaining in the battery in terms of the full capacity (1C), normalized to a count of 100_{10}. Thus, an ICA count of 100_{10} represents 1C of charge, or 100% of capacity, or fully charged, while a count of 0 represents 0% of capacity, or fully discharged. The ICA will count up to 255_{10},but will not roll over if incremented above 2.55C, which should not occur during charging. However, since charging typically provides the battery with more than its rated capacity, the ICA should be reset to a count of 100_{10} when charging is complete, to indicate that the battery is at 100% of capacity, and to ensure that later gas gauge measurements are accurate.

The ICA is only incremented/decremented if the IAD bit is set to "1" in the CONFIGURATION REGISTER. Refer to the "Memory Map" section for details of device configuration. Table 4 below illustrates the contents of the ICA. See Memory Map section for the address location of the ICA.

ICA/Data Relationships Table 4

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSb (unit = 0.01C) LSb

BATTERY CAPACITY	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
2.55C	1111 1111	FFh
1.0C	0110 0100	64h
0.5C	0011 0010	32h
0.1C	0000 1010	0Ah
0C	0000 0000	00h

The Charging Current Accumulator (CCA) is a 2–byte (0.32C resolution) non–volatile read/write counter which represents the total charging current the battery has encountered in its lifetime. It is only updated when current through RSNS, is positive; i.e., the battery is being charged. Because this is a non–volatile register, the information will accumulate over the lifetime of the battery pack and will not be lost when the battery becomes discharged.

Similarly, the Discharge Current Accumulator (DCA) is a 2–byte non–volatile counter which represents the total discharging current the battery has encountered over its lifetime. It features the same resolution as the CCA and it also is shadowed to EEPROM in the background at the rate of once per 0.32C of discharge current if the DS2437 is properly configured, thus allowing three EEPROM updates for each complete discharge cycle of

the battery pack. Table 5 illustrates the contents of the CCA/DCA registers.

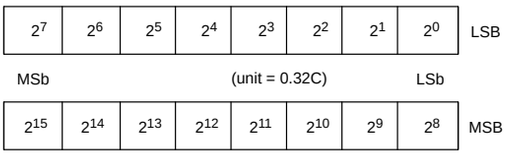
In reference to the CCA/DCA, the DS2437 can be configured to function in any of three modes. Refer to the Memory Map section for details of device configuration and for the address location of the CCA/DCA.

1. The CCA/DCA is disabled. Charging/discharging current will not be accumulated, thus allowing free use of EEPROM page 07h otherwise reserved for the CCA/DCA.
2. The CCA/DCA will accumulate charging/discharging current, but the information will NOT be shadowed to EEPROM. The information could be lost or corrupted upon discharge of the battery (depending upon the voltage to which discharged battery decays). The memory location is reserved for the CCA/DCA, and the entire page SHOULD NOT be written to.
3. The CCA/DCA will accumulate charging/discharging current, and the counter information will be shadowed to EEPROM each time the respective counter increments by 0.32C. The memory location is reserved for the CCA/DCA, and the entire page SHOULD NOT be written to.

Because the user has read/write access to the entire EEPROM array, including the CCA/DCA locations, the user's software should never allow a write to memory page 07h if the CCA/DCA are used; otherwise CCA/DCA information will be overwritten.

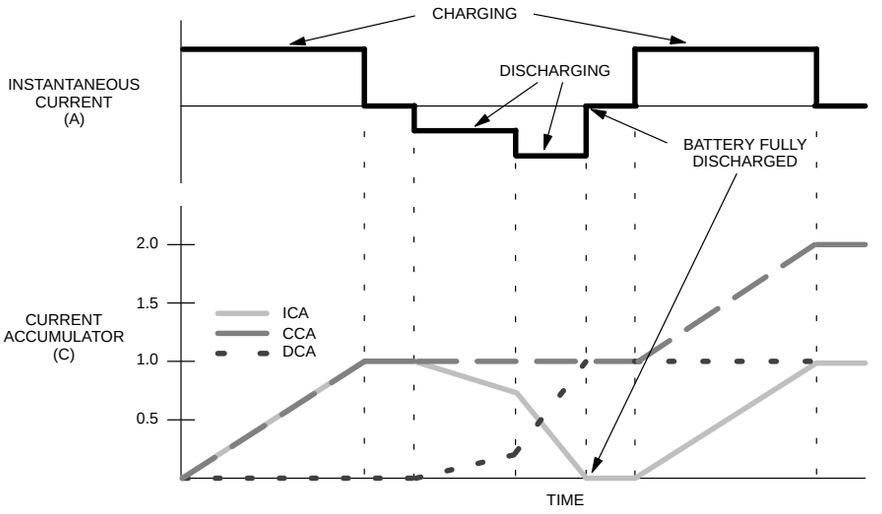
Figure 2 below illustrates the activity of the ICA, CCA, and DCA over a sample charge/discharge cycle of a battery pack, assuming the DS2437 is configured for the ICA to function and the CCA/DCA to function and shadow data to EEPROM. To simplify the illustration of the accumulators, they are treated as analog values, although they are digital counters in the DS2437. Note that when the battery becomes fully discharged, i.e., the ICA value reaches 0, the CCA and DCA register values are maintained.

CCA/DCA Data Relationships Table 5



CCA/DCA	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
0C	0000 0000 0000 0000	0000h
32C	0000 0000 0110 0100	0064
64C	0000 0000 1100 1000	00C8h
100C	0010 0001 0011 1000	0138h
20,971	1111 1111 1111 1111	FFFFh

CURRENT ACCUMULATOR ACTIVITY Figure 2



OPERATION – REAL TIME CLOCK

The 32.768 KHz crystal oscillator is used as the timebase for the timekeeping functions. The timekeeping functions are double buffered, allowing the master to read time without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to holding registers which the user accesses. This occurs after the eighth bit of the Recall Memory command.

The real–time clock is a 4–byte binary counter with a 1–second resolution. The four bytes are a count of seconds. The real–time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point, which is determined by the user. For example, 12:00 A.M., January 1, 1970 could be used as a reference point.

Two other time–related functions are available. The first is the DISCONNECT TIMESTAMP, which is written to by the DS2437 whenever it senses that the DQ line has been low for more than 1 second. This condition would signal that the battery pack has been removed from the system; the time when that occurs is written into the DISCONNECT TIMESTAMP register, so that upon replacement into the system, the system can determine how long the device has been in storage, to facilitate self–discharge corrections to the remaining battery capacity. After the disconnect has been detected, the DS2437 reverts to a sleep mode, during which nothing is active except the real time clock.

The other timestamp is the END OF CHARGE timestamp, which is written to by the DS2437 whenever it senses that charging is finished (when current changes direction). This timestamp allows the user to calculate the amount of time the battery has been in a discharge or storage state, again to facilitate self–discharge calculations.

The format of the RTC, Disconnect, and End of Charge registers are as shown in Table 6. Refer to the “Memory Map” section for the address location of the time–related registers.

Time Data Relationships Table 6

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LSB
MSb			(unit = 1s)				LSb	
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	
MSb			(unit = 1s)				LSb	
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	
MSb			(unit = 1s)				LSb	
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	MSB

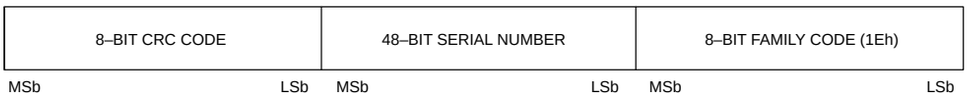
Crystal Selection

A 32.768 KHz crystal, Daiwa Part No. DT26S, Seiko Part No. DS–VT–200 or equivalent, can be directly connected to the DS2437 via pins 11 and 13 (X1, X2). The crystal selected for use should have a specified load capacitance (CL) of 6 pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, “Crystal Considerations with Dallas Real Time Clocks”.

64–BIT LASERED ROM

Each DS2437 contains a unique ROM code that is 64 bits long. The first eight bits are a 1–Wire family code (DS2437 code is 1Eh). The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 3.) The 64–bit ROM and ROM Function Control section allow the DS2437 to operate as a 1–Wire device and follow the 1–Wire protocol detailed in the section “1–Wire Bus System”. The functions required to control sections of the DS2437 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM function protocol flow chart (Figure 4). The 1–Wire bus master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, or 4) Skip ROM. After a ROM function sequence has been successfully executed, the functions specific to the DS2437 are accessible and the bus master may then provide and one of the six memory and control function commands.

64–Bit Lasered ROM Figure 3



CRC Generation

The DS2437 has an 8–bit CRC stored in the most significant byte of the 64–bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64–bit ROM and compare it to the value stored within the DS2437 to determine if the ROM data has been received error–free by the bus master. The equivalent polynomial function of this CRC is:

$$CRC = X^8 + X^5 + X^4 + 1$$

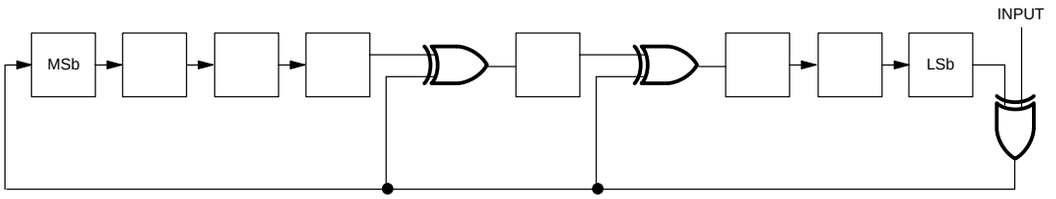
The DS2437 also generates an 8 –bit CRC value using the same polynomial function shown above and provides this value to the bus master to validate the transfer of data bytes. In each case where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function given above and compare the calculated value to either the 8–bit CRC value stored in the 64–bit ROM portion of the DS2437 (for ROM reads) or the 8–bit CRC value computed within the DS2437 (which is read as a ninth byte when a scratchpad is read). The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry inside the DS2437 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS2437 does not match the value generated by the bus master. Proper use of the CRC as outlined in the flowchart of Figure 6 can result in a communication channel with a very high level of integrity.

The 1–Wire CRC can be generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. Additional information about the

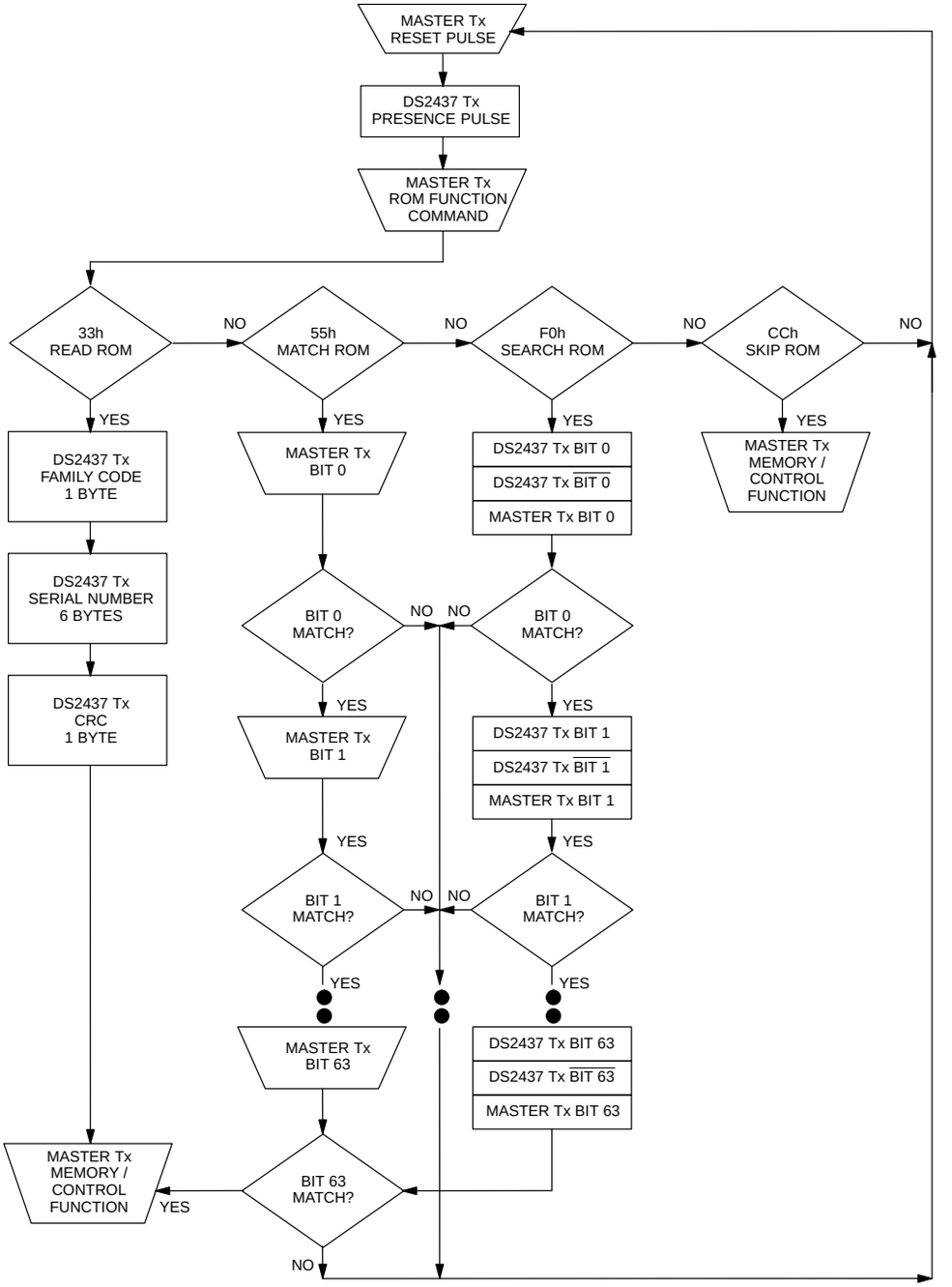
Dallas 1–Wire Cyclic Redundancy Check is available in Application Note 27 entitled “Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products”.

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value.

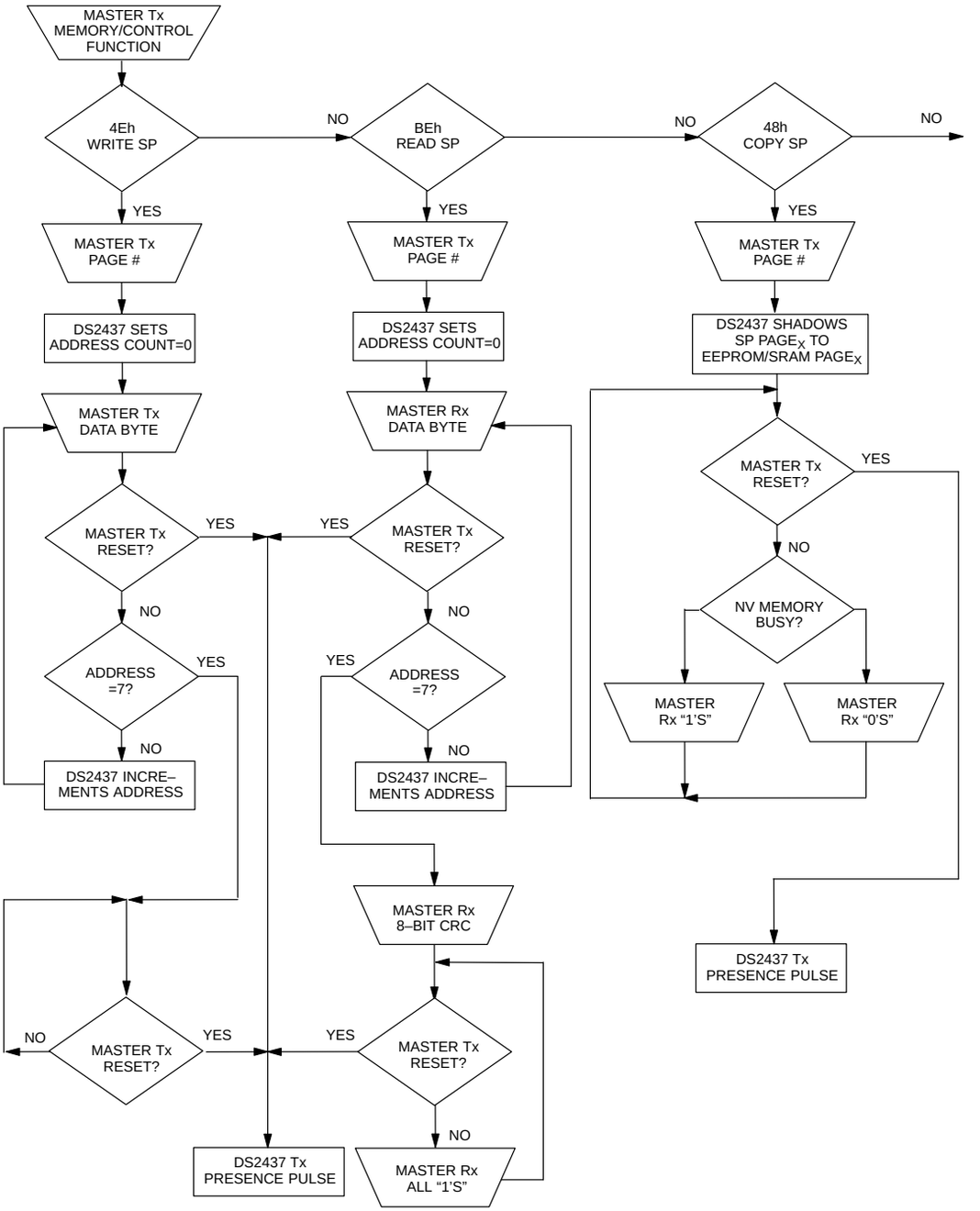
1–Wire CRC CODE Figure 4



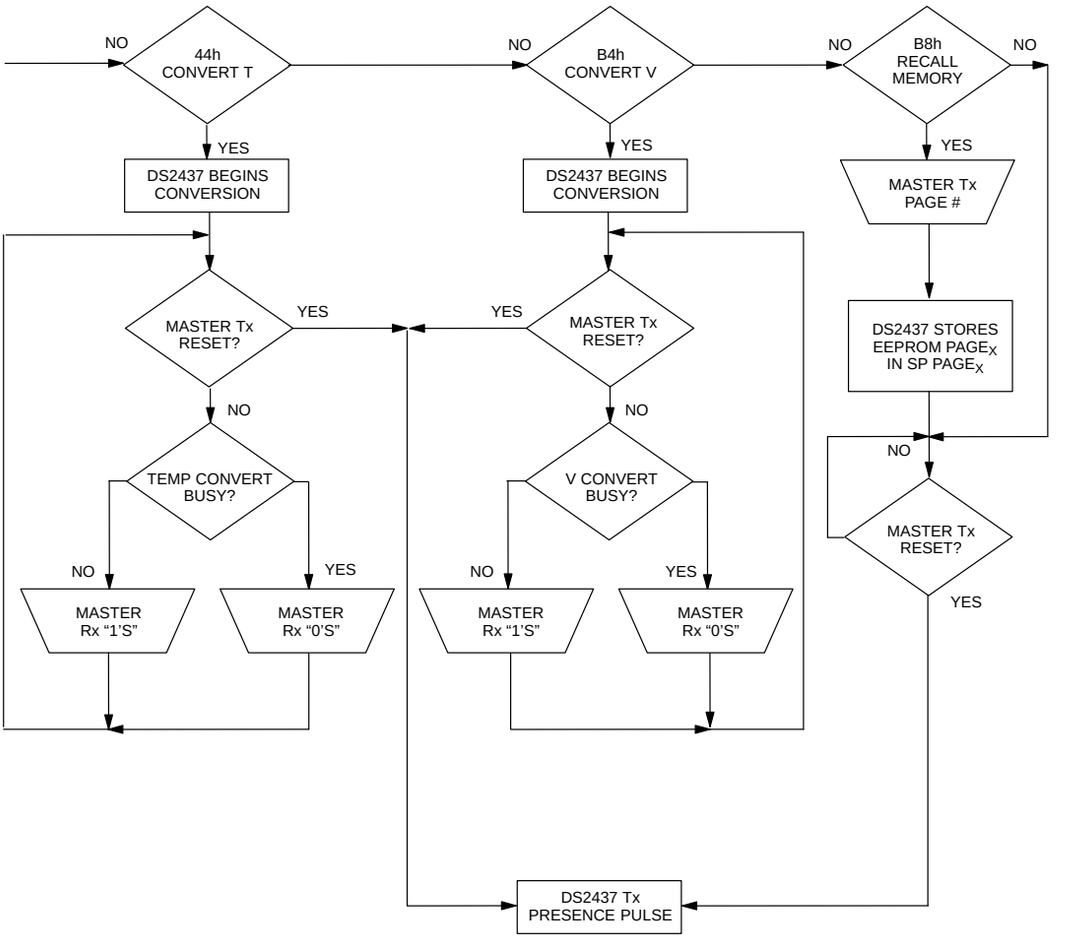
ROM FUNCTIONS FLOWCHART Figure 5



MEMORY/CONTROL FUNCTIONS FLOWCHART Figure 6



MEMORY/CONTROL FUNCTIONS FLOWCHART Figure 6 Cont'd



MEMORY MAP

The DS2437's memory is organized as shown in Figure 7. The memory consists of a scratchpad RAM and storage SRAM/EEPROM. The scratchpad helps insure data integrity when communicating over the 1–Wire bus. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to the appropriate page in memory (pages 0–2 are primarily volatile SRAM, pages 3–7 are EEPROM). This process insures data integrity when modifying the memory.

The DS2437's memory is organized as 64 bytes of memory, in 8, eight–byte pages. Each page has its own scratchpad space, organized as 8 bytes of memory. When reading a scratchpad, there is a ninth byte which may be read with a Read Scratchpad command. This byte contains a cyclic redundancy check (CRC) byte, which is the CRC over all of the 8 bytes in the currently–selected scratchpad. This CRC is implemented in the fashion described in the section titled "CRC Generation".

Page 0 (00h)

The first page contains the most frequently accessed information of the DS2437, and most locations are volatile read–only bytes with the exception of the Status / Configuration Register (Byte 0).

The Status / Configuration Register is a non–volatile read/write byte which defines which features of the DS2437 are enabled and how they will function. The register is formatted as follows:

X	ADB	NVB	TB	AD	E2?	CA	IAD
MSb							LSb

IAD = Current A/D Control Bit. "1" = the current A/D and the ICA are enabled, and current measurements will be taken at the rate of 32 Hz; "0" = the current A/D and the ICA have been disabled.

CA = Current Accumulator Configuration. "1" = CCA/DCA is enabled, and data will be stored and can be retrieved from page 7, bytes 2–7; "0" = CCA/DCA is disabled, and page 7 can be used for general EEPROM storage.

E2? = Current Accumulator Shadow Selector bit. "1" = CCA/DCA counter data will be shadowed to EEPROM each time the respective register is incremented by 0.32C; = CCA/DCA counter data will not be shadowed to EEPROM. The CCA/DCA could be lost as the battery pack becomes discharged. If the CA bit in the status/configuration register is set to "0", the E2? bit will have no effect on the DS2437 functionality.

AD = Voltage A/D Input Select Bit. "1" = the battery input (VDD) is selected as the input for the DS2437 voltage A/D converter; "0" = the general purpose A/D input (VAD) is selected as the voltage A/D input. For either setting, a Convert V command will initialize a voltage A/D conversion.

TB = Temperature Busy Flag. "1" = temperature conversion in progress; "0" = temperature conversion complete.

NVB = Nonvolatile Memory Busy Flag. "1" = Copy from Scratchpad to EEPROM in progress; "0" = Nonvolatile memory not busy. A copy to EEPROM may take from 2 ms to 10 ms (taking longer at lower supply voltages).

ADB = A/D Converter Busy Flag. "1" = A/D conversion in progress on battery voltage; "0" = conversion complete, or no measurement being made. An A/D conversion takes approximately 10 ms.

X = Don't care

Bytes 1 and 2 of page 0 contain the last completed temperature conversion in the format described in the "Operation – Measuring Temperature" section. Bytes 3–4 contain the last completed voltage A/D conversion result and Bytes 5–6 contain the instantaneous current data. Refer to the appropriate section for the data format of these locations. Byte 7 is reserved and will read out as all "1".

Page 1 (01h)

The second page, Page 1, contains the ICA and real–time clock data. Both the RTC and ICA are volatile read/write locations so that they may be set, changed, or cleared by the host software. Bytes 0–3 contain the RTC data, formatted as described in the "Operation – Real Time Clock" section. Byte 4 contains the 8–bit ICA. Bytes 5–7 are reserved and will read out as all "1's".

Page 2 (02h)

The third page of memory (Page 2) contains the DISCONNECT TIME (first four bytes) and END OF

CHARGE (remaining four bytes) timestamps. This page is volatile and read / write. Refer to the “Operation – Real Time Clock” section for the formatting of these locations.

Pages 3–7 (03h – 07h)

The remainder of the memory in the DS2437 (Pages 3 through 7) is backed with EEPROM. This memory provides 40 bytes of user memory which may be used to carry any information the user wishes to store. Additionally, the CCA/DCA information is stored in bytes 4–7 of page 7 if the DS2437 is configured appropriately. If the CCA/DCA is used, page 7 should not be written to or current accumulator data will be overwritten. See “Operation – Current Accumulators” for details.

DS2437 MEMORY MAP Figure 7.

PAGE	BYTE	CONTENTS	R/W	NV?
0	0	STATUS/CONFIGURATION	R/W	YES
	1	TEMPERATURE LSB	R	NO
	2	TEMPERATURE MSB	R	NO
	3	VOLTAGE LSB	R	NO
	4	VOLTAGE MSB	R	NO
	5	CURRENT LSB	R	NO
	6	CURRENT MSB	R	NO
	7	RESERVED		
1	0	RTC BYTE 0	R/W	NO
	1	RTC BYTE 1	R/W	NO
	2	RTC BYTE 2	R/W	NO
	3	RTC BYTE 3	R/W	NO
	4	ICA	R/W	NO
	5	RESERVED		
	6	RESERVED		
	7	RESERVED		
2	0	DISCONNECT BYTE 0	R/W	NO
	1	DISCONNECT BYTE 1	R/W	NO
	2	DISCONNECT BYTE 2	R/W	NO
	3	DISCONNECT BYTE 3	R/W	NO
	4	END OF CHARGE BYTE 0	R/W	NO
	5	END OF CHARGE BYTE 1	R/W	NO
	6	END OF CHARGE BYTE 2	R/W	NO
	7	END OF CHARGE BYTE 3	R/W	NO
3	0	USER BYTE	R/W	YES
	1	USER BYTE	R/W	YES
	2	USER BYTE	R/W	YES
	3	USER BYTE	R/W	YES
	4	USER BYTE	R/W	YES
	5	USER BYTE	R/W	YES
	6	USER BYTE	R/W	YES
	7	USER BYTE	R/W	YES
4	0	USER BYTE	R/W	YES
	1	USER BYTE	R/W	YES
	2	USER BYTE	R/W	YES
	3	USER BYTE	R/W	YES
	4	USER BYTE	R/W	YES
	5	USER BYTE	R/W	YES
	6	USER BYTE	R/W	YES
	7	USER BYTE	R/W	YES
⋮	⋮	⋮	⋮	⋮
7	0	USER BYTE	R/W	YES
	1	USER BYTE	R/W	YES
	2	USER BYTE	R/W	YES
	3	USER BYTE	R/W	YES
	4	USER BYTE/ CCA BYTE 0	R/W	YES
	5	USER BYTE/ CCA BYTE 1	R/W	YES
	6	USER BYTE/ DCA BYTE 2	R/W	YES
	7	USER BYTE/ DCA BYTE 3	R/W	YES

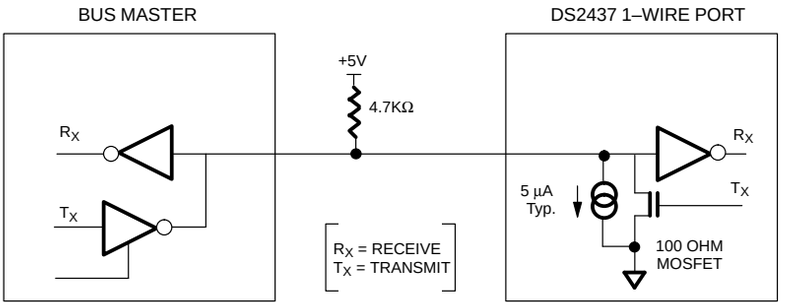
1–Wire BUS SYSTEM

The 1–Wire bus is a system which has a single bus master and one or more slaves. The DS2437 behaves as a slave. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have open drain or 3–state outputs. The 1–Wire port of the DS2437 (DQ pin) is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus requires a pull–up resistor of approximately 5KΩ.

HARDWARE CONFIGURATION Figure 8.



The idle state for the 1 wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. Infinite recovery time can occur between bits so long as the 1–Wire bus is in the inactive (high) state during the recovery period. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS2437 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2437 is on the bus and is ready to operate. For more details, see the “1–Wire Signaling” section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 5):

Read ROM [33h]

This command allows the bus master to read the DS2437’s 8–bit family code (1Eh), unique 48–bit serial number, and 8–bit CRC. This command can only be used if there is a single DS2437 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open–drain will produce a wired–AND result).

Match ROM [55h]

The Match ROM command, followed by a 64–bit ROM sequence, allows the bus master to address a specific DS2437 on a multidrop bus. Only the DS2437 that exactly matches the 64–bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64–bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64–bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull–downs will produce a wired–AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus.

Example of a ROM Search

The ROM search process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

The following example of the ROM search process assumes four different devices are connected to the same 1–Wire bus. The ROM data of the four devices is as shown (LSb first):

ROM1 = 00110101...
ROM2 = 10101010...
ROM3 = 11110101...
ROM4 = 00010001...

The search process is as follows:

1. The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.
2. The bus master will then issue the search ROM command on the 1–Wire bus (F0h).
3. The bus master reads a bit from the 1–Wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1–Wire bus. ROM1 and ROM4 will place a 0 onto the 1–Wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1–Wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line; therefore the bus master sees a 0. The bus master reads another bit. Since the Search ROM data command is being executed, all of the devices on the 1–Wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1–Wire bus. ROM1 and ROM4 will place a 1 onto the 1–wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1–wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1–Wire bus that have a 0 in the first position and others that have a 1.

   The data obtained from the two reads of the 3–step routine have the following interpretations:

   00 – There are still devices attached which have conflicting bits in this position.

   01 – All devices still coupled have a 0 bit in this bit position.

   10 – All devices still coupled have a 1–bit in this bit position.

   11 – There are no devices attached to the 1–Wire bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1–Wire bus.
5. The bus master performs two more reads and receives a 0–bit followed by a 1–bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.
6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.
7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.
8. The bus master writes a 0–bit. This deselects ROM1 leaving ROM4 as the only device still connected.
9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1–Wire bus.
10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.
11. The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.
12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.
13. The bus master starts a new ROM search by repeating steps 1 through 3.

14. The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.
15. The bus master executes two read time slots and receives two zeros.
16. The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.
17. The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.
18. The bus master starts a new ROM search by repeating steps 13 through 15.
19. The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.
20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

Note that the bus master learns the unique ID number (ROM data pattern) of one 1–Wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

960 µs + (8 + 3 x 64) 61 µs = 13.16 ms

The bus master is therefore capable of identifying 75 different 1–Wire devices per second.

MEMORY COMMAND FUNCTIONS

The following command protocols are summarized in Table 6, and by the flowchart of Figure 6.

Write Scratchpad [4Ehxxh]

This command writes to the scratchpad page xxh of the DS2437. The entire 8–byte scratchpad space may be written, but all writing begins with the byte present at address 0 of the selected scratchpad. After issuing this command, the user must send the page number of the scratchpad to be written; then the user may begin writing data to the DS2437 scratchpad. Writing may be terminated at any point by issuing a reset. Valid page numbers for writing are 00h–07h.

Read Scratchpad [BEhxxh]

This command reads the contents of the scratchpad page xxh on the DS2437. After issuing this command, the user must send the page number of the scratchpad to be read, and then may begin reading the data, always beginning at address 0 of the selected scratchpad. The user may read through the end of the scratchpad space (byte 07h), with any reserved data bits reading all logic 1's and after which the data read will be all logic 1's. If not all locations are to be read, the master may issue a reset to terminate reading at any time. Valid page numbers are 00h – 07h.

Copy Scratchpad [48hxxh]

This command copies the scratchpad page xxh into the EEPROM / SRAM memory page xxh of the DS2437. After issuing this command, the user must write a page number to direct which page of memory the scratchpad is to be copied. Valid page numbers are 00h – 07h. If the bus master issues read time slots following this command, the DS2437 will output "0" on the bus as long as it is busy copying the scratchpad to SRAM/EEPROM; it will return a "1" when the copy process is complete.

Recall Memory [B8hxxh]

This command recalls the stored values in EEPROM / SRAM page xxh to the scratchpad page xxh. This command must proceed a Read SPxx command in order to read any page of memory on the DS2437. No data is available directly with a Read SP command. Valid page numbers are 00h – 07h.

Convert T [44h]

This command begins a temperature conversion. No further data is required. The temperature conversion will be performed and then the DS2437 will remain idle. If the bus master issues read time slots following this command, the DS2437 will output "0" on the bus as long as it is busy making a temperature conversion; it will return a "1" when the temperature conversion is complete.

Convert V [B4h]

This command instructs the DS2437 to initiate a voltage analog–to–digital conversion cycle. The voltage supply that is measured is defined by the AD bit of the Status/ Configuration register. This sets the ADB flag (see Sta-

tus/Configuration register discussion in the Memory Map section). When the A/D conversion is done, the ADB flag is cleared and the current voltage value is placed in the VOLTAGE REGISTER of page 00h. While an A/D conversion is taking place, all other memory functions are still available for use. If the bus master issues read time slots following this command, the DS2437 will output “0” on the bus as long as it is busy making a voltage measurement; it will return a ”1” when the conversion is complete.

DS2437 COMMAND SET Table 6.

INSTRUCTION	DESCRIPTION	PROTOCOL	1–WIRE BUS MASTER STATUS AFTER ISSUING PROTOCOL	1–WIRE BUS DATA AFTER ISSUING PROTOCOL
MEMORY COMMANDS				
Read Scratchpad	Reads bytes from DS2437 Scratchpad page xxh	BEh <page 00h–07Fh>	Rx	<read up to nine bytes of data>
Write Scratchpad	Writes bytes to DS2437 Scratchpad page xxh	4Eh <page 00h–07h>	Tx	<write up to eight bytes of data>
Copy Scratchpad	Copies entire contents of Scratchpad page xxh to eight–byte EEPROM/ SRAM page xxh	48h<page 00h–07h>	Idle or Rx of NVB bit	{NVB bit in Status Register = 1 until copy complete (2–10 ms, typ)}
Recall Memory	Copies entire contents of EEPROM/SRAM page xxh to Scratchpad page xxh	B8h<page 00h–07h>	Idle	Idle
REGISTER COMMANDS				
Convert T	Initiates temperature conversion	44h	Idle or Rx of TB bit	{TB bit in Status Register = 1 until conversion complete}
Convert V	Initiates voltage A/D conversion	B4h	Idle or Rx of ADB bit	{ADB bit in Status Register = 1 until conversion complete}

NOTES:

1. Temperature conversion takes up to 1 second.
2. A/D conversion takes up to 2 ms.
3. EEPROM write takes up to 50 ms.

Sample Command Sequence Table 7
Example: Bus Master enables the ICA, CCA, and DCA on a single DS2437 and configures it such that the CCA/DCA information is shadowed to EEPROM. The voltage A/D is configured such that the DS2437 will perform voltage measurements on the battery (VDD) voltage.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	4Eh00h	Issue Write SP 00h command
TX	0Fh	Sets ICA, CA, E2?, AD Bits active
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	BEh00h	Issue Read SP 00h command
RX	<9 data bytes>	Read scratchpad data and CRC
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	48h00h	Issue Copy SP 00h command
RX	Read Slots	DS2437 returns a “1” when Copy SP is complete
TX	Reset	Reset pulse
RX	Presence	Presence Pulse, done

Sample Command Sequence Table 8
Example: Bus Master issues a temperature and voltage conversion, then reads the temperature, battery voltage, battery current, all on a single DS2437.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	44h	Issue Convert Temperature command, Read Slots
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	B4h	Issue Convert Voltage command
TX	Reset	Reset pulse, Read Slots
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	BEh00h	Issue Recall Memory page 00h command

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	BEh00h	Issue Read SP 00h command
RX	<9 data bytes>	Read scratchpad data and CRC. This page contains temperature, voltage, and current measurements.
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

Sample Command Sequence Table 9

Example: Assuming a single DS2437 is configured for its current accumulators to function, this sequence allows the Bus Master to read the three current accumulators.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	B8h01h	Issue Recall Memory page 01h command
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	BEh01h	Issue Read SP 01h command
RX	<9 data bytes>	Read scratchpad data and CRC. The ICA is located in byte 04h
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	B8h07h	Issue Recall Memory page 07h command
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	BEh07h	Issue Read SP 07h command
RX	<9 data bytes>	Read scratchpad data and CRC. The CCA is located in bytes 04h–05h and the DCA is located in bytes 06h–07h.
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

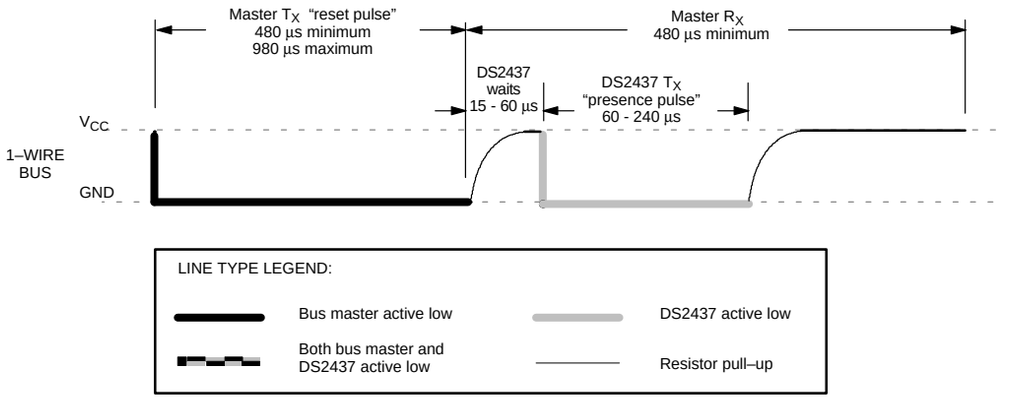
I/O SIGNALING

The DS2437 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2437 is shown in Figure 9. A reset pulse followed by a presence pulse indicates the DS2437 is ready to send or receive data given the correct ROM command and memory function command.

The bus master transmits (Tx) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into a receive mode (Rx). The 1–Wire bus is pulled to a high state via the 5KΩ pull–up resistor. After detecting the rising edge on the I/O pin, the DS2437 waits 15–60 µs and then transmits the presence pulse (a low signal for 60–240 µs). DS2437 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 9



Write Time Slots

A write time slot is initiated when the host pulls the data line from a high (inactive) logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual write cycles.

The DS2437 samples the I/O line in a window of 15 µs to 60 µs after the I/O line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero Occurs (See Figure 10).

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot.

For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot.

Read Time Slots

The host generates read time slots when data is to be read from the DS2437. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 µs; output data from the DS2437 is then valid within the next 14 µs maximum.

The host therefore must stop driving the I/O pin low in order to read its state 15 µs from the start of the read slot. (see Figure 10). By the end of the read time slot, the I/O pin will pull back high via the external pull–up

resistor. All read time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual read slots. Figure 11 shows that the sum of t_{INIT}, t_{RC}, and t_{SAMPLE} must be less than 15 µs. Figure 12 shows that system timing margin is maximized by keeping t_{INIT}, and t_{RC} as small as possible and by locating the master sample time toward the end of the 15 µs period.

RELATED APPLICATIONS NOTES

The following Application Notes can be applied to the DS2437. These notes can be obtained from the Dallas Semiconductor Application Note Book, via our web–site at http://www.dalsemi.com/, or through our faxback service at (972) 371–4441.

Application Note 27: "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Product"

Application Note 55: "Extending the Contact Range of Touch Memories"

Application Note 74: "Reading and Writing Touch Memories via Serial Interfaces"

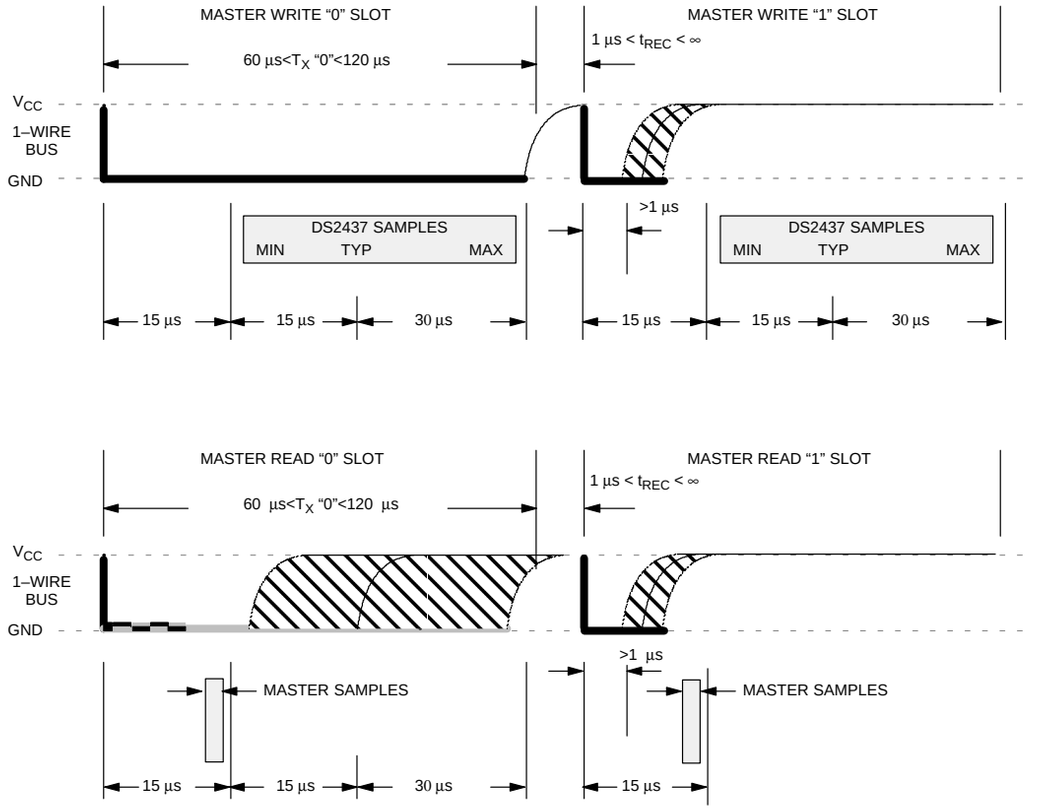
Application Note 106: "Complex MicroLANs"

Application Note 108: "MicroLAN In the Long Run"

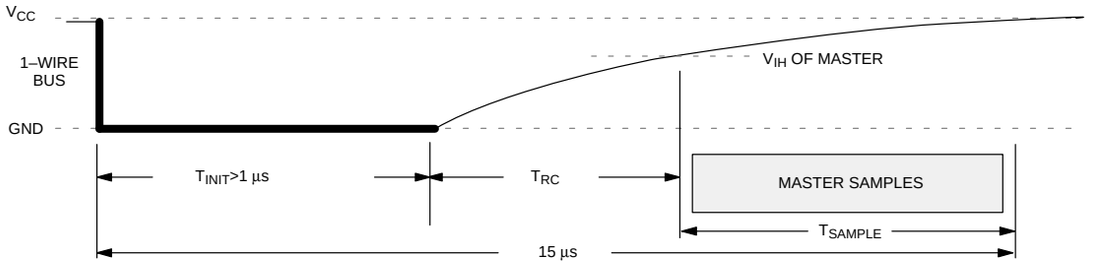
Application Note 110: "NiCd/NiMH Intelligent Battery System Reference Design Using the DS2437"

Sample 1–Wire subroutines that can be used in conjunction with AN74 can be downloaded from the website or our Anonymous FTP Site.

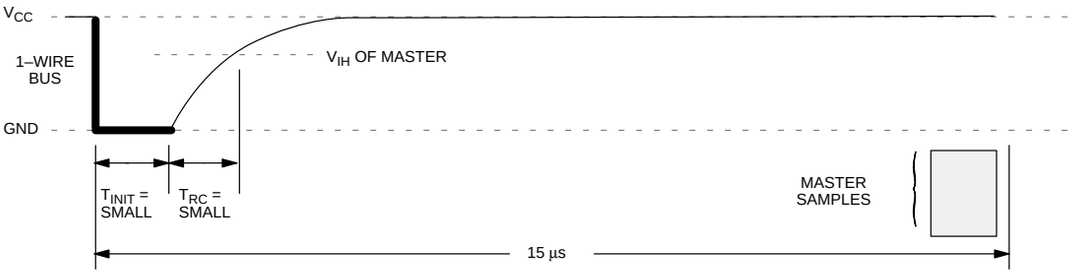
READ / WRITE TIMING DIAGRAM Figure 10

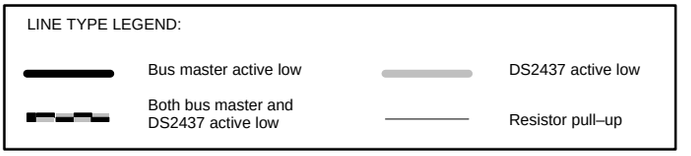


DETAILED MASTER READ ONE TIMING Figure 11



RECOMMENDED MASTER READ ONE TIMING Figure 12





ABSOLUTE MAXIMUM RATINGS*

Voltage on VDD and VAD, Relative to Ground	–0.3V to +12V
Voltage on VSENS+, VSENS–, Relative to Ground	>±300 mV
Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C; 2.7V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}		2.7		10.0	V	3
Data Pin	DQ		–0.3		+5.5	V	3
DQ Pull–up Voltage			2.7		5.5		
Analog Ground	AGND		GND –0.5		GND +0.5	V	3

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; 2.7V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Input Logic High	V_{IH}		2.0			V	3
Input Logic Low	V_{IL}		–0.3		0.8	V	3
Shutdown Current	I_{DD1}	DQ=0, RTC Active		10	15	µA	2, 4
Standby Current	I_{DD2}	DQ=1, ICA Active		50	100	µA	2, 4
Active Current	I_{DD}	Temperature or Voltage Conversions or EEPROM write in progress		250	1000	µA	4
Input Resistance	R_I	DQ			500	KΩ	5

ELECTRICAL CHARACTERISTICS: DIGITAL THERMOMETER

(–40°C to +85°C; 2.7V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error ($T_{ACTUAL} - T_{MEASURED}$)	T_{ERR}	0°C to 70°C			±2	°C	6
Resolution					13	bits	
Conversion Time	t_{CONVT}			400	1000	ms	

ELECTRICAL CHARACTERISTICS: VOLTAGE A/D CONVERTER

(–40°C to +85°C; 2.7V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
A/D Error	VAD_{ERR}			±10	±50	mV	
V_{AD} Input Range	V_{ADR}	2.7V ≤ V_{DD} ≤ 5.0V	0		$2V_{DD}$	V	3
V_{AD} Input Range	V_{ADR1}	V_{DD} > 5.0V	0		10.0	V	3
V_{DD} Input Range	V_{DDR}		2.7		10.0	V	3
Resolution					10	bits	
Conversion Time	t_{CONVV}				2	ms	
No Missing Code Temperature Range			–40		+85	°C	
Monotonicity				Guaranteed			

ELECTRICAL CHARACTERISTICS: CURRENT A/D CONVERTER

(–40°C to +85°C; 4.5V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Current Measurement Error	IAD_{ERR}			±2		LSB	1
Integrated Current Error	CA_{ERR}			2	5	%	
Instantaneous Current Resolution					10	bits	

ELECTRICAL CHARACTERISTICS: RTC COUNTER

(–40°C to +85°C; 2.7V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Clock Error	RTC_{ERR}						7
Resolution			1			sec	

AC ELECTRICAL CHARACTERISTICS: 1–WIRE INTERFACE

(–40°C to +85°C; 2.7V ≤ V_{DD} ≤ 10.0V)

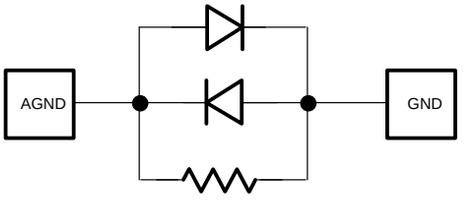
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}		60		120	µs	
Recovery Time	t_{REC}		1			µs	
Write 0 Low Time	t_{LOW0}		60		120	µs	
Write 1 Low Time	t_{LOW1}		1		15	µs	
Read Data Valid	t_{RDV}				15	µs	
Reset Time High	t_{RSTH}		480			µs	
Reset Time Low	t_{RSTL}		480			µs	
Presence Detect High	t_{PDH}		15		60	µs	

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Presence Detect Low	t_{PDL}		60		240	µs	
DQ Capacitance	C_{DQ}				25	pF	

NOTES:

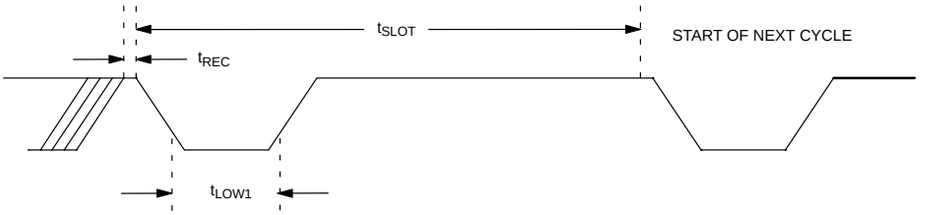
1. Current measurement accuracy is ±2 LSb or 2%, whichever is greater. Contact the factory for applications with less than 4.5V supply voltage.
2. Shutdown and Standby currents specified for the range 0°C to 70°C.
3. All Voltages are referenced to GND.
4. I_{DD} specified with V_{DD} = 5.0V.
5. Input load is to GND.
6. See Typical Curve for thermometer specification limits beyond 0°C to 70°C range.
7. Refer to AN58.
8. See Figure 13 for internal ground connections. GND and AGND must be connected to the same potential.

INTERNAL GROUND CONNECTIONS Figure 13

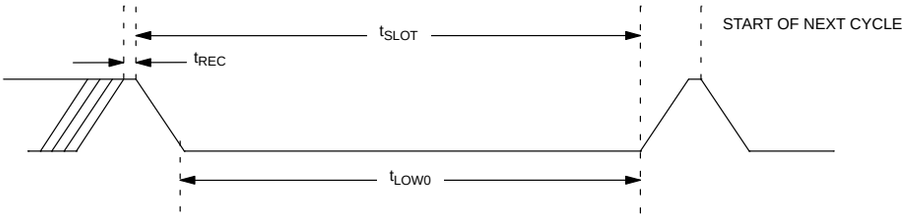


TIMING DIAGRAMS Figure 14

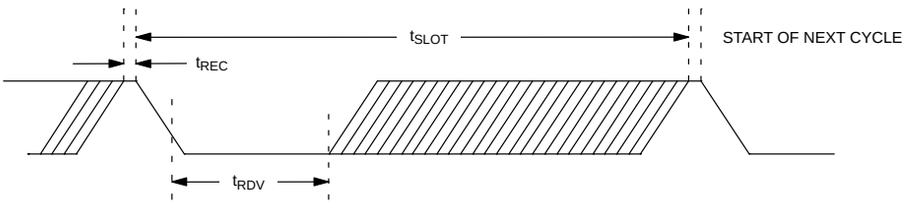
1–WIRE WRITE ONE TIME SLOT



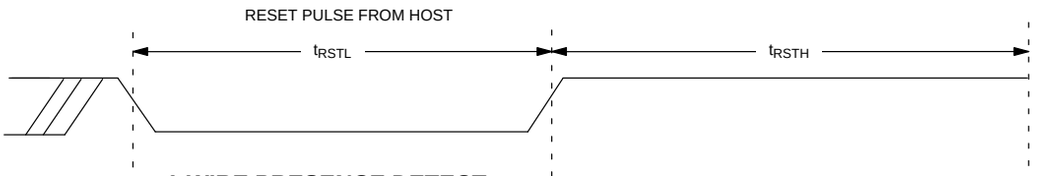
1–WIRE WRITE ZERO TIME SLOT



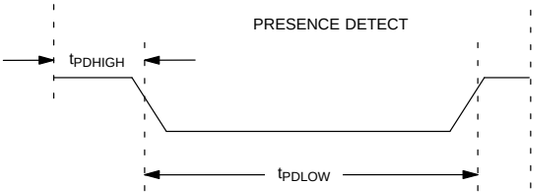
1–WIRE READ TIME SLOT



1–WIRE RESET PULSE



1-WIRE PRESENCE DETECT



TYPICAL THERMOMETER PERFORMANCE CURVE Figure 15

TBD