DALLAS SEMICONDUCTOR

DS83CH20
Unified I/O

PRODUCT SPECIFICATION

Revision 1.3

1.0 OVERVIEW

1.1 DESCRIPTION

The DS83CH20 provides a complete solution for all of the desired functions in desktop PC I/O. It incorporates a complete floppy disk controller with a digital data separator, keyboard controller, real time clock, IEEE 1284 compliant parallel port, and two 16550A compatible UARTs with infrared communication support. Also provided are two programmable chip selects and 12 general purpose I/O pins. Full Plug and Play support and advanced power management features make the DS83CH20 an ideal choice for advanced green desktop PC designs.

The DS83CH20 meets or exceeds all Microsoft recommendations for the PC'95 Plug and Play system designs. The system interface supports a direct connection to the ISA bus that decodes all 16 address lines for the on–chip functions. All internal devices can be enabled and disabled independently. In addition, all non–static on–chip devices can be relocated within the I/O address map and assigned interrupt and DMA channels per the PC'95 recommendations.

The FDC is fully 82077SL compatible and supports the standard PC data rates of 250, 300, and 500 kbps, and 1 Mbps in MFM–encoded data mode. A perpendicular recording mode supports high density media. When used with the 1 Mbps data rate, this new mode allows the use of a 4 Mbyte floppy drives which format ED media to 2.88 Mbyte capacity. The FDC also supports power saving features that are software compatible with the 82077SL. These include clock disable, immediate auto–powerdown, low–latency awakening, and a power–saving state for the write precompensator. The high performance digital data separator needs no external components, and is compatible with the strict data separator requirements of floppy and floppy–tape drives. In software, the FDC can be located to one of two standard addresses within the ISA map, and can be assigned one of ten interrupt channels and one of 4 DMA channels.

The two UARTs are fully 16550A compatible and support MIDI baud rates. One port also supports a full complement of infrared transmit and receive communication with IrDA 1.0, and Sharp ASK. The UARTs can be independently located to one of 256 possible locations within the ISA map, and independently assigned one of ten interrupt channels.

The IEEE 1284 parallel port is fully compatible with the IEEE 1284 standard, including level 2 support. This port supports Enhanced Parallel Port (EPP) including both V1.7 and V1.9 modes, and an Extended Capabilities Port (ECP). Full compatibility is maintained with ISA, EISA, and Micro Channel parallel ports. Software can locate the parallel port to one of 256 possible locations within the ISA map, and assign the port to one of ten interrupt channels and one of four DMA channels.

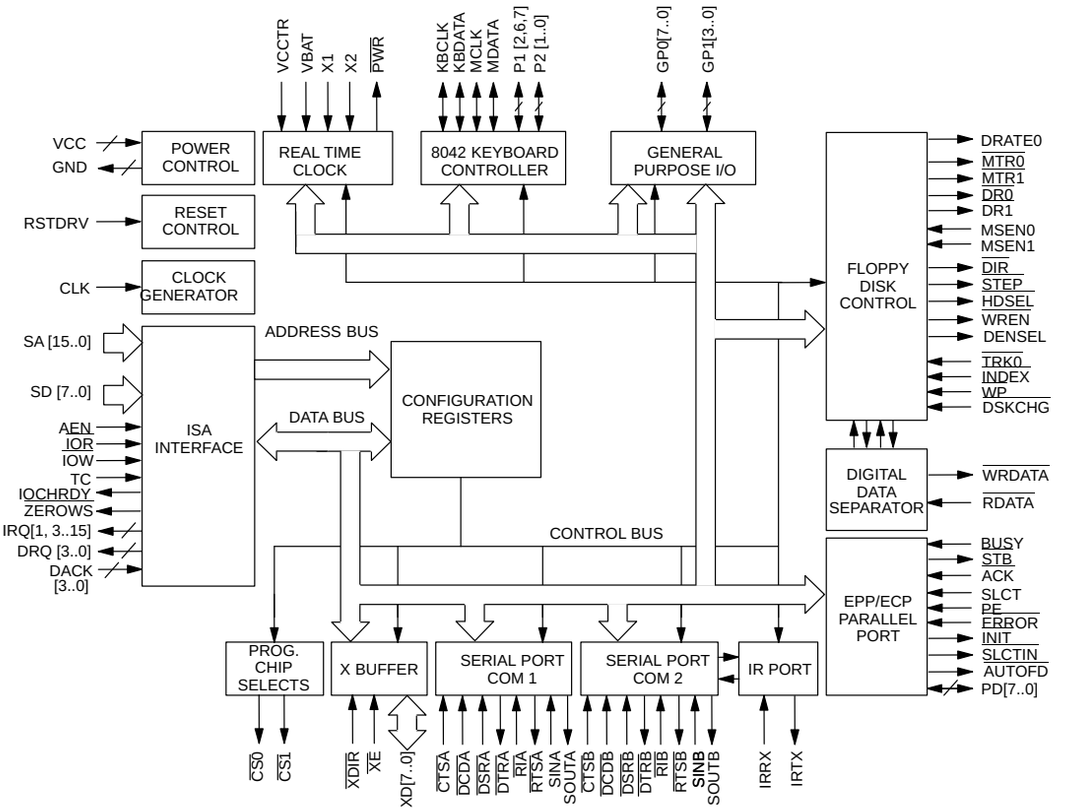
The keyboard controller is fully software and hardware compatible with the 8042AH. It incorporates 4K bytes of ROM as compared to the standard 2K byte amount to support additional firmware desired for advanced keyboard BIOS functions. A full 256 bytes of RAM are available for scratchpad storage. Nine programmable I/O lines support necessary dedicated control functions.

Two general purpose chip select pins can each be programmed to select a range of 16, 64, 256, or 1K bytes from any base ISA address that falls on a range boundary. Twelve general purpose I/O port pins are available that can be located to any even–byte boundary within the 64K byte ISA map.

The real time clock is fully compatible with the DS1685 and supplies 242 bytes of configuration RAM. The RTC also provides advanced power control circuitry for soft power on by an external stimulus (kickstart) or by a time and date alarm (wake–up). The RTC's kickstart source can be a switch closure on the KBC P16 pin, a modem ring on UART A or B, infrared input activity on the IRRX pin, or a combination of the above. An independent supply pin powers the RTC that allows power down of the rest of chip along with the motherboard. This makes it possible to power the kickstart and wake up circuitry from a small trickle supply source while the main supply, and the rest of the system, are powered down.

In addition to the soft power on feature described above, the DS83CH20 supports individual power down of all devices with system power applied. This allows power down of an on–chip device during periods of inactivity. When enabled, an auto power down feature intelligently detects inactivity of selected on–chip devices and automatically removes power without software intervention. As an option, a device's inputs are disabled and its output pins placed in a high–Z condition whenever that device is powered down.

DS83CH20 BLOCK DIAGRAM Figure 1–1



1.2 DS83CH20 DETAILED FEATURE SUMMARY

- **ISA Bus Interface**
  - Direct interface to ISA bus
  - All address decoding performed on–chip
  - All 16 address lines decoded for all internal functions
  - X–Bus buffer for BIOS memory interface (10 pins)
- **Real Time Clock**
  - DS12885, DS1685 compatible clock/calendar
  - Calendar: day, date, months, years with leap year compensation
  - Time: seconds, minutes, hours; 12–or 24–hour format
  - Supports daylight savings time adjustment
  - 242 bytes NV configuration RAM
  - System wake–up and date alarms
  - On–chip crystal oscillator
  - < 1 µA battery backup current
- **Keyboard Controller**
  - 8042AH software compatible
  - 4K ROM for program storage
  - 256 bytes data RAM
  - Asynchronous access to two data registers and one status register
  - Power saving modes
  - Supports interrupt and polled access
  - Four dedicated open–drain bi–directional pins
  - 10 programmable I/O pins
  - 8–bit timer/counter
- **Floppy Disk Controller**
  - 82077SL software compatible
  - PC–AT and PS/2 operating modes
  - High performance digital data separator

- Data rates up to 1 Mbps
- Perpendicular recording format support
- Low power CMOS with power down modes
- 16 byte FIFO

- **UARTs (2)**
  - 16550A software compatible
  - 16–byte send/receive FIFO's
  - Programmable baud rate generator
  - Supports 115.2K baud

- **Infrared I/O**
  - Supported via UART 2
  - Transmit / receive for IRDA 1.0 and Sharp ASK

- **IEEE 1284 Parallel Port**
  - Enhanced Parallel Port (EPP) compatible
  - Extended Capabilities (ECP) compatible, including level 2 support
  - Compatible with ISA, EISA, and Micro Channel architectures
  - Includes protection circuit against damage caused when printer is powered up

- **General Purpose Pins**
  - 12 general purpose I/O pins programmable as input / output or isolated
  - Two general purpose chip select outputs

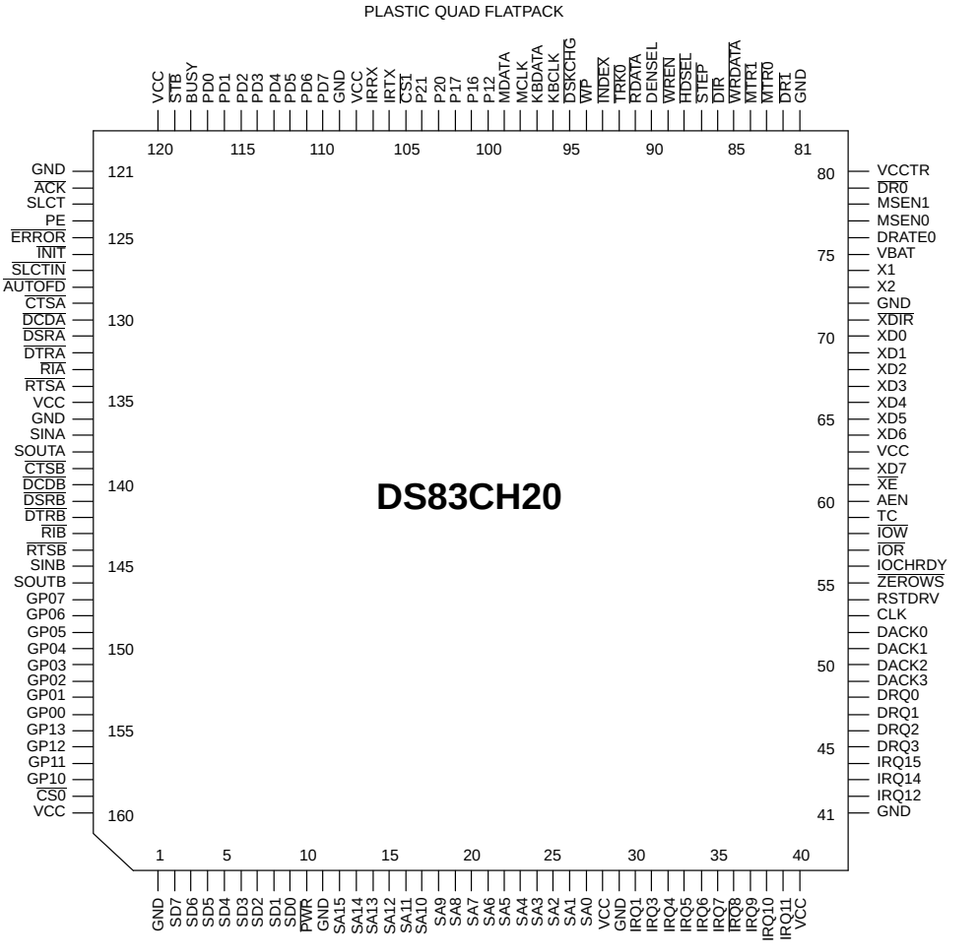
- **Plug and Play Support**
  - Meets Microsoft PC'95 requirements
  - Supports two address locations for FDC
  - Supports 256 base address location for UARTs and Parallel Port
  - Supports any even byte boundary base address locations for GP I/O
  - Supports 16, 64, 256, or 1K byte range select for programmable chip selects on any range byte boundary
  - Ten IRQ options for FDC, UARTs and Parallel Port
  - Four DMA options for FDC and Parallel Port

- **Power Management**
  - Ability to power down individual modules
  - Intelligent auto power management available to all modules
  - Optional input disable and output high–Z on power down
  - Full chip power down mode
  - "Kickstart" soft power on from button, modem ring, or IR detect
  - Wake–up on time, date

- **160–pin QFP package**

2.0 PIN CONFIGURATION

PIN CONNECTION DIAGRAM Figure 2–1



2.1 PIN SUMMARY

Listed in the tables below are a summary of all of the pin functions for the DS83CH20.

CHIP LEVEL PIN SUMMARY Table 2–1

SYMBOL	PIN	TYPE	FUNCTION
CLK	53	I	**Clock Input.** This input should be connected to the 48 or 24 MHz system clock source. Frequency selection is made via the XD7 signal on reset; XD7 low selects 48 MHz; high selects 24 MHz.
GND	1,11,29, 41,72,81, 109,121, 136	–	**Digital Ground.** Connections for ground. NOTE: All GND pins must be connected to ground.
V_{CC}	28,40,63, 108,120, 135,160	I	**Digital Supply Voltage.** +5V supply voltage. NOTE: All V_{CC} pins must be connected to +5V supply voltage.

ISA BUS PIN SUMMARY Table 2–2

SYMBOL	PIN	TYPE	FUNCTION
AEN	60	I	**Address Enable.** This input disable function selection via SA15–SA0 when it is high. Access during DMA transfer is NOT affected by this pin.
DACK3..0	49–52	I	**DMA Acknowledge Inputs.** These pins are used to acknowledge DMA requests and to enable the $\overline{IOR}$ and $\overline{IOW}$ lines during DMA transfers to the FDC or Parallel Port. These two devices can be assigned to any of the DMA channels via the configuration registers.
DRQ3..0	45–48	O	**DMA Request Outputs.** These pins are used to signal DMA service requests from the FDC and the Parallel Port. These two devices can be assigned to any of the DMA channels via the configuration registers. Unselected DRQ's will remain in a High–Z condition.
IOCHRDY	56	O	**I/O Channel Ready.** When this signal is driven low and EPP mode is selected, the parallel port extends the ISA bus cycle. IOCHRDY is an open–drain output.
$\overline{IOR}$	57	I	**I/O Read.** Active low input to signal a data read by the microprocessor.
$\overline{IOW}$	58	I	**Write.** Active low input to signal an I/O write from the ISA bus.
IRQ1	30	I/O	**Interrupt Request 1.** This pin is assigned as the keyboard interrupt generated from the internal P24 line of the Keyboard Controller.
IRQ3..7, 9..11, 14..15	31–35, 37–39, 43–44	O	**Interrupt Request Outputs.** These interrupt outputs are used to signal interrupt requests from the on chip devices. The interrupt sources from the FDC, Parallel Port, and UARTs can be assigned via the configuration registers to any of these IRQ lines. Unselected IRQ's will remain in a High–Z condition.
$\overline{IRQ8}$	36	O	**Interrupt Request 8.** This pin is assigned as the Real Time Clock interrupt request output. The polarity of $\overline{IRQ8}$ can be changed to active high via the configuration registers. $\overline{IRQ8}$ is in a High–Z state whenever the RTC is disabled.

SYMBOL	PIN	TYPE	FUNCTION
IRQ12	42	I/O	**Interrupt Request 12.** This pin is assigned as the mouse interrupt generated from internal P25 of the Keyboard Controller.
RSTDRV	54	I	**Master Reset.** Active high input resets the floppy disk controller to the idle state, and resets all disk interface outputs to their inactive states. The DOR, DSR, CCR, Mode command, Configure command, and Lock command parameters are cleared to their default values. The Specify command parameters are not affected. The Configuration Registers are set to their selected default values.
SA[15,,0]	12–27	I	**System Address.** These system address lines determine which internal DS83CH20 register is addressed. 16–bit decoding on all internal register is implemented. SA15–SA0 are don't cares during a DMA transfer.
SD[7..0]	2–9	I/O	**System Data.** Bi–directional system data bus. D0 is the LSB and D7 is the MSB. These signals all have 12 mA (sink) buffered outputs.
TC	59	I	**Terminal Count.** Control signal from the DMA controller to indicate the termination of a DMA transfer. TC is accepted only when an assigned DMA channel is active. TC is active high in PC–AT mode, and active low in PS/2 mode.
$\overline{\text{ZEROWS}}$	55	O	**Zero Wait State.** This pin is the Zero Wait State open drain output pin. $\overline{\text{ZEROWS}}$ is driven low when the EPP or ECP is written and the access can be shortened.

FLOPPY DISK PIN SUMMARY Table 2–3

SYMBOL	PIN	TYPE	FUNCTION
DENSEL	90	O	**FDC Density Select.** Indicates that a high FDC density data rate (500 Kbps or 1 Mbps) or a low density data rate (250 or 300 Kbps) is selected. DENSEL's polarity is controlled via the FDC Mode Configuration Register.
$\overline{\text{DIR}}$	86	O	**FDC Direction.** This output determines the direction of the floppy disk drive head movement (low = step in, high = step out) during a seek operation. During reads or writes, DIR is inactive.
$\overline{\text{DR0}}$, $\overline{\text{DR1}}$	79,82	O	**FDC Drive Select 0, 1.** These are the decoded drive select outputs that are controlled by the Digital Output Register bits D0, D1. The Drive Select outputs are gated with DOR bits 4–7. These are active low outputs.
DRATE0	76	O	**FDC Data Rate 0.** This output reflects the currently selected FDC data rate, as determined by the setting of the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), which ever was written last.
$\overline{\text{DSKCHG}}$	95	I	**FDC Disk Change.** This input indicates if the drive door has been opened. The state of this pin is available from the Digital Input Register.
$\overline{\text{HDSEL}}$	88	O	**FDC Head Select.** This output determines which side of the FDD is accessed. A low output selects side 1, a high output selects side 0.
$\overline{\text{INDEX}}$	93	I	**FDC Index.** A high to low transition on this input signals the beginning of a FDC track.
MSEN0,1	77,78	I	**Media Sense.** FDC Media Sense inputs.

SYMBOL	PIN	TYPE	FUNCTION
$\overline{MTR0,1}$	83, 84	O	**FDC Motor Select 0, 1.** These are the motor enable lines for drives 0 and 1, and are controlled by bits D7–D4 of the Digital Output register. They are active low outputs.
$\overline{RDATA}$	91	I	**FDC Read Data.** This input is the raw serial data read from the floppy disk drive.
$\overline{STEP}$	87	O	**FDC Step.** This output signal issues pulses to the disk drive at a software programmable rate to move the head during a seek operation.
$\overline{TRK0}$	92	I	**FDC Track 0.** A low level on this input indicates to the controller that the head of the selected floppy disk drive is at track 0.
$\overline{WP}$	94	I	**FDC Write Protect.** This input indicates that the disk in the selected drive is write–protected.
$\overline{WRDATA}$	85	O	**FDC Write Data.** This output is the write precompensated serial data that is written to the selected floppy disk drive. Precompensation is software selectable.
$\overline{WREN}$	89	O	**FDC Write Enable.** This output signal enables the write circuitry of the selected disk drive. $\overline{WREN}$ has been designed to prevent glitches during power up and power down. This prevents writing to the disk when power is cycled.

PARALLEL PORT PIN SUMMARY Table 2–4

SYMBOL	PIN	TYPE	FUNCTION
$\overline{ACK}$	122	I	**Parallel Port Acknowledge.** This input is pulsed low by the printer to indicate that it has received data from the parallel port.
$\overline{AUTOFD}$ / $\overline{DSTRB}$	128	O	**Parallel Port Automatic Feed/EPP Data Strobe.** In SPP mode, this pin is the $\overline{AFD}$ signal. When low, it indicates to the printer that it should automatically line feed after each line is printed. In EPP mode, this pin is the active low $\overline{DSTRB}$ signal. This pin is in High–Z condition 10 ns after a 0 is loaded into the corresponding Control Register bit.
BUSY / $\overline{WAIT}$	118	I	**Parallel Port Busy/EPP Wait.** In SPP mode, this pin serves as the BUSY input and will be set high by the printer when it cannot accept another character. In EPP mode, this pin is the $\overline{WAIT}$ input and is used by the parallel port device to extend its access cycle.
$\overline{ERROR}$	125	I	**Parallel Port Error.** This input is set low by the printer when it has detected an error.
$\overline{INIT}$	126	O	**Initialize.** When this signal is low it causes the printer to be initialized. This pin is in a High–Z condition 10 ns after a 1 is loaded into the corresponding Control Register bit.
PD[7..0]	110–117	I/O	**Parallel Port Data.** These bidirectional pins transfer data to and from the peripheral data bus and the parallel port Data Register. These pins have high current drive capability (see DC Electrical Characteristics).
PE	124	I	**Parallel Port Paper End.** This input is set high by the printer when it is out of paper.

SYMBOL	PIN	TYPE	FUNCTION
SLCT	123	I	**Parallel Port Select.** This input is set high by the printer when it is selected.
$\overline{\text{SLCTIN}}$ / $\overline{\text{ASTRB}}$	127	O	**Parallel Port Select Input/EPP Address Strobe.** In SPP mode, this pin is $\overline{\text{SLCTIN}}$, and selects the printer when it is low. In EPP mode, this pin is $\overline{\text{ASTRB}}$, which is used as an active low address strobe. This pin is in High–Z condition 10 ns after a 0 is loaded into the corresponding Control Register bit.
$\overline{\text{STB}}$/ $\overline{\text{WRITE}}$	119	O	**Parallel Port Data Strobe/EPP Write Strobe.** In SPP mode, this pin functions as the $\overline{\text{STB}}$ active low output to indicate to the printer that valid data is available at the printer port. In EPP mode, this pin serves as the $\overline{\text{WRITE}}$ active low output. This pin is in High–Z condition 10 ns after a 0 is loaded into the corresponding Control Register bit.

UARTS PIN SUMMARY Table 2–5

SYMBOL	PIN	TYPE	FUNCTION
$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$	129, 139	I	**UARTs Clear to Send.** When low, this signal indicates that the modem or data set is ready to exchange data. The $\overline{\text{CTS}}$ signal is a modem status input whose condition the CPU can test by reading bit 4 (CTS) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 4 is the complement of the $\overline{\text{CTS}}$ signal. Bit 0 (DCTS) of MSR indicates whether the $\overline{\text{CTS}}$ input has changed state since the previous reading of MSR. $\overline{\text{CTS}}$ has no effect on the transmitter. Whenever the DCTS bit of the MSR is set, an interrupt is generated if Modem Status interrupts are enabled.
$\overline{\text{DCDA}}$, $\overline{\text{DCDB}}$	130, 140	I	**UARTs Data Carrier Detect.** When low, this signal indicates that the modem or data set has detected the carrier. The $\overline{\text{DCD}}$ signal is a modem status input whose condition the CPU can test by reading bit 7 (DCD) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 7 is the complement of the $\overline{\text{DCD}}$ signal. Bit 3 (DDCD) of MSR indicates either the $\overline{\text{DCD}}$ input has changed state since the previous reading of MSR. Whenever the DDCD bit of the MSR is set, an interrupt is generated if Modem Status interrupts are enabled.
$\overline{\text{DSRA}}$, $\overline{\text{DSRB}}$	131, 141	I	**UARTs Data Set Ready.** When low, this signal indicates that the modem or data set is ready to establish a communications link. The $\overline{\text{DSR}}$ signal is a modem status input whose condition the CPU can test by reading bit 5 (DSR) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 5 is the complement of the $\overline{\text{DSR}}$ signal. Bit 1 (DDSR) of MSR indicates whether the $\overline{\text{DSR}}$ input has changed state since the previous reading of MSR. Whenever the DDSR bit of the MSR is set, an interrupt is generated if Modem Status interrupts are enabled.
$\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$	132, 142	O	**UARTs Data Terminal Ready.** When low, this signal indicates to the modem or data set that the UART is ready to establish a communications link. The $\overline{\text{DTR}}$ signal can be set to an active low by programming bit 0 (DTR) of the Modem Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal to its inactive state.

SYMBOL	PIN	TYPE	FUNCTION
$\overline{RIA}$, $\overline{RIB}$	133, 143	I	**UARTs Ring Indicator.** When low this signal indicates that a telephone ring signal has been received by the modem. The $\overline{RI}$ signal is a modem status input whose condition the CPU can test by reading bit 6 (RI) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of MSR indicates whether the $\overline{RI}$ input has changed state since the previous reading of MSR. Whenever the TERI bit of the MSR is set, an interrupt is generated if Modem Status interrupts are enabled.
$\overline{RTSA}$, $\overline{RTSB}$	134,144	O	**UARTs Request to Send.** When low, this signal indicates to the modem or data set that the UART is ready exchange data. The $\overline{RTS}$ signal can be set to an active low by programming bit 1 (RTS) of the Modem Control register to a high level. A master reset sets this signal to its inactive (high) state. Loop mode operation holds this signal to its inactive state.
SINA, SINB	137,145	I	**UARTs Serial Input.** This input receives composite serial data from the communications link (peripheral device, modem, or data set).
SOUTA, SOUTB	138, 146	O	**UARTs Serial Output**. This output sends composite serial data to the communications link (peripheral device, Modem, or data set). This OUT signal is set to a marking state (logic 1) after a Master Reset operation. If test mode is selected, this pin provides the associated serial channel baud rate generator output signal.

INFRARED PIN SUMMARY Table 2–6

SYMBOL	PIN	TYPE	FUNCTION
IRRX	107	I	**Infrared Receiver.**
IRTX	106	O	**Infrared Transmitter.**

REAL TIME CLOCK PIN SUMMARY Table 2–7

SYMBOL	PIN	TYPE	FUNCTION
$\overline{PWR}$	10	O	**Power On Output; open drain.** The $\overline{PWR}$ pin is intended for use as an on/off control for the system power. With V_{CC} voltage removed from the DS83CH20, $\overline{PWR}$ may be automatically activated from a kickstart input via the P16 / Kickstart pin, from an RTC Wake–up interrupt, from $\overline{RIA}$, $\overline{RIB}$, or IRRX.
V_{BAT}	75	I	**Battery.** Real Time Clock battery input pin. Connects to any standard 3–Volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation.

SYMBOL	PIN	TYPE	FUNCTION
V_{CCTR}	80	I	**Trickle Supply Voltage.** Independent power supply input required to power the wake–up circuitry and all enabled kickstart inputs in the full–chip power down mode. This supply input also powers clock/calendar and RTC configuration RAM as long as V_{CCTR} voltage ≥ V_{BAT} voltage.
X1, X2.	74, 73	I	**32 KHz Crystal Inputs.** Connections for a standard 32.768 KHz crystal for the on–chip real time clock. For greatest accuracy, the DS83CH20 must be used with a crystal that has a specified load capacitance of either six pF or 12.5 pF. The Crystal Select (CS) bit in Extended Control Register 4B is used to select operation with a six pF or 12.5 pF crystal. The crystal is attached directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal by guard–ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, “Crystal Considerations with Dallas Real Time Clocks”. The DS83CH20 can also be driven by an external 32.768 KHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

KEYBOARD CONTROLLER PIN SUMMARY Table 2–8

SYMBOL	PIN	TYPE	FUNCTION
KBCLK	96	I/O	**Keyboard Clock Output.** Internally connected to the KBC’s T0 line.
KBDATA	97	I/O	**Keyboard Data Output.** Internally connected to the KBC’s P10 line.
MCLK	98	I/O	**Mouse Clock Output.** Internally connected to the KBC’s T1 line.
MDATA	99	I/O	**Mouse Data Output.** Internally connected to the KBC’s P11 line.
P12, P16/$\overline{KS}$, P17	100–102	I/O	**KBC I/O Port 1.** Quasi–bidirectional port for general purpose input and output. P16 can be programmed to serve the alternate function of a kickstart soft system power on input.
P20, P21	103–104	I/O	**KBC I/O Port 2.** Open drain port for general input/output.

GENERAL PURPOSE I/O PIN SUMMARY Table 2–9

SYMBOL	PIN	TYPE	FUNCTION
GP0[7..0]	147–154	I/O	**General Purpose I/O.** General Purpose I/O pin of I/O Port 0. These pins can be independently programmed as inputs or outputs, and can be individually isolated under software control.
GP1[3..0]	155–158	I/O	**General Purpose I/O.** General Purpose I/O pins of I/O Port 1. These pins can be independently programmed as inputs or outputs, and can be individually isolated under software control.

PROGRAMMABLE CHIP SELECT PIN SUMMARY Table 2–10

SYMBOL	PIN	TYPE	FUNCTION
$\overline{CSO}$, $\overline{CS1}$	159, 105	O	**Programmable Chip Selects.** $\overline{CS0}$ and $\overline{CS1}$ are programmable chip select and/or latch enable and/or output enable signals that can be used for such devices as a game port, I/O port expander, etc. The enabling/disabling, decoded address, and the assertion conditions are configured via the chip select configuration registers.

X–BUS BUFFER PIN SUMMARY Table 2–11

SYMBOL	PIN	TYPE	FUNCTION
XD[6..0]	64–70	I/O	**X–Bus Data I/O.** Provides a buffered interface between the System Data Bus (SD6–0) and devices on the X–Bus.
XD7	62	I/O	**X–Bus Data I/O.** Provides a buffered interface between the System Data Bus (SD7–0) and devices on the X–Bus. The frequency required for the CLK input is determined by the XD7 pin on reset; XD7 low selects 48 MHz; high selects 24 MHz.
$\overline{\text{XDIR}}$	71	I	**X–Bus Direction.** Used to control the data direction for transfers between the System Data Bus (SD7–0) and an external device on the X–Bus. A logic “1” on this pin sets the data direction for a write of data from SD7–0 to the X–bus, while a logic “0” sets the direction for read.
$\overline{\text{XE}}$	61	I	**X–Bus Enable.** Used to enable a data transfer between the System Data Bus (SD7–0) and an external device on the X–Bus.

2.2 PIN CHARACTERISTICS

Listed in the Table 2–12 is a summary of the pin characteristics. For each pin the table lists the functional block that it is associated with and the I/O buffer type field that describes the I/O buffer structure that is associated with the pin. An explanation of the I/O buffer type field is given in the notes section at the end of the table. Finally, the state of the pin during a reset state (RSTDRV=1) is given.

PIN CHARACTERISTICS Table 2–12

PIN	NAME	FUNCTIONAL BLOCK	I/O BUFFER TYPE	RESET STATE
1	GND			
2	SD7	ISA I/F	I/O12–6	High–Z
3	SD6	ISA I/F	I/O12–6	High–Z
4	SD5	ISA I/F	I/O12–6	High–Z
5	SD4	ISA I/F	I/O12–6	High–Z
6	SD3	ISA I/F	I/O12–6	High–Z
7	SD2	ISA I/F	I/O12–6	High–Z
8	SD1	ISA I/F	I/O12–6	High–Z
9	SD0	ISA I/F	I/O12–6	High–Z
10	$\overline{\text{PWR}}$	PWR CTRL	OD12	Unchanged
11	GND			
12	SA15	ISA I/F	I	Enabled
13	SA14	ISA I/F	I	Enabled
14	SA13	ISA I/F	I	Enabled
15	SA12	ISA I/F	I	Enabled
16	SA11	ISA I/F	I	Enabled
17	SA10	ISA I/F	I	Enabled
18	SA9	ISA I/F	I	Enabled

PIN	NAME	FUNCTIONAL BLOCK	I/O BUFFER TYPE	RESET STATE
19	SA8	ISA I/F	I	Enabled
20	SA7	ISA I/F	I	Enabled
21	SA6	ISA I/F	I	Enabled
22	SA5	ISA I/F	I	Enabled
23	SA4	ISA I/F	I	Enabled
24	SA3	ISA I/F	I	Enabled
25	SA2	ISA I/F	I	Enabled
26	SA1	ISA I/F	I	Enabled
27	SA0	ISA I/F	I	Enabled
28	V_{CC}			+5V
29	GND			
30	IRQ1	ISA I/F	I/O4–PB2/10K	High
31	IRQ3	ISA I/F	O12–6/OD12 (see note 1)	High–Z
32	IRQ4	ISA I/F	O12–6/OD12 (see note 1)	High–Z
33	IRQ5	ISA I/F	O12–6/OD12 (see note 1)	High–Z
34	IRQ6	ISA I/F	O12–6/OD12 (see note 1)	High–Z
35	IRQ7	ISA I/F	O12–6/OD12 (see note 1)	High–Z
36	$\overline{IRQ8}$	ISA I/F	O12–6 (see note 1)	Low
37	IRQ9	ISA I/F	O12–6/OD12 (see note 1)	High–Z
38	IRQ10	ISA I/F	O12–6/OD12 (see note 1)	High–Z
39	IRQ11	ISA I/F	O12–6/OD12 (see note 1)	High–Z
40	V_{CC}			+5V
41	GND			
42	IRQ12	ISA I/F	I/O4–PB2/10K	High
43	IRQ14	ISA I/F	O12–6/OD12 (see note 1)	High–Z
44	IRQ15	ISA I/F	O12–6/OD12 (see note 1)	High–Z

PIN	NAME	FUNCTIONAL BLOCK	I/O BUFFER TYPE	RESET STATE
45	DRQ3	ISA I/F	O12–6	High–Z
46	DRQ2	ISA I/F	O12–6	High–Z
47	DRQ1	ISA I/F	O12–6	High–Z
48	DRQ0	ISA I/F	O12–6	High–Z
49	DACK3	ISA I/F	I	Enabled
50	DACK2	ISA I/F	I	Enabled
51	DACK1	ISA I/F	I	Enabled
52	DACK0	ISA I/F	I	Enabled
53	CLK	CLOCK	ICLK	Enabled
54	RSTDRV	ISA I/F	IS	High
55	$\overline{\text{ZEROWS}}$	ISA I/F	OD12	High–Z
56	IOCHRDY	ISA I/F	OD12	High–Z
57	$\overline{\text{IOR}}$	ISA I/F	I	Enabled
58	$\overline{\text{IOW}}$	ISA I/F	I	Enabled
59	TC	ISA I/F	I	Enabled
60	AEN	ISA I/F	I	Enabled
61	$\overline{\text{XE}}$	X BUFFER	I	Enabled
62	XD7	X BUFFER	I/O4–2	High–Z
63	V_{CC}			+5V
64	XD6	X BUFFER	I/O4–2	High–Z
65	XD5	X BUFFER	I/O4–2	High–Z
66	XD4	X BUFFER	I/O4–2	High–Z
67	XD3	X BUFFER	I/O4–2	High–Z
68	XD2	X BUFFER	I/O4–2	High–Z
69	XD1	X BUFFER	I/O4–2	High–Z
70	XD0	X BUFFER	I/O4–2	High–Z
71	$\overline{\text{XDIR}}$	X BUFFER	I	Enabled
72	GND			
73	X2	RTC	IOSC	Enabled
74	X1	RTC	IOSC	Enabled
75	V_{BAT}	RTC		+3V
76	DRATE0	FLOPPY	OD40	High–Z
77	MSEN0	FLOPPY	IS	Enabled

PIN	NAME	FUNCTIONAL BLOCK	I/O BUFFER TYPE	RESET STATE
78	MSEN1	FLOPPY	IS	Enabled
79	$\overline{DR0}$	FLOPPY	OD40	High–Z
80	V_{CCTR}			+5V
81	GND			
82	$\overline{DR1}$	FLOPPY	OD40	High–Z
83	$\overline{MTR0}$	FLOPPY	OD40	High–Z
84	$\overline{MTR1}$	FLOPPY	OD40	High–Z
85	$\overline{WRDATA}$	FLOPPY	OD40	High–Z
86	$\overline{DIR}$	FLOPPY	OD40	High–Z
87	$\overline{STEP}$	FLOPPY	OD40	High–Z
88	$\overline{HDSEL}$	FLOPPY	OD40	High–Z
89	$\overline{WREN}$	FLOPPY	OD40	High–Z
90	DENSEL	FLOPPY	OD40	High–Z
91	$\overline{RDATA}$	FLOPPY	IS	Enabled
92	$\overline{TRK0}$	FLOPPY	IS	Enabled
93	$\overline{INDEX}$	FLOPPY	IS	Enabled
94	$\overline{WP}$	FLOPPY	IS	Enabled
95	$\overline{DSKCHG}$	FLOPPY	IS	Enabled
96	KBCLK	KBC	I/OD16–P10K	Low
97	KBDATA	KBC	I/OD16–P10K	Low
98	MCLK	KBC	I/OD16–P10K	Low
99	MDATA	KBC	I/OD16–P10K	Low
100	P12	KBC	I/O4–PB2/10K	High
101	P16	KBC	I/O4–PB2/10K	High
102	P17	KBC	I/O4–PB2/10K	High
103	P20	KBC	I/O4–PB2/10K	High
104	P21	KBC	I/O4–PB2/10K	High
105	$\overline{CS1}$	CHIP SELECT	O4–2	High–Z
106	IRTX	IR PORT	O4–2	Low
107	IRRX	IR PORT	IS	Enabled
108	V_{CC}			+5V
109	GND			
110	PD7	PARALLEL PORT	I/O14–14	Low

PIN	NAME	FUNCTIONAL BLOCK	I/O BUFFER TYPE	RESET STATE
111	PD6	PARALLEL PORT	I/O14–14	Low
112	PD5	PARALLEL PORT	I/O14–14	Low
113	PD4	PARALLEL PORT	I/O14–14	Low
114	PD3	PARALLEL PORT	I/O14–14	Low
115	PD2	PARALLEL PORT	I/O14–14	Low
116	PD1	PARALLEL PORT	I/O14–14	Low
117	PD0	PARALLEL PORT	I/O14–14	Low
118	BUSY	PARALLEL PORT	I	Enabled
119	$\overline{\text{STB/WRITE}}$	PARALLEL PORT	OD14 or O14–14 (see note 2)	High–Z
120	V_{CC}			+5V
121	GND			
122	$\overline{\text{ACK}}$	PARALLEL PORT	I	Enabled
123	SLCT	PARALLEL PORT	I	Enabled
124	PE	PARALLEL PORT	I	Enabled
125	$\overline{\text{ERROR}}$	PARALLEL PORT	I	Enabled
126	$\overline{\text{INIT}}$	PARALLEL PORT	OD14 or O14–14 (see note 2)	High–Z
127	$\overline{\text{SLCTIN}}$	PARALLEL PORT	OD14 or O14–14 (see note 2)	High–Z
128	$\overline{\text{AUTOFD}}$	PARALLEL PORT	OD14 or O14–14 (see note 2)	High–Z
129	$\overline{\text{CTSA}}$	SERIAL PORT A	I	Enabled
130	$\overline{\text{DCDA}}$	SERIAL PORT A	I	Enabled
131	$\overline{\text{DSRA}}$	SERIAL PORT A	I	Enabled
132	$\overline{\text{DTRA}}$	SERIAL PORT A	O4–2	High
133	$\overline{\text{RIA}}$	SERIAL PORT A	I	High
134	$\overline{\text{RTSA}}$	SERIAL PORT A	O4–2	High
135	V_{CC}			+5V
136	GND			
137	SINA	SERIAL PORT A	I	Enabled
138	SOUTA	SERIAL PORT A	O4–2	High
139	$\overline{\text{CTSB}}$	SERIAL PORT B	I	Enabled
140	$\overline{\text{DCDB}}$	SERIAL PORT B	I	Enabled
141	$\overline{\text{DSRB}}$	SERIAL PORT B	I	Enabled
142	$\overline{\text{DTRB}}$	SERIAL PORT B	O4–2	High
143	$\overline{\text{RIB}}$	SERIAL PORT B	I	High
144	$\overline{\text{RTSB}}$	SERIAL PORT B	O4–2	High

PIN	NAME	FUNCTIONAL BLOCK	I/O BUFFER TYPE	RESET STATE
145	SINB	SERIAL PORT B	I	Enabled
146	SOUTB	SERIAL PORT B	O4–2	High
147	GP07	GPIO	I/OD4–P10K	High–Z
148	GP06	GPIO	I/OD4–P10K	High–Z
149	GP05	GPIO	I/OD4–P10K	High–Z
150	GP04	GPIO	I/OD4–P10K	High–Z
151	GP03	GPIO	I/OD4–P10K	High–Z
152	GP02	GPIO	I/OD4–P10K	High–Z
153	GP01	GPIO	I/OD4–P10K	High–Z
154	GP00	GPIO	I/OD4–P10K	High–Z
155	GP13	GPIO	I/OD4–P10K	High–Z
156	GP12	GPIO	I/OD4–P10K	High–Z
157	GP11	GPIO	I/OD4–P10K	High–Z
158	GP10	GPIO	I/OD4–P10K	High–Z
159	$\overline{CS0}$	CHIP SELECT	O4–2	High–Z
160	V_{CC}			+5V

NOTES:

1. The IRQ3–7, 9–11, 12, 14, and 15 pins can be programmed as open drain or totem–pole outputs.
2. $\overline{AUTOFD}$, $\overline{INIT}$, $\overline{SLCTIN}$, and $\overline{STB}$/$\overline{WRITE}$ have output structures which are configured as open–drain when ISA–or PS/2– compatible parallel port operating modes are selected. When any other parallel port mode is selected the output structures are push–pull.

PIN (I/O BUFFER) TYPE DESCRIPTIONS

I – Input
ICLK – Clock input
IOSC – Oscillator input
IS – Schmitt input
I/O04–PB2/10K – Pseudo–bidirectional I/O; 4 mA sink, –2 mA source (for 10 ns on low to high transition), 10 KΩ min. pull–up
O4–2 – Totem–pole output; 4 mA sink, –2 mA source
O12–6 – Totem–pole output; 12 mA sink, 6 mA source
O14–14 – Totem–pole output; 14 mA sink, –14 mA source
OD12 – Open drain output, 12 mA sink
OD14 – Open drain output, 14 mA sink
OD40 – Open drain Output; 40 mA sink, –4 mA source
OD4–P10K – Open–drain Output, 4 mA sink, 10KΩ min. pull–up
OD16–P10K– Open–drain Output, 16 mA sink, 10KΩ min. pull–up

PIN STATE DESCRIPTIONS

High–Z – High Impedance
Enabled – Power applied; electrically functioning input
Unchanged – Previous state not affected

3.0 CHIP CONFIGURATION

The configuration of the I/O resources of the DS83CH20 is very flexible and is optimized for design in Plug and Play compatible motherboards in which the resources required by their components are known. With its flexible resource allocation architecture, the DS83CH20 allows the BIOS to assign resources at POST.

3.1 CONFIGURATION REGISTER OVERVIEW

The configuration of the DS83CH20 is controlled via a series of registers which are accessed via an index and data register pair are located within the ISA I/O memory map at locations 02EH, and 02FH, respectively.

A summary of the DS83CH20 chip configuration registers is given in Table 3–1.

DS83CH20 CONFIGURATION REGISTER SUMMARY Table 3–1

INDEX ADDRESS	TYPE	RESET VALUE	CONFIGURATION REGISTER
002H	R/W	FCH	FDC Enable
003H	R/W	C0H	FDC Mode
006H	R/W	A6H	FDC Resource Select
007H	R/W	F8H	Parallel Port Enable
008H	R/W	00H	Parallel Port Mode
009H	R/W	00H	Parallel Port Base Address Select
00BH	R/W	40H	Parallel Port Resource Select
00CH	R/W	F8H	UART A Enable
00DH	R/W	FEH	UART A Mode
00EH	R/W	00H	UART A Base Address Select
010H	R/W	F0H	UART A Resource Select
011H	R/W	F8H	UART B Enable
012H	R/W	C4H	UART B Mode
013H	R/W	00H	UART B Base Address Select
015H	R/W	F0H	UART B Resource Select
016H	R/W	FCH	RTC Enable
018H	R/W	C0H	KBC Enable
01AH	R/W	00H	Chip Select Enable
01BH	R/W	00H	CS0 Lower Base Address/Range Select
01CH	R/W	00H	CS0 Upper Base Address Select
01DH	R/W	00H	CS1 Lower Base Address/Range Select
01EH	R/W	00H	CS1 Upper Base Address Select
020H	R	20H	Model Byte
022H	R/W	00H	GP0,1 Enable
023H	R/W	00H	GP0,1 Base Address Select

INDEX ADDRESS	TYPE	RESET VALUE	CONFIGURATION REGISTER
025H	R/W	00H	GP0 Data Direction
026H	R/W	00H	GP0 Isolation Control
027H	R/W	F0H	GP1 Data Direction
028H	R/W	F0H	GP1 Isolation Control
029H	R/W	N/A	Kickstart Source Select
02AH	R/W	N/A	Kickstart Source Status
30H	R/W	31H	IRQ8–15 Open Drain Control
31H	R/W	07H	IRQ2–7 Open Drain Control

A detailed description of each of the configuration registers is given the tables below. Unless otherwise noted, “RESET VALUE” refers to the initialized state of the register which results when the RSTDRV signal is applied.

3.2 FLOPPY DISK CONTROLLER

Table 3–2 is a description of the configuration registers for the floppy disk controller.

FLOPPY DISK CONFIGURATION TABLE 3–2

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
FDC Enable	002H, R/W	FCH	Bit [0]	FDC Enable
				= 0 FDC disabled from memory map and in power down
				= 1 FDC enabled; (FDC out of power down; s/w reset required to initialize.)
			Bit [1]	Reserved, read as 0.
			Bit [7:2]	Reserved, read as 1's
FDC Mode	003H, R/W	C0H	Bit [0]	TDR Mode
				= 0 AT Compatible TDR
				= 1 Enhanced Floppy Mode 2
			Bit [2:1]	Interface Mode
				= 00 AT Mode
				= 01 (Reserved)
				= 10 (Reserved)
				= 11 PS/2
			Bit [3]	Secondary FDC Base I/O Addr. Select
				= 0 Primary FDC Addr. selected (03F0–03F7H)
				= 1 Secondary FDC Addr. selected (0370–0377H)
			Bit [4]	Drive Mapping Enable
				= 0 Drive map disabled
				= 1 Drive map enabled; selection via Drive Map 1,0 bits in TDR.
			Bit [5]	Density Select Polarity Bit (inverse)
				= 0 DENSEL pin is active low for 500K bps or 1 Mbps data rates
				= 1 DENSEL pin is active high for 500K bps or 1 Mbps data rates
			Bit [7:6]	Reserved, read as 1's

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
FDC Resource Select	006H, R/W	A6H	Bit [3:0]	Interrupt channel assignment
				= 0000 No interrupt assigned
				= 0001 Reserved
				= 0010 Reserved
				= 0011 IRQ3
				= 0100 IRQ4
				= 0101 IRQ5
				= 0110 IRQ6
				= 0111 IRQ7
				= 1000 Reserved
				= 1001 IRQ9
				= 1010 IRQ10
				= 1011 IRQ11
				= 1100 Reserved
				= 1101 Reserved
				= 1110 IRQ14
				= 1111 IRQ15
			Bit [6:4]	DMA channel assignment
				= 000 DMA0
				= 001 DMA1
				= 010 DMA2
				= 011 DMA3
				= 1XX No DMA channel assigned
			Bit [7]	Reserved, read as 1

3.3 PARALLEL PORT

Table 3–3 is a description of the configuration registers for the parallel port.

PARALLEL PORT CONFIGURATION Table 3–3

REGISTER	INDEX ADDRESS	RESET VALUE	DESCRIPTION	
Parallel Port Enable	007H, R/W	F8H	Bit [0]	Parallel Port Enable
				= 0 Parallel port disabled from memory map and in power down
				= 1 Parallel port enabled
			Bit [1]	Parallel Port Auto–Power Management Enable
				= 0 Auto–power Management disabled
				= 1 Auto–power Management enabled
			Bit [2]	Parallel Port Leakage Control
				= 0 Parallel port pins in normal operation during power down
				= 1 Parallel port output pins in High–Z; input pins disabled during power down
			Bit [7:3]	Reserved, read as 1's
Parallel Port Mode	008H, R/W	00H	Bit [2:0]	Mode Select
				= 000 ISA Compatible*
				= 001 PS/2 Compatible**
				= 010 EPP–1.7 and ISA Compatible
				= 011 EPP–1.9 and ISA Compatible
				= 100 ECP Mode
				= 101 Reserved
				I I
				= 111 Reserved
			Bit [6:3]	FIFO Threshold Value
				= 0000 FIFO Threshold = 1
				= 0001 FIFO Threshold= 2
				I I
				= 1111 FIFO Threshold= 16
			Bit [7]	$\overline{\text{ZEROWS}}$ Enable
				= 0 Disabled
				= 1 Enabled

* Also known as standard parallel port (SPP) mode.

** Also know as bi–directional mode.

REGISTER	INDEX ADDRESS	RESET VALUE	DESCRIPTION	
Parallel Port Base Address Select	009H, R/W	00H	Bit [7:0]	Sets base I/O range: 100H: 4FCH on 8–byte boundaries. Base I/O address = (8 x Bit [7:0] value) + 100H
Parallel Port Resource Select	00BH, R/W	40H	Bit [3:0]	Interrupt channel assignment = 0000 No interrupt assigned = 0001 Reserved = 0010 Reserved = 0011 IRQ3 = 0100 IRQ4 = 0101 IRQ5 = 0110 IRQ6 = 0111 IRQ7 = 1000 Reserved = 1001 IRQ9 = 1010 IRQ10 = 1011 IRQ11 = 1100 Reserved = 1101 Reserved = 1110 IRQ14 = 1111 IRQ15
			Bit [6:4]	DMA channel assignment = 000 DMA0 = 001 DMA1 = 010 DMA2 = 011 DMA3 = 1XX No DMA channel assigned
			Bit [7]	Parallel Port IRQ polarity = 0 Active Low IRQ =1 Active High IRQ

3.4 UART A

Table 3–4 is a description of the configuration registers for UART A.

UART A CONFIGURATION Table 3–4

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
UART A Enable	00CH, R/W	F8H	Bit [0]	UART A Enable
				= 0 UART A disabled from memory map and in power down
				= 1 UART A enabled
			Bit [1]	UART A Auto–Power Management Enable
				= 0 Auto–power management disabled
				= 1 Auto–power management enabled
			Bit [2]	UART A Leakage Control
				= 0 UART A pins in normal operation during power down
				= 1 UART A output pins in High–Z; input pins disabled during power down
			Bit [7:3]	Reserved; read as 1’s
UART A Mode	00DH, R/W	FEH	Bit [0]	Test mode enable
				= 0 Test mode disabled
				= 1 Test mode enabled
			Bit [7:1]	Reserved; read as 1’s

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
UART A Base Address Select	00EH, R/W	00H	Bit [7:0]	Sets base I/O range: 100H:8F8H on 8–byte boundaries. Base I/O address = (8 x Bit [7:0] value) + 100H
UART A Resource Select	010H, R/W	F0H	Bit [3:0]	Interrupt channel assignment = 0000 No interrupt assigned = 0001 Reserved = 0010 Reserved = 0011 IRQ3 = 0100 IRQ4 = 0101 IRQ5 = 0110 IRQ6 = 0111 IRQ7 = 1000 Reserved = 1001 IRQ9 = 1010 IRQ10 = 1011 IRQ11 = 1100 Reserved = 1101 Reserved = 1110 IRQ14 = 1111 IRQ15
			Bit [7:4]	Reserved; read as 1’s

3.5 UART B

Table 3–5 is a description of the configuration registers for UART B.

UART B CONFIGURATION Table 3–5

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
UART B Enable	011H, R/W	F8H	Bit [0]	UART B Enable
				= 0 UART B disabled from memory map and in power down
				= 1 UART B enabled
			Bit [1]	UART B Auto–Power Management Enable
				= 0 Auto–power management disabled
				= 1 Auto–power management enabled
			Bit [2]	UART B Leakage Control
				= 0 UART B pins in normal operation during power down
				= 1 UART B output pins in High–Z; input pins disabled during power down
			Bit [7:3]	Reserved; read as 1's
UART B Mode	012H, R/W	C4H	Bit [0]	Test mode enable
				= 0 Test mode disabled
				= 1 Test mode enabled
			Bit [1]	Infrared Enable
				= 0 UART B input/output via SINB, SOUTB
				= 1 UART B input/output via IRRX, IRTX
			Bit [2]	IR Duplex Select
				= 0 Full duplex when IR enabled
				= 1 Half duplex when IR enabled
			Bit [5:3]	IR Mode Select
				= 000 IRDA 1.0 – 1.6 µs bit pulse width
				= 001 IRDA 1.0 – 3/16 bit pulse width
				= 010 ASK–IR (Sharp; active low)
				= 011–111 Reserved
			Bit [7:6]	Reserved; read as 1's
UART B Base Address Select	013H, R/W	00H	Bit [7:0]	Sets base I/O range: 100H:8F8H
				on 8–byte boundaries.
				Base I/O address =
				(8 x Bit [7:0] value) + 100H

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
UART B Resource Select	015H, R/W	F0H	Bit [3:0]	Interrupt channel assignment
				= 0000 No interrupt assigned
				= 0001 Reserved
				= 0010 Reserved
				= 0011 IRQ3
				= 0100 IRQ4
				= 0101 IRQ5
				= 0110 IRQ6
				= 0111 IRQ7
				= 1000 Reserved
				= 1001 IRQ9
				= 1010 IRQ10
				= 1011 IRQ11
				= 1100 Reserved
				= 1101 Reserved
				= 1110 IRQ14
				= 1111 IRQ15
			Bit [7:4]	Reserved; read as 1's

3.6 RTC

Table 3–6 is a description of the configuration registers for the RTC.

RTC CONFIGURATION Table 3–6

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
RTC Enable	016H, R/W	FCH	Bit [0]	RTC Enable
				= 0 RTC disabled from memory map and in power down; $\overline{\text{IRQ8}}$ in High–Z
				= 1 RTC enabled; $\overline{\text{IRQ8}}$ enabled
			Bit [1]	IRQ8 polarity
				= 0 IRQ8: active low
				= 1 IRQ8: active high
			Bit [7:2]	Reserved; read as 1's

3.7 KEYBOARD CONTROLLER

Table 3–7 is a description of the configuration registers for the keyboard controller.

KEYBOARD CONTROLLER CONFIGURATION Table 3–7

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
KBC Enable	018H, R/W	C0H	Bit [0]	KBC Enable
				= 0 KBC disabled from memory map and in power down
				= 1 KBC enabled
			Bit [1]	KBC Leakage Control
				= 0 KBC pins in normal operation during power down
				= 1 KBC output pins in High–Z; input pins blocked during power down
			Bit [2]	KBC Clock Speed
				= 0 8 MHz
				= 1 12 MHz
			Bit [3]	IRQ1 High–Z control
				= 0 IRQ1 is driven
				= 1 IRQ1 in High–Z
			Bit [4]	IRQ12 High–Z control
				= 0 IRQ12 is driven
				= 1 IRQ12 in High–Z
			Bit [5]	IRQ1/12 Fast Latch enable
				= 0 Fast latching disabled
				= 1 Fast latching enabled
			Bit [7:6]	Reserved; read as 1's

3.8 PROGRAMMABLE CHIP SELECT

Table 3–8 is a description of the configuration registers for the programmable chip select.

PROGRAMMABLE CHIP SELECT CONFIGURATION Table 3–8

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
Chip Select Enable	01AH, R/W	F0H	Bit [0]	CS0 Enable
				= 0 CS0 function disabled
				= 1 CS0 function enabled
			Bit [1]	CS0 Leakage Control
				= 0 CS0 pin enabled
				= 1 CS0 in High–Z
			Bit [2]	CS1 Enable
				= 0 CS1 function disabled
				= 1 CS1 function enabled
			Bit [3]	CS1 Leakage Control
				= 0 CS1 pin enabled
				= 1 CS1 in High–Z
			Bit [4:7]	Reserved; Read as 1's
CS0 Lower Base Address/ Range Select	01BH, R/W	03H	Bit [1:0]	Reserved; Read as 1's
			Bit [3:2]	Sets CS0 decode range (boundary):
				= 00 16 bytes
				= 01 64 bytes
				= 10 256 bytes
				= 11 1K bytes
			Bit [7:4]	Least significant 4–bits of CS0 base address on n–byte boundaries
CS0 Upper Base Address Select	01CH, R/W	00H	Bit [7:0]	Most significant 8–bits of CS0 base address on n–byte boundaries
CS1 Lower Base Address/ Range Select	01DH, R/W	03H	Bit [1:0]	Reserved; Read as 1's
			Bit [3:2]	Sets CS1 decode range (boundary):
				= 00 16 bytes
				= 01 64 bytes
				= 10 256 bytes
				= 11 1K bytes
			Bit [7:4]	Least significant 4–bits of CS1 base address on n–byte boundaries
CS1 Upper Base Address Select	01EH, R/W	00H	Bit [7:0]	Most significant 8–bits of CS1 base address on n–byte boundaries

3.9 MODEL BYTE

Table 3–9 is a description of the model byte. The model byte is used to identify the device type and revision of the DS83CH20.

MODEL BYTE Table 3–9

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
Model Byte	020H, R	20H	Bit [7:0]	Identifies the device as a DS83CH20

3.10 GENERAL PURPOSE I/O

Table 3–10 is a description of the configuration registers for the general purpose I/O.

GENERAL PURPOSE I/O CONFIGURATION Table 3–10

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
GP0,1 Enable	022H, R/W	FCH	Bit [0]	GP0 Enable
				= 0 GP0 disabled from memory map and in power down
				= 1 GP0 enabled
			Bit [1]	GP1 Enable
				= 0 GP1 disabled from memory map and in power down
				= 1 GP1 enabled
			Bit [2:7]	Reserve; Read as 1’s
GP0,1 Base Address Select	023H, R/W	00H	Bit [7:0]	Sets base I/O address: 000H:1FEH
				on 2–byte boundaries.
				GP0 base addr. = (2 x Bit [7:0] value)
				GP1 base addr. = (2 x Bit [7:0] value) + 1
GP0 Data Direction	025H, R/W	00H	Bit [7:0]	Controls data direction for associated GP0 line.
				= 0 Input
				= 1 Output
GP0 Isolation Control	026H, R/W	00H	Bit [7:0]	Controls isolation for associated GP0 line.
				= 0 Normal operation
				= 1 High–Z selected

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
GP1 Data Direction	027H, R/W	F0H	Bit [3:0]	Controls data direction for associated GP1 line. = 0 Input = 1 Output
			Bit [7:4]	Reserved; read as 1's
GP1 Isolation Control	028H, R/W	F0H	Bit [3:0]	Controls isolation for associated GP1 line. = 0 Normal operation = 1 High–Z selected
			Bit [7:4]	Reserved; read as 1's

3.11 KICKSTART SOURCE SELECT

Table 3–11 is a description of the kickstart source select configuration register. All of the bits in this register are powered via the V_{CCTR} pin. They are therefore maintained when V_{CC} is absence so long as a power source is applied to V_{CCTR}.

KICKSTART SOURCE SELECT Table 3–11

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
Kickstart Source Select	029H, R/W	N/A*	Bit [0]	KBC P16 kickstart source select = 0 KBC P16 disabled = 1 KBC P16 enabled
			Bit [1]	UART A $\overline{RIA}$ kickstart source select = 0 UART A $\overline{RIA}$ disabled = 1 UART A $\overline{RIA}$ enabled
			Bit [2]	UART B $\overline{RIB}$ kickstart source select = 0 UART B $\overline{RIB}$ disabled = 1 UART B $\overline{RIB}$ enabled
			Bit [3]	IRRX kickstart source select = 0 IRRX disabled = 1 IRRX enabled
			Bit [7:4]	Reserved, read as 1

* When power is applied for the first time, via V_{CCTR} or V_{BAT}, this register is initialized to a value of F1H.

3.12 KICKSTART STATUS

Table 3–12 is a description of the kickstart status configuration register. Each status bit indicates whether or not the specified kickstart source caused a kickstart condition. In order for one of these bits to be set, its associated kickstart source bit must have been enabled and a successful kickstart sequence must have been completed as a result of a transition on the specified pin.

KICKSTART STATUS Table 3–12

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
Kickstart Status	02AH, R/W	N/A*	Bit [0]	KBC P16 status
				= 0 KBC P16 did not kickstart
				= 1 KBC P16 kickstart occurred
			Bit [1]	UART A $\overline{RIA}$ status
				= 0 UART A $\overline{RIA}$ did not kickstart
				= 1 UART A $\overline{RIA}$ kickstart occurred
			Bit [2]	UART B $\overline{RIB}$ status
				= 0 UART B $\overline{RIB}$ did not kickstart
				= 1 UART B $\overline{RIB}$ kickstart occurred
			Bit [3]	IRRX status
				= 0 IRRX did not kickstart
				= 1 IRRX kickstart occurred
			Bit [7:4]	Reserved, read as 1

Note: Bits [0–3] must be written to a 0 to clear the status condition.

3.13 IRQ OUTPUT CONFIGURATION

IRQ OUTPUT CONFIGURATION Table 3–13

REGISTER	ADDRESS	RESET VALUE	DESCRIPTION	
IRQ9–15 Open Drain Control	030H, R/W	31	Bit [0]	Reserved, Read As 1
			Bit [1]	IRQ9 Output Control
				= 0 Totem–pole output
				= 1 Open drain output
			Bit [2]	IRQ10 Output Control
				= 0 Totem–pole output
				= 1 Open drain output
			Bit [3]	IRQ11 Output Control
				= 0 Totem–pole output
				= 1 Open drain output
			Bit [4]	Reserved, Read As 1
			Bit [5]	Reserved, Read As 1
			Bit [6]	IRQ14 Output Control
				= 0 Totem–pole output
				= 1 Open drain output
			Bit [7]	IRQ15 Output Control
				= 0 Totem–pole output
				= 1 Open drain output
IRQ3–7 Open Drain Control	031H, R/W	07	Bit [0]	Reserved, Read As 1
			Bit [1]	Reserved, Read As 1
			Bit [2]	Reserved, Read As 1
			Bit [3]	IRQ3 Output Control
				= 0 Totem–pole output
				= 1 Open drain output
			Bit [4]	IRQ4 Output Control
				= 0 Totem–pole output
				= 1 Open drain output
			Bit [5]	IRQ5 Output Control
				= 0 Totem–pole output
				= 1 Open drain output
			Bit [6]	IRQ6 Output Control
				= 0 Totem–pole output
				= 1 Open drain output
			Bit [7]	IRQ7 Output Control
				= 0 Totem–pole output
				= 1 Open drain output

4.0 FLOPPY DISK CONTROLLER

4.1 OVERVIEW

The DS83CH20 incorporates an industry standard floppy disk controller (FDC) core and interface circuitry required in IBM PC compatible systems. Figure 4–1 is a block diagram of the FDC. Key features include:

- IBM System 3740 format
- IBM System 34 format
- Perpendicular recording format
- Data rates up to 1 Mbps
- Directly addresses 256 tracks
- 255 step recalculate command
- Programmable write precompensation
- 16 byte FIFO
- PS/2 diagnostic register support
- Enhanced power saving features
- High performance digital data separator

The FDC supports the standard PC data rates of 250, 300, 500 Kbps, and 1 Mbps in MFM encoded data mode, but is not guaranteed through functional testing to support the older FM encoded data mode. References to the older FM mode are in this document to clarify the true functional operation of the device.

The 1 Mbps data rate is used by the high performance tape and floppy drives emerging in the PC market today. The new floppy drives utilize high density media, which require the FDC supported, perpendicular recording mode format. When used with the 1 Mbps data rate this new format allows the use of 4 Mbyte floppy drives which format ED media to 2.88 Mbyte capacity.

Power saving features which are software compatible with the 82077SL are supported. These include clock disable, immediate auto powerdown, low latency awakening and a power saving state for the write precompensator.

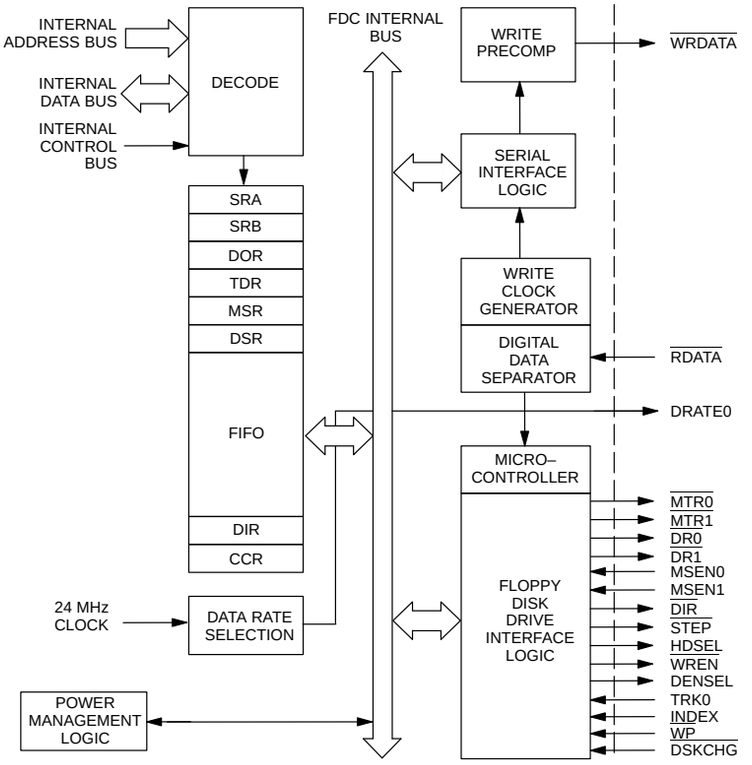
The FDC also contains multiplexors for swapping the default drive control outputs under software control.

The high performance digital data separator needs no external components, and is compatible with the strict data separator requirements of floppy and floppy tape drives.

The FDC contains write precompensation circuitry that defaults to 125 ns for 250, 300, and 500 Kbps (41.67 ns at 1 Mbps). These values can be overriden in software to disable write precompensation or to provide levels of precompensation up to 250 ns.

The internal 40 mA open drain disk interface buffers are compatible with both CMOS drive inputs and 150 ohm resistor terminated disk drive inputs.

FLOPPY DISK CONTROLLER BLOCK DIAGRAM Figure 4–1



4.2 FDC REGISTER DESCRIPTION

FDC REGISTER SUMMARY Table 4–1

A2	A1	A0	R/W	REGISTER	
0	0	0	R	Status Register A	SRA
0	0	1	R	Status Register B	SRB
0	1	0	R/W	Digital Output Register	DOR
0	1	1	R/W	Tape Drive Register	TDR
1	0	0	R	Main Status Register	MSR
1	0	0	W	Data Rate Select Register	DSR
1	0	1	R/W	Data Register (FIFO)	FIFO
1	1	0	X	None (High–Z)	
1	1	1	R	Digital Input Register	DIR
1	1	1	W	Configuration Control Register	CCR

In the following sections, the powerdown state of the various registers is given. The following notation is used:

UC A value is returned without change from the active mode.

***** The value is reflecting the actual status of the FDC, but the value is determinable in the power–down state.

N/A Reflects the values of the pins indicated.

X Value is undefined.

4.2.1 Status Register A (SRA)

This read only diagnostic register is part of the PS/2 floppy controller register set and is enabled when in the PS/2 mode. The assigned IRQ and DRQ pins are monitored as well as some of the disk interface signals. The SRA can be read at any time when in PS/2 mode. In PC–AT mode, D7–D0 are High–Z during a read.

	D7	D6	D5	D4	D3	D2	D1	D0
Description	IRQ	RES	STEP	$\overline{\text{TRK0}}$	HDSEL	$\overline{\text{INDEX}}$	$\overline{\text{WP}}$	DIR
H/W Reset	0	0	0	N/A	0	N/A	N/A	0
Auto PD	0*	UC	0*	1	0*	1	1	0*

D7 **IRQ – Interrupt Pending.** This active high status bit reflects the state of the assigned IRQ line.

D6 **RES – Reserved.**

D5 **STEP – Step Input Status.** Active high status of the STEP disk interface output.

D4 **$\overline{\text{TRK0}}$ – Track 0 Input Status.** Active low status of the TRK0 disk interface input.

D3 **HDSEL – Head Select Status.** Active high status of the HDSEL disk interface output.

D2 **$\overline{\text{INDEX}}$ – Index Status**. Active low status of the INDEX disk interface input.

D1 **$\overline{\text{WP}}$ – Write Protect Status.** Active low status of the $\overline{\text{WP}}$ disk interface input.

D0 **DIR – Direction Status**. Active high status of the $\overline{\text{DIR}}$ disk interface output.

4.2.2 Status Register B (SRB)

This read–only diagnostic register is part of the PS/2 floppy controller register set, and is enabled when in the PS/2 mode. SRB can be read at any time when the PS/2 mode is selected. In the PC–AT mode, D7–D0 are High–Z during a read.

	D7	D6	D5	D4	D3	D2	D1	D0
Description	1	1	DSEL0	WDATA	RDATA	WREN	MTR1	MTR0
H/W Reset	1	1	0	0	0	0	0	0
Auto PD	1	1	UC	0	0	0*	0	0

D7 **Reserved.** Always 1.

D6 **Reserved.** Always 1.

D5 **DSEL0 – Drive Select 0.** Active high status of the DOR Drive select 0 bit.

D4 **WDATA – Write Data.** This bit changes state (is toggled) for every positive edge output on the $\overline{\text{WRDATA}}$ pin.

D3 **RDATA – Read Data.** This bit changes state (is toggled) for every positive edge detected on the $\overline{\text{RDATA}}$ pin.

D2 **WREN – Write Enable.** This bit will be a one when the $\overline{\text{WREN}}$ output is active low.

D1 **MTR1 – Motor 1 Enable.** This bit will be a one when the $\overline{\text{MTR1}}$ output is active low.

D1 **MTR0 – Motor 0 Enable.** This bit will be a one when the $\overline{\text{MTR0}}$ output is active low.

4.2.3 Digital Output Register (DOR)

The DOR controls the drive select and motor enable disk interface outputs, enables the DMA logic, and contains a software reset bit. The contents of the DOR is cleared to 00H after a hardware reset, and is unaffected by a software reset. The DOR can be written to at any time.

	D7	D6	D5	D4	D3	D2	D1	D0
Description	ME3	ME2	ME1	ME0	DMAEN	RESET	DSEL1	DSEL0
H/W Reset	0	0	0	0	0	0	0	0
Auto PD	0*	0*	0*	0*	UC	1*	UC	UC

D7 **ME3 – Motor Enable 3.** This bit controls the internal motor 3 disk interface output signal, which is unconnected to a pin in the DS83CH20.

D6 **ME2 – Motor Enable 2.** This bit controls the internal motor 2 disk interface output signal, which is unconnected to a pin in the DS83CH20.

D5 **ME1 – Motor Enable 1.** This bit controls the motor 1 disk interface output signal, which is connected to the $\overline{\text{MTR1}}$ pin. A one in this bit causes $\overline{\text{MTR1}}$ to go active.

D4 **ME0 – Motor Enable 0.** This bit controls the motor 0 disk interface output signal, which is connected to the $\overline{\text{MTR0}}$ pin. A one in this bit causes $\overline{\text{MTR0}}$ to go active.

D3 **DMAEN – DMA Enable.** This bit has two modes of operation:

PC–AT mode: Writing a 1 to this bit enables the software assigned DRQ, $\overline{\text{DACK}}$, and IRQ pins as well as the TC pin. Writing a 0 to this bit disables the assigned $\overline{\text{DACK}}$ and TC pins and places the assigned DRQ and IRQ pins in a High–Z state. This bit is a 0 following a reset in this mode.

PS/2 mode: This bit is reserved, and the software assigned DRQ, $\overline{\text{DACK}}$, and IRQ pins as well as the TC pin is always enabled. During a reset, the assigned DRQ, $\overline{\text{DACK}}$, TC, and IRQ lines remain enabled, and D3 is 0.

D2 **RESET – Software Reset.** Writing a 0 to this bit resets the FDC. It remains in the reset condition until a one is written to this bit. A software reset will reset the status registers and clears the POWER DOWN and S/W RESET in the DSR control register. It does not affect the contents of the CCR and the reset of the DOR and DSR control register. The Configure command bits are affected (See FDC Command Set description).

D1, D0 DSEL1, 0 – Drive Select. These two bits are binary encoded for four possible drive selects, DR0–DR3, so that only one drive select output is active at a time. Table 4–2 lists the DOR values to activate the drive select and motor enable for each drive. See also logical drive exchange. DR2 and DR3 are not connected to pins on the DS83CH20.

DRIVE ACTIVATION VALUES Table 4–2

DRIVE	DOR VALUE
0	1CH
1	2DH
2	4EH
3	8FH

4.2.4 Tape Drive Register (TDR)

The TDR register is the Tape Drive Register and the floppy disk controller media and drive type register. The register has two modes of operation, as selected via the FDC Mode configuration register.

1) At–Compatible Mode:
The register is used to assign a particular drive number to the tape drive support mode of the data separator. All other logical drives can be assigned as floppy drive support. Bits 2–7 are High–Z during read.

	D7	D6	D5	D4	D3	D2	D1	D0
Description	X	X	X	X	X	X	TSEL1	TSEL0
H/W Reset	X	X	X	X	X	X	0	0
Auto PD	X	X	X	X	X	X	UC	UC

D7–D2Reserved. Read as High–Z

D1–D0TSEL1,0; Tape Drive Select. These bits assign a logical drive number to a tape drive. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive. The assignment is made according to the following table:

TSEL1	TSEL0	LOGICAL DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

2) Enhanced Floppy Mode 2:
This is the PS/2 TDR mode. Additional bits are used for operation with PS/2 floppy drives.

	D7	D6	D5	D4	D3	D2	D1	D0
Description	MSEN1	MSEN0	0	0	DMAP1	DMAP0	TSEL1	TSEL0
H/W Reset	UC	UC	0	0	0	0	0	0
Auto PD	0	0	0	0	0	0	UC	UC

D7,D6 MSEN1,0 Media Sense 1,0. These bits are used to read the state of the MSEN1 and MSEN0 pins, respectively, to allow the firmware to automatically identify the media type. The media ID field is decoded as follows:

MSEN1	MSEN0	MEDIA TYPE
0	0	5.25 ”
0	1	2.88 Mbyte
1	0	1.44 Mbyte
1	1	720 Kbyte

D5 Reserved. Returns 0 on read.

D4 Reserved. Returns 0 on read.

D3,2 DMAP1,0; Drive Map Select. When drive mapping is enabled via the Drive Map enable bit in the FDC Mode configuration register, DMAP1 and 0 can be used to determine the mapping of internal logical drive control signals onto the physical drive output pins: $\overline{DR1}$, $\overline{DR0}$, $\overline{MTR1}$, and $\overline{MTR0}$. As a result, internal Drive 0 control signals can be swapped with another drive, thus changing the physical default drive. The following table defines the mapping of the drives; upper case signal names refer to the pin names and lower case names refer to logical signals.

DRIVE MAP ENABLE	DMAP1	DMAP0	DEFAULT DRIVE	PHYSICAL MOTOR ENABLE		PHYSICAL DRIVE ENABLE	
0	X	X	0	$\overline{mtr1}$	$\overline{mtr0}$	$\overline{dr1}$	$\overline{dr0}$
1	0	0	0	$\overline{mtr1}$	$\overline{mtr0}$	$\overline{dr1}$	$\overline{dr0}$
1	0	1	1	$\overline{mtr0}$	$\overline{mtr1}$	$\overline{dr0}$	$\overline{dr1}$
1	1	0	2	$\overline{mtr1}$	$\overline{mtr2}$	$\overline{dr1}$	$\overline{dr2}$
1	1	1	3	$\overline{mtr1}$	$\overline{mtr3}$	$\overline{dr1}$	$\overline{dr3}$

D1,0 TSEL1,0; Tape Drive Select. These bits assign a logical drive number to a tape drive. Operation is the same as described for PC AT compatible mode, described above.

4.2.5 Main Status Register (MSR)

The read–only Main Status register indicates the current status of the disk FDC. The Main Status Register is always available to be read. One of its functions is to control the flow of data to and from the Data Register (FIFO). The MSR indicates when the disk controller is ready to send or receive data through the Data Register. It should be read before each byte is transferred to or from the Data Register except during a DMA transfer. No delay is required when reading this register after a data transfer.

After a hardware or software reset, or recovery from a power down state, the Main Status Register is immediately available to be read by the host µP. It contains a value of 00 hex until the internal registers have been initialized. When the FDC is ready to receive a new command, it reports an 80H to the µP. The system software can poll the MSR until it is ready. The worst case time allowed for the MSR to report an 80H value (RQM set) is 2.5 µs after reset or power up.

	D7	D6	D5	D4	D3	D2	D1	D0
Description	RQM	DIO	NDM	CB	D3B	D2B	D1B	D0B
H/W Reset	0	0	0	0	0	0	0	0
Auto PD	1	0	0	0	0	0	0	0

D7 **RQM – Request for Master.** Indicates that the controller is ready to send or receive data from the µP through the FIFO. This bit is cleared immediately after a byte transfer and is set again as soon as the FDC is ready for the next byte. During a non–DMA Execution phase, the RQM indicates the status of the interrupt pin.

D6 **DIO – Data I/O.** Indicates whether the FDC is expecting a byte to be written to (0) or read from (1) the Data Register.

D5 **NDM – Non–DMA Mode.** Indicates that the controller is in the Execution phase of a byte transfer operation in the non–DMA mode. Used for multiple byte transfers by the µP in the Execution Phase through interrupts or software polling.

D4 **CB – Command Busy.** This bit is set after the first byte of the Command phase is written. This bit is cleared after the last byte of the Result phase is read. If there is no Result phase in a command, the bit is cleared after the last byte of the Command phase is written.

D3 **D3B – Drive 3 Busy.** Set after the last byte of the Command phase of a Seek or Recalibrate command is issued for drive 3. Cleared after reading the first byte in the Result phase of the Sense Interrupt command for this drive.

D2 **D2B – Drive 2 Busy.** Same as above for drive 2.

D1 **D1B – Drive 1 Busy.** Same as above for drive 1.

D0 **D0B – Drive 0 Busy.** Same as above for drive 0.

4.2.6 Data Rate Select Register (DSR)

This write–only register is used to program the data rate, amount of write precompensation, power down mode, and software reset. The data rate is programmed via the CCR, not the DSR, for PC–AT and PS/2 applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is determined by the most recent write to either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset sets the DSR to 02H, which corresponds to the default precompensation setting and 250 Kbps.

	D7	D6	D5	D4	D3	D2	D1	D0
Description	SRST	POWD	0	PRE2	PRE1	PRE0	DRS1	DRS0
H/W Reset	0	0	0	0	0	0	1	0
Auto PD	1	0	0	UC	UC	UC	UC	UC

D7 **SRST – Software Reset.** This bit has the same function as the DOR RESET bit except that it is self–clearing.

D6 **POWD – Power Down.** A 1 written to this bit puts the FDC into the manual low power mode. It causes an immediate termination of activity in the FDC, resets the core and enters powerdown mode. Any command in progress is aborted. The FDC can only be restarted with a hardware or software reset.

D5 Reserved. Read as 0.

D4–D2 PRE2–0 – Precompensation Select. These three bits select the amount of write precompensation the FDC uses on the $\overline{\text{WRDATA}}$ disk interface output. Table 4–3 shows the amount of precompensation used for each bit pattern. In most cases, the default values (see Table 4–4) can be used; however, alternate values can be chosen for specific types of drives and media. Track 0 is the default starting track number for precompensation. The starting track number can be changed in the Configure command.

WRITE PRECOMPENSATION DELAYS Table 4–3

PRE2	PRE1	PRE0	VALUE (ns)
0	0	0	Default; see Table 4–4
0	0	1	41.7
0	1	0	83.3
0	1	1	125.0
1	0	0	66.7
1	0	1	208.3
1	1	0	250.0
1	1	1	0.0

D1–D0 DRS1,0 – Data Rate Select. These bits determine the data rate for the FDC. Table 4–4 lists the corresponding data rate for each value of D1, D0. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset. Note that bits DRS1 and DRS0 may also be written via the CCR register.

DATA RATE SELECT ENCODING Table 4–4

DRS1	DRS0	MFM DATA RATE (bps)	FM DATA RATE (bps)	DEFAULT PRECOMPENSATION
0	0	500K	250K	125.0
0	1	300K	150K	125.0
1	0	250K	125K	125.0
1	1	1M	Illegal	41.7

4.2.7 Data Register (FIFO)

	D7	D6	D5	D4	D3	D2	D1	D0
Description	Data [7:0]							
H/W Reset	Byte Mode							
Auto PD	UC							

The read/write FIFO is used to transfer all commands, data, and status between the µP and the FDC. During the Command phase, the µP writes the command bytes into the FIFO after polling the RQM and DIO bits in the MSR. During the Result phase, the µP reads the result bytes from the FIFO after polling the RQM and DIO bits in the MSR.

Enabling the FIFO, and setting the FIFO threshold, is done via the Configure command. If the FIFO is

enabled, only the Execution phase byte transfers use the 16–byte FIFO. The FIFO is always disabled during the Command and Result phases of a controller operation. If the FIFO is enabled, it is not disabled after a software reset if the LOCK bit is set in the Lock command. After a hardware reset, the FIFO is disabled to maintain compatibility with PC–AT systems.

The 16–byte FIFO can be used for DMA, interrupt, or software polling type transfers during the execution of a read, write, format, or scan command. The FIFO allows the system a larger latency time without causing a disk overrun/underrun error. Typical uses of the FIFO are at the 1 Mbps data rate, or with multi–tasking operating systems. The default state of the FIFO is disabled, with a threshold of zero. The default state is entered after a hardware reset.

During the Execution phase of a command involving data transfer to/from the FIFO, the system must respond to a data transfer service request based on the following formula:

1 Mbps Maximum Latency – approximate:

(THRESH + 1) x 8 x 1 µs

500 Kbps Maximum Latency – approximate:

(THRESH + 1) x 8 x 2 µs

THRESH is a value which can be programmed via the Configure command. Table 4–5 shows some of the 16 possible latency values for selected THRESH values. The programmable threshold feature is useful in adjusting the FDC to the speed of the system. In other words, a slow system with a sluggish DMA transfer capability uses a high value for THRESH, giving the system more time to respond to a data transfer service request (software assigned DRAM for DMA mode or IRQ for interrupt mode). Conversely, a fast system with quick response to a data transfer service request uses a low value THRESH.

SELECTED FIFO LATENCY VALUES Table 4–5

	MAX LATENCY	
THRESH VALUE	**1 Mbps**	**500 KBps**
0	8 µs	16 µs
3	32 µs	64 µs
7	64 µs	128 µs
15	128 µs	256 µs

4.2.8 Digital Input Register (DIR)

This read only diagnostic register is used to detect the state of the $\overline{\text{DSKCHG}}$ disk interface input and some diagnostic signals. The function of this register depends on the register mode of operation. When in the PC–AT mode, D6–D0 are High–Z to avoid conflict with the fixed disk status register at the same address. DIR is unaffected by a software reset.

Digital Input Register – PC–AT Mode

	D7	D6	D5	D4	D3	D2	D1	D0
Description	$\overline{\text{DSKCHG}}$	X	X	X	X	X	X	X
H/W Reset	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Auto PD	0	X	X	X	X	X	X	X

D7 **$\overline{\text{DSKCHG}}$ – Disk Changed.** Active low status of $\overline{\text{DSKCHG}}$ disk interface input. During power down this bit is invalid, if it is read by the software.

D6–D0Reserved. Read back as High–Z.

Digital Input Register – PS/2 Mode

	D7	D6	D5	D4	D3	D2	D1	D0
Description	$\overline{\text{DSKCHG}}$	1	1	1	1	DRS1	DRS0	$\overline{\text{HIDEN}}$
H/W Reset	N/A	0	0	0	0	0	1	0
Auto PD	0	0	0	0	UC	0	UC	UC

D7 **$\overline{\text{DSKCHG}}$ – Disk Changed.** Active low status of $\overline{\text{DSKCHG}}$ disk interface input. During power down this bit is invalid, if it is read by the software.

D6–D3Reserved. Always 1.

D2–1 **DRS1, 0 – Data Rate Select Status 1, 0.** These bits indicate the status of the DRS1, 0 bits programmed through the DSR/CCR.

D0 **HIDEN – High Density.** This bit is low when the 1 Mbps or 500 Kbps data rate is chosen, and is high when the 300 Kbps or 250 Kbps data rate is chosen.

4.2.9 Configuration Control Register (CCR)

This is the write–only data rate register commonly used in PC–AT applications. This register is not affected by a software reset, and is set to 250 Kbps after a hardware reset. The data rate of the FDC is determined by the last write to either the CCR or DSR.

	D7	D6	D5	D4	D3	D2	D1	D0
Description	X	X	X	X	X	X	DRS1	DRS0
H/W Reset	X	X	X	X	X	X	1	0
Auto PD	X	X	X	X	X	X	UC	UC

D7–D2.Reserved. Read as High–Z.

D1–D0Data Rate Select. These bits determine the data rate of the FDC. See Table 4–4 for the appropriate values.

4.3 FDC COMMAND SUMMARY

The DS83CH20 supports 16 basic FDC command types for PC–AT compatibility and nine additional extended commands for compatibility with other floppy disk controllers. These are listed in Table 4–6.

FDC COMMAND SUMMARY Table 4–6

COMMAND	TYPE
Configure	Extended
Dump Registers	Extended
Format Track (Write ID)	Basic
Invalid	Basic
Lock	Extended
Perpendicular Mode (Toshiba)	Extended
Powerdown Mode	Extended
Read Data	Basic
Read Deleted Data	Basic
Read A Track	Basic
Read ID	Basic
Recalibrate	Basic
Relative Seek	Extended
SCAN Equal	Basic
SCAN High or Equal	Basic
SCAN Low or Equal	Basic
Seek	Basic
Sense Device Status	Basic
Sense Interrupts	Basic
Specify	Basic
Verify	Extended
Verset	Extended
Version	Extended
Write Data	Basic
Write Deleted Data	Basic

4.3.1 Command Parameter Abbreviation

Lists the abbreviations used in the command, parameter and results tables.

COMMAND PARAMETER ABBREVIATIONS Table 4–7

SYMBOL	FULL NAME/EXPLANATION
APD	Auto Power Down
C	Cylinder number
D	Data pattern
DC3, 2, 1, 0	Drive Control (Perpendicular Mode)
DFI	Disable FIFO
DIR	Relative seek 0 = decrement, 1 = increment ”PCN”
DTL	Data transfer length. Only valid if N=0
EC	Enable Count
EIS	Enable Implied Seek
EOT	End Of Track
FTR	FDI signal 3–state (Powerdown)
FTH	FIFO THreshold setting
GAP	Gap select (Perpendicular mode)
GPL	GaP Length (gap 3)
GSL	Gap Skip Length (bytes skipped in gap 3)
H	Logical Head number on media
HD	HeaD number (0 or 1)
HLT	Head Load Time
HUT	Head Unload Time
LOC	Lock configure registers
MDL	Min Delay (Powerdown)
MFM	Modified FM (High density)
MT	Multi–Track sector
N	Sector data length
NCN	New Cylinder Number
ND	Non–Dma mode
OW	Over Write enable
PCN	Present Cylinder Number
POL	Disable POLling
PTN	Precompensation Track Number
R	Record (sector) number
RCN	Relative Cylinder Number
SC	SeCtors per track
SK	SKp
SRT	Step Rate Timer
STP	STeP
ST0, 1, 2, 3	STatus bytes 0, 1, 2 and 3
US0,1	Unit Select
VER	Version number
WGT	Write Gate (perpendicular mode)

4.3.2 Command Parameter Format

The following conventions are used for all commands/ status transferred to/from the FDC:

	MSB							LSB
PARAMETER 1	C	–	–	–	–	–	–	C

Most significant bit (MSB) is always on the left, and least significant bit (LSB) on the right. A box as above indicates bits D7–D0 describe the C parameter.

"X" in any location indicates don't care.

"0" in any location indicates must be written or is always read "0".

"1" in any location indicates must be written or is always read "1".

"?" not known or undefined.

4.3.3 Status Bytes Format

STATUS 0 (ST0)

ST0	NAME	MEANING
D7	IC1	IC = 00, Normal termination of command. IC = 01, Abnormal termination of command. IC = 10, Invalid command. IC = 11, Change in device status.
D6	IC0	
D5	SE	Seek End, always set after a seek operation.
D4	EC	Fault indication by external device or Track 0 not detected during recalibrate.
D3	NR	External device is not ready.
D2	HD	Indicates head selected at IRQ request.
D1	US1	Indicates the device number at IRQ request.
D0	US0	

STATUS 1 (ST1)

ST1	NAME	MEANING
D7	EN	Indicates read or write was tried beyond EOT.
D6	"0"	Always returns "0".
D5	DE	CRC error of ID or DATA (see ST2 DD).
D4	OR	Over Run error.
D3	"0"	Always returns "0".
D2	ND	Sector not found. ID field specified by the read ID command could not be read. Read track command could not find correct sector sequence.
D1	NW	Device is write protected.
D0	MA	Missing address mark.

STATUS 2 (ST2)

ST2	NAME	MEANING
D7	“0”	Always returns “0”.
D6	CM	Control mark, Read data command returns a deleted data address mark or Read deleted data command returns a data address mark.
D5	DD	Data CRC error.
D4	NC	Wrong cylinder. C byte read does not match stored value, except during Read A Track.
D3	SH	Scan equal hit.
D2	SN	Scan not equal.
D1	BC	Bad cylinder, set when C byte read FF, except during Read A Track.
D0	MD	Missing address mark, set when neither DAM nor DDAM is found.

STATUS 3 (ST3)

ST3	NAME	MEANING
D7	FT	Device fault signal.
D6	WP	Device write protect.
D5	RY	Device ready.
D4	T0	Device Track 0.
D3	TS	Device two sided.
D2	HD	Head select.
D1	US1	Device select.
D0	US0	

4.3.4 Invalid Command

COMMAND SEQUENCE

In command phase the system writes an invalid command to the FDC. In results phase the system reads the ST0 byte from the FDC.

COMMAND PHASE

COMMAND	?	–	–	–	–	–	–	?

RESULTS PHASE

STO	1	0	0	0	0	0	0	0

If an invalid command is written the FDC returns ST0 byte as 80h (invalid command).

4.3.5 Read Data

The Read Data command reads logical sectors containing a normal address mark (AM) from the selected drive and makes the data available to the host microprocessor.

READ DATA COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 and associated parameter bytes to the FDC. In execution phase the system reads data from the FDC. In results phase the system reads the status bytes 0,1 and 2 and associated parameter bytes from the FDC.

COMMAND PHASE

COMMAND 1	MT	MFM	SK	0	0	1	1	0
COMMAND 2	X	X	X	X	X	HD	US1	US0
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N
PARAMETER 5	EOT	–	–	–	–	–	–	EOT
PARAMETER 6	GSL	–	–	–	–	–	–	GSL
PARAMETER 7	DTL	–	–	–	–	–	–	DTL

EXECUTION PHASE: Data transfer from FDC to system.

RESULTS PHASE

ST0	0	IC0	0	0	NR	HD	US1	US0
ST1	EN	0	DE	OR	0	ND	0	MA
ST2	0	CM	DD	NC	0	0	BC	MD
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N

READ DATA ERROR STATUS

After execution of the Read Data command the following error states are reported by setting the appropriate bit of the status registers ST0–ST2.

AREA	ERROR	STATUS SET
	Command successful Not Ready	None IC0, NR
ID	IDAM not detected C not matched (≠FFh) C not matched (=FFh) H not matched R not matched N not matched CRC error	IC0, MA IC0, ND, NC IC0, ND, BC IC0, ND IC0, ND IC0, ND IC0, DE
DATA	DAM not found DDAM not found CRC error Overrun Incomplete at last sector	IC0, MA, MD CM IC0, DE, DD IC0, OR IC0, EN

AREA = Part of disk sector.
ERROR = Error state reported.

NOTE:
It is possible to have more than one error state reported at command termination.

READ DATA SEQUENCE

After the command has been accepted, the FDC loads the head and waits for the HLT (Head Load Time) before starting to read data. If the head is already loaded the FDC starts to read data immediately. Data is read until the required sector is found at which point the data is transferred to the system. The FDC continues to read consecutive sectors until either an error is detected or a terminal count received.

CRC checking is done on all sectors, if a CRC error is detected the command is terminated.

If SK=0 and a sector with DDAM set is encountered the data is read before the command is terminated.

If SK=1 sectors marked with DDAM are not read before termination of the command.

If the INDEX mark is encountered twice while the FDC is trying to read a sector the command is terminated with a sector not found error.

If MT=1, after reading the last sector on side 1 of the disk the FDC looks for the first sector on side 2. For MT (Multi track) to work the first sector read must be on side 1 of the disk.

4.3.6 Read Delete Data

The Read Deleted Data command reads logical sectors containing a deleted address mark (AM) from the selected drive and makes the data available to the host microprocessor.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 and associated parameter bytes to the FDC. In execution phase the system reads data from the FDC. In results phase the system reads the status bytes 0,1 and 2 and associated parameter bytes from the FDC.

COMMAND PHASE

COMMAND 1	MT	MFM	SK	0	1	1	0	0
COMMAND 2	X	X	X	X	X	HD	US1	US0
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N
PARAMETER 5	EOT	–	–	–	–	–	–	EOT
PARAMETER 6	GSL	–	–	–	–	–	–	GSL
PARAMETER 7	DTL	–	–	–	–	–	–	DTL

EXECUTION PHASE: Data transfer from FDC to system.

RESULT PHASE

ST0	0	IC0	0	0	NR	HD	US1	US0
ST1	EN	0	DE	OR	0	ND	0	MA
ST2	0	CM	DD	NC	0	0	BC	MD
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N

ERROR STATUS

After execution of the Read Deleted Data command the following error states are reported by setting the appropriate bit of the status registers ST0–ST2.

AREA	ERROR	STATUS SET
	Command successful Not Ready	None IC0, NR
ID	IDAM not detected C not matched (≠FFh) C not matched (=FFh) H not matched R not matched N not matched CRC error	IC0, MA IC0, ND, NC IC0, ND, BC IC0, ND IC0, ND IC0, ND IC0, DE
DATA	DAM not found DDAM not found CRC error Overrun Incomplete at last sector	CM IC0, MA, MD IC0, DE, DD IC0, OR IC0, EN

AREA = Part of disk sector.
ERROR = Error state reported.

NOTE:

It is possible to have more than one error state reported at command termination.

READ DELETED DATA SEQUENCE

The operation is identical to the read data command except for the operation of the SK bit.

If SK=0 and a sector with DAM is found, the data is read and the command terminated.

IF SK=1 sectors with DAM are not read before termination of command.

4.3.7 Write Data

The Write Data command receives data from the host and writes logical sectors containing a normal data address mark (AM) to the selected drive.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 and associated parameter bytes to FDC. In execution phase the system writes data to the FDC. In results phase the system reads the status bytes 0,1 and 2 and their associated parameter bytes from the FDC.

COMMAND PHASE

COMMAND 1	MT	MFM	SK	0	0	1	0	1
COMMAND 2	X	X	X	X	X	HD	US1	US0
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N
PARAMETER 5	EOT	–	–	–	–	–	–	EOT
PARAMETER 6	GSL	–	–	–	–	–	–	GSL
PARAMETER 7	DTL	–	–	–	–	–	–	DTL

EXECUTION PHASE: Data transfer from system to FDC.

RESULTS PHASE

ST0	0	IC0	0	EC	NR	HD	US1	US0
ST1	EN	0	DE	OR	0	ND	NW	MA
ST2	0	0	0	NC	0	0	BC	0
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N

SK bit of Command 1 has no effect.

ERROR STATUS

After execution of the write data command the following error states are reported by setting the appropriate bit of the status registers ST0–ST2.

AREA	ERROR	STATUS SET
	Command successful Not Ready Write protect	None IC0, NR IC0, NW
ID	IDAM not detected C not matched (≠FFh) C not matched (=FFh) H not matched R not matched N not matched CRC error	IC0, MA IC0, ND, NC IC0, ND, BC IC0, ND IC0, ND IC0, ND IC0, DE
DATA	Fault Overrun Incomplete at least sector	IC0, EC IC0, OR IC0, EN

AREA = Part of disk sector.
ERROR = Error state reported.

NOTE:
It is possible to have more than one error state reported at command termination.

WRITE DATA SEQUENCE

After the command has been accepted and the head is loaded the FDC then waits the Head load time (HLT) before starting to read sector IDs. If the head was already loaded the FDC starts reading sector IDs immediately.

When the required sector has been found the FDC begins writing a new data field. This consists of SYNC, DAM, DATA (supplied by system) and CRC (generated by FDC). After the sector has been written, the sector number is incremented and the FDC starts to look for the new sector unless the command is terminated.

The write data command will terminate if any of the following are found:

- The device write protect signal is true.
- The required sector cannot be found within two index markers.
- If there is a system data overrun error.
- A DMA TC cycle is received.

If MT=1, after writing the last sector on side one of the disk the FDC looks for the first sector on side two. For MT (Multi track) to work the first sector must be on side one of the disk.

4.3.8 Write Deleted Data

The Write Deleted Data command receives data from the host and writes logical sectors containing a deleted data address mark (AM) to the selected drive.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 and associated parameter bytes to the FDC. In execution phase the system writes data to the FDC. In results phase the system reads the status bytes 0,1 and 2 and associated parameter bytes from the FDC.

COMMAND PHASE

COMMAND 1	MT	MFM	SK	0	1	0	0	1
COMMAND 2	X	X	X	X	X	HD	US1	US0
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N
PARAMETER 5	EOT	–	–	–	–	–	–	EOT
PARAMETER 6	GSL	–	–	–	–	–	–	GSL
PARAMETER 7	DTL	–	–	–	–	–	–	DTL

EXECUTION PHASE: Data transfer from system to FDC.

RESULTS PHASE

ST0	0	IC0	0	EC	NR	HD	US1	US0
ST1	EN	0	DE	OR	0	ND	NW	MA
ST2	0	0	0	NC	0	0	BC	0
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N

SK bit of Command 1 has no effect.

ERROR STATUS

After execution of the Write Deleted Data command the following error states are reported by setting the appropriate bit of the status registers ST0–ST2.

AREA	ERROR	STATUS SET
	Command successful Not Ready Write protect	None IC0, NR IC0, NW
ID	IDAM not detected C not matched (≠FFh) C not matched (=FFh) H not matched R not matched N not matched CRC error	IC0, MA IC0, ND, NC IC0, ND, BC IC0, ND IC0, ND IC0, ND IC0, DE
DATA	Fault Overrun Incomplete at least sector	IC0, EC IC0, OR IC0, EN

AREA = Part of disk sector.
ERROR = Error state reported.

NOTE:

It is possible to have more than one error state reported at command termination.

WRITE DELETED DATA SEQUENCE

The execution of this command is identical to the write data command except that after detection of the required ID the FDC writes a DDAM instead of DAM to the device.

4.3.9 Read ID

The Read ID command finds the next available address field and returns the ID bytes (track, head, sector, bytes per sector) to the microprocessor.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 to the FDC. In execution phase the system reads ID data from the FDD to the FDC. In results phase the system reads the status bytes 0,1 and 2 and associated parameter bytes from the FDC.

COMMAND PHASE

COMMAND 1	MT	MFM	SK	0	1	0	1	0
COMMAND 2	X	X	X	X	X	HD	US1	US0

EXECUTION PHASE: Data transfer from disk to FDC registers C,H,R,N.

RESULTS PHASE

ST0	0	IC0	0	0	NR	HD	US1	US0
ST1	0	0	0	0	0	ND	0	MA
ST2	0	0	0	0	0	0	0	0
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N

MT and SK bits of Command 1 have no effect.

ERROR STATUS

After execution of the Read ID command the following error states are reported by setting the appropriate bit of the status registers ST0–ST2.

AREA	ERROR	STATUS SET
	Command successful Not Ready	None IC0, NR
ID	IDAM not detected No valid ID is detected	IC0, MA IC0, ND

AREA = Part of disk sector.
ERROR = Error state reported.

READ ID SEQUENCE

If the head is already loaded the FDC begins to read the track immediately. Otherwise, the FDC loads the head and waits the head load time (HLT) before starting to read the track.

The ID of the first sector to be read without error (good CRC) is written into the FDC registers C,H,R and N. These registers are read by the system during the results phase.

4.3.10 Format Track (WRITE ID)

The Format Track command formats one track on the selected drive.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 and associated parameter bytes to the FDC. In execution phase the system writes ID Data to the FDC. In results phase the system reads the status bytes 0,1 and 2 and associated parameter bytes from the FDC.

COMMAND PHASE

COMMAND 1	MT	MFM	SK	0	1	1	0	1
COMMAND 2	X	X	X	X	X	HD	US1	US0
PARAMETER 1	N	–	–	–	–	–	–	N
PARAMETER 2	SC	–	–	–	–	–	–	SC
PARAMETER 3	GPL	–	–	–	–	–	–	GPL
PARAMETER 4	D	–	–	–	–	–	–	D

EXECUTION PHASE: Data transfer from system to FDC.

RESULTS PHASE

ST0	0	IC0	0	EC	NR	HD	US1	US0
ST1	0	0	0	OR	0	0	NW	0
ST2	0	0	0	0	0	0	0	0
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N

MT and SK bits of Command 1 have no effect.

NOTE:
Returned status parameters 1,2 and 3 (C,H and R) are undefined.

ERROR STATUS

After execution of the write ID command the following error states are reported by setting the appropriate bit of the status registers ST0–ST2.

AREA	ERROR	STATUS SET
	Command successful Not Ready Write protect	None IC0, NR IC0, NW
	Fault Overrun	IC0, EC IC0, OR

AREA = Part of disk sector.
ERROR = Error state reported.

NOTE:

It is possible to have more than one error state reported at command termination.

WRITE ID SEQUENCE

After the FDC has accepted the command it waits for the INDEX mark to be detected before starting to write the track. The track is then written according to the format chosen (see section on Data Formats).

During the execution phase the system must supply four bytes for each sector written. These are here designated as CYL, HED, SEC and NO, and represent the cylinder number, head number, sector number, and sector size values to be written into the sector header fields on the media during the format operation (see section on Data Formats for an illustration of the position of these bytes in a sector format string). Only the SEC number should change between sectors. After the last sector is written the FDC continues writing GAP 4b information until the INDEX mark is again detected. Normally CYL would be the same as the present cylinder number, as set by a previous seek command, and HED would reflect the state of the physical head select bit (HD) in the second command word. NO would normally agree with the N parameter specified during the command phase.

NOTES:

3. During write ID all sectors are marked DAM (Data Address Mark FB*). Sectors found to be bad are then marked with DDAM (Deleted Data Address Mark F8*) using the write deleted data command.
4. The data written during the Write ID command (CYL, HED, SEC and NO) has no affect on the track format specified in Parameter bytes 1, 2, 3 and 4.
5. Subsequent accesses to the formatted cylinder will require that the CYL, HED, SEC, and NO bytes read back from the disk correspond to the C, H, R, and N parameters supplied as part of that access command.

PARAMETERS

N specifies the length of the data segment in each sector.

N	DATA SIZE (bytes)	
0	128	
1	256	
2	512	
3	1024	(1K)
4	2048	(2K)
5	4096	(4K)
6	8192	(8K)
7	16384	(16K)

Only values of N in the range 0 to 7 are allowed, values of N larger than 7 wrap (i.e. N=8 data size = 128).

SC specifies the number of sectors per track.

GPL specifies the length of GAP 3 in bytes.

4.3.11 Read A Track

The Read A Track command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track.

execution phase the system reads data from the FDC. In results phase the system reads the status bytes 0,1 and 2 and associated parameter bytes from the FDC.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 and associated parameter bytes to the FDC. In

COMMAND PHASE

COMMAND 1	0	MFM	0	0	0	0	1	0	
COMMAND 2	X	X	X	X	X	HD	US1	US0	
PARAMETER 1	C	–	–	–	–	–	–	C	
PARAMETER 2	H	–	–	–	–	–	–	H	
PARAMETER 3	R	–	–	–	–	–	–	R	SEE NOTE
PARAMETER 4	N	–	–	–	–	–	–	N	
PARAMETER 5	EOT	–	–	–	–	–	–	EOT	
PARAMETER 6	GSL	–	–	–	–	–	–	GSL	
PARAMETER 7	DTL	–	–	–	–	–	–	DTL	

EXECUTION PHASE: Data transfer from FDC to system.

RESULTS PHASE

ST0	0	IC0	0	0	NR	HD	US1	US0
ST1	EN	0	DE	OR	0	ND	0	MA
ST2	0	CM	DD	NC	0	0	BC	MD
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N

NOTE:

The R parameter is forced to “01h” at start of command execution phase.

ERROR STATUS

After execution of the Read Diagnostic command the following error states are reported by setting the appropriate bit of the status registers ST0–ST2.

AREA	ERROR	STATUS SET
	Command successful Not Ready	None IC0, NR
ID	IDAM not detected C not matched (≠FFh) H not matched R not matched N not matched CRC error	IC0, MA ND ND ND ND DE
DATA	DAM not detected DDAM not detected CRC error Overrun Incomplete at last sector	IC0, MA, MD CM DE, DD IC0, OR IC0, EN

AREA = Part of disk sector.
ERROR = Error state reported.

NOTE:

It is possible to have more than one error state reported at command termination.

READ DIAGNOSTIC SEQUENCE

After the command has been accepted the FDC enters the head load sequence then waits for the INDEX mark before reading all data on the track in the order found (regardless of sector number). The command does not terminate if an error is encountered. Command termination occurs only when the specified number of sectors have been read.

Any errors found will set the appropriate bits in the status bytes. The status bytes will only indicate that an error has occurred, but not the sector in which the error was found.

4.3.12 Scan Equal

The Scan Equal command reads data from the selected drive and checks to see if it is equal to that of the microprocessor data.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 and associated parameter bytes to the FDC. In execution phase the system writes data to the FDC. In results phase the system reads the status bytes 0,1 and 2 and associated parameter bytes from the FDC.

COMMAND PHASE

COMMAND 1	MT	MFM	SK	1	0	0	0	1
COMMAND 2	X	X	X	X	X	HD	US1	US0
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N
PARAMETER 5	EOT	–	–	–	–	–	–	EOT
PARAMETER 6	GSL	–	–	–	–	–	–	GSL
PARAMETER 7	DTL	–	–	–	–	–	–	DTL

EXECUTION PHASE: Data transfer from system to FDC.

RESULTS PHASE

ST0	0	IC0	0	0	NR	HD	US1	US0
ST1	EN	0	DE	OR	0	ND	0	MA
ST2	0	CM	DD	NC	SH	SN	BC	MD
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N

ERROR STATUS

After execution of the Scan Equal command the following error states are reported by setting the appropriate bit of the status registers ST0–ST2.

AREA	ERROR	STATUS SET
	SCAN Equal	SH
	SCAN not Equal	SN
	Not Ready	IC0, NR
ID	IDAM not detected	IC0, MA
	C not matched (≠FFh)	IC0, ND, NC
	C not matched (=FFh)	IC0, ND, BC
	H not matched	IC0, ND
	R not matched	IC0, ND
	N not matched	IC0, ND
	CRC error	IC0, DE
DATA	DAM not detected	IC0, MA, MD
	DDAM not detected	CM
	CRC error	IC0, DE, DD
	Overrun	IC0, OR

AREA = Part of disk sector.
ERROR = Error state reported.

NOTE:

It is possible to have more than one error state reported at command termination.

SCAN EQUAL OPERATION

Data read from the selected sector is compared with data written to the FDC, if all bytes are the same the command terminates normally.

Any bytes where FFh is written to the FDC are not compared with data read from the disk.

4.3.13 Scan Low or Equal

The Scan Low or Equal command reads data from the selected drive and checks to see if it is equal to or less than that of the microprocessor data.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 and associated parameter bytes to the FDC. In execution phase the system writes data to the FDC. In results phase the system reads the status bytes 0,1 and 2 and associated parameter bytes from the FDC.

COMMAND PHASE

COMMAND 1	MT	MFM	SK	1	1	0	0	1
COMMAND 2	X	X	X	X	X	HD	US1	US0
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N
PARAMETER 5	EOT	–	–	–	–	–	–	EOT
PARAMETER 6	GSL	–	–	–	–	–	–	GSL
PARAMETER 7	DTL	–	–	–	–	–	–	DTL

EXECUTION PHASE: Data transfer from system to FDC.

RESULTS PHASE

ST0	0	IC0	0	0	NR	HD	US1	US0
ST1	EN	0	DE	OR	0	ND	0	MA
ST2	0	CM	DD	NC	SH	SN	BC	MD
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N

ERROR STATUS

After execution of the Scan Equal or Low command the following error states are reported by setting the appropriate bit of the status registers ST0–ST2.

AREA	ERROR	STATUS SET
	SCAN Equal SCAN Low SCAN High Not Ready	SH None SN IC0, NR
ID	IDAM not detected C not matched (≠FFh) C not matched (=FFh) H not matched R not matched N not matched CRC error	IC0, MA IC0, ND, NC IC0, ND, BC IC0, ND IC0, ND IC0, ND IC0, DE
DATA	Fault Overrun Incomplete at last sector	IC0, DE IC0, OR IC0, EN

AREA = Part of disk sector.
ERROR = Error state reported.

NOTE:
It is possible to have more than one error state reported at command termination.

SCAN LOW OR EQUAL OPERATION

Data read from the selected sector is compared with data written to the FDC. If bytes read from the disk are equal to or less than those written by the system then the command terminates normally.

4.3.14 Scan High or Equal

The Scan High or Equal command reads data from the selected drive and checks to see if it is equal to or greater than that of the microprocessor data.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 and associated parameter bytes to the FDC. In execution phase the system writes data to the FDC. In results phase the system reads the status bytes 0,1 and 2 and associated parameter bytes from the FDC.

COMMAND PHASE

COMMAND 1	MT	MFM	SK	1	1	1	0	1
COMMAND 2	X	X	X	X	X	HD	US1	US0
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N
PARAMETER 5	EOT	–	–	–	–	–	–	EOT
PARAMETER 6	GSL	–	–	–	–	–	–	GSL
PARAMETER 7	DTL	–	–	–	–	–	–	DTL

EXECUTION PHASE: Data transfer from system to FDC.

RESULTS PHASE

ST0	0	IC0	0	0	NR	HD	US1	US0
ST1	EN	0	DE	OR	0	ND	0	MA
ST2	0	CM	DD	NC	SH	SN	BC	MD
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N

ERROR STATUS

After execution of the Scan Equal or High command the following error states are reported by setting the appropriate bit of the status registers ST0–ST2.

AREA	ERROR	STATUS SET
	SCAN High SCAN Equal SCAN Low Not Ready	None SH SN IC0, NR
ID	IDAM not detected C not matched (≠FFh) C not matched (=FFh) H not matched R not matched N not matched CRC error	IC0, MA IC0, ND, NC IC0, ND, BC IC0, ND IC0, ND IC0, ND IC0, DE
DATA	DAM not detected DDAM detected CRC error Overrun	IC0, MA, MD CM IC0, DE, DD IC0, OR

AREA = Part of disk sector.
ERROR = Error state reported.

NOTE:

It is possible to have more than one error state reported at command termination.

SCAN HIGH OR EQUAL OPERATION

Data read from the selected sector is compared with data written to the FDC. If bytes read from the disk are equal to or greater than those written by the system then the command terminates normally.

4.3.15 Seek

The Seek command steps the selected drive in or out until the desired track number is reached.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 and associated parameter bytes to Data channel. In execution phase the FDC issues step commands.

COMMAND PHASE

COMMAND 1	0	0	0	0	1	1	1	1
COMMAND 2	X	X	X	X	X	HD	US1	US0
PARAMETER 1	NCN	–	–	–	–	–	–	NCN

EXECUTION PHASE: Generation of STEP commands.

ERROR STATUS

After execution of the Seek command the following error states are reported by setting the appropriate bit of the status registers ST0–ST2.

AREA	ERROR	STATUS SET
	Command successful Not Ready	SE IC0, SE, NR

AREA = Part of disk sector.
ERROR = Error state reported.

NOTE:

Status is not automatically returned at the end of command execution, however the ST0 status register may be read by issuing the Sense Interrupt Status command.

SEEK OPERATION

The PCN (Present Cylinder Number) is compared with the NCN (New Cylinder Number) as follows:

If the PCN is equal to the NCN then the command terminates immediately.

If the PCN is less than the NCN, then the PCN is incremented at the step rate until the PCN becomes equal to the NCN. Note: The step rate is documented in the Specify command.

However, if the PCN is greater than the NCN then the PCN is decremented at the step rate until the PCN and NCN are the same.

Since the FDC is not busy during the seek command it is possible for the FDC to handle seeks on more than one device at the same time.

NOTE:

Read/Write commands should not be issued while seek operations are in progress.

4.3.16 Recalibrate

Recalibrate causes the read/write head of the disk drive to return to the track 0 position.

COMMAND PHASE

COMMAND 1	0	0	0	0	0	1	1	1
COMMAND 2	X	X	X	X	X	HD	US1	US0

EXECUTION PHASE: Generation of step pulses.

ERROR STATUS

After execution of the Recalibrate command the following error states are reported by setting the appropriate bit of the status register ST0.

AREA	ERROR	STATUS SET
	Command successful Not Ready Track 0 not detected	SE IC0, SE, NR IC0, SE, EC

AREA = Part of disk sector.
ERROR = Error state reported.

NOTE:

Status is not automatically returned at the end of command execution, however the ST0 status register may be read by issuing the Sense Interrupt Status command.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 to the FDC.

RECALIBRATE SEQUENCE

The FDC issues step commands towards track 0 until the TK0 signal is detected. If TK0 has not been found after 255 steps the command terminates with an error.

As with the Seek command multiple Recalibrate commands can be issued to different devices but no read/write operations will be accepted while they are being executed.

4.3.17 Sense Interrupt Status

The Sense Interrupt Status command resets the interrupt status and identifies the cause of the interrupt (via the IC code and SE bits of SR0).

COMMAND SEQUENCE

In command phase the system writes command byte 1 to the FDC. In results phase the system reads status byte ST0 and associated parameter byte from the FDC.

COMMAND PHASE

COMMAND 1	0	0	0	0	1	0	0	0

EXECUTION PHASE: None.

RESULTS PHASE

ST0	IC1	IC0	SE	EC	NR	0	US1	US0
PARAMETER 1	PCN	–	–	–	–	–	–	PCN

AREA	ERROR	STATUS SET
	Invalid command Status change Seek end abnormal	IC1 IC1, IC0 IC0
	Seek end*	SE
	Seek fail* Equipment check	EC
	Device became not ready	NR

* This applies to SEEK, RECALIBRATE and RELATIVE SEEK operations.

PCN is always for the drive indicated by US1 and US0.

Invalid command status is returned if no interrupt is pending.

4.3.18 Sense Device Status

The Sense Device Status command returns the status of the selected disk drive in ST3.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 to the FDC. In results phase the system reads the ST3 status byte returned by the FDC.

COMMAND PHASE

COMMAND 1	0	0	0	0	0	1	0	0
COMMAND 2	X	X	X	X	X	HD	US1	US0

RESULTS PHASE

ST3	FT	WP	RY	T0	TS	HD	US1	US0

The command begins immediately provided that a polling cycle is not in progress, if a polling cycle is in progress the command waits for it to finish. The selected drive is enabled and 15 ms later the inputs FT, WP, RY, T0 and TS are sampled, the sampled inputs are then returned with HD, US1 and US0 in the results phase as ST3.

4.3.19 Specify

The Specify command sets the initial values for the Head Unload Time (HUT), Step Rate Time (SRT), and the Head Load Time (HLT).

COMMAND SEQUENCE

In command phase the system writes command byte 1 and associated parameter bytes to the FDC.

There is no execution or results phase.

COMMAND PHASE

COMMAND 1	0	0	0	0	0	0	1	1
PARAMETER 1	SRT	–	–	SRT	HUT	–	–	HUT
PARAMETER 2	HLT	–	–	–	–	–	HLT	ND

SRT

SRT (Step Rate Timer) specifies the step rate generated by Seek commands.

STEP RATE TIMER (ms)

	DATA RATE			
SRT	**1M**	**500K**	**300K**	**250K**
0	8.0	16	26.7	32
1	7.5	15	25	30
. .	. .	. .	. .	. .
E	1.0	2	3.33	4
F	0.5	1	1.67	2

HUT

HUT (Head Unload Time) specifies the time the head remains loaded after the execution of a read or write command.

HUT prevents the system having to wait the head load time (HLT) during consecutive read/write commands.

HEAD UNLOAD TIME (ms)

	DATA RATE			
HUT	**1M**	**500K**	**300K**	**250K**
0	128	256	426	512
1	8	16	26.7	32
. .	. .	. .	. .	. .
E	112	224	373	448
F	120	240	400	480

HLT
HLT (Head Load Time) specifies the minimum time required for the head to stabilize after being loaded on to the disk.

HEAD LOAD TIME (ms)

	DATA RATE			
HLT	**1M**	**500K**	**300K**	**250K**
00	128	256	426	512
01	1	2	3.3	4
02	2	4	6.7	8
. .	. .	. .	. .	. .
7E	126	252	420	504
7F	127	254	423	508

ND
ND specifies Non–DMA mode transfers in the execution phase of a command. When sent, each byte to be transferred causes an interrupt.

4.3.20 Configure

The Configure command controls some operation modes of the controller. It should be issued during the initialization of the FDC after power–up.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 and associated parameter bytes to the FDC. There are no execution or results phases.

COMMAND PHASE

COMMAND 1	0	0	0	1	0	0	1	1
COMMAND 2	0	0	0	0	0	0	0	0
PARAMETER 1	0	EIS	DFI	POL	FTH	–	–	FTH
PARAMETER 2	PTN	–	–	–	–	–	–	PTN

Following a hardware reset or software reset, if LOC=0 the following bits are reset: EIS=0, DFI=1, POL=0, FTH=0 and PTN=0.

Following a software reset, if LOC=1 the following bits are reset: EIS=0, POL=0.

EIS

EIS, Enable Implied Seek; When enabled, a seek operation is performed prior to the execution of a read, write, scan, or verify operation.

DFI

DFI, Disable FIfo; When set the FIFO is disabled (only one byte deep) and the FTH value has no meaning.

POL

POL, Polling disable; When set normal polling operation is suspended.

FTH

FTH, Fifo THreshold; These four bits set the point at which the FIFO requests service.

The FIFO is only used during the execution phase of a read or write command, it is held clear at all other times. During writes if a FIFO underrun occurs the remainder of the sector is filled with zero (0h). During Reads the FDC requires all the data to be read from the FIFO before the results phase of a command can be entered.

Either a software reset, if LOC =0 or hardware reset sets FTH to 0 (1 byte).

When enabled the FIFO threshold value allows maximum system latency as outlined in the table below. Only some of the 16 possible values of threshold setting are are shown. At 1 Mbps data rate maximum latency is approximately = 1 ms x 8 x (FTH+1), at 500 Kbps data rate maximum latency is approximately = 2 ms x 8 x (FTH+1).

FTH VALUE	MAX LATENCY 1 Mbps	MAX LATENCY 500 Kbps
0	8 ms	16 ms
3	32 ms	64 ms
7	64 ms	128 ms
15	128 ms	256 ms

PTN

PTN precompensation Track number; This bit defines the starting track number for write precompensation during MFM writes.

4.3.21 Dump Registers

The dump Registers command is designed to support system run–time diagnostics and application software development and debug.

COMMAND SEQUENCE

In command phase the system writes command byte 1 to the FDC. In results phase the system reads the 10 returned register bytes from the FDC.

COMMAND PHASE

COMMAND 1	0	0	0	0	1	1	1	0

RESULTS PHASE

PARAMETER 1	PCN	–	–	–	–	–	–	PCN	DRIVE 0
PARAMETER 2	PCN	–	–	–	–	–	–	PCN	DRIVE 1
PARAMETER 3	PCN	–	–	–	–	–	–	PCN	DRIVE 2
PARAMETER 4	PCN	–	–	–	–	–	–	PCN	DRIVE 3
PARAMETER 5	SRT	–	–	SRT	HUT	–	–	HUT	
PARAMETER 6	HLT	–	–	–	–	–	HLT	ND	
PARAMETER 7	SC	–	–	–	–	–	–	SC	SC/EOT
PARAMETER 8	LCO	0	DC3	DC2	DC1	DC0	GAP	WGT	
PARAMETER 9	0	EIS	DFI	POL	FTH	–	–	FTH	
PARAMETER 10	PTN	–	–	–	–	–	–	PTN	

This command is ignored if NSM=1.

4.3.22 Perpendicular Mode

The Perpendicular Mode command is designed to support the Format and Write Data requirements of the Perpendicular Recording disk drives (4 Mbyte unformated capacity).

COMMAND SEQUENCE

In command phase the system writes command 1 and associated parameter byte to the FDC.

COMMAND PHASE

COMMAND 1	0	0	0	1	0	0	1	0
PARAMETER 1	OW	0	DC3	DC2	DC1	DC0	GAP	WGT

A software reset clears GAP and WGT only, a hardware reset will clear all bits.

GAP, WGT

The Gap (Gap Select) and WGT (Write Gate) bits determine the length of the GAP2 field and whether any bits are written within the GAP2 field, respectively. These bits must be updated in software in accordance with the DSR speed bits if the DCx bits are not used. The table below illustrates the effect of the GAP and WGT bits on the FDC. Note that GAP2 is 22 bytes long except when in perpendicuar mode at 1 Mbps and that part of GAP2 is overwritten during sector writes in perpendicular mode.

GAP and WGT must be set to 0 in order for the DCx bits to function. If GAP and WGT are not set to 0, they override whatever is programmed in the DCx bits.

Effect of GAP and WGT on Format and Write Commands

GAP	WGT	GAP2	GAP2 Written	COMMENT
0	0	22	0	See section on DC 3, 2, 1, 0
0	1	22	19	Perpendicular 500 Kbps
1	0	22	0	Normal
1	1	41	38	Perpendicular 1 Mbps

DC3, 2, 1, 0

Drive Control bits – A 0 written to DCx sets Drive x to conventional mode while a 1 sets Drive x to Perpendicular Mode. The DCx bits have meaning only if both GAP and WGT are cleared to 0 and OW is set to 1.

Effect of Drive Mode and Data Rate on Format and Write Commands

DATA RATE	DRIVE MODE	GAP2 LENGTH WRITTEN DURING FORMAT	PORTION OF GAP2 REWRITTEN BY WRITE DATA COMMAND
250 kbps/300 kbps/500 kbps	Conventional Perpendicular	22 Bytes 22 Bytes	0 Bytes 19 Bytes
1 Mbps	Conventional Perpendicular	22 Bytes 41 Bytes	0 Bytes 38 Bytes

OW

Overwrite – The OW bit offers additional control. When set to 1, the values of DCx are changeable. When set to 0, the internal values of DCx are unaffected, regardless of what is written to the DCx bits.

4.3.23 Relative Seek

The Relative Seek command steps the selected drive in or out the selected number of steps.

COMMAND SEQUENCE

In command phase the system writes command bytes 1 and 2 and associated parameter byte to the FDC. In execution phase the FDC issues step commands to the FDD.

COMMAND PHASE

COMMAND 1	1	DIR	0	0	1	1	1	1
COMMAND 2	0	0	0	0	0	HD	US1	US0
PARAMETER 1	RCN	–	–	–	–	–	–	RCN

EXECUTION PHASE The FDC issues step commands specified by RCN and DIR.

If DIR = 0 the track number is decremented.
If DIR = 1 the track number is incremented.

RELATIVE SEEK OPERATION

This command is used to step the read/write head to tracks beyond 255. For further details, see the seek command.

4.3.24 Verify

The Verify command is used to verify the data stored on a disk. This command acts exactly like a Read Data command except that no data is transferred to the host. Data is read from the disk, the CRC computed and is checked against the previously stored valve.

COMMAND SEQUENCE

In command phase the system writes command byte 1 and 2 and associated parameter bytes to the FDC. In execution phase no data is transferred. In results phase the system reads the status bytes 0, 1 and 2 and associated parameter bytes from the FDC.

COMMAND PHASE

COMMAND 1	MT	MFM	SK	1	0	1	1	0
COMMARD 2	EC	0	0	0	0	HD	USI	US0
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N
PARAMETER 5	EOT	–	–	–	–	–	–	EOT
PARAMETER 6	GSL	–	–	–	–	–	–	GSL
PARAMETER 7	DTL	–	–	–	–	–	–	DTL

EXECUTION PHASE: Data on device is verified.

RESULTS PHASE

ST0	0	IC0	0	0	NR	HD	US1	US0
ST1	EN	0	DE	0	0	ND	0	MA
ST2	0	CM	DD	NC	0	0	BC	MD
PARAMETER 1	C	–	–	–	–	–	–	C
PARAMETER 2	H	–	–	–	–	–	–	H
PARAMETER 3	R	–	–	–	–	–	–	R
PARAMETER 4	N	–	–	–	–	–	–	N

ERROR STATUS

During execution of the Verify command the following error states are reported by setting the appropriate error bit in the status registers ST0–ST2.

AREA	ERROR	STATUS SET
	Command successful Not Ready	None IC0, NR
ID	IDAM not detected C not matched (≠FFh) H not matched R not matched N not matched CRC error	IC0, MA ND ND ND ND DE
DATA	DAM not detected DDAM detected CRC error Incomplete at last sector	IC0, MA, MD CM DE, DD IC0, EN

AREA = Part of disk sector.
ERROR = Error state reported.

NOTE:
It is possible to have more than one error state reported at command termination.

VERIFY SEQUENCE

After the command has been accepted the FDC enters the head load sequence. The FDC then starts reading data and data is read until the required sector is found. When this happens, the sector is then read and its CRC verified but no data is transferred to the system. The sector number register (R) is incremented and the FDC starts looking for the next sector.

The command does not terminate if an error is encountered. Termination only occurs when the specified number of sectors has been read.

Any errors found will set the appropriate bit in the status bytes 0,1 and 2. The status bytes will only indicate that an error has occurred, but not the sector in which the error was encountered.

This command is identical to the Read Data command, except no data is transferred to the system.

4.3.25 Version

The Version command can be used by the system to identify the type of floppy controller being used.

COMMAND SEQUENCE

In command phase the system writes command byte 1 to the FDC. In results phase the system reads the version status byte (VER) from the FDC.

COMMAND PHASE

COMMAND 1	0	0	0	1	0	0	0	0

RESULTS PHASE

PARAMETER 1	VER	–	–	–	–	–	–	VER

NOTE:

The Version status byte is programmable (see VERSET command), the VER register is not cleared by a software reset, VER is set to 90h by a hardware reset.

4.3.26 VERSET

The VERSET command is used to set the floppy disk controller version number that is read during the VERSION command. The version number should normally be set to 90h to indicate that the controller is compatible with the 82077 floppy disk controller.

COMMAND SEQUENCE

In command phase the system writes command 1 and parameter 1 bytes to the FDC. There is no execution or results phases.

COMMAND PHASE

COMMAND 1	0	0	1	1	0	0	0	0
PARAMETER 1	VER	–	–	–	–	–	–	VER

NOTE:

VER is read by the VERSION command. A software reset has no effect on the VER register.

4.3.27 Lock

The Lock command allows the user to protect the status of the FIFO parameters in the event of a software reset.

COMMAND SEQUENCE

In command phase the system writes command byte 1 to the FDC. In results phase the system reads the LOC byte returned by the FDC.

COMMAND PHASE

COMMAND 1	LOC	0	0	1	0	1	0	0

RESULTS PHASE

PARAMETER 1	0	0	0	LOC	0	0	0	0

When set (LOC=1) the parameters DFI, FTH and PTN set by the configure command are not cleared by a software reset.

The LOC bit is cleared to 0 (inactive) by a hardware reset.

NOTE:

A software reset is any reset issued via the DSR or DOR registers.

4.3.28 Powerdown Mode

The Powerdown command allows the system to set the powerdown characteristics of the FDC.

COMMAND SEQUENCE

In command phase the system writes command 1 and parameter 1 to the FDC. In results phase the system reads the parameter byte returned by the FDC.

COMMAND PHASE

COMMAND 1	0	0	0	1	0	1	1	1
PARAMETER 1	0	0	0	0	0	FTR	MDL	APD

RESULTS PHASE

PARAMETER 1	0	0	0	0	0	FTR	MDL	APD

The POWERDOWN MODE register is only reset by a hardware reset. Software resets have no effect. When RSTDRV is active FTR, MDL and APD are cleared.

4.4 SPECIAL DATA FORMATS

The FDC supports four different data formats:

1A) SYSTEM 3740 FM (IBM)

1B) SYSTEM 34 MFM (IBM)

2A) Perpendicular MFM 500K Bits/Second (Toshiba)

2B) Perpendicular MFM 1M Bits/Second (Toshiba)

Formats 1A and 1B are the default data formats, other data formats have to be explicitly requested by issuing the Perpendicular command.

4.4.1 Format Outline

All four supported formats have some common features as follows:

1. Synchronization is done using special data formats with missing clock marks, this is true for both FM and MFM formats.
2. Data is written to or read from the device most significant bit first (D7, D6, D5,....D0)
3. Start of tracks is synchronized to INDEX mark.
4. Track format is independent of track number.
5. CRC is always 16 bit, written D15–D8 and D7–D0.
6. CRC for sector identifier (IDAM) is calculated from all data between the SYNC and CRC (for System 3740 format, data used to generate the CRC is FE*, CYL, HED, SEC, NO).
7. CRC for sector data is calculated from all data between the SYNC and CRC (for System 3740 it is FB* or F8* and all DATA).

4.4.2 Special Data Formats

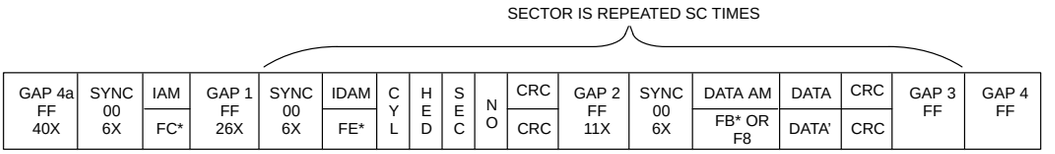
To allow the FDC to synchronize to the incoming serial data, special characters are written with missing clock marks, these are shown followed by a asterisk for easy identification (e.g. FC*).

FIELD	FM DATA	MFM DATA	
IAM	FC*	C2*	Index Address Mark
IDAM	FE*	A1*	ID Address Mark
DAM	FB*	A1*	Data Address Mark
DDAM	F8*	A1*	Deleted Data Address Mark

All values in the table are hexadecimal.

4.4.3 System 3740 Format (IBM)

System 3740 Format is FM. This is recorded at either 125, 150 or 250K bits/second.



All data is expressed in hexadecimal. 'N indicates the number of bytes in the section. If N is not specified then the number of bytes is programmable. * Indicates special data format with missing clock marks.

Values not specified; CYL, HED, SEC, NO are all programmable and are specified separately for each sector written.

The data written during the track format is defined in the Write ID command.

4.4.4 System 34 Format (IBM)

System 34 Format is MFM. This is recorded at either 250, 300, 500K bits/second, or 1 Mbps.

SECTOR IS REPEATED SC TIMES

GAP 4a	SYNC	IAM	GAP 1	SYNC	IDAM	CYL	HED	SEC	NO	CRC	GAP 2	SYNC	DATA AM	DATA	CRC	GAP 3	GAP 4
4E 80X	00 12X	C2* 3X FC*	4E 50X	00 12X	A1* 3X FE					CRC	4E 22X	00 12X	A1*3X FB OR F8	DATA	CRC	4E	4E

All data is expressed in hexadecimal. 'N indicates the number of bytes in the section. If N is not specified, then the number of bytes is programmable. * indicates special format data with missing clock marks.

Values not specified; CYL, HED, SEC, NO are all programmable and are specified separately for each sector written.

The data written during the track format is defined in the Write ID command.

4.4.5 Perpendicular 500K Format (TOSHIBA)

Perpendicular Format is MFM. This is recorded at 500K bits/second. Perpendicular mode is very similar to SYSTEM 34 format except for the timing of data write and SYNC.

SECTOR IS REPEATED SC TIMES

GAP 4a	SYNC	IAM	GAP 1	SYNC	IDAM	CYL	HED	SEC	NO	CRC	GAP 2	SYNC	DATA AM	DATA	CRC	GAP 3	GAP 4
4E 80X	00 12X	C2* 3X FC*	4E 50X	00 12X	A1* 3X FE					CRC	4E 22X	00 12X	A1*3X FB OR F8	DATA	CRC	4E	4E

All data is expressed in hexadecimal. 'N indicates the number of bytes in the section. If N is not specified, then the number of bytes is programmable. * Indicates special data format with missing clock marks.

Values not specified; CYL, HED, SEC, NO are all programmable and are specified separately for each sector written.

The data written during the track format is defined in the Write ID command.

4.4.6 Perpendicular 1M Format (TOSHIBA)

Perpendicular Format is MFM. This is recorded at 1M bits/second. Perpendicular mode is very similar to SYSTEM 34 format except Gap 2 is larger (41/22) and timing of write data and SYNC is different.

SECTOR IS REPEATED SC TIMES

GAP 4a	SYNC	IAM	GAP 1	SYNC	IDAM	CYL	HED	SEC	NO	CRC	GAP 2	SYNC	DATA AM	DATA	CRC	GAP 3	GAP 4
4E 80X	00 12X	C2* 3X FC*	4E 50X	00 12X	A1* 3X FE					CRC	4E 41X	00 12X	A1* 3X FB OR F8	DATA	CRC	4E	4E

All data is expressed in hexadecimal. 'N indicates the number of bytes in the section. If N is not specified, then the number of bytes is programmable. * indicates special format data with missing clock marks.

Values not specified CYL, HED, SEC, NO are all programmable and and are specified separately for each sector written.

The data written during the track format is defined in the Write ID command.

4.5 CYCLIC REDUNDANCY CHECK

The CRC is always 2 bytes, a CRC is appended to the sector identifier and the sector data.

SYSTEM 3740 FORMAT (FM)

The sector identifier CRC is calculated from the bytes: FE*, CYL, HED, SEC and NO. The sector data CRC is calculated from the bytes: FB* or F8* and all data.

MFM FORMATS

The sector identifier CRC is calculated from the bytes: A1*, A1*, A1*, FE, CYL, HED, SEC and NO. The sector data CRC is calculated from the bytes: A1*, A1* A1*, FB or F8 and all data.

4.6 FIFO

A 16 byte FIFO (First In First Out) is supported. The FIFO when enabled by the Configure command (DFI =0), reduces latency effects of high data transfer rates (1 Mbps) on the system.

The FIFO is only used during the data transfer phase of a command , at other times it is held clear.

DFI, FTH

- DFI = Disable FIfo
- FTH = Fifo THreshold

See Configure command for details of DFI bit and FTH control bits.

4.6.1 FIFO Operation

(WHEN DISABLED DFI=1)

The FIFO is used for both read and write data transfers. However when disabled it is forced to be only 1 byte deep.

(WHEN ENABLED DFI=0 READ)

The FIFO is used during the read data transfer phase. All data must be read from the FIFO at the end of a read sequence to allow the command to enter the results phase. Any data in the FIFO on receipt of a TC (Terminal Count) is discarded forcing the FIFO to become empty.

Data is read from the disk and written into the FIFO. When 16–FTH bytes have been written the FDC requests transfer to the system (DREQ or IRQ). Transfers continue until the FIFO becomes empty. At the end of a sector the FDC requests transfer to allow the FIFO to be emptied regardless of how full the FIFO is.

(When enabled DFI=0 write)

The FIFO is used during the write data transfer phase. Any data in the FIFO upon abnormal command termination is discarded.

Data is requested from the system and written into the FIFO. When the FIFO becomes full the data request is terminated. Data is written to the disc until the FIFO contains less than FTH bytes. When the FIFO contains less than FTH bytes the data is requested from the system until the FIFO is again full. When a TC (Terminal Count) is received the system data requests are terminated. Should TC occur before the end of a sector the remainder of the sector is padded with 00h.

4.7 WRITE

WRITE TIMING

The $\overline{\text{WREN}}$ signal (write) is only active for data writes.

WE–SIDE TIMING

For all multiple track writes a delay of (1.0 ms + 16 ms x GSL) is imposed between the end of the last sector written on side 0 of the disk and the side select signal changing.

For all writes (including write ID) a delay of (1.0 ms + 16 ms x GSL) is imposed after the last sector has been written and the results phase of the command being entered.

Some drives with tunnel erase heads require at least 1.0 ms to fully turn the write electronics off. Changing sides or stepping tracks in this time could cause corruption of the disk.

WRITE ID (FORMAT)

The sequence is the same for all data formats.

After the command has been accepted the FDC waits for detection of an index pulse. Upon detection of the index pulse the FDC starts to write track information as described in DATA FORMATS, the FDC then continues

to write GAP4b information until the next index pulse is detected.

SYSTEM 3740 (FM)
Data field only.

After reading and verifying the correct ID mark the FDC waits the GAP2 (11 bytes) before starting to write the SYNC, DATA AM, DATA, CRC and GAP3 (one byte only). When the GAP3 byte has been written the write signal is turned off.

SYSTEM 34 (MFM)
Data field only.

After reading and verifying the correct ID mark the FDC waits the GAP2 (22 bytes) before starting to write the SYNC, DATA AM, DATA, CRC and GAP3 (one byte only). When the GAP3 byte has been written write signal is turned off.

PERPENDICULAR 500K (MFM)
Data field only.

After reading and verifying the correct ID mark the FDC waits three bytes of GAP2 before starting to write 19 bytes of GAP2, SYNC, DATA AM, DATA, CRC and GAP3 (one byte only). When the GAP3 byte has been written the write signal is turned off.

The 19 bytes of GAP2 written is not properly recorded as the recording media will not have been preconditioned by the erase head.

PERPENDICULAR 1M (MFM)
Data field only.

After reading and verifying the correct ID mark the FDC waits 3 bytes of GAP2 before starting to write 38 Bytes of GAP2, SYNC, DATA AM, DATA, CRC and GAP3 (one byte only). When the GAP3 byte has been written the write signal is turned off.

The 38 bytes of GAP2 written are not properly recorded as the recording media will not have been preconditioned by the erase head.

4.8 SEEK

There are three possible types of seek operation; command Seek where the new cylinder number is given, command Relative Seek where the required cylinder offset is given and Recalibrate where the head is stepped out until track 0 is found or /255 steps have been completed.

The rate of stepping is defined by the Specify command. Step rate is programmable from 0.5 ms to 8 ms (1 Mbps).

All of the seek operations operate in the same way and follow the same basic rules:

1. If the head is on track 0 or track 0 is encountered during execution of a command requiring the head to be stepped out the command is terminated. The FDC does not allow the head to be stepped past track 0.
2. During execution of a seek command the READY input is sampled at the poll rate (1 ms). If the device is found to be not ready at any of the samples the seek operation is terminated.
3. After the last step of a seek operation the FDC waits one step period before termination of the seek command. The FDC waits one step period to allow the device to return valid status, this is especially true during Recalibrate where track 0 must be detected.

4.9 INTERRUPT

There are four sources of interrupts from within the FDC:

1. Device status change, via polling.
2. Seek end.
3. Commands in results phase (only some commands).
4. Data transfer in non DMA mode.

Device status change (1) and Seek end (2) interrupts only occur when the FDC is not executing a command requiring data transfer. Multiple interrupts (1 or 2) may occur and these are stored. Priorities for these are set as follows:

- When multiple interrupts have been generated those from the device with smallest number (drive 0) are serviced first via the sense interrupt status command.
- If a device status change interrupt is pending and a seek end interrupt occurs for the same device the device status change interrupt is lost.
- If a seek end interrupt is pending and device status change interrupt occurs for the same device the device change interrupt is lost.

The IRQ interrupt signal is generated from seek or change status interrupts as follows:

- The IRQ signal is regenerated after an interrupt service, providing a seek end interrupt is still pending.
- The IRQ signal is not regenerated after an interrupt service if only device status change interrupts are pending, of which there may be a further 3.
- The IRQ signal is generated for a status change interrupt even if the interrupt in the stack for the same device has not yet been serviced.

Commands in results phase (3) and Data transfer (4) interrupts only occur when the FDC is executing a command requiring data transfer. Only single interrupts (3 or 4) may occur, no storage or prioritization is applied.

The IRQ interrupt signal is generated from the command end and data transfer interrupts as required.

4.10 FDC DIGITAL DATA SEPARATOR

The FDC incorporates a digital data separator (DDS) that is suitable for use with a floppy disk or tape controller. It takes the “raw” FM or MFM data pulses from a disk or tape drive and outputs a clock at the bit rate and data pulses synchronized to that clock. These separated clock and data signals are internally connected to the floppy disk controller logic.

An internal clock of 24 MHz is derived from the 48 or 24 MHz clock input for data rates up to 1 Mbps.

The DDS can be configured for use with tape drives. This will increase the frequency range of the data separator at the cost of a slight reduction in jitter performance.

4.10.1 DDS Performance

The DDS uses an internal clock running at a nominal frequency of 24 MHz, which is derived from the input clock source of 24 or 48 MHz. Small variations in the input frequency will have little effect on the performance of the data separator except with regard to the lock range, which will be reduced by a roughly proportional amount. So an error in the input clock frequency of 1%, for example, will reduce the specified lock range by approximately 1%.

5.0 PARALLEL PORT

The DS83CH20 provides a flexible parallel port for the system designer. It provides five different parallel port modes, a programmable base address, programmable IRQ line, and programmable DMA channel. The parallel port can also be programmed into several power management modes. The configuration of the parallel port is provided through five configuration registers (007h – 00Bh).

These parallel port modes and the associated parallel interface protocols supported by the DS83CH20 are:

PARALLEL PORT MODE	PARALLEL INTERFACE PROTOCOL
ISA-Compatible Mode (SSP)	Compatibility, Nibble
PS/2-Compatible Mode	Byte
EPP (rev. 1.7) Mode	Enhanced Parallel Port (EPP)
EPP (rev. 1.9) Mode	Enhanced Parallel Port (EPP)
ECP Mode	Extended Capabilities Port (ECP)

In ISA–Compatible mode, the parallel port exactly emulates a standard ISA–style parallel port. The parallel port data bus (PD[7:0]) is uni–directional. The compatibility protocol transfers data to the peripheral device via PD[7:0] (forward direction). Note that the Nibble protocol permits data transfers from the peripheral device (reverse direction) by using four peripheral status signal lines to transfer four bits data at a time.

PS/2–Compatible mode differs from ISA–Compatible mode by providing bi–directional transfers on PD[7:0]. A bit is added to the PCON register to allow software control of the data transfer direction.

For both the ISA–Compatible and PS/2–Compatible modes, the actual data transfer over the parallel port interface is accomplished by software handshake (i.e., automatic hardware handshake is not used). Software controls data transfer by monitoring handshake signal status from the peripheral device via the PSTAT register and controlling handshake signals to the peripheral device via the PCON register.

EPP mode provides bi–directional transfers on PD[7:0]. The DS83CH20 automatically generates the address and data strobes in hardware.

ECP is a high performance peripheral interface mode. This mode uses an asynchronous automatic handshake to transfer data over the parallel port interface. In addition, the parallel port contains a FIFO for transferring data in ECP mode. The ECP register set contains an Extended Control Register (ECR) that provides a wide range of functions including the ability to operate the parallel port in either ECP, ISA–Compatible, or PS/2–Compatible modes.

NOTE:
In general, this document describes parallel port operations and functions in terms of how the DS83CH20 parallel port hardware operates. Detailed descriptions of the parallel interface protocols are beyond the scope of this document. Readers should refer to the proposed IEEE Standard 1284 for detailed descriptions of the Compatibility, Nibble, Byte, EEP, ECP protocols.

Special circuitry on the DS83CH20 prevents it from being powered up or being damaged while a parallel port peripheral is powered on and the DS83CH20 is powered off.

5.1 PARALLEL PORT REGISTERS

This section is organized into three sub–sections: ISA–Compatible and PS/2–Compatible Modes, EPP Mode, and ECP Mode. Since the register sets are similar for ISA–Compatible and PS/2–Compatible modes (differing by a direction control bit in the PCON register) the register set descriptions are combined. The EPP mode and ECP mode register sets are described separately. Each register set description contains the I/O address assignment and a complete description of the registers and register bits. Note that the PSTAT (parallel status) and PCON (parallel control) registers are common to all modes and for completeness are repeated in each sub–section. Any difference in bit operations for a particular mode is noted in that particular register description.

The registers provide parallel port control/status information and data paths for transferring data between the parallel port interface and the 8–bit host interface. All registers are accessed as byte quantities.

The base address is determined via software configuration by programming the appropriate configuration register; namely, the Parallel Port Base Address Select Register (009h). The parallel port can be programmed for a base address of 100h to 8F8h on 8–byte boundaries.

During a hard reset (RSTDRV asserted), the DS83CH20 registers are set to predetermined default states. The default values are indicated in the individual register description.

The following nomenclature is used for register access attributes:

RO **Read Only.** Note that for registers with read–only attributes, writes to the I/O address have no affect on parallel port operations.

WO **Write Only.** Note that for registers with write–only attributes, data read will be indeterminate.

R/W **Read/Write**. A register with this attribute can be read and written. Note that individual bits in some read/write registers may be read only.

5.1.1 ISA–Compatible and PS/2–Compatible Modes

This section contains the registers used in ISA Compatible and PS/2 Compatible modes. The I/O address assignment for this register set is shown in Section 5.1.1.1 and the register descriptions are presented in the order that they appear in the table.

PARALLEL PORT REGISTER (ISA–COMPATIBLE AND PS/2–COMPATIBLE) Table 5–1

PARALLEL PORT REGISTER ADDRESS ACCESS (AEN=0) BASE +	ABBREVIATION	REGISTER NAME	ACCESS
0h	PDATA	Data Register	R/W
1h	PSTAT	Status Register	RO
2h	PCON	Control Register	R/W

5.1.1.1 PDATA – Parallel Port Data Register (ISA–Compatible and PS/2–Compatible modes)

I/O Address: Base + 00h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

ISA–Compatible Mode

The PDATA register is a unidirectional data port that transfers 8–bit data from the host to the peripheral device (forward transfer). A write to this register drives the written data onto PD[7:0]. Reads of this register should not be performed in ISA Compatible mode.

PS/2–Compatible Mode

The PDATA register is a bi–directional data port that transfers 8–bit data between the peripheral device and host. The direction of transfer is determined by the $\overline{DIR}$ bit in the PCON register. If $\overline{DIR}$ = 0 (forward direction), and the host writes to this register, the data is stored in the PDATA register and driven onto PD[7:0]. If $\overline{DIR}$ = 1 (reverse direction), a host read of this register returns the data on PD[7:0]. Note that read data is not stored in the PDATA register.

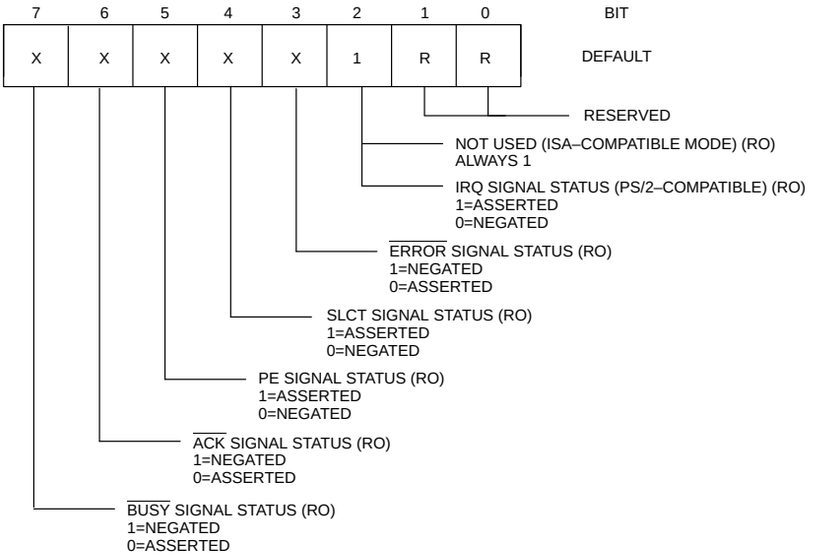
BIT	DESCRIPTION
7:0	**Parallel Port Data.** Bits [7:0] correspond to parallel port data lines PD[7:0] and ISA bus data lines SD[7:0].

5.1.1.2 PSTAT – Status Register (ISA–Compatible and PS/2–Compatible Modes)

I/O Address: Base + 01h
Default Value: XXXX X1RR
Attribute: Read Only
Size: 8 bits

The PSTAT register provides the status of certain parallel port signals and whether a CPU interrupt has been generated by the parallel port. This register indicates the current state of the BUSY, $\overline{ACK}$, PE, SLCT, $\overline{ERROR}$ and IRQ signals.

STATUS REGISTER (ISA–COMPATIBLE AND PS/2–COMPATIBLE MODES) Figure 5–1



NOTE:
X = Default value is determined by signal state at reset.

BIT	DESCRIPTION
7	**$\overline{BUSY}$ Status (BUSYS).** This bit indicates the state of the parallel port interface BUSY signal. When BUSY is asserted, BUSYS=0. When BUSY is negated, BUSYS=1. This bit is an inverted version of the parallel port BUSY signal.
6	**$\overline{ACK}$ Status (ACKS).** This bit indicates the state of the parallel port interface $\overline{ACK}$ signal. This bit indicates when the peripheral has received a data byte and is ready for another. When $\overline{ACK}$ is asserted, ACKS=0. When $\overline{ACK}$ is negated, ACKS=1. Note that if interrupts are enabled (via bit 4 of the PCON register), the assertion of the $\overline{ACK}$ signal generates an interrupt to the CPU.
5	**PE Status (PES).** This bit indicates the state of the parallel port interface PE signal. This bit indicates when an error has occurred in the peripheral paper path (e.g., out of paper). When PE is asserted, PE=1. When PE is negated, PE=0.
4	**SLCT Status (SELS).** This bit indicates the state of the parallel port interface SLCT signal. When the SLCT signal is asserted, SELS=1. When the SLCT signal is negated, SELS=0.

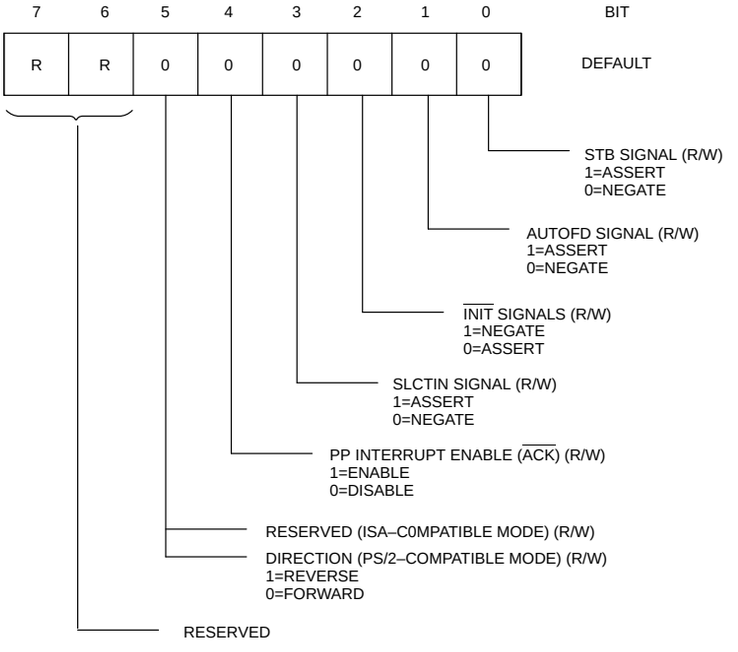
BIT	DESCRIPTION
3	**$\overline{\text{ERROR}}$ Status (ERRORS).** This bit indicates the state of the parallel port interface, $\overline{\text{ERROR}}$ signal being driven by the peripheral device. When the $\overline{\text{ERROR}}$ signal is asserted, ERRORS=0. When the $\overline{\text{ERROR}}$ signal is negated, ERRORS=1.
2	**Parallel Port Interrupt Status (PIRQ).** This bit indicates a CPU interrupt by the parallel port. PIRQ indicates that the printer has accepted the previous character and is ready for another. In ISA–Compatible mode, interrupt status is not reported in this register and this bit is always 1. In PS/2–Compatible mode, if interrupts are enabled via the PCON register and the $\overline{\text{ACK}}$ signal is asserted (low–to–high transition), PIRQ is set to a 0 (and an IRQ is generated to the CPU). The DS83CH20 sets PIRQ to 1 when this register is read or by a hard reset. If interrupts are disabled via the PCON register, this bit is never set to 0.
1,0	**Reserved.**

5.1.1.3 PCON – Control Register (ISA–Compatible and PS/2–Compatible Modes)

I/O Address: Base + 02h
Default Value: RR00 0000
Attribute: Read/Write
Size: 8 bits

The PCON register controls certain parallel port interface signals and enables/disables parallel port interrupts. This register permits software to control the $\overline{\text{STB}}$, $\overline{\text{AUTOFD}}$, $\overline{\text{INIT}}$, and $\overline{\text{SLCTIN}}$ signals. For PS/2–Compatible mode, this register also controls the direction of transfer on PD[7:0].

CONTROL REGISTER (ISA–COMPATIBLE AND PS/2–COMPATIBLE MODES) Figure 5–2



BIT	DESCRIPTION
7,6	**Reserved.**
5	**Reserved (ISA–Compatible Mode).** Not used and undefined when read. Writes have no affect on parallel port operations **Direction ($\overline{DIR}$) (PS/2–Compatible Mode).** This bit is used to control the direction of data transfer on the parallel port data bus (PD[7:0]). When $\overline{DIR}$=0, PD[7:0] are outputs. When $\overline{DIR}$ =1, PD[7:0] are inputs.
4	**$\overline{ACK}$ Interrupt Enable (ACKINTEN).** ACKINTEN enables CPU interrupts to be generated when the $\overline{ACK}$ signal on the parallel port interface is asserted. When ACKINTEN=1, a CPU interrupt is generated when $\overline{ACK}$ is asserted. When ACKINTEN=0, the $\overline{ACK}$ interrupt is disabled.
3	**SLCTIN Control (SELINC).** This bit controls the $\overline{SLCTIN}$ signal. SELINC is set to 1 to select the printer. When SELINC=1, the $\overline{SLCTIN}$ signal is asserted. When SELINC=0, the $\overline{SLCTIN}$ signal is negated. This bit is the inverse of the $\overline{SLCTIN}$ pin.
2	**$\overline{INIT}$ Control (INITC).** This bit controls the $\overline{INIT}$ signal. When INITC=1, the $\overline{INIT}$ signal is negated. When INITC=0, the $\overline{INIT}$ signal is asserted.
1	**AUTOFD Control (AUTOFDC).** This bit controls the $\overline{AUTOFD}$ signal. AUTOFDC is set to 1 to instruct the printer to advance the paper one line each time a carriage return is received. When AUTOFDC=1, the $\overline{AUTOFD}$ signal is asserted. When AUTOFDC=0, the $\overline{AUTOFD}$ signal is negated. This bit is the inverse of the $\overline{AUTOFD}$ pin.
0	**STROBE Control (STROBEC).** This bit controls the $\overline{STB}$ signal. The $\overline{STB}$ signal is set active to instruct the printer to accept the character being presented on the data lines. When STROBEC=1, the $\overline{STB}$ signal is asserted. When STROBEC=0, the $\overline{STB}$ signal is negated. This bit is the inverse of the $\overline{STB}$ pin.

5.1.2 EPP Mode

This section contains the registers used in EPP mode. The I/O address assignment for this register set is shown in Section 5.1.2.1 and the register descriptions are presented in the order that they appear in the table. These registers are accessible only when the device is properly configured via the configuration registers. More specifically, the Parallel Port Enable [0] must be set to 1 and Parallel Port Mode [2:0] must be 010 (for EPP 1.7 operation) or 011 (for EPP 1.9 operation).

PARALLEL PORT REGISTERS (EPP MODE) Table 5–2

PARALLEL PORT REGISTER ADDRESS ACCESS (AEN=0) BASE +	ABBREVIATION	REGISTER NAME	ACCESS
0h	PDATA	Data Register	R/W
1h	PSTAT	Status Register	RO
2h	PCON	Control Register	R/W
3h	ADDSTR	Address Strobe Register	R/W
4h – 7h	DATASTR	Data Strobe Register	R/W

5.1.2.1 PDATA–Parallel Port Data Register (EPP Mode)

I/O Address: Base + 00h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The PDATA register is a bi–directional data port that transfers 8–bit data between the peripheral device and host. The direction of transfer is determined by the $\overline{DIR}$ bit in the PCON register. If $\overline{DIR}$=0 (forward direction) and the host writes to this register, the data is stored in the PDATA register and driven onto PD[7:0]. If $\overline{DIR}$=1 (reverse direction), a host read of this register returns the data on PD[7:0]. However, read data is not stored in the PDATA register.

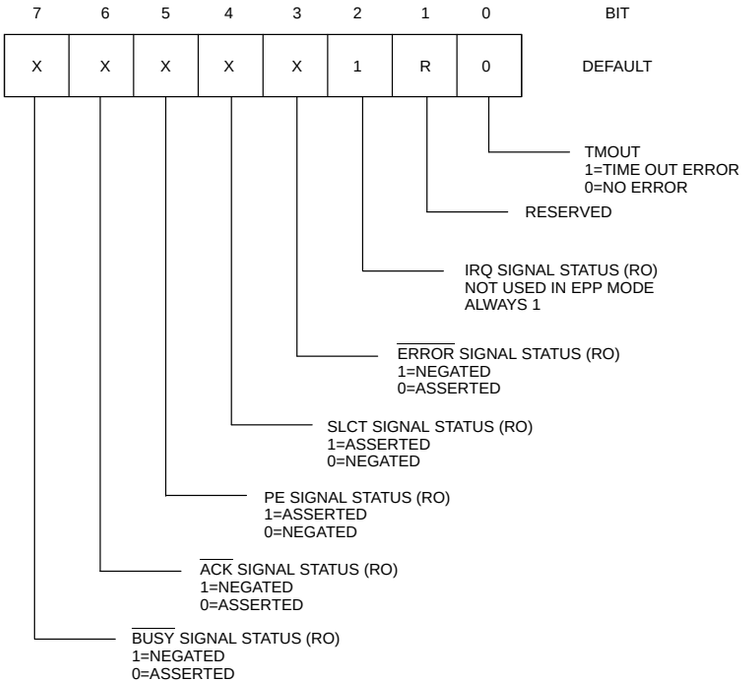
BIT	DESCRIPTION
7:0	**Parallel Port Data.** Bits [7:0] correspond to parallel port data lines PD[7:0] and ISA bus data lines.

5.1.2.2 PSTAT–Status Register (EPP Mode)

I/O Address: Base + 01h
Default Value: XXXX X1R0
Attribute: Read/Write
Size: 8 bits

The PSTAT register provides the status of certain parallel port signals. This register indicates the current state of the BUSY, $\overline{ACK}$, PE, SLCT, and $\overline{ERROR}$ signals.

STATUS REGISTER (EPP MODE) Figure 5–3



NOTE:
X = Default value is determined by signal state at reset.

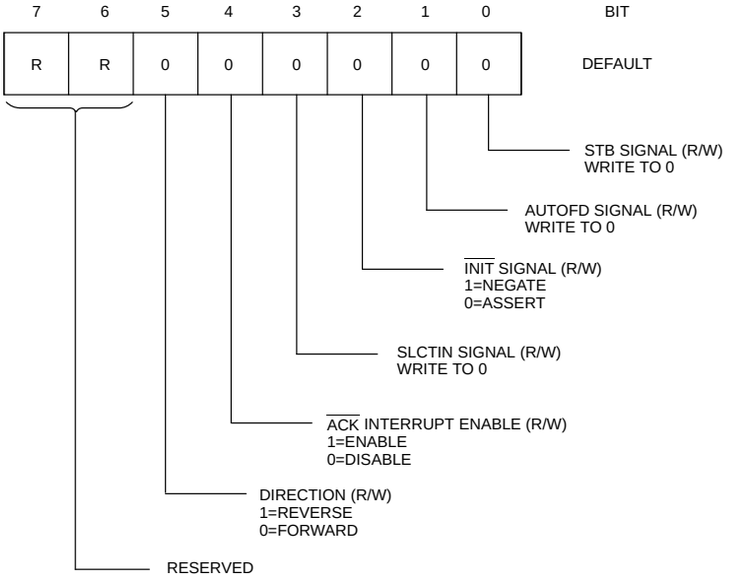
BIT	DESCRIPTION
7	**$\overline{\text{BUSY}}$ Status (BUSYS):** This bit indicates the state of the parallel port interface BUSY signal. When BUSY is asserted, BUSYS=0. When BUSY is negated, BUSYS=1. This bit is an inverted version of the parallel port BUSY signal.
6	**$\overline{\text{ACK}}$ Status (ACKS):** This bit indicates the state of the parallel port interface $\overline{\text{ACK}}$ signal. This bit indicates when the peripheral has received a data byte and is ready for another. When $\overline{\text{ACK}}$ is asserted, ACKS=0. When $\overline{\text{ACK}}$ is negated, ACKS=1. Note that if interrupts are enabled (via bit 4 of the PCON Register), the assertion of the $\overline{\text{ACK}}$ signal generates an interrupt to the CPU.
5	**PE Status (PES):** This bit indicates the state of the parallel port interface PE signal. This bit indicates when an error has occurred in the peripheral paper path (e.g.,out of paper). When PE is asserted, PES=1. When PE is negated, PES=0.
4	**SLCT Status (SELS):** This bit indicates the state of the parallel port interface SLCT signal. When the SLCT signal is asserted, SELS=1. When the SLCT signal is negated, SELS=0.
3	**$\overline{\text{ERROR}}$ Status (ERRORS):** This bit indicates the state of the parallel port interface, $\overline{\text{ERROR}}$ signal being driven by the peripheral device. When the $\overline{\text{ERROR}}$ signal is asserted, ERRORS=0. When the $\overline{\text{ERROR}}$ signal is negated, ERRORS=1.
2	**Parallel Port Interrupt (PIRQ):** In EPP mode, the interrupt status is not reported in this register and this bit is always 1.
1	**Reserved.**
0	**TMOUT Status (TMOUTS):** This bit indicates whether a 10 µs time out error has occurred. TMOUTS=0 when no time out error has occurred. TMOUTS=1 when an error has been detected. This bit is cleared to 0 after PSTAT is read, i.e., consecutive reads (after the first read) always return 0. This bit is also cleared when EPP is enabled and by a RESET.

5.1.2.3 PCON–Control Register (EPP Mode)

I/O Address: Base + 02h
Default Value: RR00 0000
Attribute: Read/Write
Size: 8 bits

The PCON register controls certain parallel port interface signals, enables/disables parallel port interrupts, and selects the direction of data transfer on PD[7:0]. This register permits software to control the $\overline{\text{INIT}}$ signal. Note that in the EPP parallel interface protocol, the $\overline{\text{STB}}$, $\overline{\text{AUTOFD}}$, and $\overline{\text{SLCTIN}}$ signals are automatically generated by the parallel port and are not controlled by software.

CONTROL REGISTER (EPP MODE) Figure 5–4



BIT	DESCRIPTION
7,6	**Reserved.**
5	**Direction (DIR):** This bit is used to control the direction of data transfer on the parallel port data bus (PD[7:0]). When DIR=0 (forward direction), PD[7:0] are output. When DIR=1 (reverse direction), PD[7:0] are inputs.
4	**ACK Interrupt Enable (ACKINTEN):** ACKINTEN enables CPU interrupts to be generated when the ACK signal on the parallel port interface is asserted. When ACKINTEN=0, the ACK interrupt is disabled.
3	**SLCTIN Control (SELINC):** Write to 0 when programming this register. This bit must be 0 for the parallel port handshake to operate properly. This bit is the inverse of the SLCTIN pin.
2	**INIT Control (INITC):** This bit controls the INIT signal. When INITC=1, the INIT signal is negated. When INITC=0, the INIT signal is asserted.
1	**AUTOFD Control (AUTOFDC):** Write to 0 when programming this register. This bit is the inverse of the AUTOFD pin.
0	**STROBE Control (STROBEC):** Write to 0 when programming this register. This bit must be 0 for the parallel port handshake to operate properly. This bit is the inverse of the STB pin.

5.1.2.4 ADDSTR–EPP Auto Address Strobe Register (EPP Mode)

I/O Address: Base + 03h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The ADDSTR register provides a peripheral address to the peripheral (via PD[7:0]) during a host address write operation and to the host (via PD[7:0]) during a host address read operation. An automatic address strobe is generated on the parallel port interface when data is read from or written to this register.

BIT	DESCRIPTION
7:0	**EPP Address:** Bits [7:0] correspond to SD[7:0] and PD[7:0].

5.1.2.5 DATASTR–Auto Data Strobe Register (EPP Mode)

I/O Address: Base + 04h, 05h, 06h, 07h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The DATASTR register provides data from the host to the peripheral device (via PD[7:0]) during host write operations and from the peripheral device to the host (via PD[7:0]) during a host read operation. An automatic data strobe is generated on the parallel port interface when data is read from or written to this register. To maintain compatibility with a 32–bit host interface, 4 consecutive byte address locations are provided for transferring data.

BIT	DESCRIPTION
7:0	**EPP Address:** Bits [7:0] correspond to SD[7:0] and PD[7:0].

5.1.3 ECP Mode

This section contains the registers used in ECP mode. The I/O address assignment for this register set is shown in Table 5–3 and the register descriptions are presented in the order that they appear in the table. These registers are accessible only when the device is properly configured via the configuration registers. More specifically, Parallel Port Enable [0] must be set to 1 and the Parallel Port Mode [2:0] must be 100. The Extended Control Register (ECR) permits various modes of operation. Note that ECR[7:5]=000 selects ISA–Compatible mode and ECR[7:5]=001 selects PS/2–Compatible mode. These modes are discussed in Section 5.1.1, ISA–Compatible and PS/2 Compatible modes. The other modes selected by ECR[7:5] are discussed in this section.

PARALLEL PORT REGISTERS (ECP MODE) Table 5–3

PARALLEL PORT REGISTER ADDRESS ACCESS (AEN=0) BASE +	ABBREVIATION	REGISTER NAME	ACCESS	
			ECR[7:5]	READ/ WRITE ATTRI–BUTE
0h	DATAR	Parallel Port Data Register	000,001	R/W
0h	ECPAFIFO	ECP Address/RLE FIFO	011	WO
1h	PSTAT	Status Register	All	RO
2h	PCON	Control Register	All	R/W
400h	SDFIFO	Standard Parallel Port Data FIFO	010	WO
400h	ECPDFIFO	ECP Data FIFO	011	R/W
400h	TFIFO	Test FIFO	110	R/W
400h	ECPCFGA	ECP Configuration A	111	R/O
401h	ECPCFGB	ECP Configuration B	111	R/O
402h	ECR	Extended Control Register	All	R/W

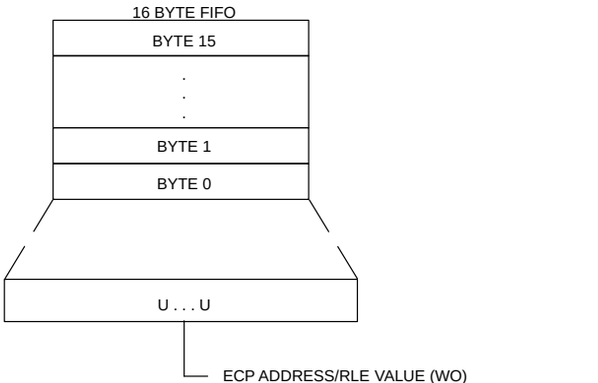
NOTE:
A register is accessible when the ECR[7:5] field contains the value specified in the ECR[7:5] column. The register is not accessible if the ECR[7:5] field does not match the value specified in this column. The term “All” means that the register is accessible in all modes selected by ECR[7:5].

5.1.3.1 ECPAFIFO–ECP Address/RLE FIFO Register (ECP Mode)

I/O Address: Base + 00h
Default Value: UUUU UUUU (Undefined)
Attribute: Write
Size: 8 bits

The ECPAFIFO register provides a channel address or a Run Length Count (RLE) to the peripheral, depending on the state of bit 7. This I/O address location is only used in ECP mode (ECR bits[7:5]=011). In this mode, bytes written to this register are placed in the parallel port FIFO and transmitted over PD[7:0] using ECP protocol.

ECP ADDRESS/RLE FIFO REGISTER (ECP MODE) Figure 5–5



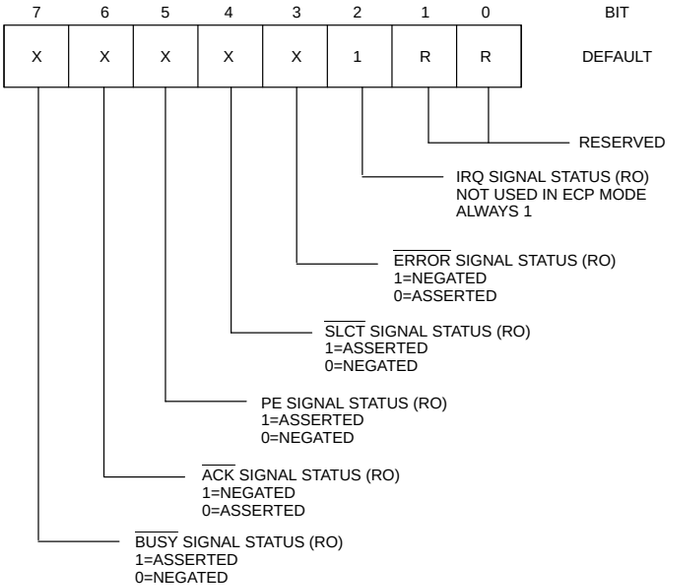
NOTE:
U=UNDEFINED

BIT	DESCRIPTION
7:0	**ECP Address/RLE Value:** Bits[7:0] correspond to parallel port data lines PD[7:0] and ISA Bus data lines SD[7:0]. The Peripheral device should interpret bits [6:0] as a channel address when bit 7=1 and as a run length count when bit 7=0. Note that this interpretation is performed by the peripheral device and the value of bit 7 has no affect on DS83CH20 operations. Note that the DS83CH20 asserts $\overline{\text{AUTOFD}}$ to indicate that the information on PD[7:0] represents an ECP address/RLE count. The DS83CH20 negates $\overline{\text{AUTOFD}}$ (drives high) when PD[7:0] is transferring data. The operation of this register is defined only for the forward direction.

5.1.3.2 PSTAT–Status Register (ECP Mode)

I/O Address: Base + 01h
Default Value: XXXX X1RR
Attribute: Read
Size: 8 bits

STATUS REGISTER (ECP MODE) Figure 5–6



NOTE:
X = Default value is determined by the state of the corresponding signal pin at reset.

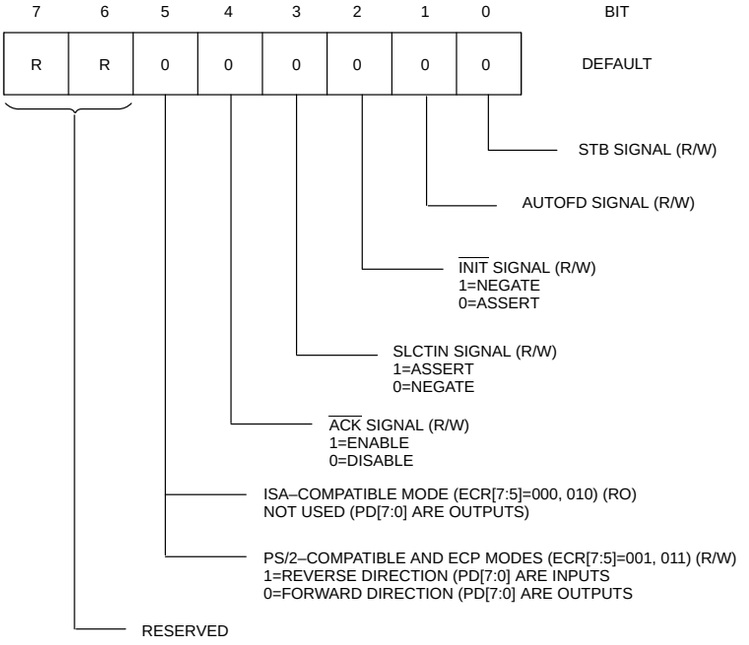
BIT	DESCRIPTION
7	**$\overline{\text{BUSY}}$ Status (BUSYS):** This bit indicates the state of the parallel port interface BUSY signal. When BUSY is asserted, BUSYS=0. When BUSY is negated, BUSYS=1. This is an inverted version of the parallel port BUSY signal. Refer to Section 5.2.3 ECP Mode for more detail.
6	**$\overline{\text{ACK}}$ Status (ACKS):** This bit indicates the state of the parallel port interface $\overline{\text{ACK}}$ signal. This bit indicates when the peripheral has received a data byte and is ready for another. When $\overline{\text{ACK}}$ is asserted, $\overline{\text{ACK}}$=0. When $\overline{\text{ACK}}$ is negated, ACKS=1. Note that if interrupts are enabled (via bit 4 of the PCON Register), the assertion of the $\overline{\text{ACK}}$ signal generates an interrupt to the CPU. Refer to section 5.2.3, ECP Mode, for more detail.
5	**PE Status (PES):** This bit indicates the state of the parallel port interface PE signal. This bit indicates when an error has occurred in the peripheral paper path (e.g., out of paper). When PE is asserted, PES=1. When PE is negated, PES=0.
4	**SLCT Status (SELS):** This bit is used in all parallel port modes and indicates the state of the parallel port interface SLCT signal. When the SLCT signal is asserted, SELS=1. When the SLCT signal is negated, SELS=0.
3	**$\overline{\text{ERROR}}$ Status (ERRORS):** This bit is used in all parallel port modes and indicates the state of the parallel port interface $\overline{\text{ERROR}}$ signal being driven by the peripheral device. When the $\overline{\text{ERROR}}$ signal is asserted, ERRORS=0. When the $\overline{\text{ERROR}}$ signal is negated, ERRORS=1.
2	**Parallel Port Interrupt (PIRQ):** In ECP mode, interrupt status is not reported in this register and this bit is always 1.
1,0	**Reserved.**

5.1.3.3 PCON–Control Register (ECP Mode)

I/O Address: Base + 02h
Default Value: RR00 0000
Attribute: Read/Write
Size: 8 bits

The PCON register controls certain parallel port interface signals, enables/disables parallel port interrupts, and selects the direction of data transfer on PD[7:0]. Note that the function of some bits depends on the programming of the ECR.

CONTROL REGISTER (ECP MODE) Figure 5–7



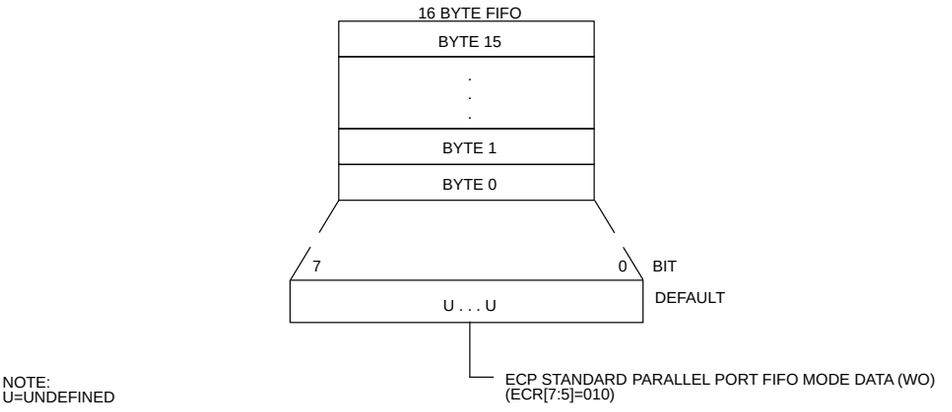
BIT	DESCRIPTION
7,6	**Reserved.**
5	**Direction (DIR):** This bit is used to control the direction of data transfer on the parallel port data bus (PD[7:0]). When DIR=0 (forward direction), PD[7:0] are outputs. When DIR=1 (reverse direction), PD[7:0] are inputs.
4	**Interrupt Enable (ACK) (IRQEN):** IRQEN enables interrupts to the CPU to be generated when the ACK signal on the parallel port interface is asserted and is used in all parallel port interface modes. When IRQEN=1, a CPU interrupt is generated when ACK is asserted. When IRQEN=0, parallel port interrupts are disabled.
3	**SLCTIN Control (SELINC):** This bit controls the SLCTIN signal. SELINC is set to 1 to select the printer. When SELINC=1, the SLCTIN signal is asserted. When SELINC=0, the SLCTIN signal is negated. This bit is the inverse of the SLCTIN pin.
2	**INIT Control (INITC):** This bit controls the INIT signal. When INITC=1, the INIT signal is negated. When INITC=0, the INIT signal is asserted.
1	**AUTOFD Control (AUTOFDC):** In ECP mode (ECR[7:5]=011), this bit has no effect. Refer to section 5.2.3 ECP, Mode, for more details. This bit is the inverse of the AUTOFD pin.
0	**STROBE Control (STROBEC):** In ECP mode or ISA–Compatible FIFO mode (ECR[7:5]=011, 010), this bit has no effect. Refer to section 5.2.3, ECP Mode, for more details. This bit is the inverse of the STB pin.

5.1.3.4 SDFIFO–Standard Parallel Port Data FIFO

I/O Address: Base + 400h and (ECR[7:5]=010)
Default Value: UUUU UUUU (undefined)
Attribute: Write
Size: 8 bits

SDFIFO is used to transfer data from the host to the peripheral when the ECR register is set for ISA–Compatible FIFO mode (bits[7:5]=010). Data bytes written or DMA'ed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard ISA–Compatible protocol. This mode is only defined for the forward direction. Note that bit 5 in the PCON register must be set to 0 for a forward transfer direction.

ECP ISA–COMPATIBLE DATA FIFO Figure 5–8



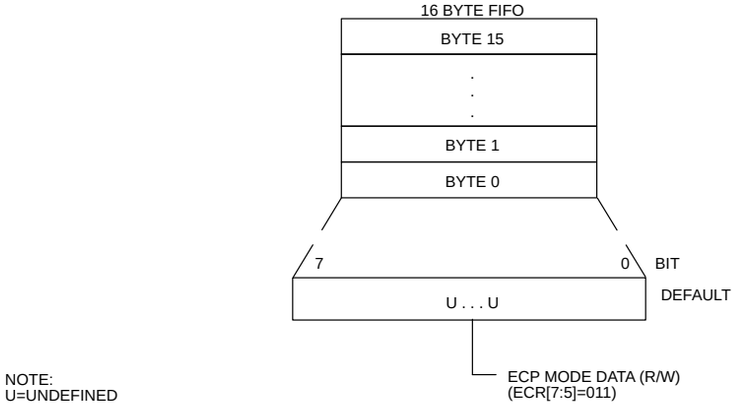
BIT	DESCRIPTION
7:0	**ECP Standard Parallel Port Data:** Bits [7:0] correspond to SD[7:0] and PD[7:0].

5.1.3.5 DFIFO–Data FIFO (ECP Mode)

I/O Address: Base + 400h and (ECR[7:5]=011)
Default Value: UUUU UUUU (undefined)
Attribute: Read/Write
Size: 8 bits

This I/O address location transfers data between the host and peripheral device when the parallel port is in ECP mode (ECR Bits[7:5]=011). Transfers use the parallel port FIFO. Data is transferred on PD[7:0] via hardware handshakes on the parallel port interface using ECP parallel port interface handshake protocol.

ECP DATA FIFO (ECP MODE) Figure 5–9



BIT	DESCRIPTION
7:0	**ECP Mode Data:** Data Bytes written or DMA'ed from the system to this FIFO in the forward direction (PCON bit 5=0) are transmitted to the peripheral by an ECP mode protocol hardware handshake. In the reverse direction (PCON bit 5=1) data bytes from the peripheral are transferred to the FIFO using the ECP mode protocol hardware handshake. Reads or DMAs from the FIFO return bytes of ECP data to the system. Bits[7:0] and PD[7:0]. Reading this register while in the forward direction (PCON bit 5=0) has no effect and data read is undefined. Writes to this register while in the reverse direction (PCON bit 5=1) have no effect and data written is ignored.

5.1.3.6 TFIFO–ECP Test FIFO Register (ECP Mode)

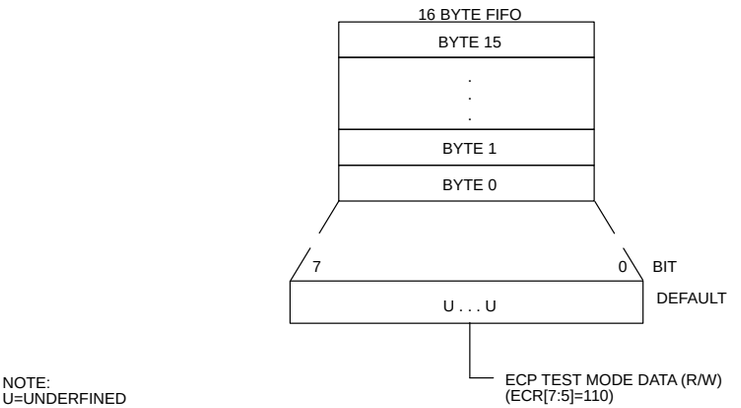
I/O Address: Base + 400h and (ECR[7:5]=110)
Default Value: UUUU UUUU (undefined)
Attribute: Read/Write
Size: 8 bits

The TFIFO register provides a test mechanism for the ECP mode FIFO. Test mode is enabled via the ECR register. In test mode (ECR[7:5]=110), data can be read, written or DMA'ed to/from the FIFO by accessing this register I/O address.

Data bytes may be read, written or DMA'ed to or from the system to this FIFO in any direction (PCON bit 5=0, 1). The parallel port interface signals are not affected by TFIFO accesses and TFIFO data is not transmitted to PD[7:0]. The test FIFO does not stall when overwritten or underrun. Data is simply rewritten or overrun. The full and the empty bits in the ECR always keep track of the correct FIFO state.

The test FIFO transfers data at the maximum ISA rate so that software can generate performance metrics. The FIFO write threshold can be determined by starting with a full TFIFO and emptying it a byte at a time until a service interrupt is set to 1 in the ECR. The FIFO read threshold can be determined by setting the direction bit in the PCON register to 1, and filling the FIFO a byte at a time until the service interrupt is set to 1 in the ECR.

ECP TEST FIFO REGISTER (ECP MODE) Figure 5–10



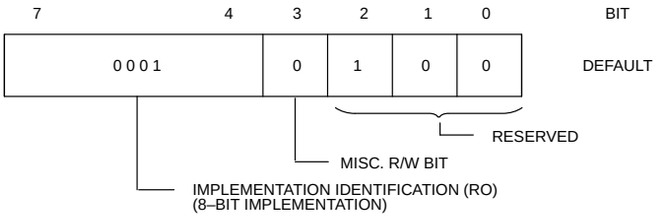
BIT	DESCRIPTION
7:0	**ECP Test FIFO:** Data: Bits[7:0] correspond to SD[7:0].

5.1.3.7 ECPCFGA–ECP Configuration A Register (ECP Mode)

I/O Address: Base + 400h and (ECR[7:5]=111)
Default Value: 0001 0100
Attribute: Read/Write
Size: 8 bits

The ECPCFGA register provides information about the ECP mode implementation. Access to this register is enabled by programming the ECR register (ECR[7:5]=111).

ECP CONFIGURATION A REGISTER (ECP MODE) Figure 5–11



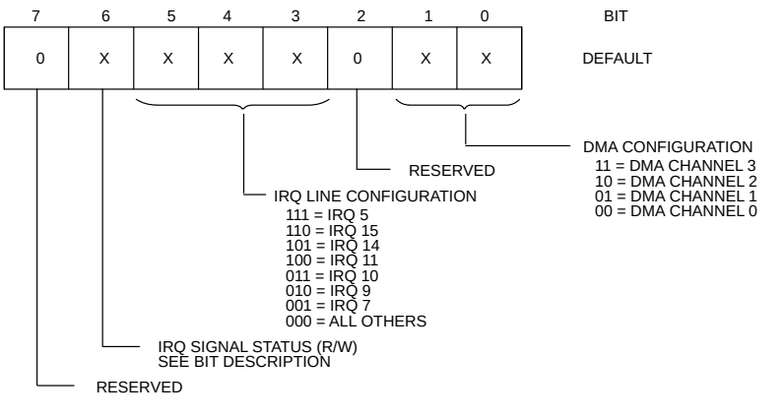
BIT	DESCRIPTION
7:4	**Implementation Identification (IMPID):** This field is hardwired to 0001 to indicate an 8–bit implementation (bit 4) and a pulsed interrupt (bit 7). This field is read only and writes have no affect.
3	**Misc. R/W Bit:** This bit may be used as a design–specific status bit. This bit may be read or written.
2:0	**Reserved.**

5.1.3.8 ECPCFGB–ECP Configuration B Register (ECP Mode)

I/O Address: Base + 401h and (ECR[7:5]=111)
Default Value: 0XXX X0XX
Attribute: Read
Size: 8 bits

Configuration Register B is a read–only register. Access to the ECPCFGB register is enabled by programming the ECR register (ECR[7:5]=111). Reading this register returns the configured parallel port interrupt line and its state as follows:

ECP CONFIGURATION B REGISTER (ECP MODE) Figure 5–12



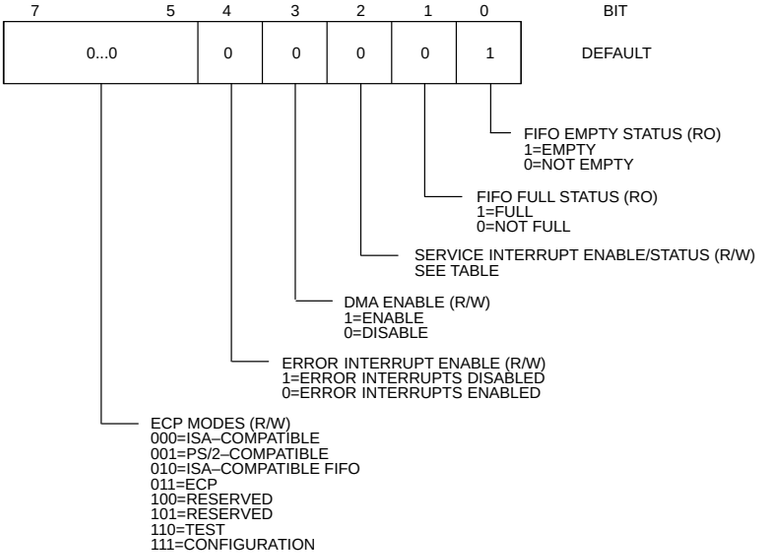
BIT	DESCRIPTION
7	**Reserved:** This bit always reads back as 0.
6	**INTRVALUE (INTRV):** This bit returns the value on the ISA IRQ line to determine possible conflicts. The value of the IRQ line is read back based on the parallel port interrupt selection in the DS83CH20 configuration registers. The IRQ line is tri–stated in ECP configuration mode (ECR[7:5]=111] to allow the state of the selected parallel port interrupt line to be read back. Note that the ACKINTEN bit in the PCON register must be written to 0 before the interrupt status can be read on this bit.
5:3	**IRQ Line Configuration:** 111: IRQ 5 selected, 110: IRQ 15, 101: IRQ 14, 100: IRQ 11, 011: IRQ 10, 010: IRQ 9, 001: IRQ 7, 000: all others.
2	**Reserved:** This bit always reads back as 0.
1,0	**DMA Configuration:** 11: DMA Channel 3 selected 10: DMA Channel 2 selected 01: DMA Channel 1 selected 00: DMA Channel 0 selected

5.1.3.9 ECR ECP–Extended Control Register (ECP Mode)

I/O Address: Base + 402h
Default Value: 01h
Attribute: Read/Write
Size: 8 bits

This register selects the ECP mode, enables service and error interrupts and provides interrupt status. The ECR also enables/disables DMA operations and provides FIFO empty and FIFO empty and FIFO full status. The FIFO empty and FIFO full status bits are also used to report FIFO overrun and underrun conditions.

ECP EXTENDED CONTROL REGISTER (ECP MODE) Figure 5–13



BIT	DESCRIPTION
7:5	**ECP Mode Select:** This field selects one of the following ECP Modes: **Mode** **Operation** **000** **ISA–Compatible Mode.** In this mode the parallel port operates in ISA–Compatible mode. The FIFO is reset and common collector drivers are used on the control lines ($\overline{STB}$, $\overline{AUTOFD}$, $\overline{INIT}$ and $\overline{SLCTIN}$). Setting the direction bit to 1 in the PCON register does not affect the parallel port interface. For register descriptions in this mode, see section 5.1.1, ISA–Compatible and PS/2–Compatible Modes. **001** **PS/2–Compatible Mode.** In this mode the parallel port operates in PS/2–Compatible mode. The FIFO is reset and common collector drivers are used on the control lines ($\overline{STB}$, $\overline{AUTOFD}$, $\overline{INIT}$ and $\overline{SLCTIN}$). Unlike mode 000 above, setting the direction bit to 1 in the PCON register tri–states the data lines and reading the data register returns the value on the PD[7:0]. For register descriptions in this mode, see section 5.1.1, ISA–Compatible and PS/2–Compatible Modes. **010** **ISA–Compatible FIFO Mode.** This mode is the same as mode 000 above, except that data is written or DMA'ed to the FIFO. FIFO data is automatically transmitted using the ISA–style protocol. For this mode, the direction control bit in the PCON register must be 0. **011** **ECP Mode.** In the forward direction, bytes written to the ECP DFIFO location and bytes written to the ECP AFIFO location are placed in the ECP FIFO and transmitted automatically to the peripheral using ECP protocol. In reverse direction bytes are transferred from PD[7:0] to the ECP FIFO. **100** **Reserved.** **101** **Reserved.** **110** **Test Mode.** In this mode, the FIFO may be written and read, but the data will not be transmitted on PD[7:0]. **111** **Configuration Mode.** In this mode, the ECP Configuration A and B Registers are accessible. **ECP Mode Switching Guidelines** Software will execute P1284 negotiations and all operation prior to a data transfer phase under programmed I/O (using mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (using modes 011 or 010). Setting the mode to 011 or 010 causes the hardware to initiate the data transfer. If the parallel port is in mode 000 or 001, the port can be switched to any other mode. If the parallel port is not in mode 000 or 001, the port can only be switched into mode 000 or 001. The direction and the FIFO threshold can only be changed in modes 000 or 001. Note that the FIFO, FIFO Error, and TC conditions are also reset when the mode is switched to 000 or 001. Once in an extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case, all control signals are negated before the mode switch. In an ECP reverse mode the software waits for all the data to be read from the FIFO before changing to mode 000 or 001.
4	**ERROR Interrupt Disable (ERRINTREN):** This bit enables error interrupts to the host. In ECP Mode, When ERRINTREN=1, interrupts are disabled. When ERRINTREN=0, interrupts are enabled. When enabled and a high–to–low transition occurs on the $\overline{ERROR}$ signal ($\overline{ERROR}$ asserted), an interrupt is generated to the host. Note that if this bit is written from a 1 to a 0 while $\overline{ERROR}$ is asserted, an interrupt is generated to the host.

BIT	DESCRIPTION
3	**DMA Enable (DMAEN):** This bit enables/disables DMA. When DMAEN=1, DMA is enabled and the host uses DRQ, $\overline{\text{DACK}}$, and TC to transfer data. When DMAEN=0, DMA is disabled and the DREQ output is tri–stated. In this case, programmed I/O is used to transfer data between the host and the DS83CH20 FIFO. The Service Interrupt (bit 2) needs to be set to 0 to allow generation of a TC interrupt. This bit must be written to 0 to reset the TC interrupt.
2	**Service Interrupt (SERVICEINTR):** This bit enables FIFO and TC service interrupts. When the CPU writes SERVICEINTR=1, FIFO request interrupts, FIFO error interrupts, and TC interrupts are disabled. Setting this bit to a 0 enables interrupts for one of the four cases listed below. When enabled (set to 0) and one of the four conditions below occurs, the DS83CH20 sets SERVICEINTR to a 1 and generates an interrupt to the host. 1. During DMA operations (DMAEN=1), when terminal count is reached (TC asserted). To clear the TC interrupt, switch to ISA–Compatible or PS/2–Compatible mode (write ECR[7:5] to 000, 001) or set DMAEN to 0. 2. In the forward direction and DMAEN=0, when there is a threshold number of bytes in the FIFO to be written. 3. In the reverse direction and DMAEN=0, when there is a threshold number of bytes in the FIFO to be read. 4. In either DMA or programmed I/O mode when there is a FIFO overrun or underrun. Reading the SERVICEINTR bit indicates the presence of an active interrupt when this bit has been written to a 0 prior to reading it back. To enable interrupts, the SERVICEINTR bit must be explicitly written to a 0. **NOTE:** The $\overline{\text{ACK}}$ and $\overline{\text{ERROR}}$ interrupts can be generated independent of the value of the SERVICEINTR bit. $\overline{\text{ACK}}$ and $\overline{\text{ERROR}}$ interrupts are enabled via the ACKINTREN bit in the PCON register and the ERRINTREN bit in the ECR registers, respectively. The parallel port IRQ output is enabled when ACKINTREN=1 in the PCON register or when ECR[7:5]=010, 011, or 110. Otherwise, the IRQ output is tri–stated.
1	**FIFO Full Status (FIFOFS):** This bit indicates when the FIFO is full. When FIFOFS=1 (and FIFOES=0), the FIFO is full and cannot accept another byte of data. When FIFOFS=0, at least one byte location is free in the FIFO, This bit is read only and writes have no affect. When a FIFO overrun or underrun occurs, the DS83CH20 sets both FIFOES and FIFOFS to 1. To clear the FIFO error condition interrupt, switch the parallel port mode from ECP (011) to either ISA–Compatible or PS/2–Compatible modes (000 or 001).
0	**FIFO Empty Status (FIFOES):** This bit indicates when the FIFO is empty. When FIFOES=1 (and FIFOFS=0), the FIFO is empty. When FIFOES=0, the FIFO contains at least one byte. This bit is read only and writes have no affect. When a FIFO overrun or underrun occurs, the DS83CH20 sets both FIFOES and FIFOFS to 1. To clear the FIFO error condition interrupt, switch the parallel port mode from ECP (011) to either ISA–Compatible or PS/2–Compatible modes (000 or 001).

5.2 PARALLEL PORT OPERATIONS

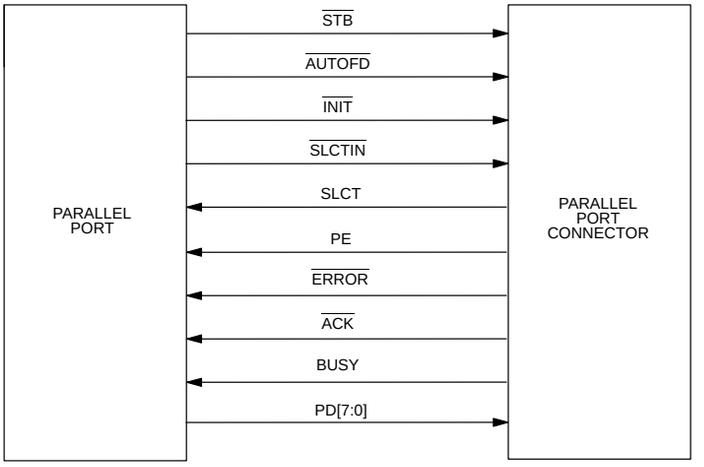
The Parallel port can be placed in ISA–Compatible, PS/2–Compatible, or EPP mode by writing to the Parallel Port Mode Register or the DS83CH20 configuration registers.

ECP mode is entered by programming the ECP Extended Control Register (ECR). Writing to this register changes any previously selected parallel port mode (via writing the Parallel Port Mode Register) to one of the ECP ECR register modes selected via ECR[7:5].

5.2.1 ISA–Compatible And PS/2–Compatible Modes

This ISA–Compatible mode is used for standard ISA–type parallel port interfaces. Figure 5–14 shows the parallel port interface for ISA–Compatible mode. $\overline{STB}$, $\overline{AUTOFD}$, $\overline{INIT}$, and $\overline{SLCTIN}$ are controlled by software via the PCON register and the status of SLCT, PE, $\overline{ERROR}$, $\overline{ACK}$, and BUSY are reported in the PSTAT register. PD[7:0] are outputs only. Note that for a reverse data transfer using the Nibble protocol, the peripheral device, supplies data 4 bits at a time using the BUSY, SLCT, PE, and $\overline{ERROR}$ signals.

ISA–COMPATIBLE MODE Figure 5–14



The following general protocol is used when communicating with a printer or other parallel port device.

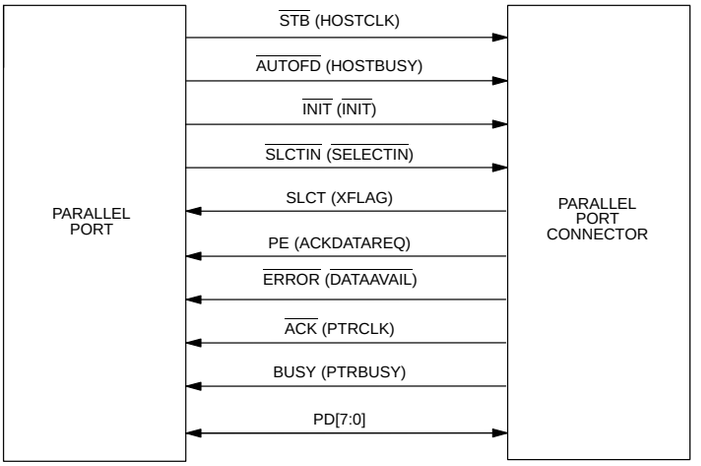
Software selects the peripheral device by asserting the $\overline{SLCTIN}$ signal. The peripheral device, in turn, acknowledges that it is selected by asserting the SLCT signal. The $\overline{INIT}$ signal is used to initialize the peripheral device. If an error is encountered during initialization or normal operations, the peripheral device asserts $\overline{ERROR}$. If a printer (or plotter) encounters problems in the paper path, the device asserts PE. Other peripheral devices may not use the PE signal.

During normal operation, the peripheral device asserts BUSY when it is not ready to receive data. When it has finished processing the previous data, the peripheral device asserts $\overline{ACK}$ and negates BUSY. If interrupts are enabled, a low–to–high transition on $\overline{ACK}$ when the signal is negated generates an interrupt. If interrupts are not enabled, software must poll the PSTAT register to determine when $\overline{ACK}$ is pulsed.

The parallel port driver software sends data to the peripheral device by writing to the PDATA register and asserting the $\overline{STB}$ signal after an appropriate data stabilization interval. After a sufficient setup time has elapsed, software then negates $\overline{STB}$. Valid data is read by the peripheral device.

In the PS/2–Compatible mode, data can be written to or read from the parallel port. Figure 5–15 shows the parallel port interface for PS/2–Compatible mode. The Byte protocol signal names are shown in parenthesis. Before reading or writing the PDATA register, the direction control bit in the PCON register must be set to the proper transfer direction on PD[7:0]. During a write to the PDATA register (with $\overline{DIR}$=0), data is latched by the PDATA register and driven onto PD[7:0]. During a parallel port read of the PDATA register (with $\overline{DIR}$=1), the data on PD[7:0] is driven onto SD[7:0]. The data is not latched by the PDATA register during the read cycle.

PS/2–COMPATIBLE MODE Figure 5–15



5.2.2 EPP Mode

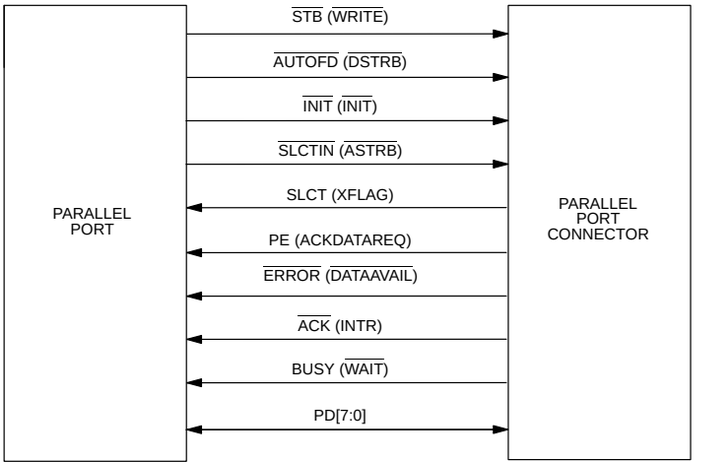
The DS83CH20 provides two different EPP modes; rev. 1.7 and rev 1.9. The EPP modes provide greater thoughput, and more complexity, than the ISA–compatible and PS/2–compatible modes by supporting faster transfer times and a mechanism that allows the host to address peripheral device registers directly. Faster transfers are achieved by automatically generating the address and data strobes.

When an EPP mode is selected in the configuration register (register 008h), the ISA–compatible and PS/2–compatible modes are also available. If no EPP read, write, or address cycle is currently executing, then the PD[7:0] bus is in the ISA–Compatible or PS2–Compatible mode, and all output signals ($\overline{STB}$, $\overline{AUTOFD}$, $\overline{SLCTIN}$, and $\overline{INIT}$) are as set by the PCON register.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lock–up. The timer indicates if more than 10 µs have elapsed from the start of the EPP cycle ($\overline{IOR}$ or $\overline{IOW}$ asserted) to $\overline{WAIT}$ being deserted (after command). If a time–out occurs, the current EPP cycle is aborted and the time–out condition is indicated in PSTAT.0.

Figure 5–16 shows the parallel port interface for EPP mode. The EPP protocol interface signal names are shown in parenthesis. In EPP mode, the initialization, printer selection, and error signals (PE and $\overline{ERROR}$) operate the same way as in the ISA–Compatible mode. However, in EPP mode, $\overline{SLCTIN}$ and $\overline{AUTOFD}$ are automatically generated and become Address Strobe (ASTRB) and Data Strobe ($\overline{DSTRB}$), respectively, enabling direct access to parallel port devices. $\overline{STB}$ ($\overline{WRITE}$) is used to indicate a read or write cycle. Note that BUSY ($\overline{WAIT}$) is an active low signal in EPP mode rather than active high as in ISA–Compatible mode. In addition, BUSY ($\overline{WAIT}$), in combination with IOCHRDY on the ISA BUS, extends clock cycles to enable the completion of a Read and Write without additional WAIT states. EPP 1.7 and 1.9 Write and Read cycles are explained below.

EPP MODE Figure 5–16

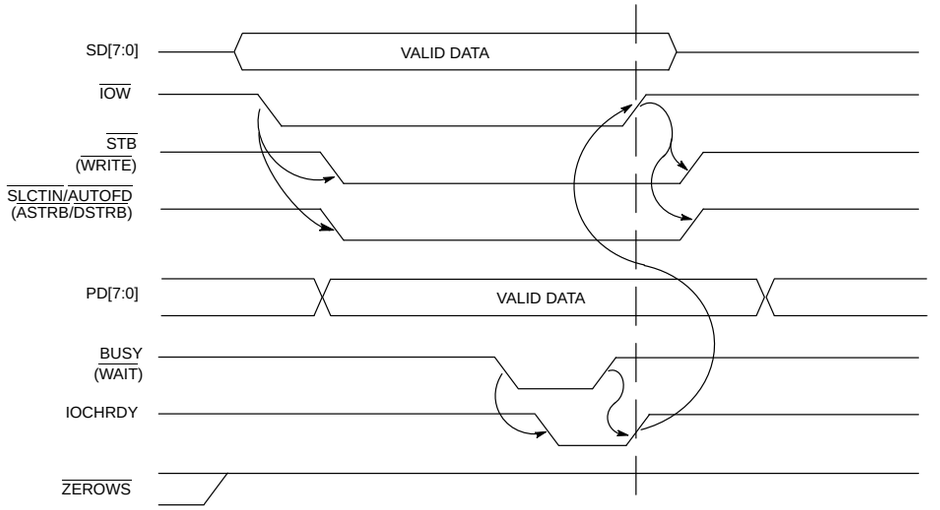


EPP 1.7 Address Write

The following procedure selects a peripheral device or register:

1. The host writes a byte to the EPP address register. IOW goes low to latch SD[7..0] into the address register. The latch drives the address register onto PD[7:0] and the EPP pulls WRITE low.
2. The EPP pulls ASTRB low to indicate that data has been sent.
3. If WAIT is low during the host write cycle, IOCHRDY goes low. When WAIT goes high, the EPP pulls IOCHRDY high.
4. When IOCHRDY goes high it allows IOW to go high. If WAIT is high during the host write cycle then the EPP does not pull IOCHRDY low.
5. When IOW goes high it causes the EPP to pull WRITE and ASTRB high. Only when WRITE and ASTRB are high can the EPP change PD[7:0].

EPP MODE WRITE (REV. 1.7) CYCLE Figure 5–17

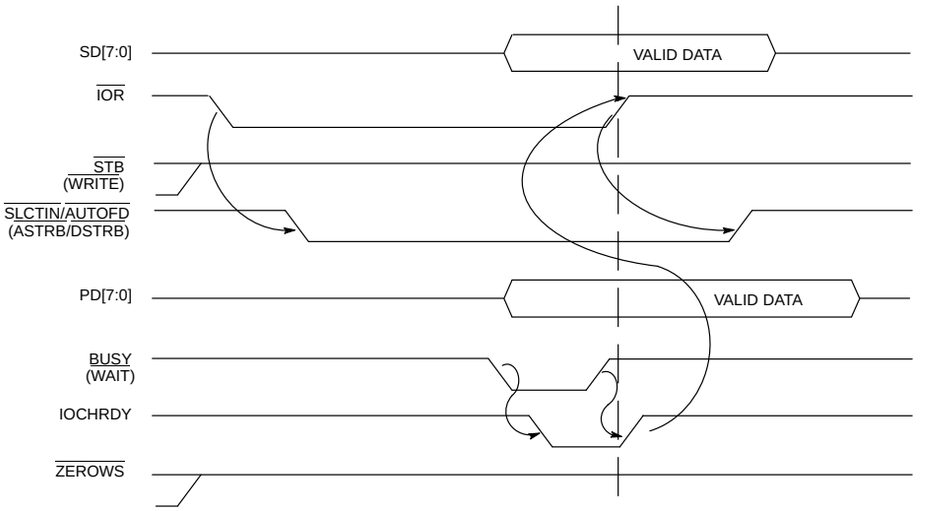


EPP 1.7 Address Read

The following procedure reads from the address register:

1. The host reads a byte from the EPP address register. IOR goes low to gate PD[7:0] into SD[7:0].
2. The EPP pulls ASTRB low to signal the peripheral to start sending data.
3. If WAIT is low during the host read cycle, then the EPP pulls IOCHRDY low. When WAIT goes high, the EPP stops pulling IOCHRDY low.
4. When IOCHRDY goes high it allows IOR to go high. If WAIT is high during the host read cycle then the EPP does not pull IOCHRDY low.
5. When IOR goes high, it causes the EPP to pull ASTRB high. Only when ASTRB is high can the EPP change PD[7:0]. After ASTRB goes high, the EPP tri–states SD[7:0].

EPP MODE READ (REV. 1.7) CYCLE Figure 5–18



EPP 1.7 Data Write and Data Read

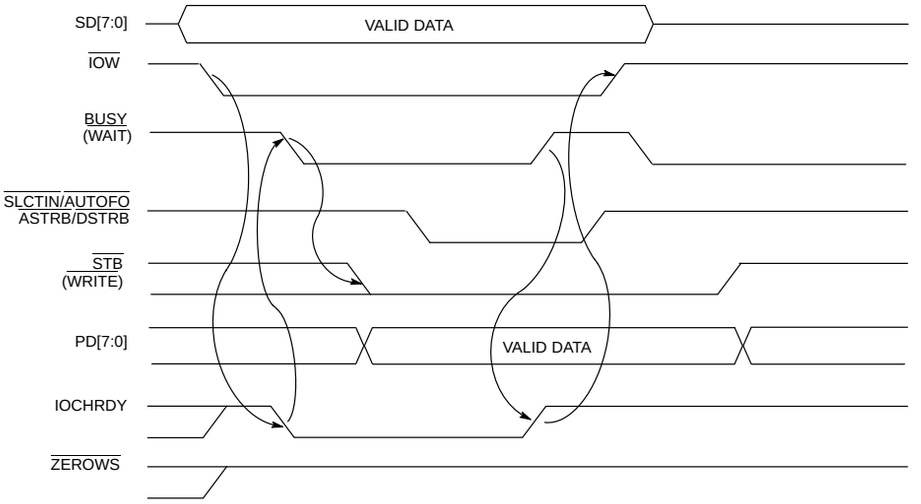
Data read and write operations are similar to address read and write operations except that the data strobe ($\overline{\text{DSTRB}}$) and the data register replace the address strobe ($\overline{\text{ASTRB}}$) and the address register, respectively.

EPP 1.9 Address Write

The following procedure selects a peripheral or register:

1. The host writes a byte to the EPP address register. $\overline{\text{IOW}}$ goes low to latch SD[7:0] into the address register.
2. The EPP pulls IOCHRDY low, and waits for $\overline{\text{WAIT}}$ to go low.
3. When $\overline{\text{WAIT}}$ goes low the EPP pulls $\overline{\text{WRITE}}$ low, and drives the latched byte onto PD[7:0]. If $\overline{\text{WAIT}}$ was already low, steps 3 and 4 occur concurrently.
4. The EPP pulls $\overline{\text{ASTRB}}$ low (indicating that PD[7:0] contain valid data and the $\overline{\text{WRITE}}$ signal is valid) and waits for $\overline{\text{WAIT}}$ to go high.
5. When $\overline{\text{WAIT}}$ goes high (indicating that any setup requirements have been satisfied), the EPP stops pulling IOCHRDY low, pulls $\overline{\text{ASTRB}}$ high, and waits for $\overline{\text{WAIT}}$ to go low (indicating that any hold time requirements have been satisfied and acknowledging the termination of the cycle).
6. Only if no EPP write is pending, when $\overline{\text{WAIT}}$ goes low, the EPP pulls $\overline{\text{WRITE}}$ to high. If an EPP write is pending, $\overline{\text{WRITE}}$ remains low and the EPP may change PD[7:0].

EPP 1.9 MODE WRITE CYCLE Figure 5–19

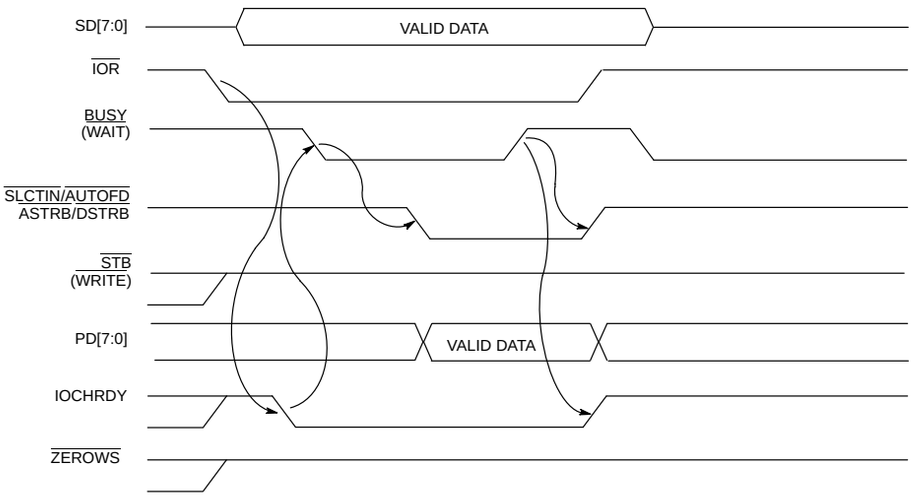


EPP 1.9 Address Read

The following procedure reads from the address register:

1. When IOR goes low, the EPP pulls IOCHROY low and waits for WAIT to go low.
2. When WAIT goes low, the EPP pulls ASTRB low and waits for WAIT to go high. If WAIT is already low, steps 2 and 3 occur concurrently.
3. When WAIT goes high, the EPP stops pulling IOCHRDY low, latches PD[7:0], and pulls ASTRB high.
4. When IOR goes high, the EPP tri–states SD[7:0].

EPP 1.9 MODE READ CYCLE Figure 5–20



EPP 1.9 Data Write and Data Read

Data read and write operations are similar to address read and write operations except that the data strobe ($\overline{\text{DSTRB}}$) and the data register replace the address strobe ($\overline{\text{ASTRB}}$) and the address register, respectively.

EPP Zero Wait State (ZEROWS) Address Write/Read Operation (both 1.7 and 1.9)

The Zero Wait State function on the DS83CH20 is enabled by setting bit 7 of the parallel port mode configuration register. The following procedure performs a short write to the selected peripheral device or register:

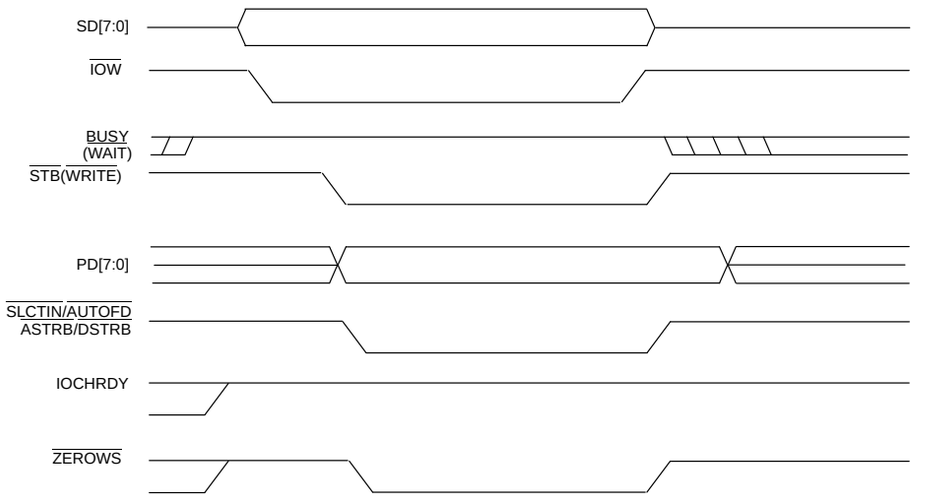
1. The host writes a byte to the EPP address register. $\overline{\text{IOW}}$ goes low to latch SD0–7 into the data register. The latch drives the data register onto PD0–7.
2. The EPP first pulls $\overline{\text{WRITE}}$ low and then pulls $\overline{\text{ASTRB}}$ low to indicate that data has been sent.
3. If $\overline{\text{WAIT}}$ is high during the host write cycle, $\overline{\text{ZEROWS}}$ goes low and IOCHRDY goes high.
4. When the host pulls $\overline{\text{IOW}}$ high, the EPP pulls $\overline{\text{ASTRB}}$, $\overline{\text{ZEROWS}}$, and $\overline{\text{WRITE}}$ to high. Only when $\overline{\text{WRITE}}$ and $\overline{\text{ASTRB}}$ are high can the EPP change PD0–7.
5. If the peripheral is fast enough to pull $\overline{\text{WAIT}}$ low before the host terminates the write cycle, the EPP pulls IOCHRDY to low, but does not pull $\overline{\text{ZEROWS}}$ to low, thus carrying out a normal (non–ZWS EPP 1.7) write operation.

NOTE:
A read operation is similar except for the data direction and the activation of $\overline{\text{IOR}}$ instead of $\overline{\text{IOW}}$.

EPP Zero Wait State (ZEROWS) Data Write/Read Operation (both 1.7 and 1.9)

An EPP 1.7 and 1.9 Zero Wait State data write/read operation is similar to the EPP Zero Wait State address write/read operation with the exception that the data strobe ($\overline{\text{DSTRB}}$) and the data register replace the address strobe ($\overline{\text{ASTRB}}$) and address register, respectively.

EPP WRITE WITH ZEROWS Figure 5–21



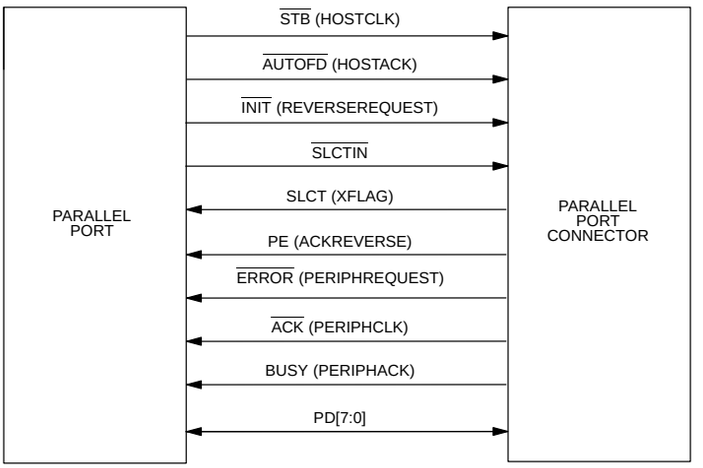
5.2.3 ECP MODE

Figure 5–22 shows the parallel port interface for ECP mode with the ECP protocol signal names in parenthesis. The ECP modes are selected by programming the Extended Control Register (ECR bits[7.5]). Two of the modes (Test and Configuration) provide information about the DS83CH20 parallel port and are not used for interfacing with a peripheral device. Four peripheral interface modes are selectable via the ECR: ISA–Compatible mode, ISA–Compatible FIFO mode, PS/2–Compatible mode, and ECP mode.

ISA–Compatible and PS/2–Compatible Modes (ECR[7:5]=000,001)

The ISA–Compatible and PS/2–Compatible mode selections in the ECR are equivalent to selecting these modes via programming the Parallel Port Mode Configuration Register. For these modes the operation is the same as described in section 5.2.1, ISA–Compatible and PS/2–Compatible Modes.

ECP MODE Figure 5–22

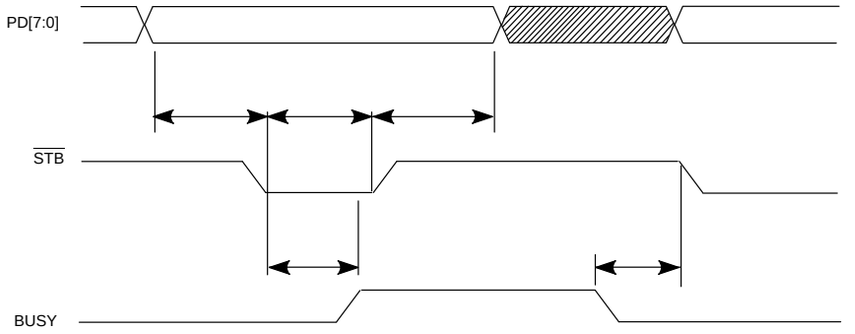


ISA–Compatible FIFO Mode (ECR[7:5]=010)

The ISA–Compatible FIFO mode uses the same signaling protocol on the parallel port interface as the ISA–Compatible mode. However, there are two major operational differences. First, data is written to a 16–byte FIFO (via the SDFIFO address location). The FIFO empty and FIFO full bits in the ECR provide FIFO status. In addition, DMA can be used to transfer data to the FIFO by enabling this feature in the ECR.

Second, the data is transferred to the peripheral using an automatic hardware handshake. This handshake emulates the standard ISA–Compatible style software generated handshake (Figure 5–23). For ISA–Compatible FIFO mode, the DS83CH20 does not monitor the ACK signal. Service interrupts are enabled and reported via the ECR. The generation of service interrupts is based on the state of the FIFO and not individual transfers (using ACK) as is the case in standard ISA–Compatible mode.

ISA–COMPATIBLE TIMING Figure 5–23



ECP Mode (ECR[7:5]=011)

When ECR[7:5]=011, the parallel port operates in ECP mode. In ECP mode, both data and commands (addresses and RLE) are transferred using the parallel port 16–byte FIFO. This information can be either written to or read from the FIFO using DMA or non–DMA ISA bus transfers. The parallel port interface transfers use an automatic handshake generated by the DS83CH20. The host controls the transfer direction by programming the DIR bit in the PCON register.

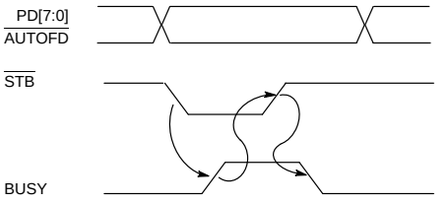
When the host is writing to the peripheral device (forward direction), STB, and BUSY provide the automatic handshake for transfer on the parallel port interface (Figure 5–24). The peripheral device negates BUSY when it is ready to receive data or commands. AUTOFD indicates whether PD[7:0] contain data (AUTOFD is high) or a command (AUTOFD is low). For commands (address or RLE), the host writes to the ECPAFIFO register I/O address and for data, the host writes to the DFIFO register I/O address. The addresses and data are placed in the same 16–Byte FIFO. When the FIFO is full and cannot accept more data/addresses, the FIFO Full status bit is set in the ECR.

Data/addresses written to the FIFO are transferred to the peripheral device via PD[7:0]. To begin a transfer on the peripheral interface, the DS83CH20 checks BUSY to make sure the peripheral is in the ready state. If BUSY is negated, the DS83CH20 drives PD[7:0] and AUTOFD, and asserts STB to indicate that the data/command is on PD[7:0]. The peripheral device asserts BUSY to indicate that it is receiving the data/command. BUSY asserted causes the DS83CH20 to negate STB.

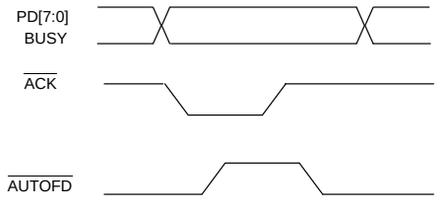
When the host is reading from the peripheral device (reverse direction), AUTOFD and ACK provide the automatic handshake for transfer on the parallel port interface (Figure 5–25). Data/commands from the peripheral device are placed in the parallel port FIFO using this handshake. In this case, BUSY indicates whether PD[7:0] contain data (BUSY is high) or a command (BUSY is low).

The peripheral device asserts ACK to indicate that a data/command is on PD[7:0]. The DS83CH20 negates AUTOFD when it is ready for a peripheral transfer and asserts AUTOFD to indicate that it is receiving the data/command. AUTOFD asserted causes the peripheral device to negate ACK. The peripheral transfers are to the parallel port 16–byte FIFO.

ECP MODE HANDSHAKE (FORWARD DIRECTION) Figure 5–24



ECP MODE HANDSHAKE (REVERSE DIRECTION) Figure 5–25



Test Mode (ECR[7:5]=110) and Configuration Mode (ECR[7:5]=111)

The test mode can be used to check the FIFO read and write interrupt thresholds as described in section 5.1.3.7, TFIFO–ECP Test FIFO Register. Note that for the DS83CH20 parallel port, the read and write FIFO interrupt thresholds are the same. The FIFO threshold is set by programming the Parallel Port Mode Register in the DS83CH20 configuration space. The configuration mode is used to access the ECPCFGA and ECPCFGB registers. This mode must first be set before the ECPCFGA and ECPCFGB registers can be accessed.

5.2.3.1 FIFO Operations

The parallel port FIFO is used for ECP transfers (ECR[7:5]=011), ISA–Compatible FIFO transfers (ECR[7:5]=010), and Test mode (ECR[7:5]=110). Either DMA or programmed I/O can be used for transfers between the host and the parallel port.

The FIFO threshold value is selected via the FIFO threshold bits in the Parallel Port Mode configuration register (bits 3–6). The FIFO threshold ranges from 1 (FIFO threshold bits=0000) to 16 (FIFO threshold bits=1111). The programmable FIFO threshold is useful in adjusting the parallel port to the speed of the system. A slow system with a sluggish DMA transfer capability uses a high FIFO threshold, giving the system more time to respond to a data transfer service request. Conversely, a fast system with a quick response to a data transfer service request uses a low FIFO threshold value.

The FIFO is reset by a hard reset (RSTDRV asserted) or whenever the parallel port is placed in ISA–Compatible or PS/2–Compatible modes. Note that the FIFO threshold can only be changed when the parallel port is in ISA–Compatible or PS/2–Compatible mode.

5.2.3.2 DMA Transfers

The DS83CH20 contains parallel port DMA request (DRQ) and acknowledge ($\overline{\text{DACK}}$) signals to communicate with a standard PC DMA controller. Before initiating a DMA transfer the direction bit in the PCON register must be set to the proper direction. To initiate DMA transfers, software sets the DMAEN bit to 1 and the SERVICEINTR bit to 0 in the ECR. The DRQ and $\overline{\text{DACK}}$ signals will then be used to fill (forward direction) or empty (reverse direction) the FIFO. When the DMA controller reaches terminal count and asserts the TC signal, an interrupt is generated and the SERVICEINTR bit is set to 1. To reset the TC interrupt, software can either switch the mode to 000 or 001 or write the DMAEN bit to 0.

In DMA mode, if 32 consecutive reads or writes are performed to the FIFO and DRQ is still asserted, the

DS83CH20 negates DRQ for the length of the last DACK/command pulse to force an arbitration cycle on the ISA Bus.

5.2.3.3 Reset FIFO and DMA Terminal Count Interrupt

The following operations are used to reset the parallel port FIFO and TC interrupt

Function	Reset Operations
FIFO	–Changing to modes 000 or 001 –Hard reset
FIFO Error	–Changing to modes 000 or 001 –Hard reset
TC Interrupt	–Changing to modes 000 or 001 –Setting DMAEN to 0 in ECR –Hard reset

5.2.3.4 Programmed I/O Transfers

Programmed I/O (non–DMA) can also be used for transfers between the host and the parallel port FIFO. Software can determine the read/write FIFO thresholds and the FIFO depth by accessing the FIFO in Test mode. To use programmed I/O transfers software sets the direction bit in the PCON register to the desired direction and sets the DMAEN bit to 0 and the SERVICEINTR bit to 0 in the ECR. The parallel port requests programmed I/O transfers from the host by asserting the IRQ output.

In the reverse direction an interrupt occurs when SERVICEINTR=0 and 1 to 16 bytes are in the FIFO (depending on the threshold setting). The IRQ Output can be used in an interrupt–driven system. The host must respond to the interrupt request by reading data from the FIFO.

In the forward direction an interrupt occurs when SERVICEINTR=0 and there are 1 to 16 byte locations available in the FIFO (depending on threshold setting). The IRQ output can be used in an interrupt–driven system. The host must respond to the interrupt request by writing data to the FIFO.

5.2.3.5 Data Compression

The DS83CH20 supports Run Length Encoded (RLE) decompression in hardware and can transfer compressed data to the peripheral. To transfer compressed data to the peripheral (forward direction), the compression count is written to the ECPAFIFO location and the data is written to ECPDFIFO location. The most significant bit (bit 7) in the byte written to the ECPAFIFO register informs the peripheral whether the value is a channel address (bit 7=1) or a run length count (bit 7=0). The RLE count in the ECPAFIFO (bit[6:0]) informs the peripheral of how many times the data in the ECPDFIFO is to be repeated. An RLE count of 0 indicates that only one byte of the data is present and a count of 127 indicates to the peripheral that the next byte should be expanded 128 times. An RLE count of 1 should be avoided as it will cause unnecessary expansions. Note that the DS83CH20 asserts AUTOFD to indicate that PD[7:0] contains address/RLE instead of data.

In the reverse direction, the peripheral negates the BUSY signal to indicate that PD[7:0] contains address/RLE. During an address/RLE cycle, the DS83CH20 checks bit 7 to see if the next byte received needs to be decompressed. If bit 7 is 0, the DS83CH20 decompresses (replicates) the next data received by the RLE count received on bits[6:0].

5.2.4 Parallel Port Summary

Table 5–4 summarizes the parallel port interrupt DMA, and parallel port signal drive type for the various modes of operation.

PARALLEL PORT REGISTERS (ECP MODE) Table 5–4

PARALLEL PORT MODE	ECR(7:5)	PD(7:0) DIRECTION	PARALLEL PORT CONTROL SIGNALS CONTROLLED BY PCON	IRQ ENABLE	DMA ENABLE
ISA–Compatible	000	Output	Open Drain	$\overline{ACK}$INTEN	
PS/2–Compatible	001	Bi–directional	Open Drain	$\overline{ACK}$INTEN	
EPP	N/A	Bi–directional	Push Pull	$\overline{ACK}$INTEN	
ISA–Compatible FIFO	010	Output	Push Pull	Always Enabled	DMAEN
ECP	011	Bi–directional	Push Pull	Always Enabled	DMAEN
ECP Test	110	Output	Push Pull	Always Enabled	DMAEN
ECP Configuration	111	Bi–directional	Push Pull	$\overline{ACK}$INTEN	DMAEN

NOTES:

1. The selected IRQ pin is enabled if ACKINTEN is enabled in the PCON register. Otherwise, the IRQ pin is tri–stated.
2. DRQ is enabled whenever the DMAEN bit is enabled in the ECR, independent of the parallel port mode.

6.0 SERIAL PORTS

6.1 INTRODUCTION

The DS83CH20 provides two 16550–compatible serial ports. Each of these serial ports function as a serial data input/output interface in a microcomputer system. The system software determines the functional configuration of the UARTs via a 8–bit bidirectional data bus.

The UARTs are completely independent. They perform serial–to–parallel conversion on data characters received from a peripheral device or a modem, and parallel–to–serial conversion on data characters received from the CPU. The CPU can read the complete status of either UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The UARTs have programmable baud rate generators that are capable of dividing the internal reference clock by divisors of 1 to (2^{16} – 1), and producing a 16 x clock for driving the transmitter logic. Provisions are also included to use this 16 x clock to drive the receiver logic. The UARTs have complete modem–control capability and a prioritized interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

The DS83CH20 provides flexibility in the configuration of the two UARTs such as programmable base I/O addresses, programmable interrupt assignment, and optional infrared port configuration. UART A and UART B are configured via configuration registers 00Ch–010h and 011h–015h, respectively.

6.2 DS83CH20 SERIAL PORTS

6.2.1 Serial Port Registers

Two identical register sets, one for each channel, are in the DS83CH20. All register descriptions in this section apply to the register sets in both channels.

UART REGISTER ADDRESSES (AEN=0) Table 6–1

DLAB1	A2	A1	A0	SELECTED REGISTER
0	0	0	0	Receiver Buffer (Read), Transmitter Holding (Write)
0	0	0	1	Interrupt Enable
0	0	1	0	Interrupt Identification (Read) FIFO Control (Write)
x	0	1	1	Line Control
x	1	0	0	Modem Control
x	1	0	1	Line Status
x	1	1	0	Modem Status
x	1	1	1	Scratch
1	0	0	0	Divisor Latch (Least Significant Byte)
1	0	0	1	Divisor Latch (Most Significant Byte)

6.2.2 Line Control Register

The system programmer uses the Line Control Register (LCR) to specify the format of the asynchronous data communications exchange and set the Divisor Latch Access bit. This is a read and write register. Table 6–2 shows the contents of the LCR. Details on each bit follow.

COMPOSITE SERIAL DATA Figure 6–1

Bits 0, 1 These two bits specify the number of data bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

BIT 1	BIT 0	DATA LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2 This bit specifies the number of Stop bits transmitted with each serial character. If it is 0, one Stop bit is generated in the transmitted data. If it is 1, when a 5–bit data length is selected, one and a half Stop bits are generated. If it is 1, when either a 6, 7, or 8 bit word length is selected, two Stop bits are generated. The receiver checks the first Stop bit only, regardless of the number of Stop bits selected.

BIT 2	WORD LENGTH	NUMBER OF STOP BITS
0	–	1
1	5 Bits	1.5
1	6 Bits	2
1	7 Bits	2
1	8 Bits	2

Bit 3 This bit is the Parity Enable bit. When is 1 a parity bit is generated (transmit data) or checked (receive data) between the last data bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data bits and the Parity bit a summed.)

Bit 4 This bit is the Even Parity Select bit. When parity is enabled and bit 4 is 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When parity is enabled and bit 4 is a 1, an even number of logic 1s is transmitted or checked.

Bit 5 This bit is the Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as a 0 (space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0, Stick Parity is disabled.

Bit 6 This bit is the Break Control bit. It causes a break condition to be transmitted to the receiving UART. When it is set to 1, the serial output (SOUT) is forced to the Spacing state (0). The break is disabled by setting bit 6 to 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

NOTE:
This feature enables the CPU to alert a terminal. If the following sequence is used, no erroneous characters will be transmitted because of the break.

1. Wait for the transmitter to be idle, (TEMT=1).

2. Set break for the appropriate amount of time. If the transmitter will be used to time the break duration then check that TEMT=1 before clearing the Break Control bit.

3. Clear break when normal transmission has to be restored.

During the break, the transmitter can be used as a character timer to accurately establish the break duration by sending characters and monitoring THRE and TEMT.

Bit 7 This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a read or write operation.

REGISTER SUMMARY FOR AN INDIVIDUAL UART CHANNEL Table 6–2

REGISTER ADDRESS												
	O DLAB=0	**0 DLAB=0**	**1 DLAB=0**	**2**	**2**	**3**	**4**	**5**	**6**	**7**	**0 DLAB=1**	**1 DLAB=1**
Bit No.	**Receiver Buffer Register (Read Only)**	**Transmitter Holding Register (Write Only)**	**Interrupt Enable Register**	**Interrupt Ident. Register (Read Only)**	**FIFO Control Register (Write Only)**	**Line Control Register**	**Modem Control Register**	**Line Status Register**	**Modem Status Register**	**Scratch-pad Register**	**(LSB)**	**(MSB)**
	RBR	**THR**	**IER**	**IIR**	**FCR**	**LCR**	**MCR**	**LSR**	**MSR**	**SCR**	**DLL**	**DLM**
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt	0 if Interrupt pending	FIFO Enabled	Word Length Select Bit 0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Interrupt Empty	Interrupt ID Bit	RCVR FIFO Reset	Word Length Select Bit 1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt	Interrupt ID Bit	XMIT FIFO Reset	Number of Stop Bits	OUT1 Bit (Note 3)	Parity Error (PE)	Trailing Edge Ring Indicator	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt	Interrupt ID Bit (Note 2)	Reserved	Parity Enable	IRQ Enable	Framing Error (FE)	Delta Data Carrier Detect	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select	Loop	Break Interrupt (BI)	Clear to Send	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 2)	RCVR Trigger (MSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 2)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 2)	Data Carrier Detect	Bit 7	Bit 7	Bit 15

NOTES:

1. Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
2. These bits are always 0 in the 16450 mode.
3. This bit no longer has a pin associated with it.

UART RESET CONFIGURATION Table 6–3

REGISTER I SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable	Master Reset	**0000** 0000 (Note 1)
Interrupt Identification	Master Reset	00**00** 0001
FIFO Control	Master Reset	00**00** 0000
Line Control	Master Reset	**000**0 0000
Modem Control	Master Reset	0000 0000
Line Status	Master Reset	0110 0000
Modem Status	Master Reset	XXXX 0000 (Note 2)
SOUT	Master Reset	High
INTR (RCVR Errs)	Read LSR I MR	Low/Tri–state
INTR (RCVR Data Ready)	Read RBR I MR	Low/Tri–state
INTR (THRE)	Read IIR I Write THR I MR	Low/Tri–state
INTR (Modem Status Changes)	Read MSR I MR	Low/Tri–state
Interrupt Enable Bit	Master Reset	Low
RTS	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
RCVR FIFO	MR/FCR1 • FCR0/ΔFCR0	All Bits Low
XMIT FIFO	MR/FCR2 • FCR0/ΔFCR0	All Bits Low

NOTES:

1. Boldface bits are permanently low.
2. Bits 7–4 are driven by the input signals.

6.2.3 Programmable Baud Rate Generator

The DS83CH20 contains two independently programmable baud rate generators. The 24 MHz or 48 MHz crystal oscillator frequency input is divided by 13 or 26, respectively, resulting in a frequency of 1.8462 MHz. This is sent to each baud rate generator and divided by the divisor of the associated UART. The output frequency of the baud rate generator (BOUT1, 2) is 16 x the baud rate.

divisor # = (frequency input) / (baud rate x 16)

The output of each baud rate generator drives the transmitter and receiver sections of the associated serial channel. Two 8–bit latches per channel store the divisor in a 16–bit binary format. These divisor latches must be loaded during initialization to ensure proper operation of the baud rate generator. Upon loading either of the divisor latches, a 16–bit baud counter is loaded. Table 6–4 provides decimal divisors needed to provide specific Baud Rates. The oscillator input to the chip should always be 24 MHz or 48 MHz to ensure that the floppy disk controller timing is accurate and that the UART divisors are compatible with existing software. Using a divisor of zero is not recommended.

UART DIVISORS, BAUD RATES AND CLOCK FREQUENCIES Table 6–4

24 MHz OR 48 MHz INPUT DIVIDED TO 1.8461 MHz		
BAUD RATE	**DECIMAL DIVISOR FOR 16 X CLOCK**	**PERCENT ERROR**
50	2304	0.1
75	1536	–
110	1047	–
134.5	857	0.4
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.5
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
57600	2	–
115200	1	–

NOTE: The percent error for all baud rates, except where indicated otherwise, is 0.2%.

6.2.4 Line Status Register

This 8–bit register provides status information to the CPU concerning the data transfer. Table 6–2 shows the contents of the line status register. Details on each bit follow:

Bit 0 This bit is the receiver Data Ready (DR indicator. It is set to 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. It is reset to 0 by reading the data in the Receiver Buffer Register or the FIFO.

Bit 1 This bit is the Overrun Error (OE) indicator. It indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to 1 upon detection of an overrun condition, and reset whenever the CPU reads the contents of the Line Status Register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an OE will occur only after the FIFO is completely full and the next character has been received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but is not transferred to the FIFO.

Bit 2 This bit is the Parity Error (PE) indicator. It indicates that the received data character does not have the correct parity, as selected by the even parity select bit. The PE bit is set 1 upon detection of a parity error and is reset to 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO that it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3 This bit is the Framing Error (FE) indicator. It indicates that the received character did not have a valid Stop bit. It is set to 1 whenever the Stop bit following the last data bit or parity bit is a 0 (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FiFO mode this error is associated with the particular character in the FIFO that it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error by assuming that the error was due to the next start bit. It samples this "start" bit twice and then takes in the bits following it as the rest of the frame.

Bit 4 This bit is the Break Interrupt (BI) indicator. It is set to 1 whenever the received data input is held in the Spacing (0) state for longer than a full word transmission time (i.e., the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO that it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs only one character is loaded into the FIFO. To restart after a break is received, the SIN pin must be 1 for at least 1/2 bit time.

NOTE: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and that interrupt is enabled.

Bit 5 This bit is the Transmitter Holding Register Empty (THRE) indicator. It indicates that the UART is ready to accept a new character for transmission. In addition, it causes the UART to issue an interrupt to the CPU when the THRE interrupt enable is set high. The THRE bit is set to 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to 0 whenever the CPU loads the Transmitter Holding Register. In the FIFO mode it is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6 This bit is the Transmitter Empty (TEMT) indicator. It is set to 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to 0 if either the THR or TSR contains a data character. In the FIFO mode this bit is set to 1 whenever the transmitter FIFO and the shift register are both empty.

Bit 7 In the 16450 mode this is 0. In the FIFO mode LSR7 is set when there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

NOTE:
The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing. In the FIFO mode the software must load a data byte in the R_X FIFO via the Loopback mode in order to write to LSR2 – LSR4. LSR0 and LSR7 cannot be written to in the FIFO mode.

6.2.5 FIFO Control Register

This is a write–only register at the same location as the IIR (the IIR is a read–only register). This register is used to enable all FIFOs, clear the FIFOs and to set the RCVR FIFO trigger level.

Bit 0 Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. Resetting FCR0 clears all bytes in both FIFOs. When changing

from FIFO mode to 16450 mode and vice versa, data is automatically cleared from the FIFOs. This bit must already be 1 when other FCR bits are written to or they will not be programmed.

Bit 1 Writing 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self–clearing.

Bit 2 Writing 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self–clearing.

Bit 3 Writing to FCR3 does not change UART operations since the RXRDY and TXRDY pins are not available on this chip.

Bits 4,5 FCR4 to FCR5 are reserved for future use.

Bits 6,7 FCR6 and FCR7 are used to designate the interrupt trigger level. When the number of bytes in the RCVR FIFO equals the designated interrupt trigger level, a Received Data Available interrupt is activated. This interrupt must be enabled by setting IER0.

FCR BITS		RCVR FIFO
7	**6**	**Trigger Level (Bytes)**
0	0	01
0	1	04
1	0	08
1	1	14

6.2.6 Interrupt Identification Register

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the Interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Entry; Transmitter Holding Register Empty; and Modem Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the current access is complete. Table 6–2 shows the contents of the IIR. Details on each bit follows.

Bit 0 This bit can be used in an interrupt environment to indicate whether an interrupt condition is pending. When it is 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When it is 1, no interrupt is pending.

Bits 1, 2 These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 6–5.

Bit 3 In the 16450 mode this bit is 0. In the FIFO mode it is set along with bit 2 when a time–out interrupt is pending.

Bits 4, 5 These bits of the IIR are always 0.

Bits 6, 7 These two bits are set when FCR0=1. (FIFO Mode enabled.)

6.2.7 Interrupt Enable Register

This register enables the five types of UART interrupts. Each interrupt can individually activate the appropriate IRQ output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of this register to 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the interrupt output signal. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. Table 6–2 shows the contents of the IER. Details on each bit follow. See Modem Control Register bit 3 for more information on enabling the interrupt pin.

Bit 0 When set to 1 this bit enables the Received Data Available Interrupt and Timeout Interrupt in the FIFO mode.

Bit 1 This bit enables the Transmitter Holding Register Empty Interrupt when set to 1.

Bit 2 This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3 This bit enables the Modem Status Interrupt when set to logic 1.

Bits 4–7 These four bits are always logic 0.

6.2.8 Modem Control Register

This register controls the interface with the Modem or data set (or a peripheral device emulating a modem). The contents of the Modem Control Register (MCR) are indicated in Table 6–2 and are described below.

Bit 0 This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When it is set to 1, the $\overline{DTR}$ output is forced to a logic 0. When it is reset to 0, the $\overline{DTR}$ output is forced to 1. In Local Loopback mode, this bit controls bit 5 of the Modem Status Register.

NOTE:
The $\overline{DTR}$ and $\overline{RTS}$ output of the UART may be applied to an EIA inverting line driver to obtain the proper polarity input at the Modem or data set.

Bit 1 This bit controls the Request to Send ($\overline{RTS}$) output. Its effect on the $\overline{RTS}$ output is identical to that described above for bit 0. In Local Loopback mode, this bit controls bit 4 of the Modem Status Register.

Bit 2 This bit is the OUT1 bit. It does not have an output pin associated with it. It can be written to and read by the CPU. In Local Loopback mode, this bit controls bit 6 of the Modem Status Register.

Bit 3 This bit enables the interrupt when set. No external pin is associated with this bit other than the selected IRQ line. In Local Loopback mode, this bit controls bit 7 of the Modem Status Register.

Bit 4 This bit provides a local loopback feature for diagnostic testing of the UART. When it is set to 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is “looped back” (connected) to the Receiver Shift Register; the four Modem Control inputs ($\overline{DSR}$, $\overline{CTS}$, RI and $\overline{DCD}$) are disconnected; and the DTR, RTS, OUT1, IRQ Enable bits in MCR are internally connected to DSR, CTS, RI and DCD in MSR, respectively. The Modem Control output pins are forced to their high (inactive) states. In the Loopback mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit–and–received data paths of the serial port.

In the Loopback mode, the receiver and transmitter interrupts are fully operational. The Modem Status interrupts are also operational, but the interrupts’ sources are the lower four bits of MCR instead of the four Modem control inputs. Writing a 1 to any of these four MCR bits will cause an interrupt. In Loopback mode the interrupts are still controlled by the Interrupt Enable Register. The serial port IRQ pins will be tri–state in the Loopback mode.

NOTE: The Test Mode Enable bit (bit 0 of the UART Mode Register) serves the same function as MCR[4] in UART A and serves the same function as MCR[4] in UART B when UART B is not in IR mode. When IR mode is selected, MCR[4] must be cleared.

Bits 5–7 These bits are permanently set to 0.

INTERRUPT CONTROL FUNCTIONS Table 6–5

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	–	None	None	–
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or R_X FIFO Trigger	Read Receiver Buffer or FIFO drops below the trigger level.
1	1	0	0	Second	Character Time–out Indication	No characters have been removed from or input to the RCVR FIFO during the last four character times and there is at least one character in it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register if Source of Interrupt or Writing the Transmitter Holding Register
0	0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the Modem Status Register

6.2.9 Modem Status Register

This register provides the current state of the control lines from the Modem (or peripheral device) to the CPU. In addition to this current state information, four bits of the Modem Status Register provide change information. These bits are set to a logic 1 whenever a control input from the Modem changes state. They are reset to logic 0 whenever the CPU reads the Modem Status Register. Table 6–2 shows the contents of the MSR. Details on each bit follows.

Bit 0 This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time the Modem Status Register was read by the CPU.

Bit 1 This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last

time the Modem Status Register was read by the CPU.

Bit 2 This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3 This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

NOTE:
Whenever bit 0, 1, 2, or 3 is set to logic 1, a Modem Status Interrupt is generated.

Bit 4 This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loopback) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5 This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6 This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7 This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to IRQ Enable in the MCR.

6.2.10 Scratchpad Register

This 8–bit read/write register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

6.3 UART B INFRARED MODES

The DS83CH20 supports a bi–directional serial infrared (IR) wireless communication port. The IR interface connects the UART's serial in and serial out signals (via external transducers) to a transmitter LED and receiver photo diode, respectively.

The IR port of the DS83CH20 is connected to UART B. In IR operation mode, SOUTB is encoded by the DS83CH20 and routed to the Infrared Transmitter (IRTX) pin. The infrared receiver pin (IRRX) is decoded by the DS83CH20 and routed to SINB.

UART B supports both the IrDA 1.0 and ASK–IR IR modes. The Specific IR mode of operation is selected by the Configuration Register 012H (UART B Mode Register).

When in an IR mode of operation, the modem input pins of UART B are not used and are set to the following default values: RIB* and DCDB* are '1'; DSRB* and CTSB* are '0'. Also, SOUTB is driven high (inactive). In normal modem mode, the default values for the IR port pins are as follows: IRRX is "1"; IRTX is driven low (inactive).

Half duplex or full duplex operation may be selected via the UART B Mode Register. In full duplex operation, both the transmitter and the receiver are enabled simultaneously. In Half duplex operation, the receiver input is blocked to '1' when the transmitter is busy – from the beginning of the start bit until the end of the stop bit(s).

If the half duplex option is chosen, there is a time–out when the direction of the transmission is changed. This time–out starts at the last bit transferred during a transmission and blocks the receiver input until the time–out expires. If the transmit buffer is loaded with more data before the time–out expires, the timer is restarted after the new byte is transmitted. If data is loaded into the transmit buffer while a character is being received, the transmission will not start until the time–out expires after the last receive bit has been received. If the start bit of another character is received during this time–out, the timer is restarted after the new character is received. The time–out is 15 bit times when the direction changes from receive to transmit and is approximately 70 ns when the direction changes from transmit to receive.

The following discusses the operation of the two infrared modes supported by the DS83CH20.

6.3.1 IrDA

IrDA allows serial communication at baud rates up to 115.2 kbps. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a single IR pulse at the beginning of the serial bit time. A one is signaled by sending no IR pulse during the bit time. The duration of an IR pulse is 3/16 of a bit cell time. This translates to a minimum pulse duration of ~1.63 µs

for a 115.2 kbps transfer and a maximum pulse duration of ~78 µs for a 2400 bps transfer. The DS83CH20 allows the width of the pulse to be fixed at 1.63 µs for all baud rates or to be scaled with the baud rate. Either of these modes meet the IrDA standard, but the fixed 1.63 µs pulses save power at lower baud rates. The fixed mode or scaled mode of operation is set by bit 6 of the UART B Mode Register. Please refer to the AC timing for the parameters of the IrDA waveform.

6.3.2 ASK–IR

The Amplitude Shift Keyed IR (ASK–IR) allows serial communications at data rates up to 57.6 kbps. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a 500 KHz waveform for the duration of the serial bit time. A one is signaled by sending no transmission during the bit time. Please refer to the AC timing for the parameters of the ASK–IR waveform.

6.3.3 Loopback Mode

The DS83CH20 has the capability to place the IR port in a local loopback mode for diagnostic testing. Enabling the loopback feature is accomplished by enabling the Test Mode Enable bit – bit 0 of the UART B Mode Register (012H). Note that MCR[4] must also be cleared to 0.

7.0 REAL TIME CLOCK

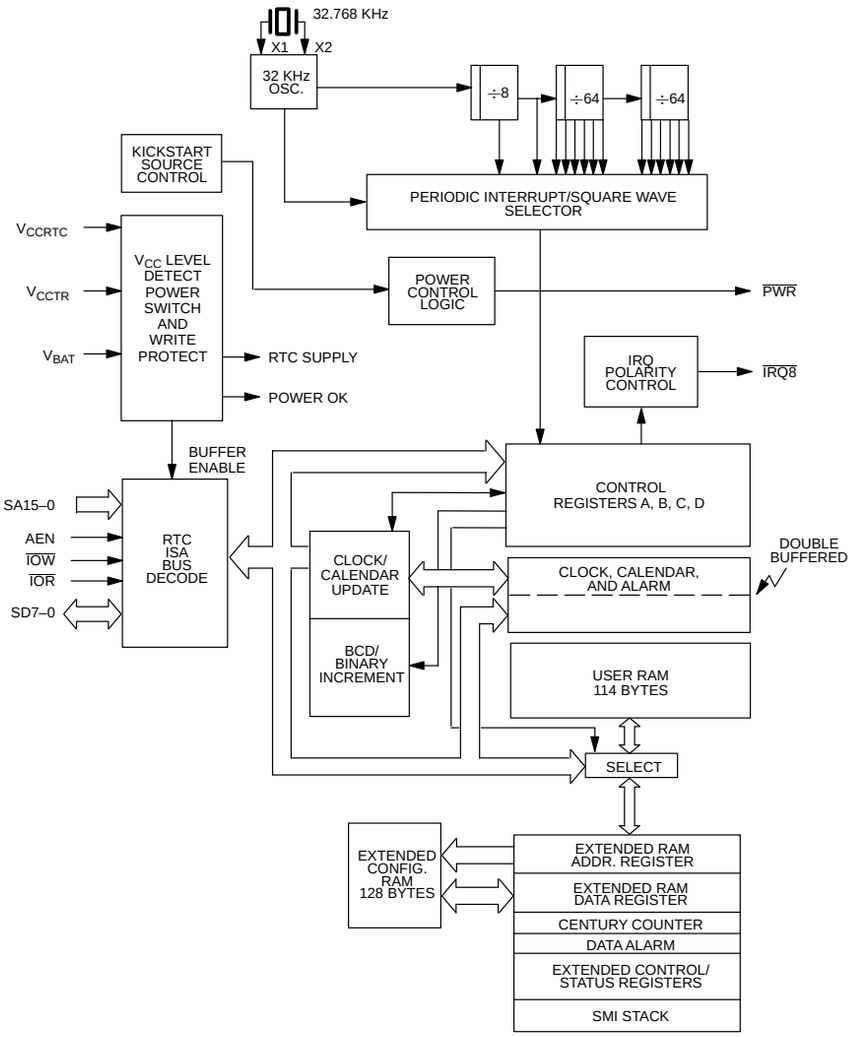
7.1 OVERVIEW

The on–chip real time clock (RTC) provides the industry standard DS1285 clock function for a AT compatible PC as well as a number of enhanced functions. A list of the enhanced features are given below:

- 242 bytes configuration NVRAM
- Crystal select bit allows RTC to operate with 6 pF or 12.5 pF crystal
- Century register
- Date alarm register
- Power control circuitry supports system power on from date/time alarm or key closure

A block diagram shown in Figure 7–1 illustrates the on–chip real time clock.

RTC BLOCK DIAGRAM Figure 7–1



7.2 POWER UP/DOWN OPERATION

The real time clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} inputs. When V_{CC} is applied and reaches a level of greater than V_{PF} (power fail trip point), the device becomes accessible after t_{REC}, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied.

When V_{CC} is below V_{PF}, read and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below V_{PF}, the RAM and timekeeper are switched over to the backup supply pin (V_{BAT} or V_{CCTR}) with the greater voltage.

7.3 RTC ADDRESS MAP

The RTC function is accessed through an index and data register pair which is mapped to I/O locations 70H (index) and 71H (data). The decode is internally performed on the DS83CH20. All RTC registers and RAM locations are accessed by writing the appropriate address to the index register at 70H and then reading or writing the data register at 71H.

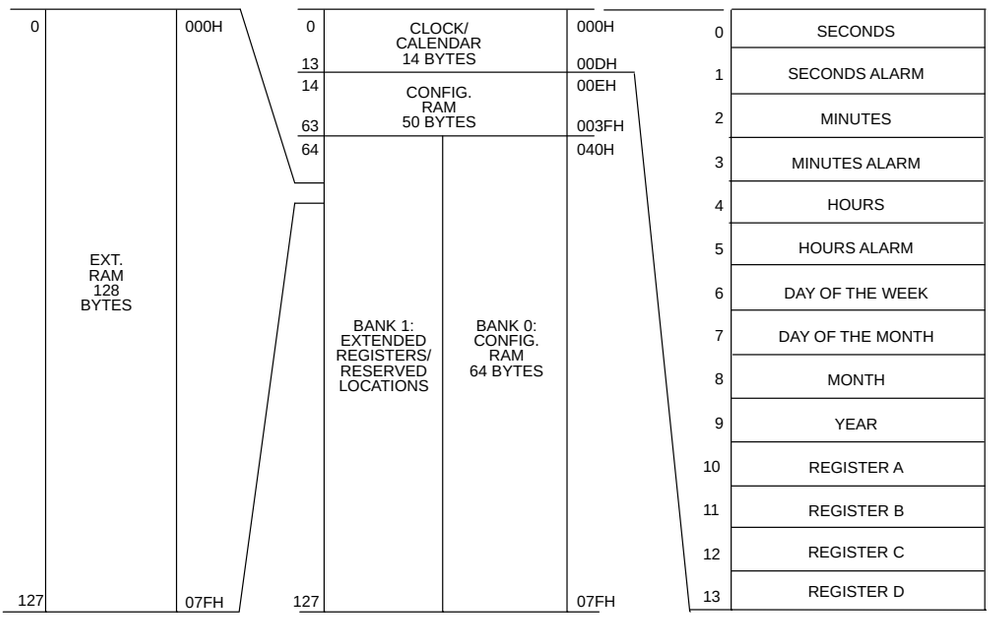
The address map for the RTC is shown in Figure 7–2. The address map contains the clock/calendar registers, the extended registers, and the 242 byte configuration RAM.

7.3.1 Clock/Calendar Registers

The address map consists of the 14 clock/calendar registers. Ten registers contain the time, calendar, and alarm data, and four bytes are used for control and status. All registers can be directly written or read except for the following:

1. Registers C and D are read–only.
2. Bit–7 of Register A is read–only.
3. The high order bit of the seconds byte is read–only.

RTC ADDRESS MAP Figure 7–2



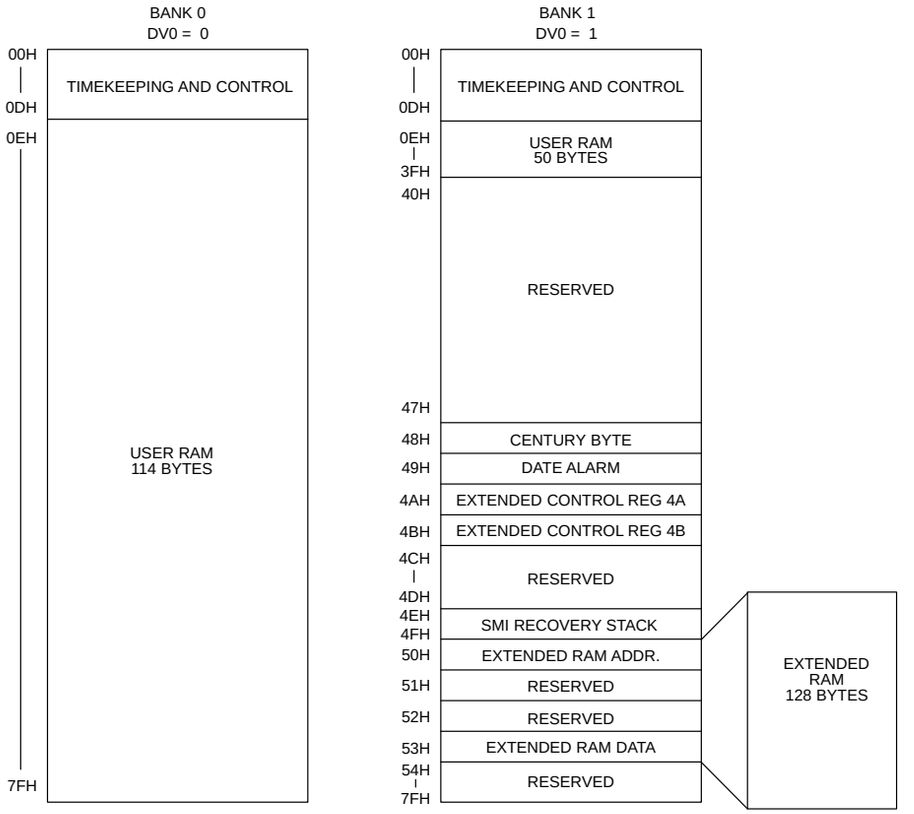
7.3.2 Extended Registers

The extended functions provided by the RTC are accessed via a software controlled bank switching scheme, as illustrated in Figure 7–3. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1285. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the RTC clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the Dallas registers which provide control and status for the extended functions will be accessed in place of the additional 64 bytes of user RAM. The major extended functions controlled by the Dallas registers are listed below:

1. Century Byte
2. Date Alarm
3. V_{CCTR} Status
4. Wake Up
5. Kickstart
6. SMI Stack Recovery

RTC EXTENDED REGISTER BANK DEFINITION Figure 7–3



The bank selection is controlled by the state of the DV0 bit in register A. To access bank 0 the DV0 bit should be written to a 0. To access bank 1, DV0 should be written to a 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Dallas Semiconductor. Bits in these locations cannot be written and will return a 0 if read.

7.3.3 Nonvolatile RAM – RTC

The 242 general purpose nonvolatile RAM bytes are not dedicated to any special function within the RTC. They can be used by the application program as nonvolatile memory and are fully available during the update cycle.

The user RAM is divided into two separate memory banks. When the bank 0 is selected, the 14 real time clock registers and 114 bytes of user RAM are accessible. When bank 1 is selected, an additional 128 bytes of user RAM are accessible through the extended RAM address and data registers.

7.4 CONTROL REGISTERS

The four main control registers, A, B, C, and D, reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

Two extended control registers are provided to supply controls and status information for the extended features offered by the RTC. These are designated as extended control registers A and B and are located in register bank 1, locations 04AH and 04BH, respectively.

7.4.1 Register A

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP – The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µS. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2 – These bits are defined as follows:

DV2 = Countdown Chain
1 – resets countdown chain only if DV1=1
0 – countdown chain enabled

DV1 = Oscillator Enable
0 – oscillator off
1 – oscillator on

DV0 = Bank Select
0 – original bank
1 – extended registers

A pattern of 01X is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 01X is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 – These four rate–selection bits select one of the 13 taps on the 15–stage divider or disable the divider output. The tap selected can be used set the rate for a periodic interrupt. Table 7–3 lists the periodic interrupt rates that can be chosen with the RS bits.

7.4.2 Register B

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	–	DM	24/12	DSE

SET – When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the RTC.

PIE – The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ8}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ8}$ pin active at a rate specified by the RS3–RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ8}$ output from being driven by a periodic interrupt, but the

Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal RTC functions.

AIE – The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ8}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ8}$ signal. The internal functions of the RTC do not affect the AIE bit.

UIE – The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ8}$. The SET bit going high clears the UIE bit.

(–) – Reserved.

DM – The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 – The 24/12 control bit establishes the format of the hours byte. A one indicates the 24–hour mode and a zero indicates the 12–hour mode. This bit is read/write.

DSE – The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions. Note, the day of the Week Register must be set correctly for this feature to function properly.

7.4.3 Register C

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF – The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1 WF = WIE = 1 UF = UIE = 1
AF = AIE = 1 KF = KSE = 1

i.e., IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE) + (WF • WIE) + (KF • KSE)

Any time the IRQF bit is a one, the $\overline{IRQ8}$ pin is driven active. Flag bits PF, AF, and UF are cleared after Register C is read by the program.

PF – The Periodic Interrupt Flag (PF) is a read–only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ8}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF – A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ8}$ pin will go active and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF – The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ8}$ pin. UF is cleared by reading Register C.

BIT 0 THROUGH BIT 3 – These are unused bits of the status Register C. These bits always read zero and cannot be written.

7.4.4 Register D

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT – The Valid RAM and Time (VRT) bit indicates the condition of the battery connected to the V_{BAT} pin. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted lithium energy source is indicated.

BIT 6 THROUGH BIT 0 – The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

7.4.5 Register 4A

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	*	*	PAB	–	WF	KF

VRT2 – This status bit gives the condition of the V_{CCTR}. It is set to a logic 1 condition when voltage is applied to the V_{CCTR} pin. If this bit is read as a logic 0, V_{CCTR} voltage is not present.

INCR – Increment in Progress status bit. This bit is set to a 1 when an increment to the time/date registers is in progress and the alarm checks are being made. INCR will be set to a 1 at 122 ms before the update cycle starts and will be cleared to 0 at the end of each update cycle.

PAB – Power Active Bar control bit. When this bit is 0, the $\overline{PWR}$ pin is in the active low state. This bit can be written to a logic 1 or 0 by the user. If either WF AND WIE = 1 OR KF AND KSE = 1, the PAB bit will be cleared to 0.

(–) – Reserved*

WF – Wake up Alarm Flag. This bit is set to 1 when a wake up alarm condition occurs or when the user writes it to a 1. WF is cleared by writing it to a 0.

KF – Kickstart Flag. This bit is set to a 1 when a kick–start condition occurs or when the user writes it to a 1. This bit is cleared by writing it to a logic 0.

7.4.6 Register 4B

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	–	CS	–	PRS	–	WIE	KSE

ABE – Auxiliary Battery Enable. This bit when written to a logic 1 will enable the V_{CCTR} backup supply pin for extended functions.

(–) – Reserved*

CS – Crystal Select Bit. When CS is set to a 0, the oscillator is configured for operation with a crystal that has a 6 pF specified load capacitance. When CS=1, the oscillator is configured for a 12.5 pF crystal.

(–) – Reserved*

PRS – PAB Reset Select Bit. When set to a 0 the $\overline{PWR}$ pin will be set to a high–Z state when the DS83CH20 goes into power fail. When set to a 1, the $\overline{PWR}$ pin will remain active upon entering power fail.

(–) – Reserved*

WIE – Wake Up Alarm Interrupt Enable. When V_{CC} voltage is absent and WIE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a wake up condition occurs, causing the WF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ8}$ pin will also be driven active. If WIE is set while system power is applied, both $\overline{IRQ8}$ and $\overline{PWR}$ will be driven active in response to WF being set to 1. When WIE is cleared to a 0, the WF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ8}$ pins.

KSE – Kickstart Interrupt Enable. When V_{CC} voltage is absent and KSE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a kickstart condition occurs ($\overline{KS}$ pulsed low), causing the KF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ8}$ pin will also be driven active. If KSE is set to 1 while system power is applied, both $\overline{IRQ8}$ and $\overline{PWR}$ will be driven active in response to KF being set to 1. When KSE is cleared to a 0, the KF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ8}$ pins.

*Reserved bits. These bits are reserved for future use by Dallas Semiconductor. They can be read and written, but have no effect on operation.

7.4.7 Register Power on Conditions

When power is first applied to the DS83CH20 from a previous unpowered condition, whether it is through V_{BAT}, V_{CCTR}, or V_{CC} certain bits are biased so that they will be initialized to a known state. These bits are summarized in Table 7–1.

FIRST POWER ON INITIALIZATION Table 7–1

BIT	NAME	REGISTER	FIRST POWER ON STATE	EXPLANATION
PAB	Power On Bar	4A	1	Initializing this bit to a 1 insures that the $\overline{PWR}$ pin will be in its inactive (high) state
WF	Wake Up Interrupt Flag	4A	0	Initialized to prevent a pending interrupt condition at power on
KF	Kickstart Interrupt Flag	4A	0	Initialized to prevent a pending interrupt condition at power on
CS	Crystal Select	4B	1	Initialized to configure the RTC osc. for a widely available 12 pF 32,768 Hz crystal
PRS	PAB Reset Select Bit	4B	1	Initialized so that $\overline{PWR}$ will remain active upon entering power fail
WIE	Wake Up Interrupt / Enable	4B	0	Initialized with the Wake–Up function and interrupt disabled
KSE	Kickstart Interrupt / Enable	4B	1	Initialized with the Kickstart function and interrupt disabled
ABE	Auxilliary Battery Enable	4B	1	Enables V_{CCTR} to Power Kickstart

In a typical application, a first power on will occur when the lithium battery is installed after the board has been assembled with the DS83CH20. Following the lithium battery installation, almost all of the control/status bits will retain their state in the absence of V_{CC} or V_{CCTR} so long as there is sufficient voltage on the V_{BAT} pin. The only exception is DV2 and DV1. Following every power on condition, DV1 is set to a 1 to insure that the oscillator is on, and DV2 is reset to 0 to enable the countdown chain.

7.5 TIME, CALENDAR AND ALARM OPERATION

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 7–1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary–Coded Decimal (BCD) format. Table 7–1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations that reside in both

bank 0 and in bank 1, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching will be explained later in this text).

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real–time clock to update the time and calendar bytes.

Once initialized, the real time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12–hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The four alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second use condition is to insert a “don’t care” state in one or more of the four alarm bytes. The “don’t care” code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the “don’t care” condition when at logic 1. An alarm will be generated each hour when the “don’t care” bits are set in the hours byte. Similarly, an alarm is generated every minute with “don’t care” codes in the hours and minute alarm bytes. The “don’t care” codes in all three alarm bytes create an interrupt every second. The three alarm bytes may be used in conjunction with the date alarm as described in the Wakeup/Kickstart section. The century counter will be discussed later in this text.

TIME, CALENDAR AND ALARM MODES Table 7–2

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE BINARY DATA MODE	BCD DATA MODE
00H	Seconds	0–59	00–3b	00–59
01H	Seconds Alarm	0–59	00–3b	00–59
02H	Minutes	0–59	00–3b	00–59
03H	Minutes Alarm	0–59	00–3b	00–59
04H	Hours 12–hr. Mode	1–12	01–0C AM, 81–8c pm	01–12 am, 81–92 pm
	Hours 24–hr. Mode	0–23	00–17	00–23
05H	Hours Alarm 12–hr. Mode	1–12	01–0C AM, 81–8c pm	01–12am, 81–92 pm
	Hours Alarm 24–hr. Mode	0–23	00–17	00–23
06H	Day of Week Sunday=1	1–7	01–07	01–07
07H	Date of Month	1–31	01–1f	01–31
08H	Month	1–12	01–0c	01–12
09H	Year	0–99	00–63	00–99
bank 1, 48H	Century	0–99	00–63	00–99
bank 1, 49H	Date Alarm	1–31	01–1f	01–31

7.5.1 DV2–0 Bit Operation

A pattern of 01X in the DV2, DV1, and DV0, bits respectively, will turn the oscillator on and enable the countdown chain. Note that this is different than the DS1285, which required a pattern of 010 in these bits. DV0 is now a “don’t care” because it is used for selection between register banks 0 and 1.

A pattern of 11X will turn the oscillator on, but the oscillator’s countdown chain will be held in reset, as it was in the DS1285. Any other bit combination for DV2 and DV1 will keep the oscillator off.

7.6 INTERRUPT CONTROL

The RTC includes five separate, fully automatic sources of interrupt for a processor:

1. Alarm interrupt
2. Periodic interrupt
3. Update–ended interrupt
4. Wake up interrupt
5. Kickstart interrupt

The conditions which generate each of these independent interrupt conditions are described in greater detail later in the RTC chapter. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, are to be used. There are a total of five bits including three bits in Register B and two bits in Extended Register B which enable the interrupts. Writing a logic 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt enable bit prohibits the $\overline{IRQ8}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ8}$ will immediately be set at an active level, even though the event initiating the interrupt condition may have occurred much earlier. As a result, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to a logic 1 in Register C or in Extended Register A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C as they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that bits which are set remain stable throughout the read cycle. All bits which were set are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The flag bits in Extended Register A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the $\overline{IRQ8}$ line will be driven active when an interrupt flag bit is set and its corresponding enable bit is also set. $\overline{IRQ8}$ will be held active as long as at least one of the five possible interrupt sources has it s flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the $\overline{IRQ8}$ pin is being driven active as a result of one of the five possible active sources. Therefore, determination that the RTC initiated an interrupt is accomplished by reading Register C and finding IRQF=1. IRQF will remain set until all enabled interrupt flag bits are cleared to 0.

7.6.1 Periodic Interrupt Selection

The periodic interrupt will cause the $\overline{IRQ8}$ pin to go to an active state from once every 500 ms to once every 122 ms. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same RS3–0 bits in Register A which select the square wave frequency (see Table 7–1). Changing the bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

7.6.2 Update Cycle

The RTC executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, alarm and elapsed time byte is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows the time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a “don’t care” code is present in all alarm locations.

There are three methods that can handle access of the real–time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update–ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

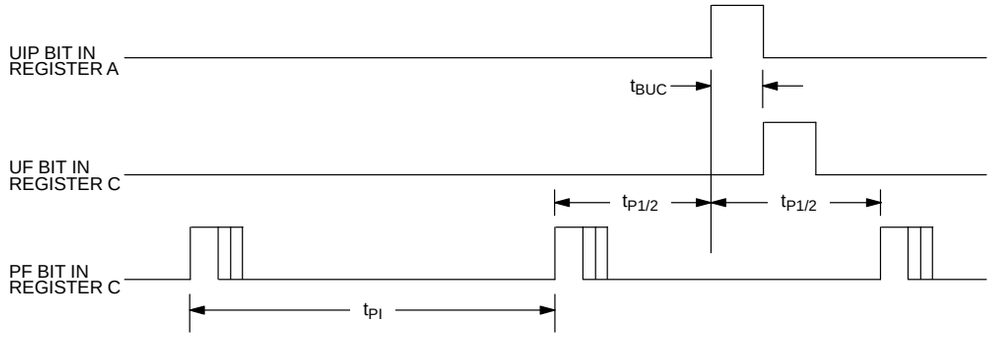
A second method uses the update–in–progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 ms later. If a low is read on the UIP bit, the user has at least 244 ms before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 ms.

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 7–3

SELECT BITS REGISTER A				TPI PERIODIC INTERRUPT RATE
RS3	RS2	RS1	RS0	
0	0	0	0	None
0	0	0	1	3.90625 ms
0	0	1	0	7.8125 ms
0	0	1	1	122.070 µs
0	1	0	0	244.141 µs
0	1	0	1	488.281 µs
0	1	1	0	976.5625 µs
0	1	1	1	1.953125 ms
1	0	0	0	3.90625 ms
1	0	0	1	7.8125 ms
1	0	1	0	15.625 ms
1	0	1	1	31.25 ms
1	1	0	0	62.5 ms
1	1	0	1	125 ms
1	1	1	0	250 ms
1	1	1	1	500 ms

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 7–4). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within (t_{PI} / 2+t_{BUC}) to ensure that data is not read during the update cycle.

UPDATE–ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 7–4



t_{PI} = PERIODIC INTERRUPT TIME INTERNAL PER TABLE 1
t_{BUC} = DELAY TIME BEFORE UPDATE CYCLE = 244 µs

7.7 CENTURY BYTE

A register has been added in bank 1, location 48H, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

7.8 V_{CCTR}

The V_{CCTR} input is provided to supply power from a trickle power supply source for the DS83CH20 kickstart, wake up, and SQW output features in the absence of V_{CC}. This power source must be available in order to use these auxiliary features when no V_{CC} is applied to the device.

The Auxiliary Battery Enable (ABE; bank 1, register 04BH) bit in extended control register B is used to turn on and off the auxiliary power source for the above functions in the absence of V_{CC}. When set to a 1, V_{CCTR} battery power is enabled, and when cleared to 0, V_{CCTR} power is disabled to these functions.

In the DS83CH20, this auxiliary supply may be used as the primary backup power source for maintaining the clock/calendar, user RAM, and extended external RAM functions. This occurs if the V_{BAT} pin is at a lower voltage than V_{CCTR}. If the DS83CH20 is to be backed–up using a single battery with the auxiliary features enabled, then V_{CCTR} should be used and connected to V_{BAT}. If V_{CCTR} is not to be used, it should be grounded and ABE should be cleared to 0.

7.9 WAKE UP/KICKSTART

The RTC incorporates both a wake up and kickstart feature which can power the system on at a pre–determined date through activation of the $\overline{PWR}$ output pin. The operation of these feature is fully described in the Power Management section of this specification.

7.10 SMI RECOVERY STACK

An SMI (System Management Interrupt) recovery register stack is located in the extended register bank, locations 4Eh and 4Fh. This register stack, shown below, can be used by the BIOS to recover from an SMI occuring during an RTC read or write.

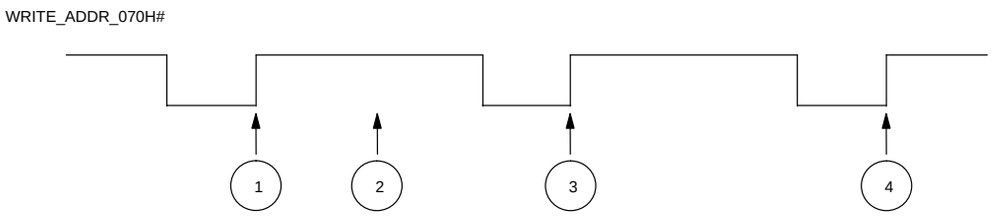
SMI RECOVERY STACK Figure 7–5

	RTC ADDRESS
	RTC ADDRESS – 1
4Eh	RTC ADDRESS – 2
4Fh	RTC ADDRESS – 3

SMI RECOVERY STACK

The RTC address is latched on each write to I/O address 070H. Each time an RTC address is latched, the register address stack is pushed. The stack is only four registers deep, holding the three previous RTC addresses in addition to the current RTC address being accessed. The following waveform illustrates how the BIOS could recover the RTC address when an SMI occurs.

SMI RECOVERY EXAMPLE TIME LINE Figure 7–6



NOTES:

1. The RTC address is latched.
2. An SMI is generated before an RTC read or write occurs.
3. RTC address 0Ah is latched and the address from “1” is pushed to the “RTC Address – 1” stack location. This step is necessary to change the bank select bit, DV0 = 1.
4. RTC address 4Eh is latched and the address from “1” is pushed to location 4Eh, “RTC Address – 2” while 0Ah is pushed to the “RTC Address – 1” location. The data in this register, 4Eh, is the RTC address lost due to the SMI.

8.0 KEYBOARD CONTROLLER

8.1 INTRODUCTION

The keyboard controller (KBC) is a general purpose 8–bit microcontroller. It consists of 256 bytes of data RAM, 4K bytes of Read–Only Memory (ROM), two 8–bit I/O ports, a three register system interface, an 8–bit timer/counter, and facilities for both binary and Binary Coded Decimal (BCD) arithmetic. Figure 8–1 shows the relationships of these functional blocks and Figure 8–2 displays the interface between the DS83CH20 and a host system.

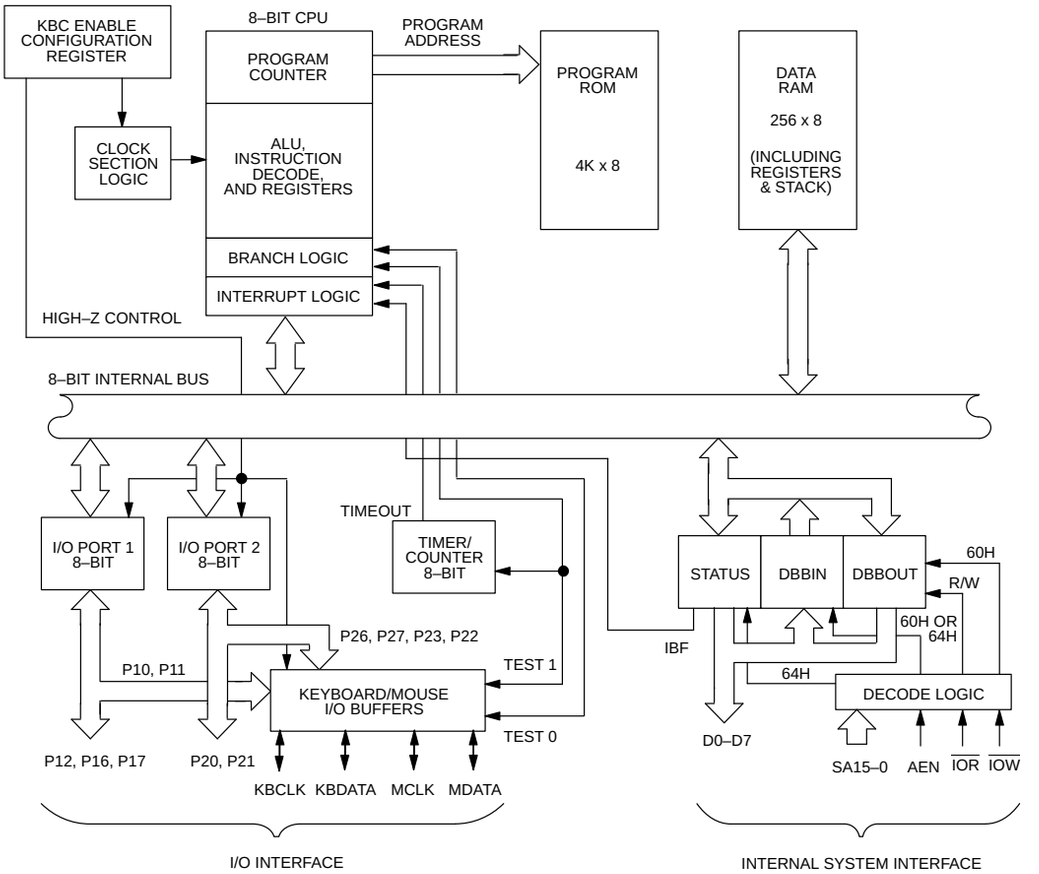
The ROM may be custom programmed during manufacture according to customer requirements. These versions of devices are available by special order.

The KBC is software compatible with the 8042AH industry standard keyboard controller. The DS83CH20 can execute code previously written for an 8042 without further development.

8.2 KBC ENABLE

Following a hardware reset, the keyboard controller is disabled and in power down mode with its I/O pins enabled. The KBC Leakage Control bit can be used to place the KBC pins in a high–Z condition during a power down state. Finally, the clock speed of the KBC can be set to 8 or 12 MHz via the speed select bit in the KBC enable register.

KEYBOARD CONTROLLER FUNCTIONAL BLOCK DIAGRAM Figure 8–1



8.3 HOST SYSTEM INTERFACE

8.3.1 Common Signals

The keyboard controller is interfaced to the host system through a common system interface. The interface consists of the address bus SA15–0, Address Enable (AEN) signal, data bus SD7–0, and control signals I/O Read ($\overline{IOR}$), and I/O Write ($\overline{IOW}$), (see Figure 8–2).

Address bus SA15–0 connects to the ISA system address bus. The DS83CH20 uses the system address and the AEN signal to decode the access to the configuration register.

Data bus SD7–0 connects to the ISA data bus of the system.

The $\overline{IOR}$ and $\overline{IOW}$ inputs connect to the $\overline{IOR}$ and $\overline{IOW}$ lines of the system. All read and write operations to the DS83CH20 are I/O operations.

The DS83CH20 decodes the keyboard controller chip–select from SA15–0 (60h or 64h).

8.3.2 System Interface Registers

The keyboard controller consists of three 8–bit registers: Data Byte Buffer Output (DBBOUT), Data Byte Buffer Input (DBBIN), and STATUS. See Table 8–1.

The DBBOUT register is used to transfer data from the keyboard controller to the host system. It is written by the keyboard controller using the OUT DBB,A instruction. A data read operation by the host system reads its content.

The DBBIN register is used to transfer data from the host system to the keyboard controller. It is written by the host system. It is read by the keyboard controller using an IN A, DBB instruction.

The STATUS register holds status information related to the system interface. Figure 8–3 shows the bit definition. It is read–only by the host CPU.

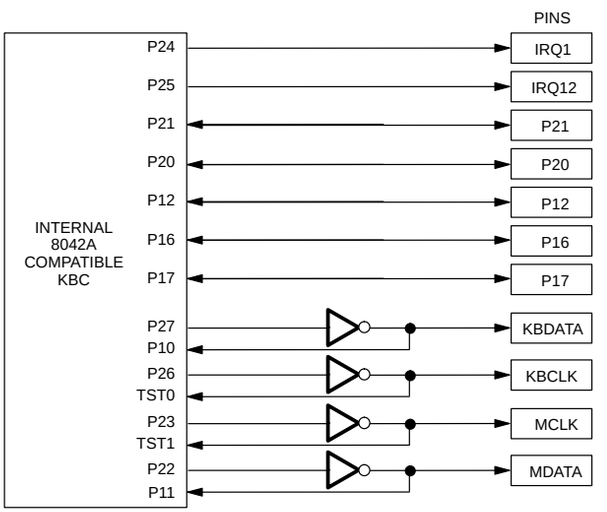
STATUS REGISTER Figure 8–3

	ST7	ST6	ST5	ST4	F1	F0	IBF	OBF
BIT	7	6	5	4	3	2	1	0

Bit 0 **OBF.** Output Buffer Full. A 1 indicates that data is written into the DBBOUT register. It is cleared by a system read operation.

Bit 1 **IBF.** Input Buffer Full. When a write operation is performed by the host system, it will be set to 1. Upon executing an IN A,DBB instruction, it will be cleared.

KEYBOARD CONTROLLER TO HOST SYSTEM INTERFACE Figure 8–2



Bit 2 **IF0.** A general purpose flag that can be cleared or toggled by the keyboard controller software.

Bit 3 **F1.** Command/Data Flag. This flag holds the state of SA2 when the host system performs a write operation. It is typically used to distinguish between commands and data coming from the host system. For example; when SA2 = 1, F1 = 1 and indicates a command was written by the host. When SA2 = 0, F1 = 0, indicating data was written by the host.

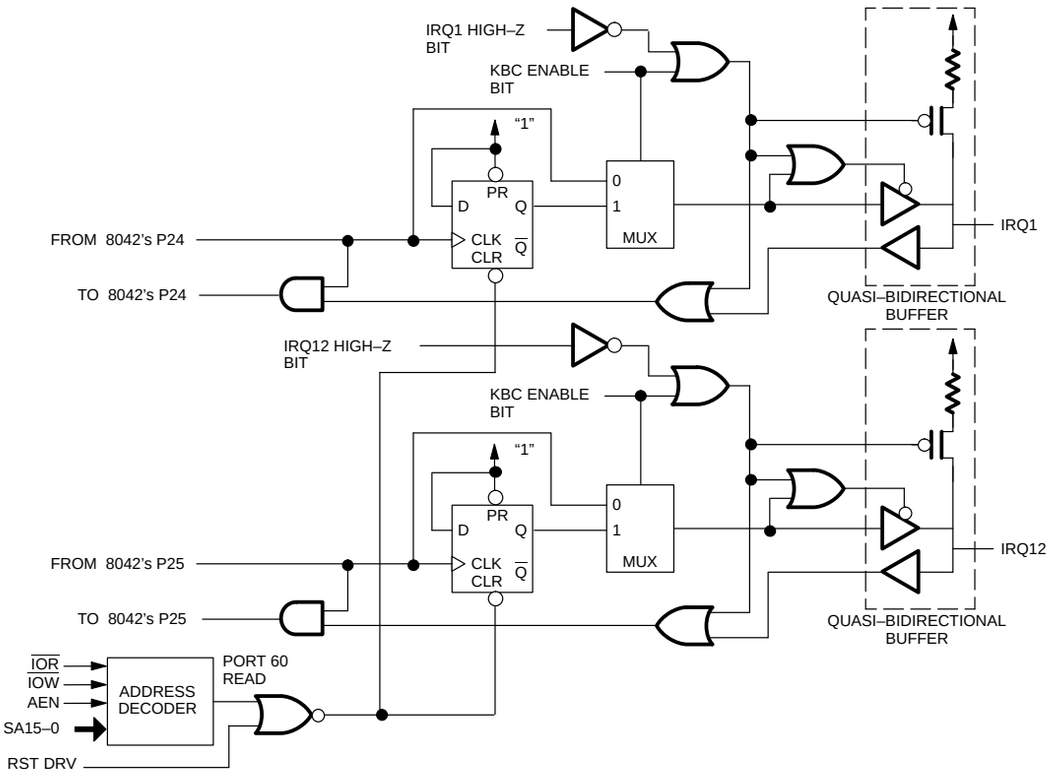
Bit 4–7 **ST4–ST7.** General purpose flags. They can be written by a MOV STS,A instruction.

Table 8–1 shows the register address decoding utilized by the keyboard control system interface.

SUMMARY OF SYSTEM INTERFACE OPERATIONS Table 8–1

$\overline{IOR}$	$\overline{IOW}$	SA2	SA15–SA0	OPERATION
0	1	0	060h	Read DBBOUT
1	0	0	060h	Write DBBIN, F1 Clear
0	1	1	064h	Read STATUS
1	0	1	064h	Write DBBIN, F1 Set
X	X	X	$\overline{060h} \bullet \overline{064h}$	No Operation

FAST IRQ LATCHING AND CLEARING Figure 8–4



8.3.3 IRQ1 and IRQ12

When the KBC is disabled, both IRQ1 and IRQ12 are in a High–Z condition.

When the KBC is enabled, the keyboard and mouse IRQ lines (IRQ1 and IRQ12) are either identical to, or a function of, the 8042's P24 and P25; as detailed in Figure 8–4.

IRQ1 or IRQ12 can be placed in High–Z by setting the associated High–Z control bit in the KBC enable configuration register. When its High–Z bit is set, the IRQ input is blocked to 1.

NOTE: EN FLAGS command (used for routing OBF and IBF onto P24 and P25) will cause unpredictable results and should not be issued.

8.4 PROGRAM MEMORY

The keyboard controller of the DS83CH20 has a 4K x 8 ROM based program memory. A 12–bit program counter allows direct access to every location of the program memory. Figure 8–5 shows the memory map. There are three special locations associated with hardware functions.

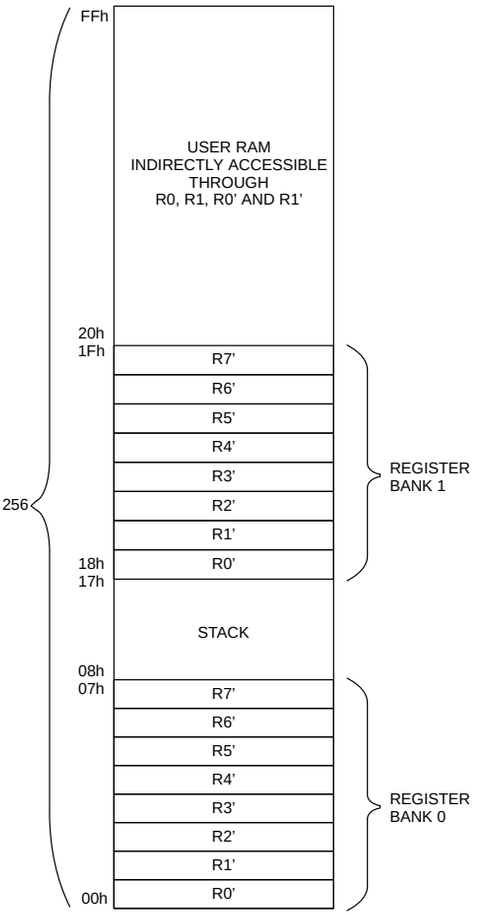
1) 000h After the keyboard controller is reset, the program counter is initialized to 000h.
2) 003h When the input buffer of the host interface (DBBIN) is full, and the IBF interrupt is enabled, the CPU makes an interrupt call to this location.
3) 007h When the timer overflows and the timer interrupt is enabled, the CPU makes an interrupt call to this location.

8.5 DATA RAM AND REGISTERS

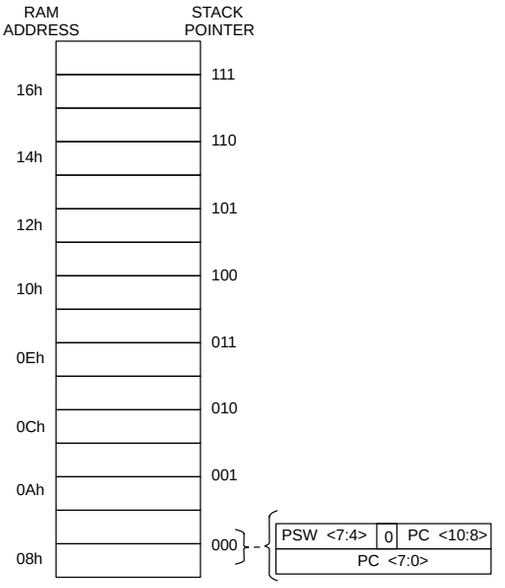
The keyboard controller has 256 bytes of data RAM, including two banks of registers, eight registers each, and an 8–level stack. Figure 8–5 shows the data RAM organization.

RAM locations 0h–7h are used as register bank 0. They are designated as R0–R7 respectively. Register bank 1 (R0'–R7') is located in 18h–1Fh of the address map. Bank 0 is the default register bank when the chip comes out from reset. Bank switching is accomplished by using "register bank select" instructions (SEL RB0, SEL RB1). Locations 8h–17h are reserved for the stack. Each stack entry consists of 2 bytes. Figure 8–6 shows the organization of the stack. The stack pointer in the PSW register points to the top of the stack. A 0 in the stack pointer corresponds to RAM locations 8h and 9h.

KEYBOARD CONTROLLER DATA RAM MAP
Figure 8–5



KEYBOARD CONTROLLER STACK ORGANIZATION Figure 8–6



8.6 PROGRAM STATUS WORD (PSW)

This 8–bit register holds the program execution status. The bit definition of the PSW register is shown in Figure 8–7.

PSW REGISTER BITS Figure 8–7

Bit 7 **CY.** Carry flag of the accumulator.

Bit 6 **AC.** Auxiliary Carry flag of the accumulator, i.e., carry from bit 3 to 4 of the ALU.

Bit 5 **F0.** Flag 0. A general purpose software flag.

Bit 4 **BS.** The current active register bank. 0 = bank0, 1 = bank 1.

Bit 3 **Reserved.** User should not change its power–up value.

Bits 2–0 **Stack Pointer.** 3–bit Stack Pointer for 8–level stack.

When the CPU performs a subroutine call or interrupt call, the PC and the upper four bits of the PSW are pushed into the stack. Upon return, the PSW can be restored in option. If a RETR Return instruction is executed, PSW is restored. PSW is not restored if an RET Return instruction is executed. See Figure 8–6.

8.7 I/O INTERFACE

The keyboard controller of the DS83CH20 provides several general purpose I/O lines, and four open drain I/O lines with internal pull–ups (KBCLK, KBDATA, MCLK, MDATA) as shown in the functional Block Diagram in Figure 8–1.

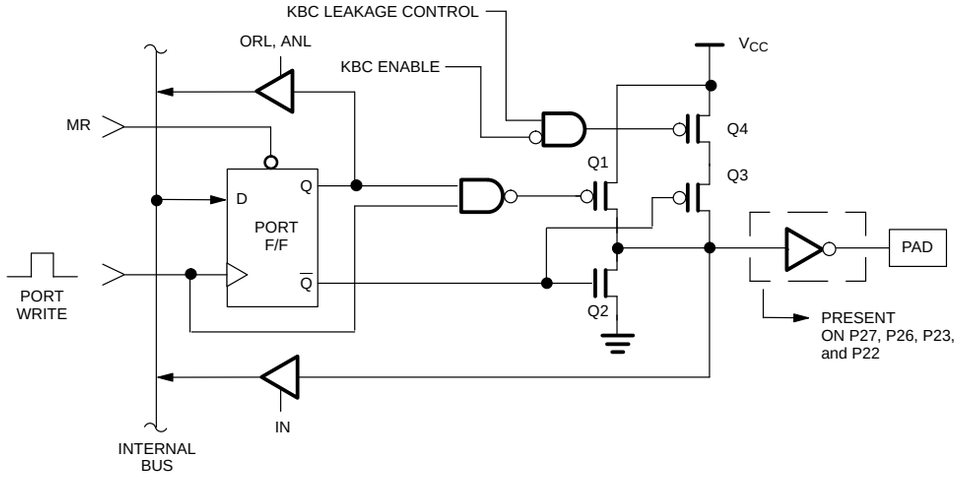
8.7.1 General Purpose I/O

The five general purpose I/O lines, P12, P16, P17, P20 and P21 are mapped to Port 1 and Port 2. These I/O lines are quasi–bidirectional because in normal operation the output buffer cannot be turned off even if the I/O line is intended for input. When a 0 is written to an I/O line, it behaves like an output. When a 1 is written to an I/O line, it behaves like an input. On reset, all I/O lines are inputs.

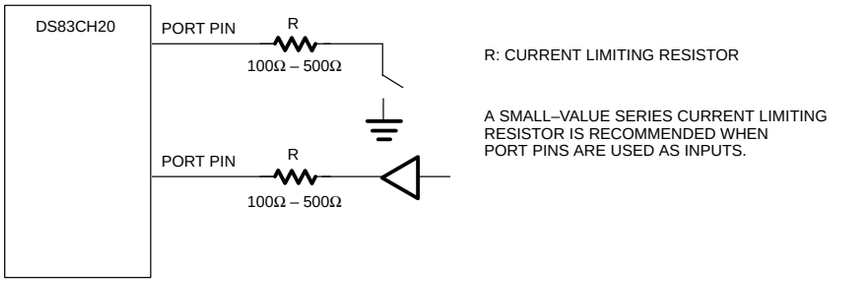
Figure 8–8 illustrates the structure of the I/O line. Q1 and Q2 are the normal output transistors. When the I/O line is intended for output, 0 is written into the flip–flop, which latches, and Q2 turns on. When 1 is written, Q1 turns on briefly because it is gated by a short port–write pulse also. Q1 charges up the pad to near V_{CC} and then turns off. An active pull–up transistor Q3 turns on also, but it provides a large pull–up resistance because it is a weak transistor. At this stage, the I/O line can be used as input: a low impedance low voltage can override the pin and the input buffer reads a low level input. If the pin is driven high or undriven, a high level is read. Therefore, to use a port pin as input, a logic 1 must first be written to it. When the DS83CH20 is reset, all port lines will be initalized to logic 1.

Because Q1 turns on momentarily when a write to the port is performed there is potential for a current surge. A series resistor connected to those port lines used as inputs, is recommended to limit the potential surge (Figure 8–9).

ACTIVE PULL–UP I/O PORT STRUCTURE Figure 8–8



USING PORT PINS AS INPUTS Figure 8–9



8.8 KEYBOARD/MOUSE I/O

In order to reduce the glue logic used in a PC–AT compatible environment, four dedicated outputs are provided: KBCLK, KBDATA, MCLK and MDATA. KBCLK is the complement of P26. KBDATA is the complement of P27. MCLK is the complement of P23. MDATA is the complement of P23. These four drivers can drive 16 mA, making them suitable for driving keyboard and mouse cables. TEST0 and TEST1 are internally connected to KBCLK and KBDATA, respectively, in the PC–AT compatible applications. P10 and P11 are connected internally to KBDATA and MDATA, respectively. 10KΩ Pull–up resistors are provided on KBCLK, KBDATA, MCLK, and MDATA.

8.9 TEST INPUTS

KBCLK and MCLK are two dedicated input pins. Conditional jump instructions directly check the level of these two pins. MCLK also serves as the event counter input.

8.10 TIMER/COUNTER

The keyboard controller is equipped with an 8–bit counter which can be used as a timer or an event counter. Figure 8–10 shows the two different clock sources for the counter. The clock source is selected by software.

8.10.1 Timer Operation

The counter can be set to the timer operation mode by connecting its clock source to the internal timing generator. The clock frequency to the timer is equal to the oscillator frequency divided by 480.

The initial value of the timer is programmable. After the timer is started (by STRT T instruction), it counts up continuously until it is stopped or the keyboard controller is reset. The Timer Overflow Flag is set when the count value overflows from FFh back to 00h. The Timer Overflow Flag can be tested by a conditional jump instruction (JTF). This instruction also resets the flag. When the timer interrupt is enabled, an interrupt occurs when the timer overflows. This is discussed more detail in the interrupt section.

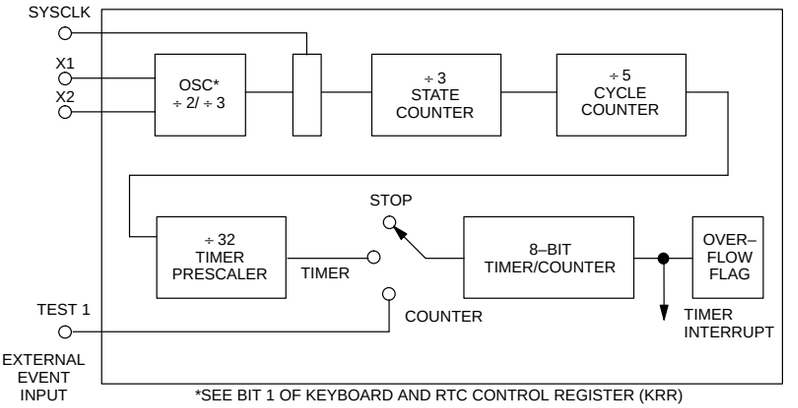
8.10.2 Event Counter Operation

When the clock input of the counter is switched to the external input (MCLK), it essentially becomes an event counter. The falling edge of the signal on the MCLK pin causes the counter to increment. Timer Overflow Flag and Timer Interrupt operate in the same way as they do in the timer mode.

8.11 INTERRUPTS

The keyboard controller of the DS83CH20 provides two different internal interrupts. They are the Input Buffer Full (IBF) interrupt and Timer Overflow interrupt. These two interrupts can be independently enabled or disabled by software. Both of them are disabled when the chip comes out from reset.

TIMING GENERATION AND TIMER CIRCUIT Figure 8–10



8.11.1 Timer Interrupt

If the timer interrupt is enabled upon the timer overflow, an interrupt occurs. It causes the program to perform a subroutine call to program address 007h. The interrupt is cleared by the subroutine call. The current Program Counter (PC) and the upper 4 bits of the PSW is pushed into the stack before the call occurs. At the end of the timer interrupt service routine, an RETR instruction restores the PSW and the PC. Because the timer interrupt has a lower priority than the IBF interrupt, simultaneous IBF and timer interrupts cause the timer interrupt to be pending. It is served as soon as the program returns from the IBF interrupt service routine.

8.11.2 Input Buffer Full (IBF) Interrupt

If the IBF interrupt is enabled, when there is a host write operation to the keyboard controller ($\overline{IOW}$) = 0), an interrupt occurs. The processor saves the current Program Counter and the upper 4 bits of the PSW into the stack and performs a subroutine call to the program address 003h. Upon entering the interrupt service routine, further interrupts are held off. The interrupt is re–enabled upon the execution of the RETR instruction.

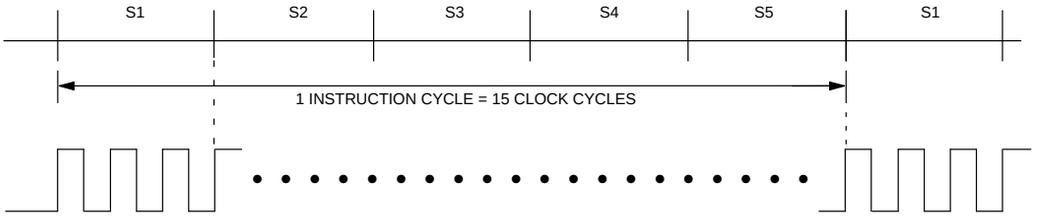
8.12 INSTRUCTION TIMING

The clock for the keyboard controller is derived from the 48/24 MHz clock input. The speed select bit in the KBC Enable configuration register sets the basic clock rate for the keyboard controller at either 8 or 12 MHz.

The oscillator clock is divided by 3 to generate the state timing, then is further divided down by 5 to generate the instruction timing (Figure 8–11). Hence each instruction cycle consists of five states and 15 clock cycles.

Most of the keyboard controller instructions require only one instruction cycle. The others require two cycles. Refer to the instruction set details.

INSTRUCTION CYCLE TIMING Figure 8–11



8.13 SOFT POWER DOWN MODE

The soft power down mode is not supported in the standard keyboard BIOS package. However, the keyboard controller does support this mode and it could be implemented in a modified keyboard BIOS package.

The keyboard controller is placed into this mode by executing a HALT instruction. The execution of program code is halted until either a Master Reset is generated or a data byte is written to the DBBIN register by the host system. If this mode is exited by writing a byte to the DBBIN register and the IBF interrupt is enabled, then program execution resumes with a CALL to the interrupt routine. Otherwise, the next instruction is executed. If the soft power down mode is exited by a Master Reset the a normal reset sequence is initiated and program execution starts from program memory location 0.

8.14 HARD POWER DOWN MODE

The hard power down mode is not supported in the standard keyboard BIOS package. However, the keyboard controller does support this mode and it could be implemented in a modified keyboard BIOS package.

The hard power down mode is entered by executing the STOP instruction. In this mode, the oscillator input to the keyboard controller is disabled. This mode is exited by a Master Reset or by writing a data byte to the DBBIN register. Program execution when exiting the hard power down mode is analogous to that described for the soft power down mode.

9.0 AUXILIARY I/O FUNCTIONS

The DS83CH20 implements three auxiliary I/O functional elements in addition to the FDC, UARTS, parallel port, KBC, and RTC. These auxiliary I/O functions are the general purpose I/O (GPIO) pins, programmable chip select pins, and the X–Bus buffer.

9.1 GENERAL PURPOSE I/O

The GPIO function consists of 12 bits of programmable I/O pins. The entire GPIO function can be enabled or disabled. When enabled, each pin can be individually programmed to perform as an input only, input/output, or electrically isolated from the system (high–Z). The control of the GPIO function is accomplished via the GPIO configuration registers. Refer to the Configuration Register section in this document for a detailed description of these registers.

9.1.1 GPIO Function Programming

The general purpose I/O function can be enabled or disabled via the GPIO Enable bit in the GPIO Enable configuration register. When enabled, the GPIO function consists of 12 bits of programmable I/O pins which are accessible via two contiguous registers located within the ISA map. The location of these two registers within the ISA map is programmable via the GPIO base address configuration register. This allows selection of the base address on any 2–byte boundary within the range of 000H through 1FEH.

During reset, the GPIO function is disabled and removed from the memory map. However, all pins are initialized as inputs and pulled up to V_{CC}.

9.1.2 GPIO Pin Programming

GPIO configuration registers are implemented to select the data direction and isolation control for each individual GPIO bit. Reads and writes to the GPIO pin are accomplished through the GPIO data registers; summarized below:

GP0 DATA REGISTER (GPIO BASE ADDRESS+0)

	D7	D6	D5	D4	D3	D2	D1	D0
Description	GP0.7	GP0.6	GP0.5	GP0.4	GP0.3	GP0.2	GP0.1	GP0.0
H/W Reset	1	1	1	1	1	1	1	1

D7:D0 GP0.7–GP0.0 Data. When GP0 Enable = 1, these bits are used to read/write data from/to the associated GP0 port pins according to the programming of the associated GP0 Data Direction and GP0 Isolation Control bits.

GP1 DATA REGISTER (GPIO BASE ADDRESS+1)

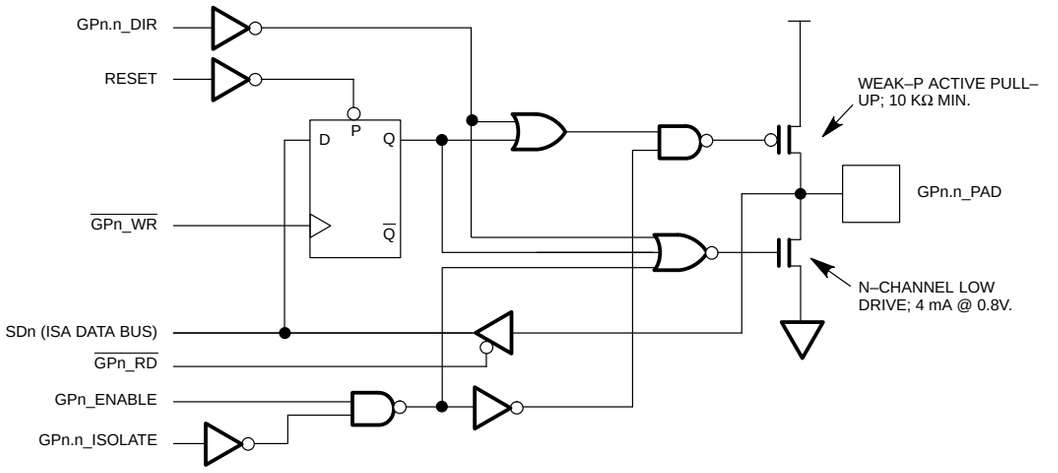
	D7	D6	D5	D4	D3	D2	D1	D0
Description	–	–	–	–	GP1.3	GP1.2	GP1.1	GP1.0
H/W Reset	1	1	1	1	1	1	1	1

D7:D4 Reserved; read as 1.

D3:D0 GP1.3–GP1.0 Data. When GP1 Enable = 1, these bits are used to reads/write data from/to the associated GP1 port pins according to the programming of the associated GP1 Data Direction and GP1 Isolation Control bits.

A functional schematic applicable to all GPIO pins is given in Figure 9–1.

GPIO PIN FUNCTIONAL SCHEMATIC Figure 9–1



As stated above, each pin can be individually programmed to perform as an input only, input/output, or electrically isolated from the system (high–Z).

In order to select a pin as an input only, the associated bit in the GP n Data Direction register must be cleared to 0. In addition, the GP n Enable Bit must be set and the pin's isolation control bit must be cleared to 0. This action will cause the weak–P pull–up to remain on. Reads from the pin are performed by reading the GP n Data Register. Writes to the data register load the latch with the specified data; but the pin's state will be unaffected.

Input/output operation is selected by setting the associated bit in the GP n Data Direction register to a 1. Again, the GP n Enable Bit must be set and the pin's isolation control bit must be cleared to 0. When the data register latch is written to a 0, the weak–p will be off, the n–channel driver will be on, and the pin will be held low. When the data register latch is written to a 1, the weak–P pull–up will be on and the n–channel will be off. In this case, the pin will be at a 1 unless an external device pulls it down to 0. A read from the pin's current state can be performed in this mode by reading the GP n Data Register.

Isolation is performed by setting the associated bit in the GP n Isolation Control register to a 1. In this event both the weak–P and n–channel will be off, and the input buffer will be disabled. The pin's impedance will remain in a high–Z condition. Writes to the data register will load the latch with the specified data, but the pin's state will still be high–Z. Reads from the data register will result in the return of a "1".

9.2 PROGRAMMABLE CHIP SELECT

Two programmable chip select pins are provided on the DS83CH20; $\overline{CS0}$ and $\overline{CS1}$. The function of these pins can be individually controlled via and Programmable Chip Select configuration registers. Refer to the Configuration Register section in this document for a detailed description of these registers.

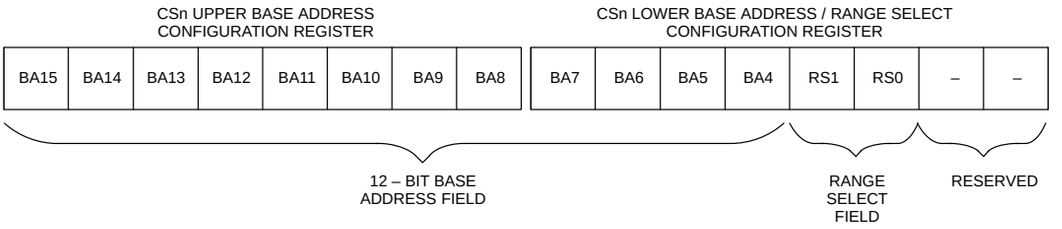
The CS0 and CS1 function can be individually enabled and disabled via the CS0 and CS1 Enable bits. When enabled, the chip select pin will go active when a valid ISA I/O read or write access takes place within a specified decode range starting from a selected base address.

Both $\overline{CS0}$ and $\overline{CS1}$ have a pair of configuration registers used to select the base address and decode range. This pair consists of an upper base address select register, and a lower base address/range select register. The upper register is used to specify bits 15–8 of the chip select function base address. Bits 7–4 of the base address are contained in the upper nibble of the lower register. Bits 3–2 are used to select the four possible decode ranges of 16, 64, 256, and 1K bytes. The base address is programmable on n–byte boundaries

throughout the entire 64K bytes ISA/I/O map; where n is equal to the selected decode range.

Only the required most significant bits of the 12–bit field are used to determine the base address as shown in Figure 9–2.

PROG. CHIP SELECT BASE AND RANGE ADDRESS SELECTION Figure 9–2



RANGE SELECT FIELD VALUE		RANGE VALUE	RESULTING BASE ADDRESS
RS1	RS0		
0	0	16 BYTES	A15 – A4: BA15 – BA4; A3 – A0: X
0	1	64 BYTES	A15 – A6: BA15 – BA6; A5 – A0: X
1	0	256 BYTES	A15 – A8: BA15 – BA8; A7 – A0: X
1	1	1K BYTES	A15 – A10: BA15 – BA10; A9 – A0: X

9.3 X–BUS BUFFER

The DS83CH20 contains one ’245 type buffer that can be used to interface to a BIOS memory or other type of external device. If the X–Bus buffer is not used, then $\overline{XDIR}$ and $\overline{XE}$ must both be tied high.

This function allows data transfers from the X–bus to the ISA bus, or vice–versa. The direction of the transfer is controlled by XDIR. The $\overline{XE}$ enable input, can be used to disable the transfer and isolate the busses. Table 9–1 is a truth table summarizing the operation of the X–bus buffer control pins.

X–BUS BUFFER CONTROL Table 9–1

$\overline{XE}$	$\overline{XDIR}$	OPERATION
0	0	Xfer X–bus data to SD7:0
0	1	Xfer SD7:0 data to X–bus
1	X	Isolation

10.0 POWER MANAGEMENT

10.1 OVERVIEW

The DS83CH20 supports three major modes for power management which are summarized as follows:

1. **Direct Power Down:** Any or all of the on chip devices can be directly powered down under software control. The pins associated with any device can be selected for high–Z while in the power down state.
2. **Auto Power Down:** Any or all of the on–chip devices can be automatically powered down when on–chip hardware detects inactivity to one or more on–chip devices. The pins any device can be selected for high–Z while in the power down state.
3. **Full Chip Power Down:** The entire chip may be powered down by removing system V_{CC} voltage with only minimal functions of the chip powered via a trickle supply voltage on V_{CCTR}. This mode is intended to support a full–board power down, where the entire board is powered down except for the DS83CH20's kickstart and wake–up circuitry and possibly other critical functions on the motherboard. The DS83CH20 can then initiate a power on sequence as a result of a time or date or alarm or from an external stimulus.

Direct and auto power down states and considerations for each type of on–chip device is given below followed by a description of the full–chip power down mode. Much of this description refers to programming of bits within the configuration registers. Refer to the Configuration Register section for a complete description of programming of these bits.

10.2 FLOPPY DISK

Both direct and auto–power down modes are supported for the floppy disk controller.

10.2.1 FDC direct power down

Direct power–down causes an immediate termination of activity in the FDC and holds it in a software reset state. Any command in progress is aborted, so direct power–downs should be avoided during any commands that involve writing to disk. Direct power–down cannot be initiated by software while a software reset is in progress.

One of two methods can be used to place the floppy disk controller in the direct power down state:

METHOD 1:

In method 1 the FDC is placed in direct power down by clearing the FDC Enable bit in the FDC Enable configuration register to 0. The FDC is in a power down state and is removed from the ISA I/O map. The FDC POWD bit is forced to a 1. The drive interface output signals will be inactive and the drive inputs will be enabled while FDC Enable = 0. Note that the inactive state of active low open drain output pins are actually high–Z in this condition.

To exit the power down state invoked using method 1, the FDC Enable bit must first be set to a 1, followed by a FDC software reset sequence. A software reset sequence can be performed by a write of a "1" to the SRST bit (FDC DSR register) or by a write of a "1" to the $\overline{\text{RESET}}$ bit (FDC DOR register).

METHOD 2:

In method 2 the FDC is placed in direct power down by setting the POWD bit (FDC DSR register bit 6) to a 1. The FDC is in power down, but all of the registers will remain in the I/O map according to the programming of the rest of the FDC configuration registers. Registers may be read or written. Values read from registers will reflect their current values in the case of drive interface inputs and register control/status bits. Register writes are stored, but with the exception of a software reset will have no effect until the FDC is restarted. The drive interface output signals will be inactive.

To exit the power down state invoked using method 2, a software reset sequence must be performed either by a write of a "1" to the SRST bit (FDC DSR register) or by a write of a "1" to the $\overline{\text{RESET}}$ bit (FDC DOR register).

The state of the FDC interface pins while in direct power down is summarized in Table 10–1.

FDC PIN STATES – DIRECT POWER DOWN MODE Table 10–1

SYMBOL	I/O	PIN STATE FDC ENABLE = 1; POWD = 1
DENSEL	O	Low
$\overline{\text{DIR}}$	O	High (High–Z)
$\overline{\text{DR0}}$, $\overline{\text{DR1}}$	O	High (High–Z)
DRATE0	O	Low
$\overline{\text{DSKCHG}}$	I	Input – enabled
$\overline{\text{HDSEL}}$	O	Low
INDEX	I	Input – enabled
MSEN0,1	I	Input – enabled
$\overline{\text{MTR0}}$,$\overline{1}$	O	High (High–Z)
$\overline{\text{RDATA}}$	I	Input – enabled
$\overline{\text{STEP}}$	O	High (High–Z)
TRK0	I	Input – enabled
$\overline{\text{WP}}$	I	Input – enabled
$\overline{\text{WRDATA}}$	O	High (High–Z)
$\overline{\text{WREN}}$	O	High (High–Z)

10.2.2 FDC Auto Power Down

Auto power–down mode is set and cleared using the power–down mode command. Once this mode is selected, an auto power–down will occur when both the following conditions are met:

1. The core is idle, indicated by the idle signal being active. For this to be true the following conditions are met:
   - MSR register equals 80h,
   - The head unload time has expired,
   - No interrupts are pending.
2. All motor enable (ME) bits in the DOR register are zero.

Note that there is no auto power–down latency in the FDC so it will auto power–down immediately when the above conditions are met. The power–down mode command bit MDL has no effect on auto power–down. Behavior of the FDC during auto power–down is similar to that during direct power–down.

The part may be restarted after auto power–down with a hardware or software reset, in the same way as described for direct power–down. In addition, either of the following register accesses during auto power–down will restart the part, with all register values and status information preserved:

1. Writing to the data FIFO register.
2. Setting any motor enable bit in the DOR register.

These accesses do not reset the FDC on restart from power–down.

If the FDC is restarted from auto power–down with a software reset, it will return to the power–down condition on exit from reset, if the necessary conditions are still true.

The FDC interface pin conditions during auto power down are summarized in Table 10–2.

FDC PIN STATES – AUTO POWER DOWN MODE Table 10–2

SYMBOL	TYPE	FDC I/F Pin Conditions
DENSEL	O	Output – unchanged
$\overline{\text{DIR}}$	O	Output – unchanged
$\overline{\text{DR0}}$, $\overline{\text{DR1}}$	O	Output – unchanged
DRATE0	O	Output – unchanged
$\overline{\text{DSKCHG}}$	I	Input – enabled
HDSEL	O	Output – unchanged
INDEX	I	Input – enabled
MSEN0, 1	I	Input – enabled
$\overline{\text{MTR0}}$, $\overline{1}$	O	Output – unchanged
RDATA	I	Input – enabled
$\overline{\text{STEP}}$	O	Output – unchanged
TRK0	I	Input – enabled
$\overline{\text{WP}}$	I	Input – enabled
WRDATA	O	Output – unchanged
$\overline{\text{WREN}}$	O	Output – unchanged

10.3 UARTS

Both direct and auto–power down modes are independently supported for each of the two on–chip UARTs as described below.

10.3.1 UART Direct Power Down

Either of the two UARTs can be placed in a direct power down state by clearing the UART Enable bit in the UART Enable configuration register. In this mode, all clocks are disabled to the UART and the device is removed from the ISA I/O map.

The UART output signals will be inactive and its inputs will be enabled while UART (A or B) Enable = 0, if the UART Leakage Control bit is also cleared to 0. If the UART Leakage Control bit is set to 1 while UART Enable = 0, the UART outputs will be in high–Z and the inputs will be disabled.

The UART interface pin conditions during direct power down are summarized in Table 10–3.

UART PIN STATES – DIRECT POWER DOWN MODE Table 10–3

		UART n I/F PIN CONDITIONS	
SYMBOL	**TYPE**	**UART n LEAKAGE CONTROL = 0**	**UART n LEAKAGE CONTROL = 1**
$\overline{\text{CTSn}}$	I	Input – enabled	Input – enabled
$\overline{\text{DCDn}}$	I	Input – enabled	Input – enabled
$\overline{\text{DSRn}}$	I	Input – enabled	Input – enabled
$\overline{\text{DTRn}}$	O	High	High–Z
$\overline{\text{RIn}}$	I	Input – enabled	Input – enabled
$\overline{\text{RTSn}}$	O	High	High–Z
SINn	I	Input – enabled	Input – enabled
SOUTn	O	High	High–Z

10.3.2 UART Auto Power Down

Each of the two UARTs has a Auto Power Management enable bit in its UART Enable configuration register. Setting this bit enables auto power management for the UART; clearing disables it.

When auto power management is enabled, the UART transmitter enters auto power down when the transmit buffer and shift register are empty. The transmitter exits power down on a write to the transmit buffer.

When enabled, the receiver enters auto power down when the receive FIFO is empty and it is awaiting a start bit. Note that while in power down the Ring Indicator interrupt is still valid and transitions when the RI input changes.

When the transmitter or receiver is in auto power down, its associated input pins will be enabled, and its output pins will be driven to their inactive state.

10.4 PARALLEL PORT

Both direct and auto power management modes are supported for the parallel port as described below.

10.4.1 Parallel Port Direct Power Down

The parallel port can be placed in a direct power down state by clearing the Parallel Port Enable bit in the Parallel Port Enable configuration register. In this mode, all clocks are disabled to the parallel port and the device is removed from the ISA I/O map.

The parallel port output signals will be inactive and its inputs will be enabled while Parallel Port Enable = 0, if the leakage control bit is also cleared to 0. If the leakage control bit is set to 1 while Parallel Port Enable = 0, the parallel port outputs will be in high–Z and the inputs will be disabled.

The parallel port interface pin conditions during direct power down are summarized in Table 10–4.

PARALLEL PORT PIN STATES – DIRECT POWER DOWN Table 10–4

		PARALLEL PORT PIN STATES	
SYMBOL	**TYPE**	**PAR. PORT LEAKAGE CONTROL = 0**	**PAR. PORT LEAKAGE CONTROL = 1**
$\overline{\text{ACK}}$	I	enabled	Disabled
$\overline{\text{AUTOFD}}$ / $\overline{\text{DSTRB}}$	O	enabled	High–Z
BUSY / $\overline{\text{WAIT}}$	I	enabled	Disabled
$\overline{\text{ERROR}}$	I	enabled	Disabled
$\overline{\text{INIT}}$	O	enabled	High–Z
PD[7..0]	O	enabled	High–Z
PE	I	enabled	Disabled
SLCT	I	enabled	Disabled
$\overline{\text{SLCTIN}}$ / $\overline{\text{ASTRB}}$	O	enabled	High–Z
$\overline{\text{STB}}$ / $\overline{\text{WRITE}}$	O	enabled	High–Z

10.4.2 Parallel Port Auto Power Auto

When the parallel port is used in either the ISA or PS/2 compatible modes, auto power management is always invoked whenever no data transfer is being performed. In addition, the parallel port has an Auto Power Management Enable bit in the Parallel Port Enable configuration register. When set, this bit allows the ECP or EPP logic to be placed into power down when not being used.

The EPP logic is in powerdown under the following condition:

EPP is not enabled in the Parallel Port Mode configuration register.

The EPP logic will be powered on when it is selected via the mode configuration register.

The ECP logic is in powerdown under any of the following conditions:

1. ECP is not enabled in the configuration registers.
2. ISA or PS/2 parallel port mode is selected through the ECR register while in ECP mode.

The ECP logic will be powered on when ECP mode is selected via the mode configuration register and ISA or PS/2 modes are not selected through the ECR register.

10.5 KEYBOARD CONTROLLER

Both direct and auto power management modes are supported for the parallel port as described below:

10.5.1 Keyboard Controller Direct Power Down

The keyboard controller can be placed in a direct power down state by clearing the Keyboard Controller Enable bit in the Keyboard Controller Enable configuration register. In this mode, all clocks are disabled to the keyboard controller and the device is removed from the ISA I/O map.

The keyboard controller I/O signals will be enabled and in a high condition while Keyboard controller Enable = 0, if the leakage control bit is also cleared to 0. If the leakage control bit is set to 1 while Keyboard Controller Enable = 0, all of the keyboard controller I/O signals will be in high–Z (input function disabled).

The keyboard controller interface pin conditions during direct power down are summarized in Table 10–5.

KEYBOARD CONTROLLER PIN STATES – DIRECT POWER DOWN Table 10–5

		KEYBOARD CTL. PIN STATES	
SYMBOL	**TYPE**	**KEY. CTL. LEAKAGE CONTROL = 0**	**KEY. CTL. LEAKAGE CONTROL = 1**
KBCLK	O	High	High–Z
KBDATA	O	High	High–Z
MCLK	O	High	High–Z
MDATA	O	High	High–Z
P12	O	High	High–Z
P16 / $\overline{KS}$	O	High	High–Z
P17	O	High	High–Z
P20	O	High	High–Z
P21	O	High	High–Z

10.5.2 Keyboard Controller Auto Power Down

Two types of auto power down operation are implemented within the keyboard controller micro core. These are soft power down and hard power down operation as described below:

Soft Power Down Mode

This mode is entered by executing a HALT instruction. The execution of program code is halted until either RSTDRV is driven active or a data byte is written to the DBBIN register by the system CPU. If this mode is exited using the interrupt, and the IBF interrupt is enabled, then program execution resumes with a CALL to the interrupt routine, otherwise the next instruction is executed. If it is exited using RSTDRV then a normal reset sequence is initiated and program execution starts from program memory location 0.

Hard Power Down Mode

This mode is entered by executing a STOP instruction. The microcontroller oscillator is stopped internally by hardware. When either RSTDRV is driven active or a data byte is written to the DBBIN register by a master CPU, this mode will be exited (as above). However, as the oscillator will require an initialization time, either RSTDRV must be held low for sufficient time to allow the oscillator to stabilize.

10.6 FULL CHIP POWER DOWN

As described above the entire DS83CH20 can be powered down by removing V_{CC} voltage while still powering the RTC's wake–up and kickstart functions via a trickle supply voltage on V_{CCTR}. This allows the system to be automatically powered on in response to a wake–up or kickstart condition, resulting in the activation of the $\overline{PWR}$ output pin. The wake–up function allows the system to be automatically powered on at a predetermined date and time. The kickstart functions allows the system to automatically powered on in response to an external stimulus such as a momentary switch closure, modem ring detect signal, or infrared input activity.

In order to use either the wake up or the kickstart features, the DS83CH20 must have an auxiliary power supply connected to the V_{CCTR} pin and the RTC's oscillator must be running and the countdown chain must not be in reset (Register A; DV2, DV1, DV0 = 01X). If DV2, DV1, and DV0 are not in this required state, the $\overline{PWR}$ pin will not be driven low in response to a kickstart or wakeup condition, while in battery–backed mode.

10.6.1 Wake–up

The wake up feature is controlled through the Wake Up Interrupt Enable bit in the RTC's extended control register 4B (WIE, bank 1, 04BH). Setting WIE to 1 enables the wake up feature, clearing WIE to 0 disables it. Simi-

larly, the kickstart feature is controlled through the Kickstart Interrupt Enable bit in the RTC's extended control register 4B (KSE, bank 1, 04BH).

A wake up sequence will occur as follows: When wake up is enabled via WIE = 1 while the system is powered down (no V_{CC} voltage), the clock/calendar will monitor the current date for a match condition with the date alarm register (bank 1, register 049H). In conjunction with the date alarm register, the hours, minutes, and seconds alarm bytes in the clock/calendar register map (bank 0, registers 05H, 03H, and 01H) are also monitored. As a result, a wake up will occur at the date and time specified by the date, hours, minutes, and seconds alarm register values. This additional alarm will occur regardless of the programming of the AIE bit (bank 0, register B, 0BH). When the match condition occurs, the $\overline{PWR}$ pin will automatically be driven low. This output can be used to turn on the main system power supply which provides V_{CC} voltage to the DS83CH20 as well as the other major components in the system. Also at this time, the Wake Up flag (WF, bank 1, register 04AH) will be set, indicating that a wake up condition has occurred.

10.6.2 Kickstart

A kickstart sequence will occur when kickstarting is enabled via by setting the RTC's KSE bit to a 1. This is a global enable, which enables the overall kickstart function and its interrupt via $\overline{IRQ8}$. There are four pins which can be programmed as kickstart sources:

1. Keyboard Controller port pin P16
2. UART A Ring Indicate ($\overline{RIA}$)
3. UART B Ring Indicate ($\overline{RIB}$)
4. Infrared Receive input (IRRX)

Individual bits to enable or disable each of these pins as a kickstart source are provided in the Kickstart Source Select configuration register. Writing a 1 to one of these bits enables the associated pin as a kickstart source; writing a 0 disables it. When a pin is enabled as a kickstart source, it is powered via V_{CCTR} in the absence of V_{CC}. When a pin is disabled as kickstart source, it is powered off in the absence of V_{CC}.

While the system is powered down, the enabled input pins will be monitored for a low going transition of minimum pulse width t_{KSPW}. When such a transition is detected, the $\overline{PWR}$ line will be pulled low, as it is for a wake up condition. Also at this time, the Kickstart Flag (KF, RTC bank 1, register 04AH) will be set, indicating that a kickstart condition has occurred.

10.6.3 Wake–up/Kickstart Timing Description

The timing associated with both the wake up and kickstarting sequences is divided into 5 intervals, labeled 1–5 on the Wake–up/Kickstart timing diagram in the Electrical Characteristics section.

The occurrence of either a kickstart or wake up condition will cause the $\overline{PWR}$ pin to be driven low, as described above. During interval 1, if the supply voltage on the DS83CH20 V_{CC} pin rises above the V_{PF} power fail level before the power on timeout period (t_{POTO}) expires, then $\overline{PWR}$ will remain at the active low level. If V_{CC} does not rise above the power fail voltage in this time, then the $\overline{PWR}$ output pin will be turned off and will return to its high impedance level. In this event, the $\overline{IRQ8}$ pin will also remain tri–stated. The interrupt flag bit (either WF or KF) associated with the attempted power on sequence will remain set until cleared by software during a subsequent system power on.

If V_{CC} is applied within the timeout period, then the system power on sequence will continue as shown in intervals 2–5 in the timing diagram. During interval 2, $\overline{PWR}$ will remain active and $\overline{IRQ8}$ will be driven to its active level, indicating that either WF or KF was set in initiating the power on. In the diagram the kickstart source pin (P16, $\overline{RIA}$, $\overline{RIB}$, or IRRX) is assumed to be pulled up to the V_{CCTR} supply. Also at this time, the PAB bit will be automatically cleared to 0 in response to a successful power on. The $\overline{PWR}$ line will remain active as long as the PAB remains cleared to 0.

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing zeroes to both of these control bits. As long as no other interrupt within the RTC is pending, the $\overline{IRQ8}$ line will be taken inactive once these bits are reset. Execution of the application software may proceed. During this time, both the wake up and kickstart functions may be used to generate status and interrupts. WF will be set in response to a date, hours, minutes, and seconds match condition. KF will be set in response to a low going transition on the enabled kickstart source pin. If the associated interrupt enable bit is

set (WIE and/or KSE) then the $\overline{IRQ8}$ line will driven active in response to enabled event. In addition, the other possible interrupt sources within the RTC may cause $\overline{IRQ8}$ to be driven active. While system power is applied, the on chip logic will always attempt to drive the $\overline{PWR}$ pin active in response to the enabled kickstart or wake up condition. This is true even if $\overline{PWR}$ was previously inactive as the result of power being applied by some means other than wake up or kickstart.

The system may be powered down under software control by setting the PAB bit to a logic 1. This causes the open–drain $\overline{PWR}$ pin to be placed in a high impedance state, as shown at the beginning of interval 4 in the timing diagram. As V_{CC} voltage decays, the $\overline{IRQ8}$ output pin will be placed in a high impedance state when VCC goes below V_{PF}. If the system is to be again powered on in response to a wake up or kickstart, then the both the WF and KF flags should be cleared and WIE and/or KSE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and nonvolatile RAM is in effect, $\overline{PWR}$ and $\overline{IRQ8}$ are tri–stated, and monitoring of wake up and kickstart takes place as programmed.

11.0 ELECTRICAL SPECIFICATIONS

11.1 ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

The Dallas Semiconductor DS83CH20 is built to the highest quality standards and manufactured for long term reliability. All Dallas Semiconductor devices are made using quality materials and manufacturing methods. However, standard versions of the DS83CH20 are not exposed to environmental stresses, such as burn–in. As a results, this device may not conform to Dallas' standard product qualification requirements. For specific reliability information on this product, please contact the factory at (214) 450–0485.

11.2 RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C; V_{CC}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Trickle Supply Voltage	V_{CCTR}	4.5	5.0	5.5	V	1
Lithium Battery Voltage	V_{BAT}	2.5	3.0	3.7	V	1

11.3 DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC}			TBD	mA	1
Standby Current	I_{STBY}		TBD		mA	1, 2, 3
RTC Power Fail Trip Point	V_{PF}	4.25	4.37	4.50	V	1, 2, 6
Battery Switch Voltage	V_{SW}		V_{BAT}, V_{CCTR}		V	1, 7
Battery Leakage OSC ON	I_{BAT1}			1000	nA	
Battery Leakage OSC OFF	I_{BAT2}			100	nA	
Input Leakage Current (all types)	I_{LI}	–10		+10	µA	
I Type Input Buffer Input high level Input low level	 V_{IH} V_{IL}	 2.0		 0.8	 V V	 1
ICLK Type Input Buffer Input high level Input low level	 V_{IHCK} V_{ILCK}	 3.0		 0.4	 V V	 1

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
IS Type Input Buffer (Schmitt)						
Input high level	V_{IHS}	2.2			V	1
Input low level	V_{ILS}			0.8	V	
I/O4–PB2/10K Pseudo–bi–directional Input/Output Buffer						
Output high voltage @ I_{OH1} = –2.0 mA	V_{OH}	2.4		0.4	V	1, 4
Output low voltage @ I_{OH2} = –100 µA	V_{OH}	2.4		0.4	V	1, 4
Output low voltage @ I_{OL} = +4.0 mA	V_{OL}					1, 4
Input/Output leakage	I_{LO}	–10		+10	µA	
O4–2 Totem Pole Output Buffer						
Output high voltage @ I_{OH} = –2.0 mA	V_{OH}	2.4				1
Output low voltage @ I_{OL} = +4.0 mA	V_{OL}			0.4	V	1
Input/Output leakage	I_{LO}	–10		+10	µA	
O12–6 Totem Pole Output Buffer						
Output high voltage @ I_{OH} = –6.0 mA	V_{OH}	2.4				1
Output low voltage @ I_{OL} = +12.0 mA	V_{OL}			0.4	V	1
Input/Output leakage	I_{LO}	–10		+10	µA	
O14–14 Totem Pole Output Buffer						
Output high voltage @ I_{OH} = –14.0 mA	V_{OH}	2.4				1
Output low voltage @ I_{OL} = +14.0 mA	V_{OL}			0.4	V	1
Input/Output leakage	I_{LO}	–10		+10	µA	
OD12 Open Drain Output Buffer						
Output low voltage @ I_{OL} = +12.0 mA	V_{OL}			0.4	V	1
Input/Output leakage	I_{LO}	–10		+10	µA	
OD14 Open Drain Output Buffer						
Output low voltage @ I_{OL} = +14.0 mA	V_{OL}			0.4	V	1
Output leakage	I_{LO}	–10		+10	µA	
OD40 Open Drain Output Buffer						
Output low voltage @ I_{OL} = +40.0 mA	V_{OL}			0.4	V	1
Output leakage	I_{LO}	–10		+10	µA	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
OD4–P10K Type Output Buffer						
Output high voltage	V_{OH}	2.4			V	
@ I_{OH} = –100 µA						
Output low voltage	V_{OL}			0.4	V	1
@ I_{OL} = 4.0 mA						
Output leakage	I_{LO}	–10		+10	µA	
OD16–P10K Type Output Buffer						
Output high voltage	V_{OH}	2.4			V	
@ I_{OH} = –100 µA						
Output low voltage	V_{OL}			0.4	V	1
@ I_{OL} = 16.0 mA						
Output leakage	I_{LO}	–10		+10	µA	
OD40 Type Output Buffer						
Output low voltage	V_{OL}			0.4	V	1
@ I_{OL} = 40.0 mA						
Output leakage	I_{LO}	–10		+10	µA	

NOTES:

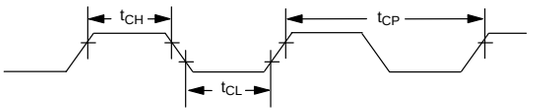
1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supply voltages.
3. Measured with no internal resources selected and all outputs open.
4. I_{OH} is driven for 10 ns on switch from low to high.
5. Open–drain outputs with 10KΩ minimum pull–up resistors.
6. Write protection trip point occurs during power fail prior to switchover from V_{CC} to $V_{BAT.}$
7. V_{SW} is determined by the larger of V_{BAT} and V_{CCTR}.

11.4 SYSTEM INTERFACE TIMING

11.4.1 CCK Input Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock High Pulse Width – 24 MHz	t_{CH24}	16			ns	
Clock Low Pulse Width –24 MHz	t_{CL24}	16			ns	
Clock Period – 24 MHz	t_{CP24}	40		43	ns	
Clock High Pulse Width – 48 MHz	t_{CH48}	8			ns	
Clock Low Pulse Width – 48 MHz	t_{CL48}	8			ns	
Clock Period – 48 MHz	t_{CP48}	20		22	ns	

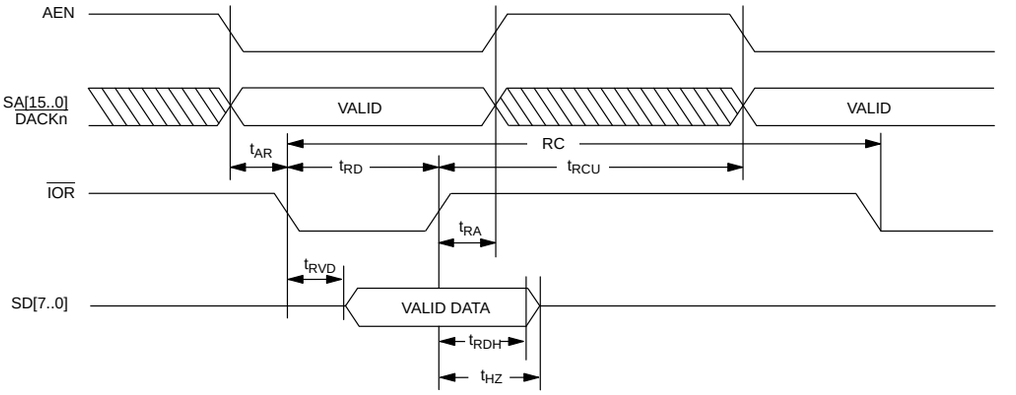
CLOCK TIMING Figure 11–1



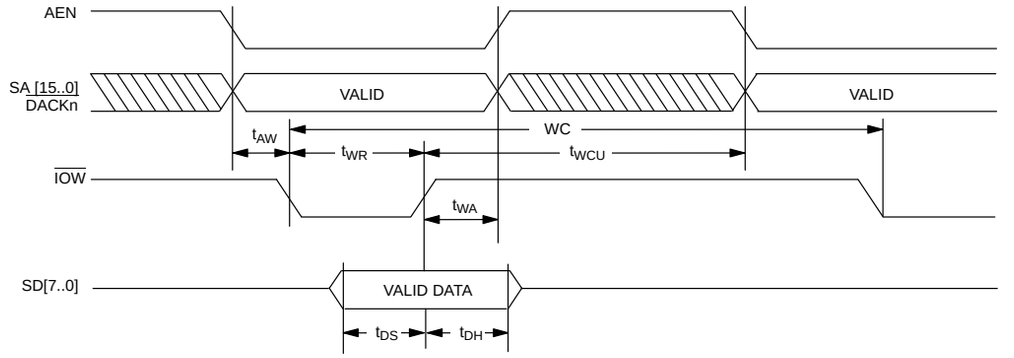
11.4.2 ISA Bus Interface Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Valid Address to Read Active	t_{AR}	18			ns	
Valid Address to Write Active	t_{AW}	18			ns	
Data Hold	t_{DH}	0			ns	
Data Setup	t_{DS}	18			ns	
Read to Floating Data Bus	t_{HZ}	13		35	ns	
Active Read to Valid Data	t_{RVD}			55	ns	
Address Hold from Inactive Write	t_{WA}	0			ns	
Write Cycle Update	t_{WCU}	45			ns	
Address Hold from Inactive Read	t_{RA}	0			ns	
Read Cycle Update	t_{RCU}	45			ns	
Read Strobe Width	t_{RD}	60			ns	
Read Data Hold	t_{RDH}	10			ns	
Write Strobe Width	t_{WR}	60			ns	
Read Cycle = $t_{AR} + t_{RD} + t_{RCU}$	RC	123			ns	
Write Cycle = $t_{AW} + t_{WR} + t_{WCU}$	WC	123			ns	
$\overline{IOR}$ Low after $\overline{IOW}$ High	t_{WRR}	80			ns	

ISA BUS READ CYCLE TIMING Figure 11–2



ISA BUS WRITE CYCLE TIMING Figure 11–3

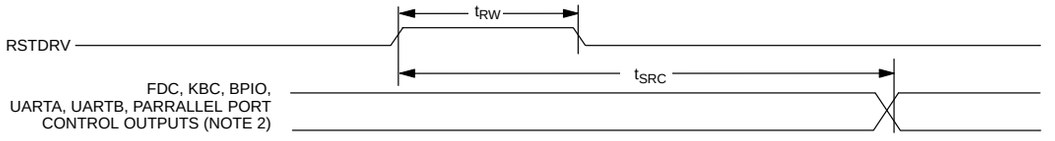


11.4.3 Reset Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Width (Note 1)	t_{RW}	100			µs	
Reset to Control Inactive	t_{SRC}			300	ns	

NOTE 1: The FDC Software reset pulse width is 100 ns.

ISA BUS WRITE CYCLE TIMING Figure 11–4



NOTE 2: All DRQn and IRQn lines go to high–Z after time t_{SRC}.

11.5 FDC TIMING

11.5.1 FDC Clock Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Internal Clock Period	t_{ICP}		(Table 11–1)		ns	
Data Rate Period	t_{DRP}		(Table 11–1)		ns	

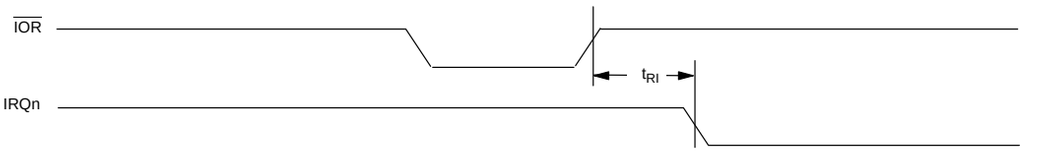
NOMINAL t_{ICP}, t_{DRP} VALUES Table 11–1

MFM DATA RATE	t_{DRP}	t_{ICP}	VALUE	UNITS
1 Mbps	1000	3 x t_{CP}	125	ns
500 Kbps	2000	3 x t_{CP}	125	ns
3333	3333	5 x t_{CP}	208	ns
250 Kbps	4000	6 x t_{CP}	250	ns

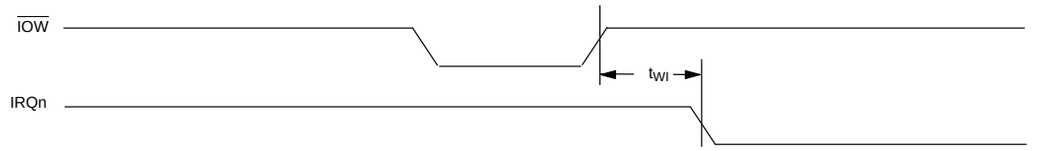
11.5.2 FDC Interrupt Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read strobe to clear FDC IRQn	t_{RI}			55	ns	
Write strobe to clear FDC IRQn	t_{WI}			55	ns	

FDC READ CYCLE INTERRUPT TIMING Figure 11–5



FDC WRITE CYCLE INTERRUPT TIMING Figure 11–6



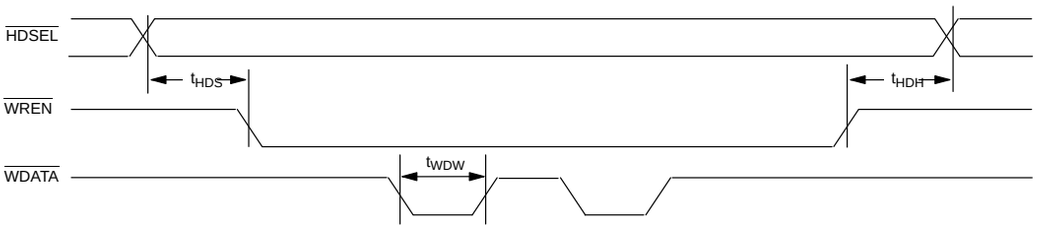
11.5.3 FDC Write Data Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{\text{HDSEL}}$ Hold from $\overline{\text{WGATE}}$ Inactive	t_{HDH}	750			µs	
$\overline{\text{HDSEL}}$ Setup to $\overline{\text{WGATE}}$ Active	t_{HDS}	100			µs	
Write Data Pulse Width	t_{WDW}	(Table 11–2)			ns	

MINIMUM t_{WDW} VALUES Table 11–2

Data Rate	t_{DRP}	t_{WDW}	t_{WDW} VALUE	UNITS
1 Mbps	1000	2 x t_{ICP}	250	ns
500 kbps	2000	2 x t_{ICP}	250	ns
300 kbps	3333	2 x t_{ICP}	375	ns
250 kbps	4000	2 x t_{ICP}	500	ns

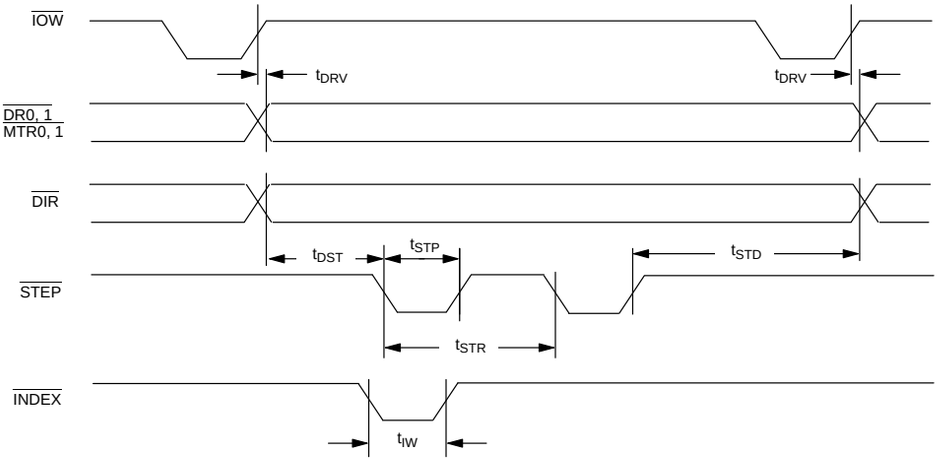
FDC WRITE CYCLE INTERRUPT TIMING Figure 11–7



11.5.4 FDC Drive Control Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{\text{DR0–1}}$, $\overline{\text{MTR0–1}}$ From End of $\overline{\text{WR}}$	t_{DRV}			100	ns	
$\overline{\text{DIR}}$ Setup to $\overline{\text{STEP}}$ Active	t_{DST}	6			µs	
Index Pulse Width	t_{IW}	100			ns	
$\overline{\text{DIR}}$ Hold from $\overline{\text{STEP}}$ Inactive	t_{STD}	t_{STR}			ms	
$\overline{\text{STEP}}$ Active High Pulse Width	t_{STP}	8			µs	
$\overline{\text{STEP}}$ Rate Time (see Table 4–15)	t_{STR}	0.5			ms	

DRIVE CONTROL TIMING Figure 11–8



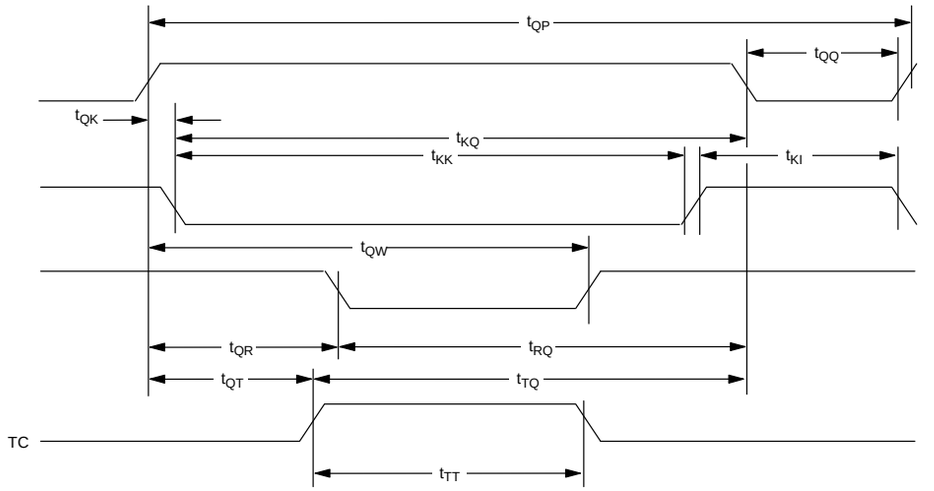
11.5.5 FDC DMA Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{\text{DACK}}$n Inactive Pulse Width	t_{KI}	25			ns	
$\overline{\text{DACK}}$n Active Pulse Width	t_{KK}	65			ns	
$\overline{\text{DACK}}$n Active Edge to FDRQ Inactive	t_{KQ}			65	ns	
DRQn to $\overline{\text{DACK}}$n Active Edge	t_{QK}	10			ns	
DRQn Period (except Non–Burst DMA) (Note 3)	t_{QP}	8 x t_{DRP}			µs	
DRQn Inactive Non–Burst Pulse Width	t_{QQ}	300		400	ns	
DRQn to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Active	t_{QR}	15			ns	
DRQn to End of $\overline{\text{RD}}$, $\overline{\text{WR}}$ (Notes 2, 3) (DRQn Service Time)	t_{QW}			(8 x t_{DRP}) – (16 x t_{ICP})	µs	
DRQn to TC Active (Notes 2, 3) (DRQn Service Time)	t_{QT}			(8 x t_{DRP}) – (16 x t_{ICP})	µs	
$\overline{\text{RD}}$, $\overline{\text{WR}}$ Active Edge to DRQn Inactive (Note 1)	t_{RQ}			65	ns	
TC Active Edge to DRQn Inactive	t_{TO}			75	ns	
TC Active Pulse Width	t_{TT}	50			ns	

NOTES:

1. The active edge of $\overline{RD}$ or $\overline{WR}$ and TC is recognized only when $\overline{DACKn}$ is active.
2. Values shown are with the FIFO disabled, or with FIFO enabled and THRESH = 0. For nonzero values of THRESH, add (THRESH x 8 x t_{DRP}) to the values shown.
3. t_{DRP} and t_{ICP} are defined in Table.

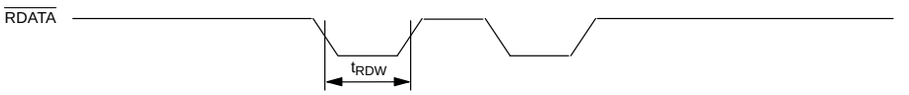
FDC DMA TIMING Figure 11–9



11.5.6 FDC Read Data Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Data Pulse Width	t_{RDW}	50			ns	

READ DATA TIMING Figure 11–10

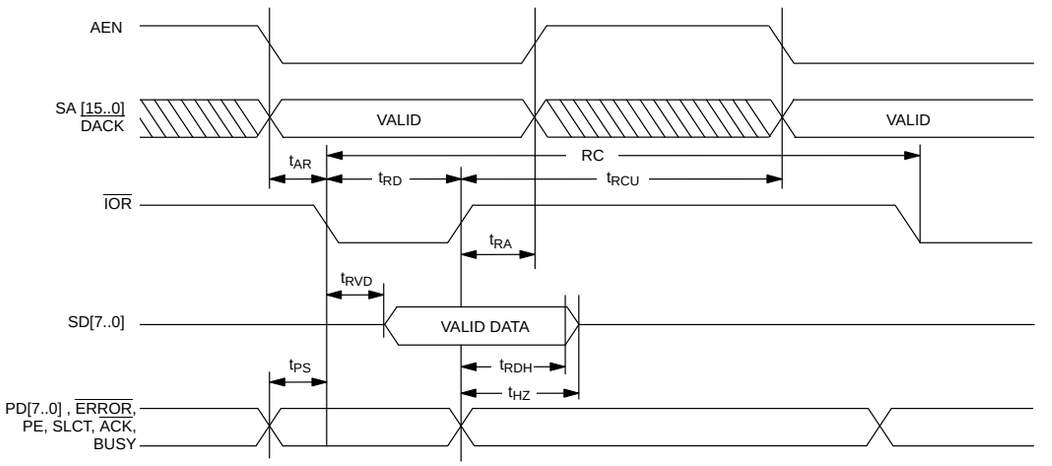


11.6 PARALLEL PORT TIMING

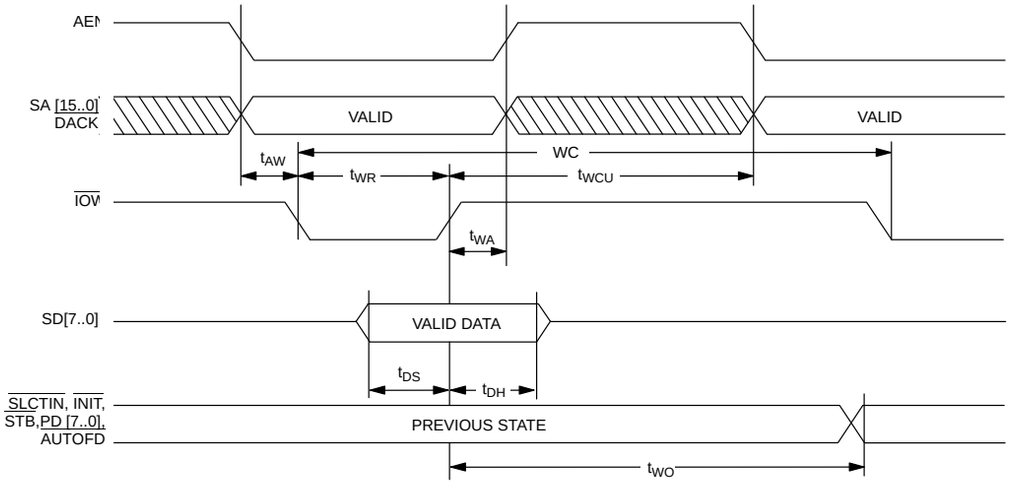
11.6.1 Microprocessor Interface to Parallel Port Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Valid Address to Read Active	t_{AR}	18			ns	
Valid Address to Write Active	t_{AW}	18			ns	
Data Hold	t_{DH}	0			ns	
Data Setup	t_{DS}	18			ns	
Read to Floating Data Bus	t_{HZ}	13		25	ns	
Port Setup	t_{PS}	10			ns	
Address Hold from Inactive Read	t_{RA}	0			ns	
Read Cycle Update	t_{RCU}	45			ns	
Read Strobe Width	t_{RD}	60			ns	
Read Data Hold	t_{RDH}	10			ns	
Active Read to Valid Data	t_{RVD}			55	ns	
Address Hold from Inactive Write	t_{WA}	0			ns	
Write Cycle Update	t_{WCU}	45			ns	
Write Data to Port Update	t_{WO}			60	ns	
Write Strobe Width	t_{WR}	60			ns	
Read Cycle = $t_{AR} + t_{RD} + t_{RCU}$	RC	123			ns	
Write Cycle = $t_{AW} = t_{WR} + t_{WCU}$	WC	123			ns	
$\overline{RD}$ Low after $\overline{WR}$ High	t_{WRR}	80			ns	

MICROPROCESSOR READ FROM PARALLEL PORT TIMING Figure 11–11



MICROPROCESSOR WRITE TO PARALLEL PORT TIMING Figure 11–12

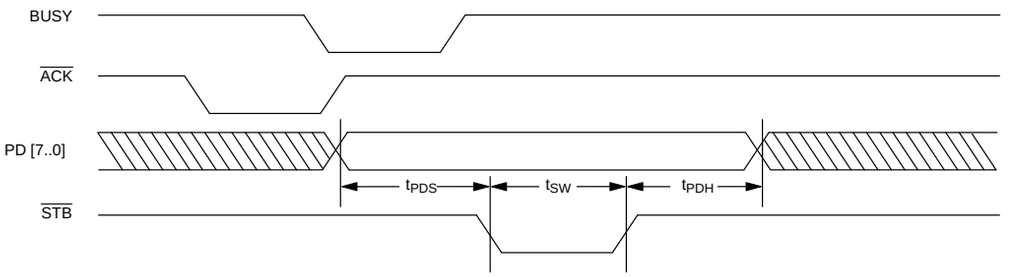


11.6.2 ISA–Compatible and PS/2 Compatible Parallel Port Timing

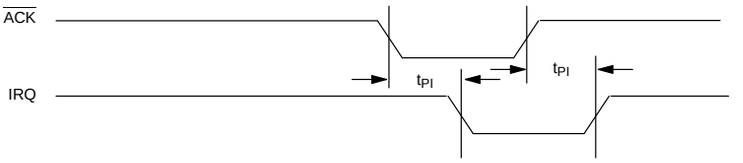
PARAMETER	SYMBOL	MIN	TYPE	MAX	UNITS	NOTES
Port Data Hold	t_{PDH}		500		ns	1
Port Data Setup	t_{PDS}		500		ns	1
Port Interrupt	t_{PI}			33	ns	
Strobe Width	t_{SW}		500		ns	1

NOTE:
These times are system dependent and are therefore not tested.

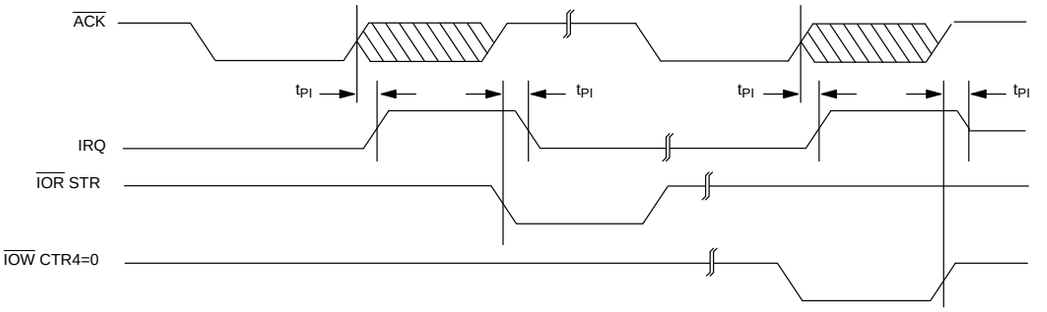
ISA–COMPATIBLE PARALLEL PORT DATA EXCHANGE Figure 11–13



ISA–COMPATIBLE MODE PARALLEL PORT INTERRUPT TIMING Figure 11–14



PS/2 COMPATIBLE MODE PARALLEL PORT INTERRUPT TIMING Figure 11–15



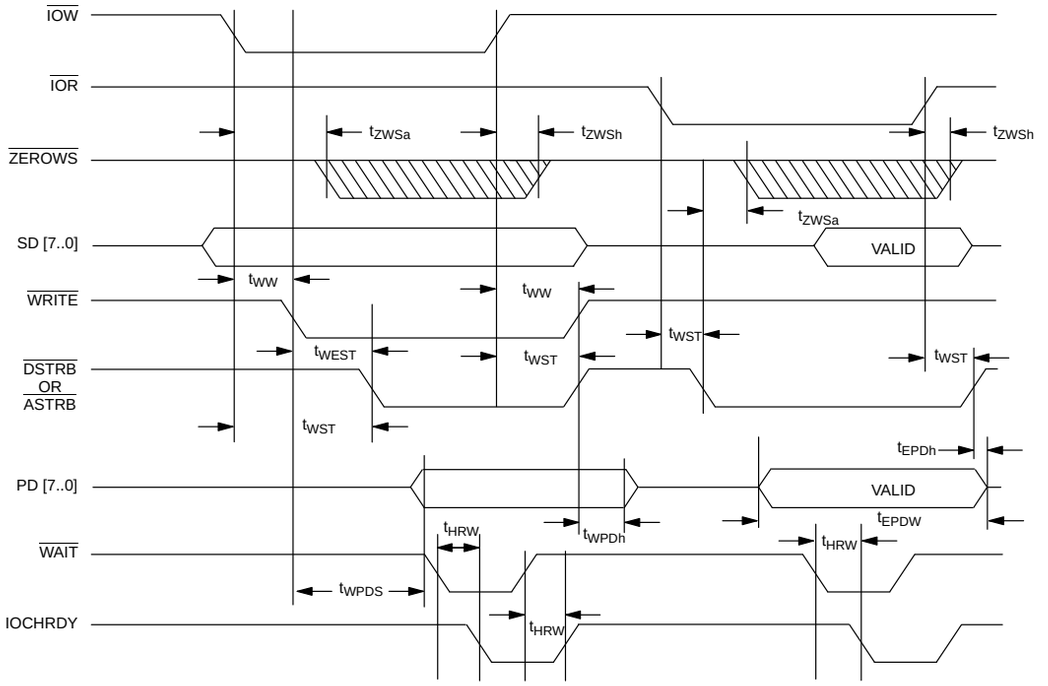
11.6.3 Enhanced Parallel Port (EPP) Timing

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
$\overline{\text{WRITE}}$ Active from $\overline{\text{IOW}}$ Active	t_{WW}			45	ns	1
$\overline{\text{DSTRB}}$ or $\overline{\text{ASTRB}}$ Active from $\overline{\text{IOW}}$ Active	t_{WST}	EPP 1.7 EPP 1.9		45 65	ns ns	1, 2 1, 2
$\overline{\text{DSTRB}}$ or $\overline{\text{ASTRB}}$ Active after $\overline{\text{WRITE}}$ Active	t_{WEST}	EPP 1.7 EPP 1.9	0 10		ns ns	
PD0–PD7 Hold after $\overline{\text{DSTRB}}$ or $\overline{\text{ASTRB}}$I inactive	t_{WPDh}		50		ns	
IOCHRDY Active after $\overline{\text{WAIT}}$ Active	t_{HRW}	EPP 1.7		40	ns	3
PD0–PD7 Valid after $\overline{\text{WRITE}}$ Active	t_{WPDS}	DO–7 is stable 15 ns before $\overline{\text{IOW}}$ Active		15	ns	
EPP Data Width	t_{EPDW}		80		ns	
EPP Data Width Hold after STRB inactive	t_{EPDh}		0		ns	
$\overline{\text{ZEROWS}}$ Valid after $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Active	t_{ZWSa}			45	ns	
$\overline{\text{ZEROWS}}$ Hold after $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Inactive	t_{ZWSh}		0		ns	

NOTES:

1. t_{WST} and t_{WW} are valid in EPP 1.9 only if $\overline{\text{WAIT}}$ is low when $\overline{\text{IOW}}$ becomes active, else t_{WST} and t_{WW} are measured from $\overline{\text{WAIT}}$.
2. The DS83CH20 design guarantees that $\overline{\text{WRITE}}$ will not change from low to high before $\overline{\text{DSTRB}}$ or $\overline{\text{ASTRB}}$ goes from low to high.
3. In EPP 1.9, IOCHRDY inactive is measured from $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$.

ENHANCED PARALLEL PORT (EPP) TIMING Figure 11–16

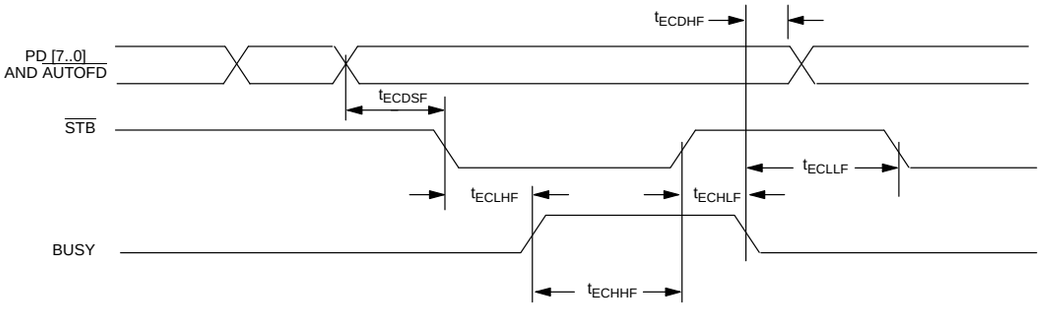


11.6.4 Extended Capabilities Port Timing

11.6.4.1Forward

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Setup before $\overline{STB}$ Active	t_{ECDSF}	0			ns	
Data Hold after BUSY	t_{ECDHF}	0			ns	
BUSY Setup after $\overline{STB}$ Active	t_{ECLHF}	75			ns	
$\overline{STB}$ Active after BUSY	t_{ECHHF}	0		1	s	
BUSY Setup after $\overline{STB}$ Inactive	t_{ECHLF}	0		35	ms	
$\overline{STB}$ Active after BUSY	t_{ECLLF}	0			ns	

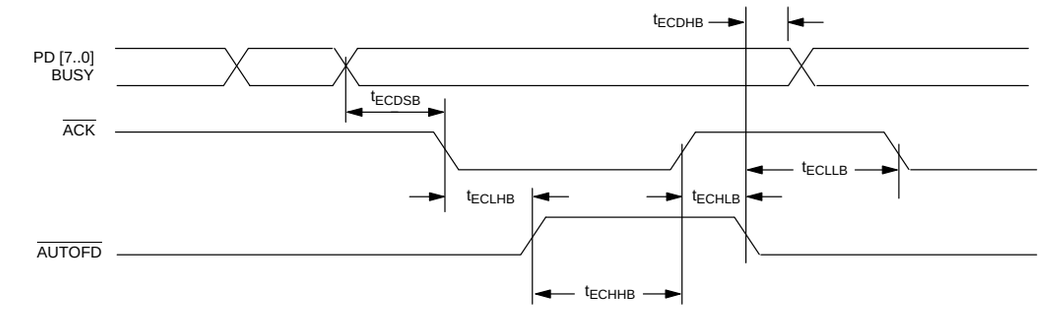
ECP PARALLEL PORT FORWARD TIMING DIAGRAM Figure 11–17



11.6.4.2 Backward

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Setup before $\overline{ACK}$ Active	t_{ECDSB}	0			ns	
Data Hold after $\overline{AUTOFD}$	t_{ECDHB}	0			ns	
$\overline{AUTOFD}$ Setup after $\overline{ACK}$ Active	t_{ECLHB}	75			ns	
$\overline{ACK}$ Active after $\overline{AUTOFD}$	t_{ECHHB}	0		1		
$\overline{AUTOFD}$ Setup after $\overline{ACK}$ Inactive	t_{ECHLB}	0		35	ms	
$\overline{ACK}$ Active after $\overline{AUTOFD}$	t_{ECLLB}	0			ns	

ECP PARALLEL PORT BACKWARD TIMING DIAGRAM Figure 11–18

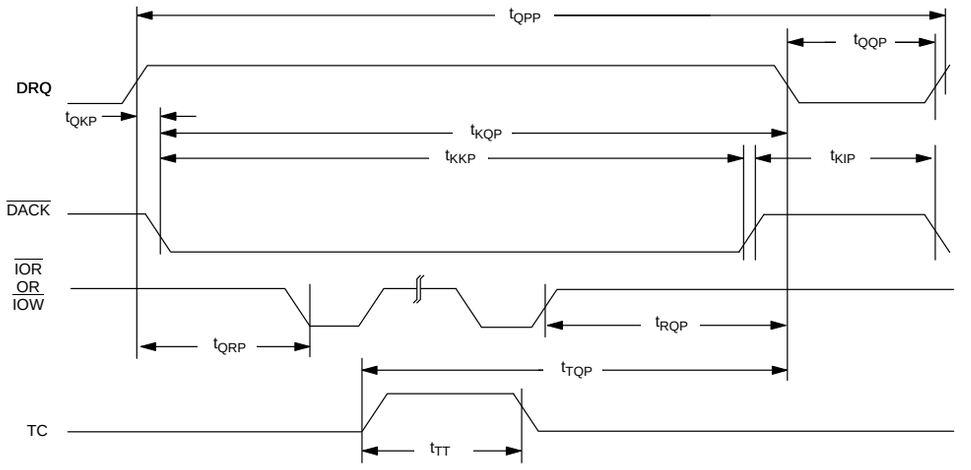


11.6.4.3ECP DMA Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{DACK}$ Inactive Pulse Width	t_{KIP}	25			ns	
$\overline{DACK}$ Active Pulse Width	t_{KKP}	65			ns	
$\overline{DACK}$ Active Edge to DRQ Inactive	t_{KQP}			65 + 32 DMA Cycle	ns	
DRQ to $\overline{DACK}$ Active Edge	t_{QKP}	0			ns	
DRQ Period	t_{QPP}	6.25			µs	
DRQ Inactive Non–Burst Pulse Width	t_{QQP}	100			ns	
DRQ to $\overline{IOR}$, $\overline{IOW}$ Active	t_{QRP}	0			ns	
$\overline{IOR}$ or $\overline{IOW}$ Active Edge to DRQ Inactive	t_{RQP}			65	ns	1
TC Active Edge to DRQ Inactive	t_{TQP}			75	ns	
TC Active Pulse Width	t_{TT}	50			ns	

NOTE:
The active edge of $\overline{IOR}$ or $\overline{IOW}$ and TC is recognized only when $\overline{DACK}$ is active.

ECP DMA TIMING Figure 11–19



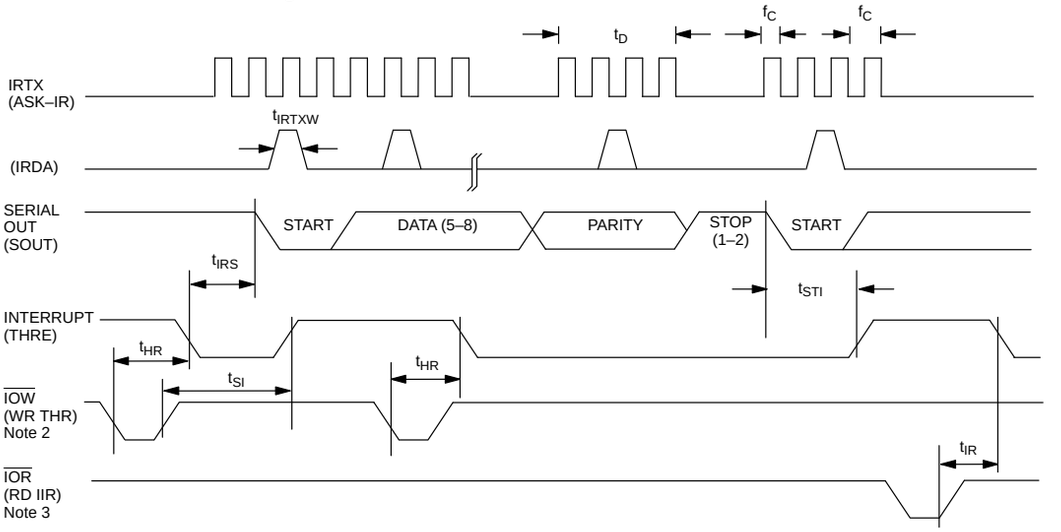
11.7 SERIAL PORTS TIMING

11.7.1 Transmitter Timing

TRANSMITTER TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
IRTX Pulse Width	t_{IRTXW}	1.6 µs		3/16	Baud Rate	
Delay from $\overline{IOW}$ (WR THR) to reset IRQ	t_{HR}			40	ns	
Delay from $\overline{IOR}$ (RD IIR) to reset IRQ (THRE)	t_{IR}			55	ns	
Delay from initial IRQ reset to Transmit Start	t_{IRS}	8		24	16x Clock Cycles	1
Delay from initial write to IRQ	t_{SI}	16		24	16x Clock Cycles	1
Delay from Start bit to IRQ (THRE)	t_{STI}			8	16x Clock Cycles	1
Carrier Frequency	f_C				KHz	
Wave Form Duration	t_D				s	

TRANSMITTER TIMING Figure 11–20



NOTES:

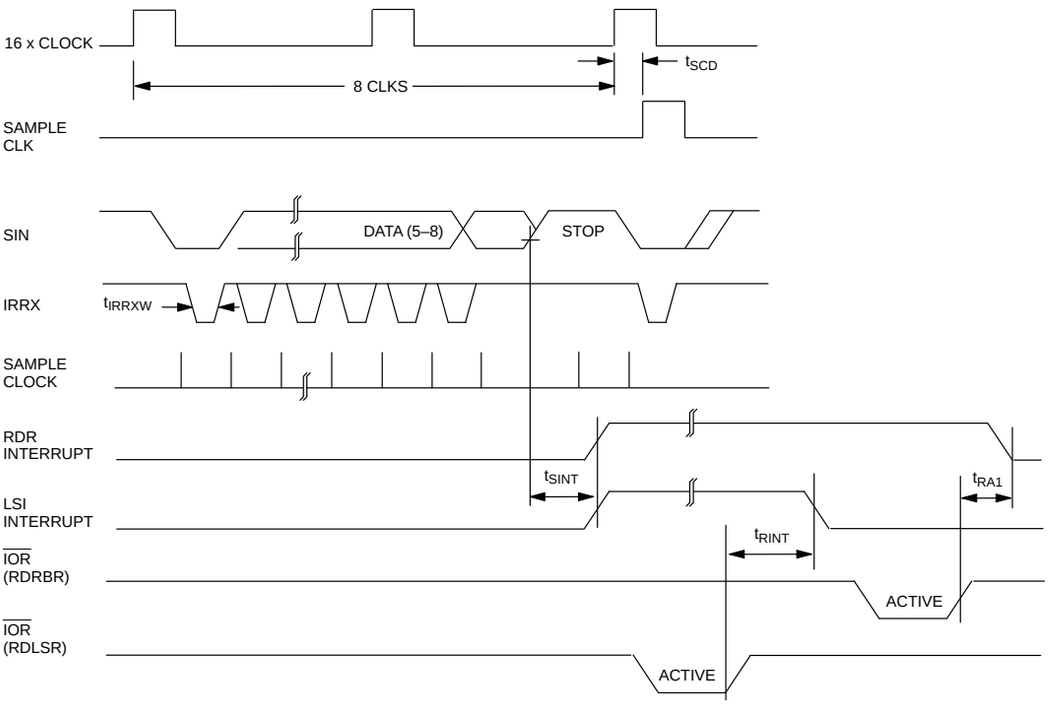
1. “16 x clock” is an internal reference clock that oscillates at 16x the Baud Rate.
2. See ISA Write cycle timing.
3. See ISA Read cycle timing.

11.7.2 Receiver Timing

RECEIVER TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
IRRX Pulse Width	t_{IRRXW}	1.6 µs		3/16	Baud Rate	
Delay from active edge of $\overline{IOR}$ to reset IRQ	t_{RAI}			78	ns	
Delay from inactive edge of $\overline{IOR}$ (RD LSR) to reset IRQ	t_{RINT}			55	ns	
Delay from RCLK to sample time	t_{SCD}			41	ns	1
Delay from Stop bit to Set Interrupt	t_{SINT}			1	16x Clock Cycles	2

RECEIVER TIMING FIGURE 11–21

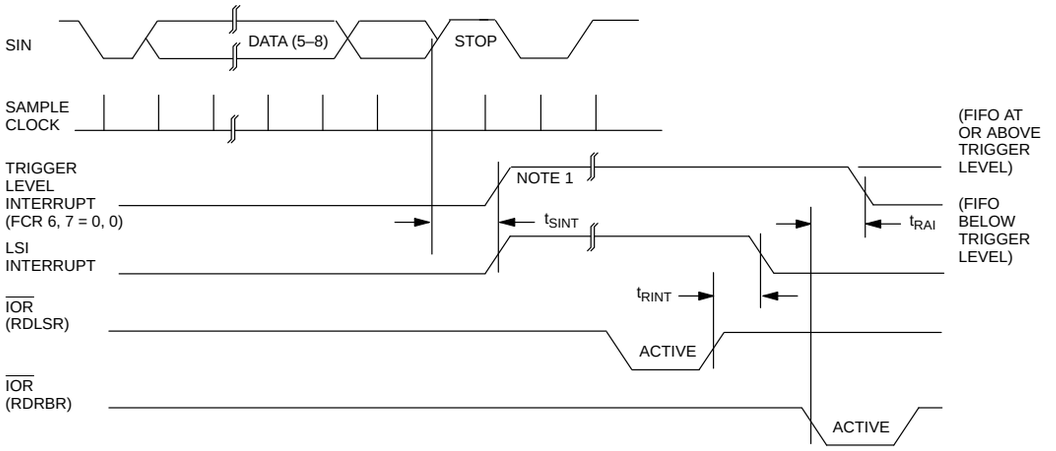


NOTES:

1. This is an internal timing and is therefore not tested.
2. In the FIFO mode (FCR0=1), the trigger level interrupts, the receiver data available indication, and the overrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RDRBR goes inactive. Timeout interrupt is delayed 8 RCLKs.

11.7.3 Receiver FIFO Timing

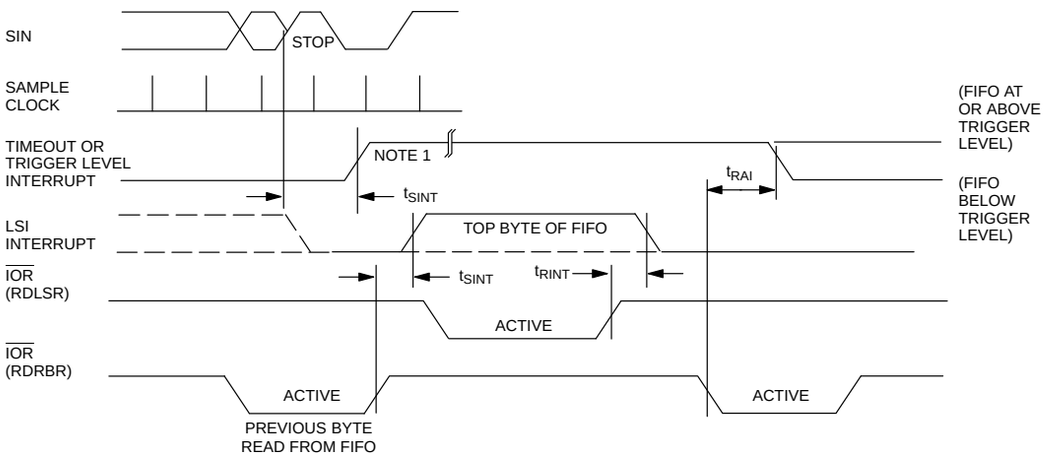
RECEIVER FIFO FIRST BYTE TIMING Figure11–22



NOTE:

1. If FCR0 = 1, then t_{SINT} = 3 RCLKs. For a BREAK interrupt, t_{SINT} = 8 RCLKs.

RECEIVER FIFO BYTES (OTHER THAN THE FIRST BYTE) Figure 11–23



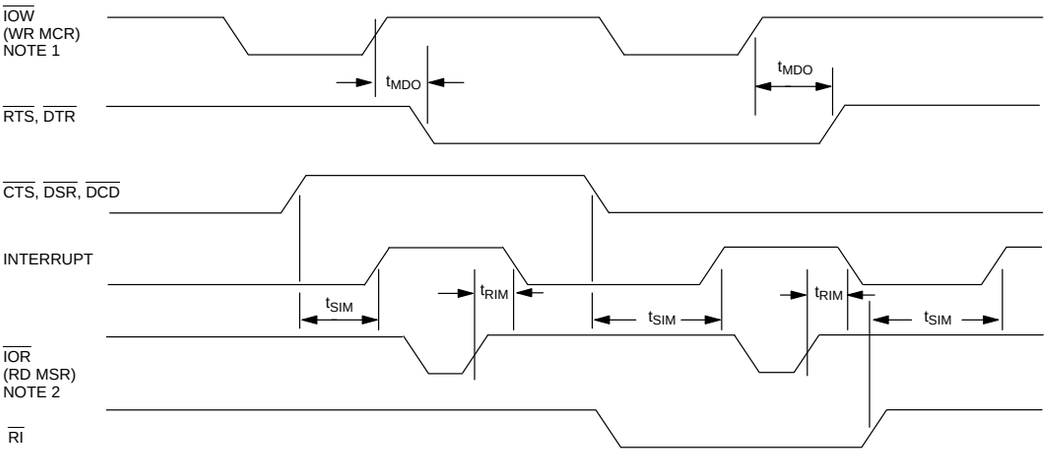
NOTE:

If FCR0 = 1, then t_{SINT} = 3 RCLKs. For a BREAK interrupt, t_{SINT} = 8 RCLKs.

RECEIVER TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Delay from $\overline{IOW}$ (WR MCR) to Output	t_{MDO}			40	ns	1
Delay to reset IRQ from $\overline{IOR}$ (RD MSR)	t_{RIM}			78	ns	2
Delay to set IRQ from MODEM Input	t_{SIM}			40	ns	

MODEM CONTROL TIMING Figure 11–24



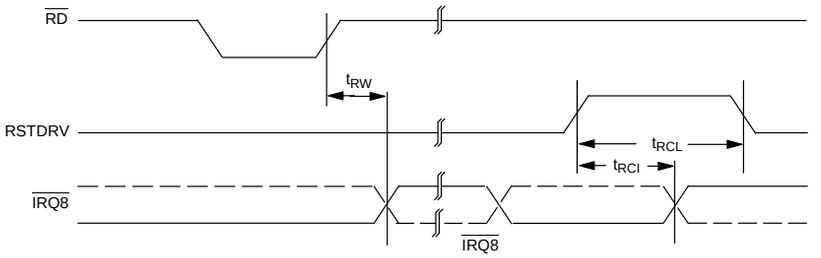
NOTES:

1. See Write cycle timing.
2. See Read cycle timing.

11.8 RTC TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{IOR}$ to $\overline{IRQ8}$ Inactive	t_{RW}			36	ns	
RSTDRV to $\overline{IRQ8}$ Inactive	t_{RCI}			25	ns	

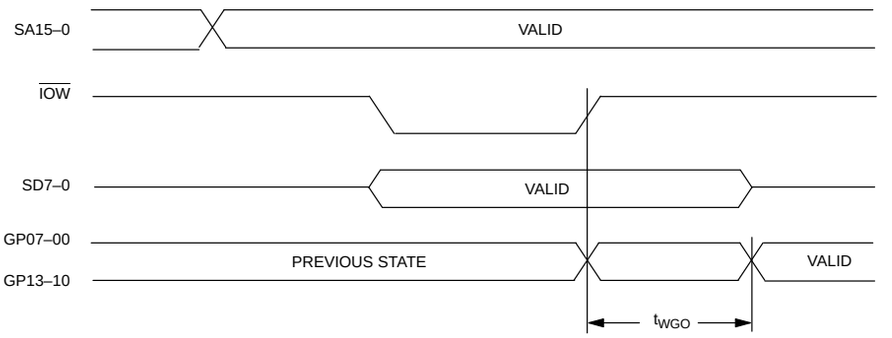
RTC IRQ TIMING Figure 11–25



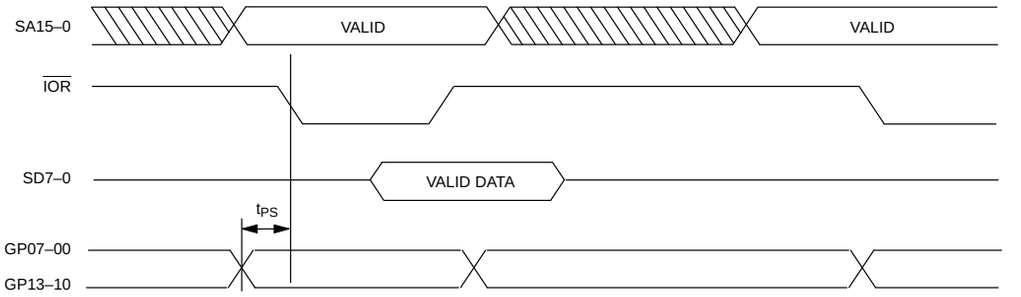
11.9 GPIO TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write data to GPIO update	t_{WGO}			300	ns	
GPIO read data setup	t_{GS}	10			ns	

GPIO WRITE TIMING Figure 11–26



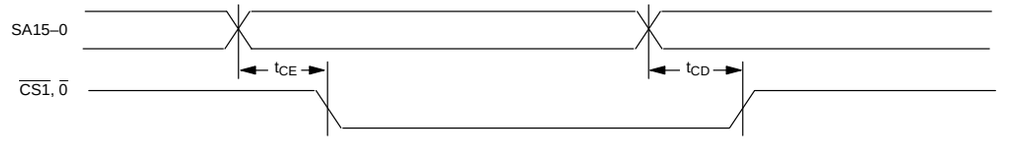
GPIO READ TIMING Figure 11–27



11.10 PROGRAMMABLE CHIP SELECT TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Delay from Command to Enable Chip Select	t_{CE}	0		25	ns	
Delay from Command to Disable Chip Select	t_{CD}	0		25	ns	

PROGRAMMABLE CHIP SELECT TIMING Figure 11–28

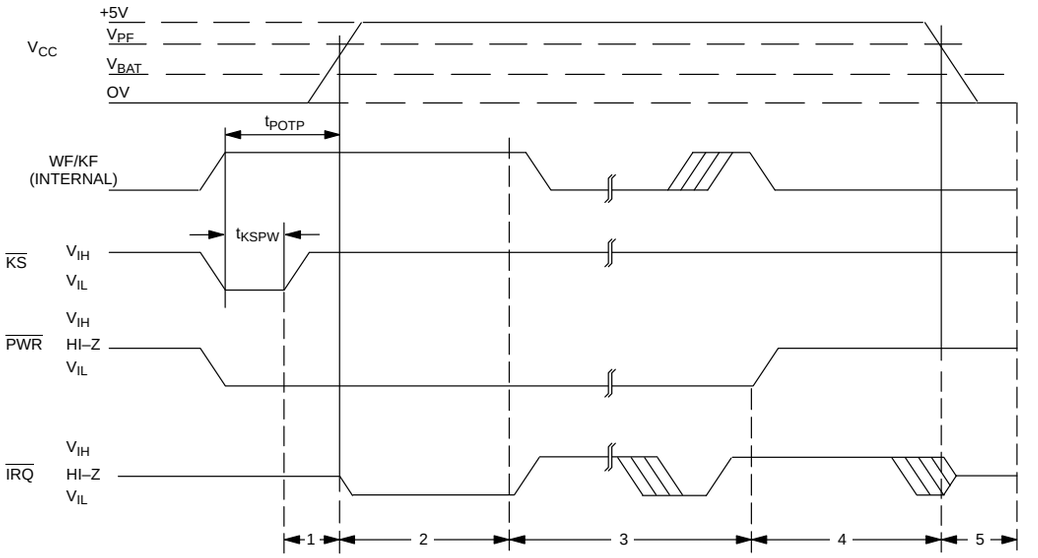


11.11 WAKE UP/KICKSTART TIMING

WAKE UP/KICKSTART TIMING (t_A = 25°)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart Input Pulse Width	t_{KSPW}	2			µs	
Wake up/Kickstart Power On Timeout	t_{POTO}	2			seconds	

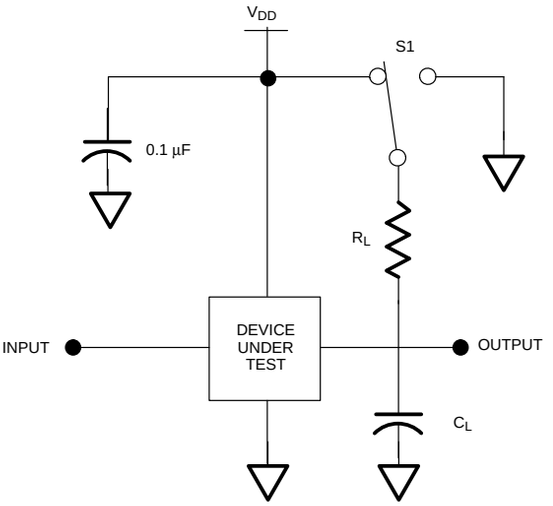
WAKE UP/KICKSTART TIMING Figure 11–29



NOTE:
Time intervals shown above are referenced in Wake up/Kickstart Timing Description section (10.6.3).

11.12 AC TEST CONDITION T_A = 0°C to 70°C; V_{DD} = 5.0V ± 10%

MODEM CONTROL TIMING Figure 11–30

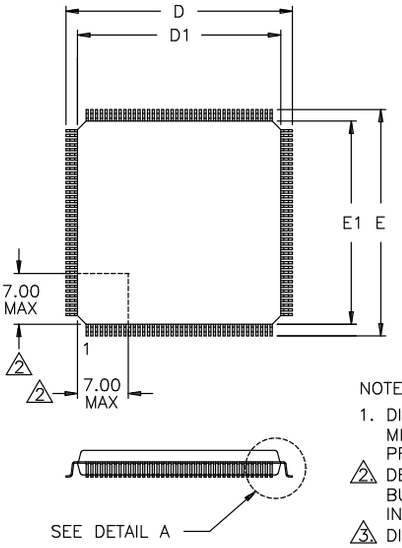


AC TESTING INPUT, OUTPUT WAVEFORM

NOTES:

1. C_L =100 pF, includes jig and scope capacitance.
2. S_1 = Open for push–pull outputs. S_1 = V_{DD} for high impedance to active low and active low to high impedance measurements. S_1 = GND for high impedance to active high and active high to high impedance measurements. R_L = 1.0KΩ for µP interface pins.
3. For the FDC Open Drive Interface Pins S_1 = V_{DD} and R_L = 150Ω..

DS83CH20 160–PIN QFP PACKAGE



NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.
4. ALL DIMENSIONS ARE IN MILLIMETERS.

DIM	MIN	MAX
A	–	4.07
A1	0.05	–
A2	3.17	3.67
b	0.20	0.40
c	0.13	0.23
D	30.35	31.45
D1	28.00 BSC	
E	30.35	31.45
E1	28.00 BSC	
e	0.65 BSC	
L	0.73	1.03