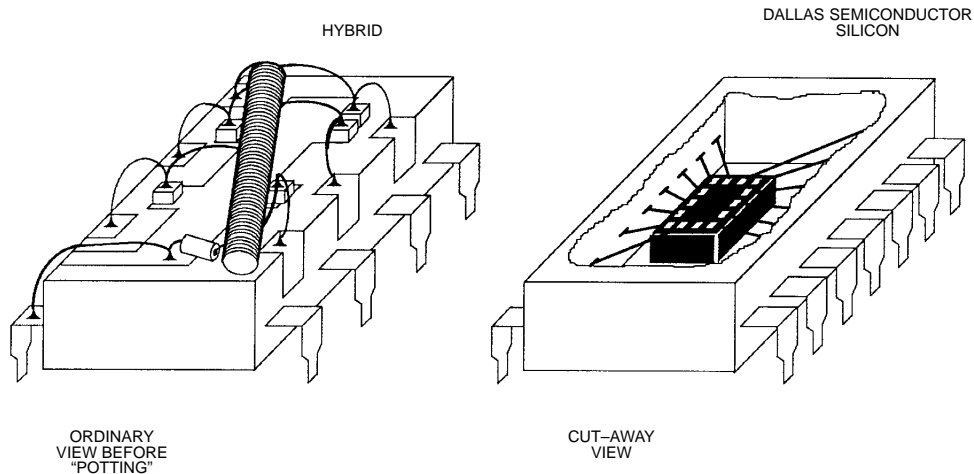


SILICON DELAY LINES VS. HYBRID L-C NETWORKS

Figure 1 shows internal views of a typical 5-tap hybrid delay line and its silicon counterpart. A hybrid is manufactured using a commercially available hex inverter DIP (e.g., 74LS04) with a small PC board placed on top to supply a ground plane. Next, several

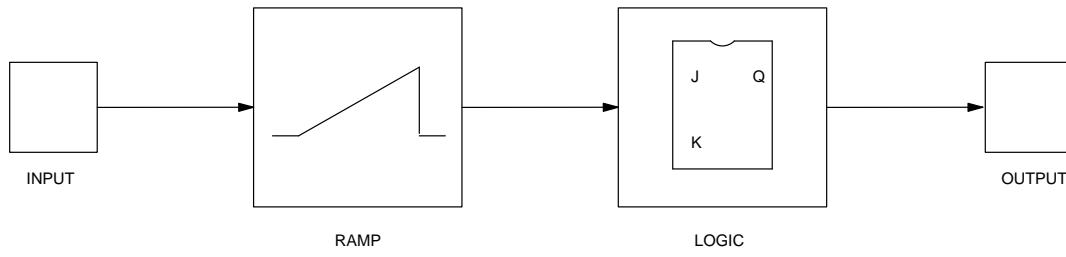
leads are bent up and over the top of the PC board. Five chip capacitors and a terminating resistor are soldered to the ground plane and a 5-tap ferrite inductor is positioned above. Note that nearly two dozen solder joints are required to electrically connect the various components. Finally, the entire assembly is placed into an oversized plastic tub and filled with a potting material.

INTERNAL VIEWS Figure 1


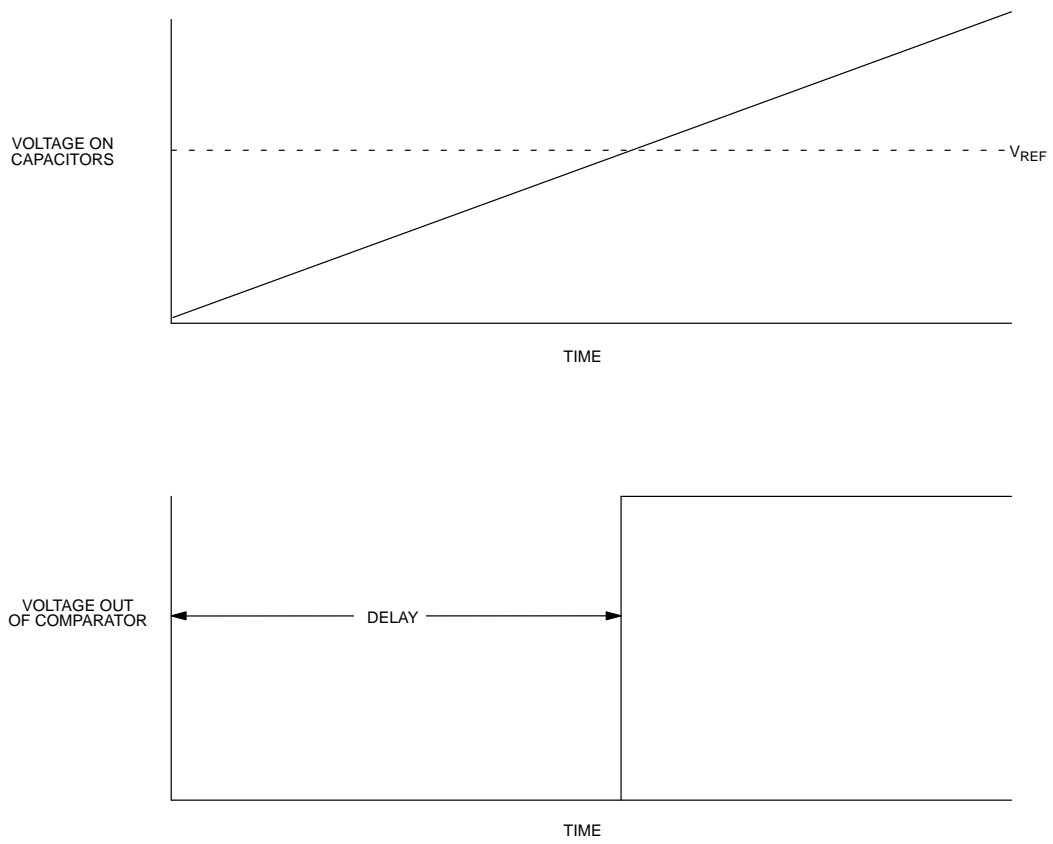
By comparison, the silicon delay line consists of a laser-optimized die bonded to a conventional lead frame molded into an auto-insertable industry standard DIP or surface mount SOIC package. The die is a low-power CMOS design fabricated on six-inch wafers by Dallas Semiconductor's Class 1 facility. Using lasers for late definition of finished wafers provides both economy and maximum flexibility; both rising and falling edges can be programmed to standard or custom delays over a wide range of values. A post-laser final passivation step protects against contamination by covering the laser fuse windows before packaging.

The basic building block of a silicon delay line consists of a ramp generator with associated logic (Figure 2). The input signal triggers a ramp generator that supplies a laser-adjusted voltage-to-time relationship (Figures 3 and 4). A comparator is used to detect the ramp reaching the reference voltage (V_{REF}); this sets or resets the output latch. The DS1013 family has three independent blocks in parallel while the DS1000, DS1005, and DS1010 families have the blocks connected in series with a single external input (Figure 5). All silicon delay lines, unlike most TTL-based hybrids, have true CMOS output levels.

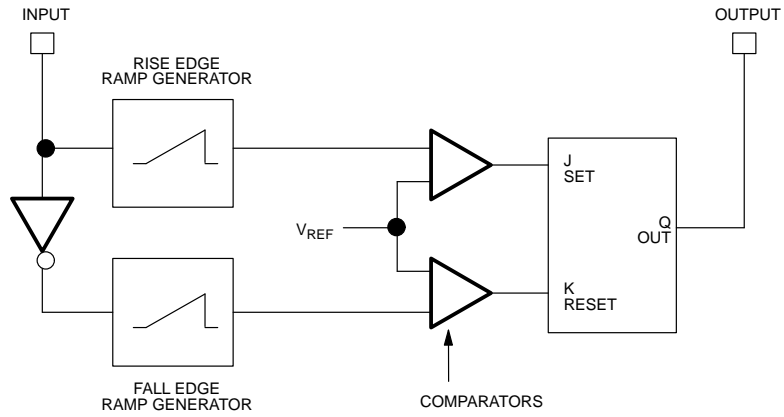
BASIC BUILDING BLOCK Figure 2



VOLTAGE TO TIME CONVERSION Figure 3

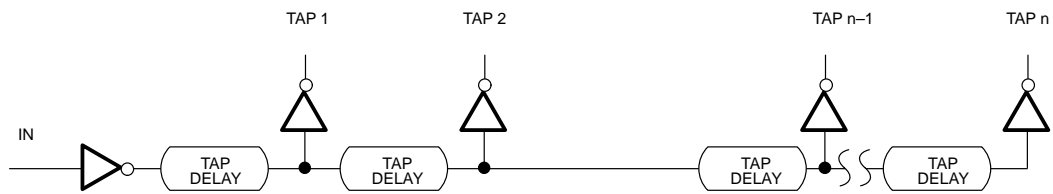


EXPANDED BASIC BLOCK Figure 4

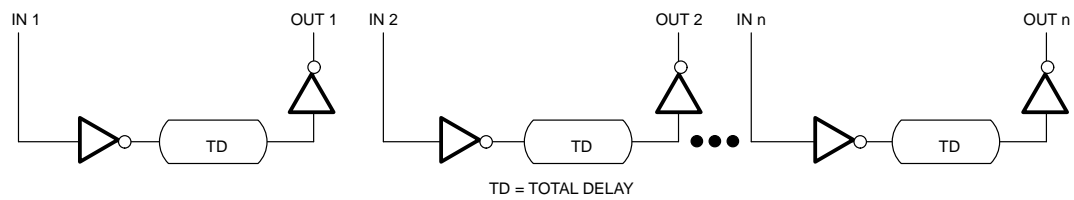


DELAY LINE FAMILIES Figure 5

Tapped Delays (e.g., DS1000 and DS1010)



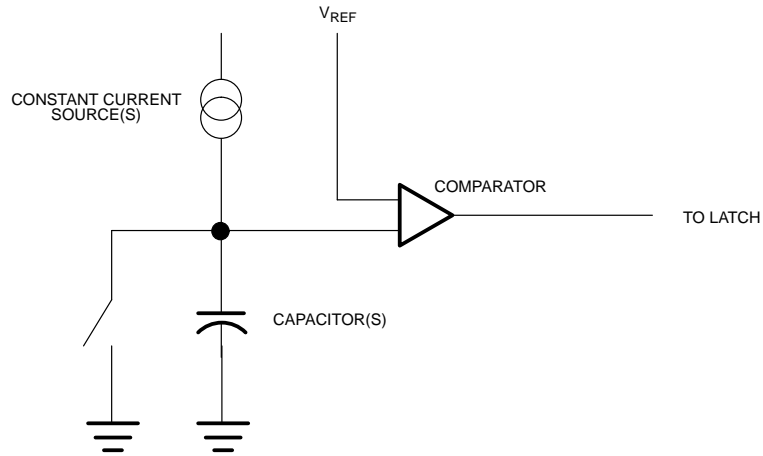
Multiple Independent Delays (e.g., DS1013, DS1007, and DS1044)



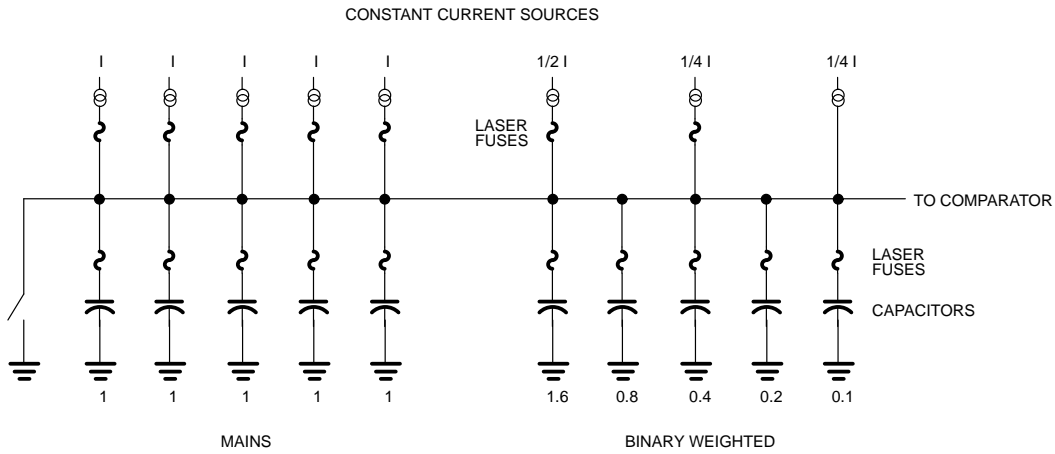
The linear ramp generator is implemented with constant current sources charging capacitors (Figure 6). By using a combination of several large current sources and capacitors and binary weighted smaller current sources and capacitors, maximum flexibility with subnanosecond adjustment is obtained on a single silicon die

(Figure 7). Under the direction of a computer-controlled tester with 20 picosecond resolution, the proper slope of the ramp (Figure 8) is obtained by directing a laser to remove the unnecessary current sources and capacitors. This is accomplished by opening polysilicon fuses

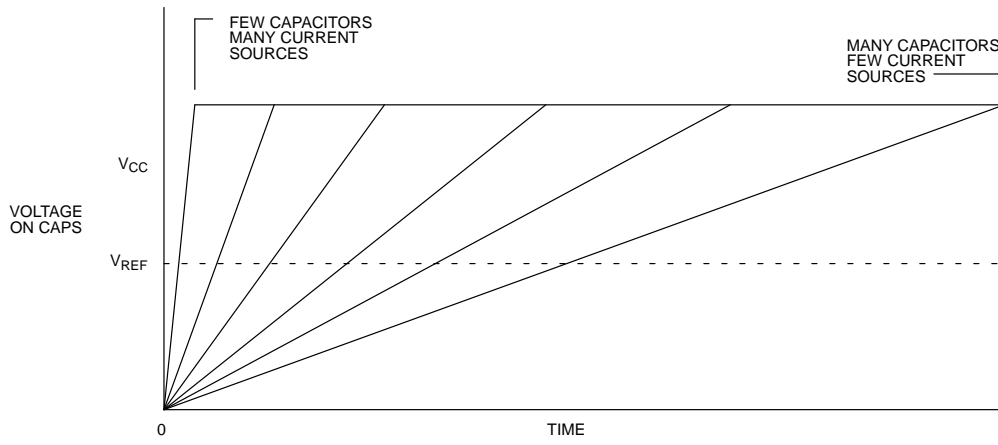
BASIC RAMP GENERATOR Figure 6



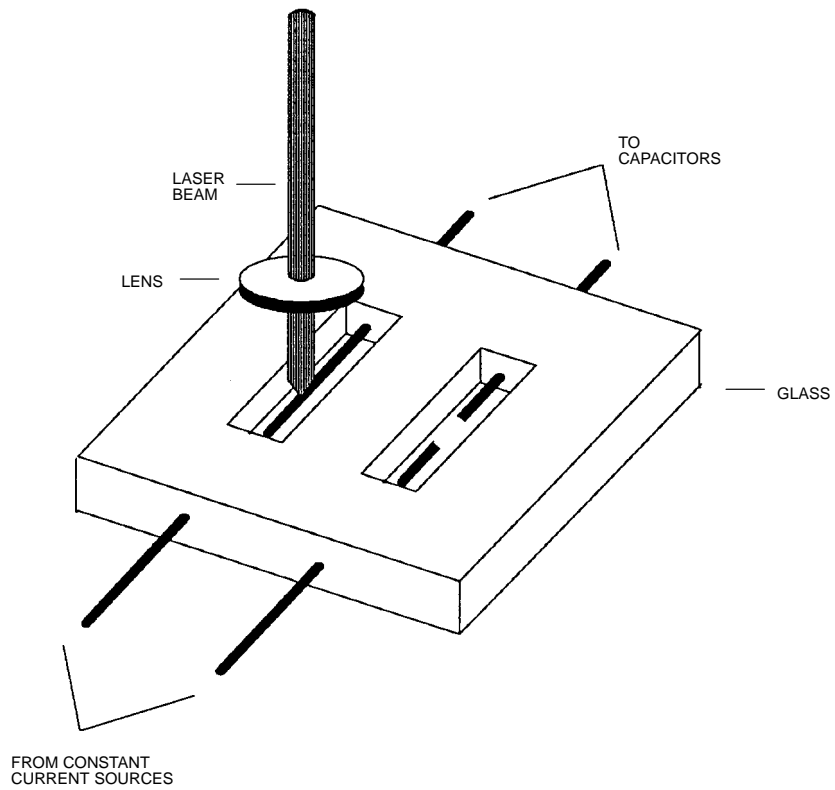
LASER PROGRAMMABLE ELEMENTS Figure 7



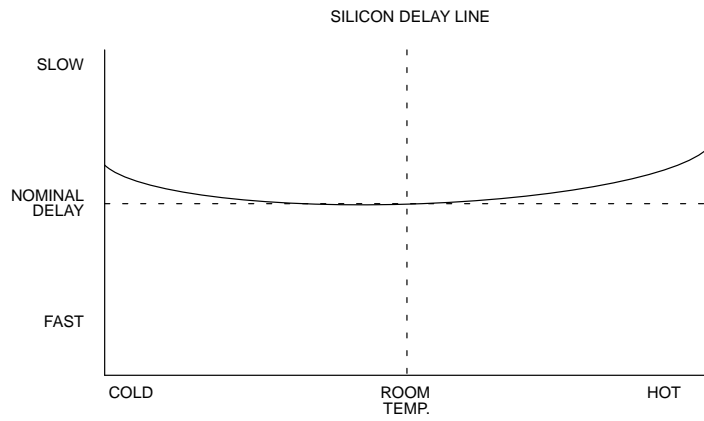
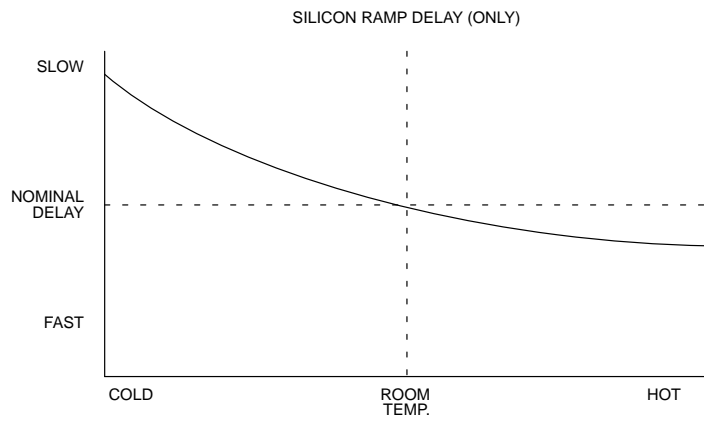
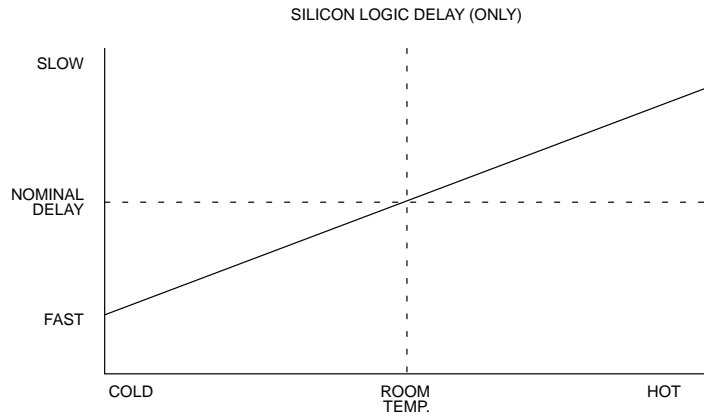
RANGE OF ADJUSTMENT Figure 8



LASER BLOWING POLYSILICON FUSE Figure 9



DELAY VS. TEMPERATURE Figure 10



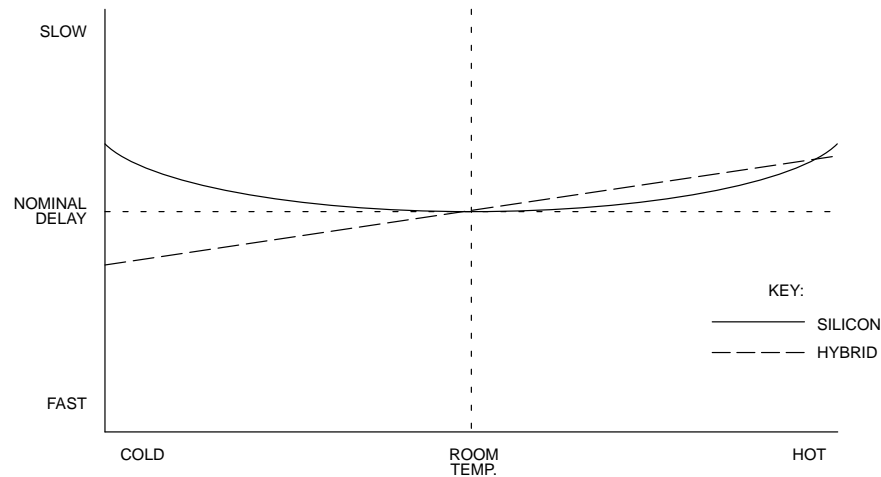
Timing on hybrid lines is determined by coil winding and/or capacitor selection or trimming. Achieving both rising and falling edge accuracy at the same time is difficult to achieve and comes at a premium price. Furthermore, timing is subject to the variations of the 74LS04 devices procured from other manufacturers.

On silicon delay lines, temperature compensation is implemented by balancing the positive temperature coefficient of the CMOS logic against the negative coefficient of the ramp generator. Figure 10 shows that the logic portion of the circuit, like hybrid delay lines in general, slows linearly with increasing temperature. Since the ramp speeds up non-linearly, the two effects tend to cancel, minimizing the effects of temperature. Because the net result resembles a parabolic shape, temperature

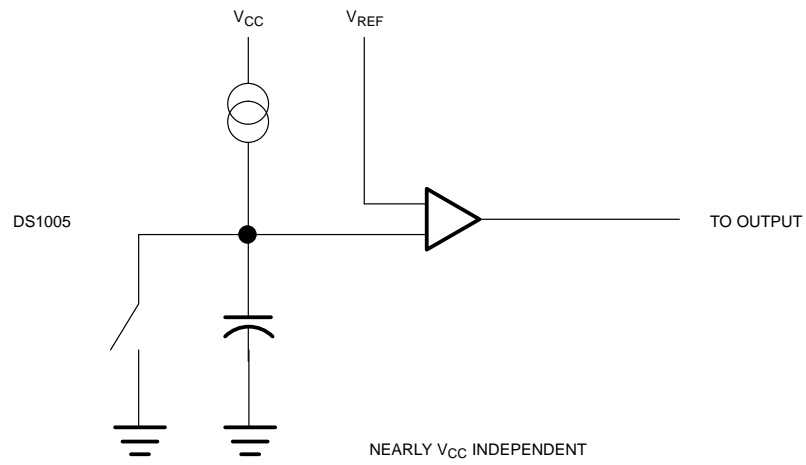
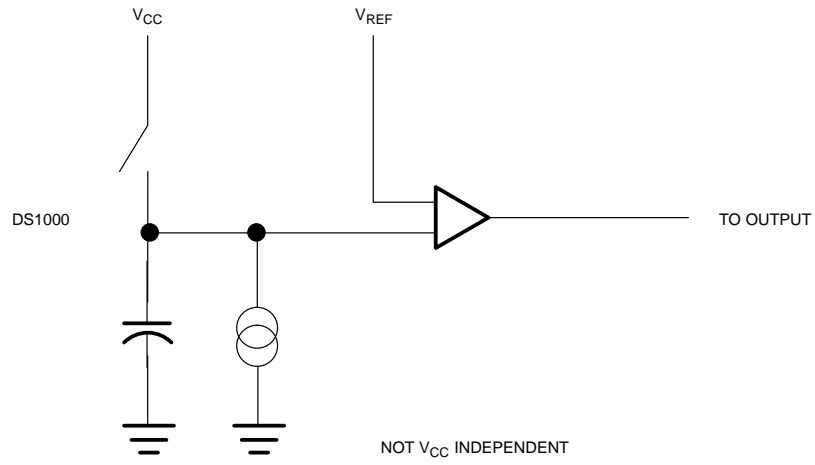
coefficients specified in parts per million (ppm) are inappropriate to describe the behavior of silicon delay lines. A more meaningful parameter is maximum shift from nominal, anywhere over the rated temperature range. Figure 11 compares the two technologies over temperature.

While some silicon delay line families (DS1000, DS1010) provide minimal voltage independence (4% delay change for 5% supply variation), the newer designs (DS1005 and DS1013) provide a higher degree of supply isolation ($\leq 1\%$ delay change for 5% supply variation). The newer designs achieve supply voltage independence by employing positive ramps referenced to ground rather than negative ramps referenced to V_{CC} (Figure 12).

HYBRID VS. SILICON OVER TEMPERATURE Figure 11



COMPARISON OF DELAY DESIGNS Figure 12



While hybrids offer little flexibility in packaging, silicon lines are available in a variety of industry standard DIP and SOIC packages (Figure 13). To maintain compatibility with existing designs based on hybrids having missing pins, a clipped lead version is offered. Finally, for surface mount applications, two solutions are available: 300 mil DIPs with the leads trimmed and “gull winged,” and industry standard SOIC packages.

Table 1 summarizes some of the disadvantages of the hybrid design and some of the advantages of the silicon solution.

TABLE 1

Disadvantages of Hybrids:	
•	Unreliable solder joints
•	Difficult to control falling edge accuracy
•	TTL output levels
•	Large, non-standard package dimensions
Advantages of Silicon	
•	Reliable all-silicon design
•	Accurate rise and fall edges
•	Easily customized
•	CMOS output levels
•	No inductors
•	Industry standard DIP and SOIC packaging
•	Standard IC handling including reflow soldering

PACKAGING OPTIONS Figure 13

DUAL-IN-LINE (DIP)

DIP packages are available in pin counts of 8, 14 and 16 pins. Three lead-forming options are available:

Straight lead. This is the conventional package and is used for through-hole mounting in PCBs.

Gullwing. The leads are formed to sit flat on the surface of a PCB for surface mount applications.

Sheared NC. All “no connect” (NC) leads are sheared off the package. This package is commonly used for hybrid replacement applications.

NOTE: The use of gullwing or sheared NC packages is not encouraged for new designs; however, these packages will continue to be made available for existing designs.

SMALL OUTLINE (SOIC)

Small outline surface mount packages are available in pin counts of 8, 14 and 16 pins. Two package widths are also available: 150 mil and 300 mil.

PACKAGE AVAILABILITY/LETTER DESIGNATIONS					
# PINS	DIP			SOIC	
	STD	GULLWING	SHEARED	150 mil	300 mil
8	M	H		Z	
14	none*	G	K	R	
16					S

* Default package, no letter designator required.

Tape and reel packaging is also available; contact the factory for more information

QUESTIONS AND ANSWERS**QUESTION: How do silicon timed delays differ from hybrid devices?**

ANSWER: A typical hybrid consists of a hex inverter DIP, a PC board acting as a ground plane plus chip capacitors, a terminating resistor and a multiple tap ferrite inductor. Timing is determined by coil winding and/or capacitor selection or trimming. The Dallas Semiconductor Silicon Timed Circuit (STC) design uses a laser-optimized die bonded to a conventional lead frame molded into an auto-insertable DIP or SOIC package.

QUESTION: What are the advantages of silicon timed circuits over hybrid devices?

ANSWER: STC (Silicon Timed Circuits) offer advantages in design, packaging and manufacture over hybrids. Specifically, STCs offer the increased reliability of silicon and greater accuracy on both rise and fall edges. Unlike TTL devices, STCs are CMOS devices and offer true output levels. Using standard DIP and SOIC packaging, STCs are well suited to standard IC handling including reflow soldering.

QUESTION: What's the basic operation of a silicon delay line device?

ANSWER: The basic building block of the silicon delay line is a ramp generator and associated logic. The input signal triggers a ramp generator that supplies a laser-adjusted voltage-to-time relationship.

QUESTION: Is there a way to correlate the performance of silicon time delays against hybrids?

ANSWER: Following this procedure will provide a correlation. At a fast (3 ns) rise/fall input pulses with 0/3 volt logic levels, low inductance decoupling techniques using 0.01 to 0.1 μF capacitors, low capacitance measurement probes placed as close as possible to the package, and relaxed timing

(500 ns pulse width, μs period) will aid in timing correlation when measured at 1.5 volt levels.

QUESTION: How does laser-adjustment time the delay?

ANSWER: Under the direction of a computer-controlled tester with 20 picosecond resolution, the proper slope of the ramp is obtained by directing a laser to open polysilicon fuses removing unnecessary current sources and capacitors.

QUESTION: Can I get any delay time I need?

ANSWER: Yes, silicon delay lines can be customized to meet your design timing requirements. We can even supply sample quantities in ceramic packages for evaluation.

QUESTION: Do STCs need to compensate for temperature like hybrids?

ANSWER: On silicon delay lines, temperature compensation is implemented by balancing the positive temperature coefficient of the CMOS logic against the negative coefficient of the ramp generator. The logic portion of the circuit speeds up linearly with increasing temperature while the ramp speeds up non-linearly. These two effects tend to cancel, minimizing the effects of temperature. Rather than measuring the coefficients in parts per million, silicon delay lines are meaningfully measured as the maximum shift from nominal anywhere along the rated temperature range.

QUESTION: Do silicon timed delays require decoupling?

ANSWER: STCs contain noise sensitive voltage detection circuits and fast rise time output circuits so decoupling is indicated. A 0.01 to 0.1 μF low inductance capacitor should be used in close proximity to the delay line to assure the highest performance.



QUESTION: Do silicon delay lines also function as glitch discriminators?

ANSWER: Yes, if a pulse or glitch is less than about 60% of the first stage delay of a 5- or 10-tap serial device (DS1000, DS1005 or DS 1010) or less than about 60% of any tap on a 3-in-1 parallel device (DS1013) there will be no output.

QUESTION: Can a silicon delay line be used to time-shift a square wave?

ANSWER: Yes, it s a good solution. Just be certain the period specification is met.

QUESTION: What temperature parameters do silicon timed delays meet?

ANSWER: STCs function over the full military (-55°C to $+125^{\circ}\text{C}$) temperature range, yet have been optimized for the commercial (0°C to $+70^{\circ}\text{C}$) range. One product family the DS1000-Ind is available in the industrial temperature range. Other parts may be specified for the industrial temperature range on a custom basis.

QUESTION: Can I add or daisy chain several devices to achieve a longer delay?

ANSWER: Daisy chaining silicon delay lines presents a problem that is increased with the number of packages in a chain. A voltage chopped stabilization circuit in the design causes a slight time jitter (well within specifications and almost transparent to the circuit) on the output. When packages are daisy chained, the time jitter is cumulative and degrades the accuracy of downline stages. If four to six packages are chained in a series, the results are generally unacceptable.

QUESTION: What about daisy chaining the stages of a parallel STC?

ANSWER: With the exception of the fast taps on the DS1007, some jitter will be added with each stage when added in a series. This will not be a problem in most cases. Users report that daisy chaining this way is a convenient method of implementing non standard series delays.