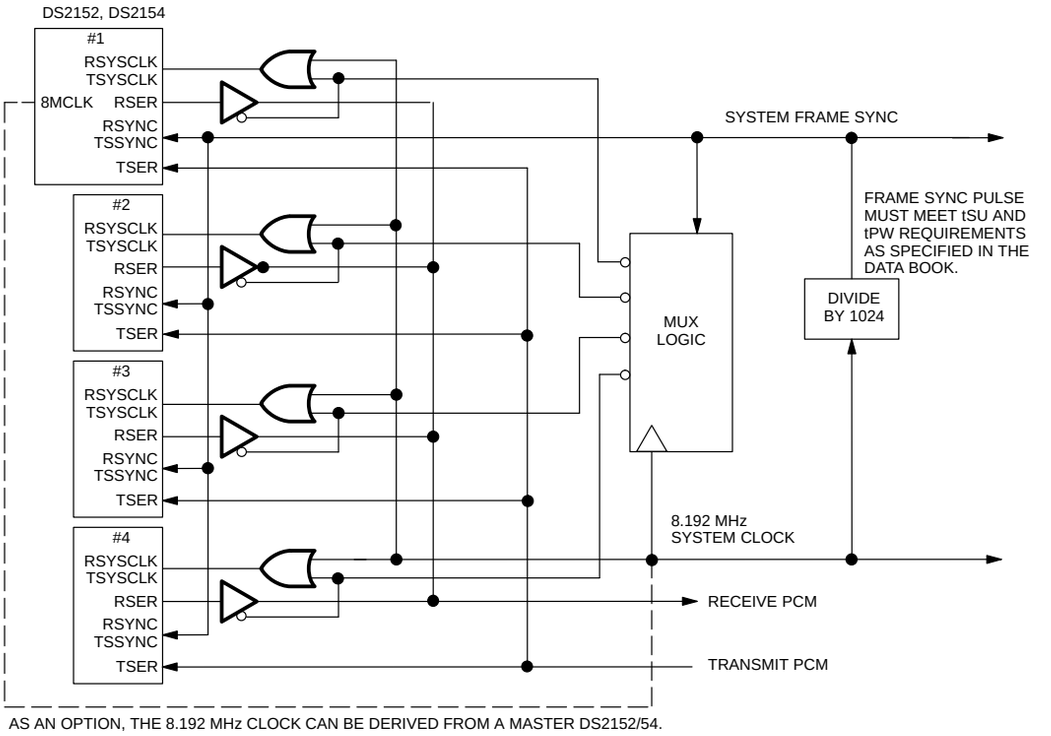
DALLAS SEMICONDUCTOR

Application Note 301
DS2152, DS2154 PCM Interface, 8 MHz System Clock Operation

The DS2152 and DS2154 PCM signals can interface to an 8 MHz system backplane. Typically this application is used to multiplex four 2.048 MHz PCM streams onto a single 8 MHz PCM stream. To accomplish this, the elastic stores are enabled and placed in the 2.048 MHz System Clock mode. Figure 1 describes a timing scheme in which a single RSYNC is generated for all four framers. Each framer in turn is driven with an 8.192 MHz clock burst of 8 cycles. Each clock burst causes the elastic store to output 1 DS0. This results in a "Byte Interleaved" 8.192 MHz PCM steam, Figure 2.

QUAD MULTIPLEXED FRAMERS Figure 1



MASTER CLOCK SOURCE

In Figure 1, the 8.192 MHz system clock may be derived from a T1 line as indicated by the dotted line. This line becomes the timing Master for the other three devices. In this example, device #1 is used as the master. The other three devices may experience frame slips since there is no guarantee that their inbound T1 rates are synchronous to device #1's inbound rate. The elastic stores will manage frame slip events in a logical manner by either repeating or deleting a full frame.

MASER CLOCK FAILURE

In the event that the master lines fails (goes in Carrier Loss) the following events will occur. RCLK will be replaced by MCLK. If the jitter attenuator is enabled and in the receive path this transition will be very smooth. Consequently, the 8.192 MHz clock output on the 8MCLK pin will make a slight and smooth transition to be phased locked to the clock at MCLK. The 8.192 MHz system timing will not experience any disturbance of the byte interleave structure. Device #1 will report an RCL (Receive Carrier Loss) event via the status registers. When the failure of the master line is detected by the host processor selection logic may be used to switch to another active line.

Figure 2