PRELIMINARY

DALLAS SEMICONDUCTOR

Application Note 302
DS2141, DS21Q41/DS21Q43 PCM Interface, 8 MHz System Clock Operation

The DS2141, DS21Q41, DS21Q43, DS2151and DS2153 PCM signals can interface to an 8 MHz system backplane. Typically this application is used to multiplex four 2.048 MHz PCM streams onto a single 8MHz PCM stream. To accomplish this the elastic stores are enabled and placed in the 2.048 MHz SYSCLK mode. Figure 1. describes a timing scheme in which a single RSYNC is generated for all four framers. Each framer in turn is driven with an 8.192 MHz clock burst of 8 cycles. Each clock burst causes the elastic store to output 1 DS0. This results in a Byte Interleaved 8.192 MHz PCM steam, Figure 2.

QUAD MULTIPLEXED FRAMES Figure 1

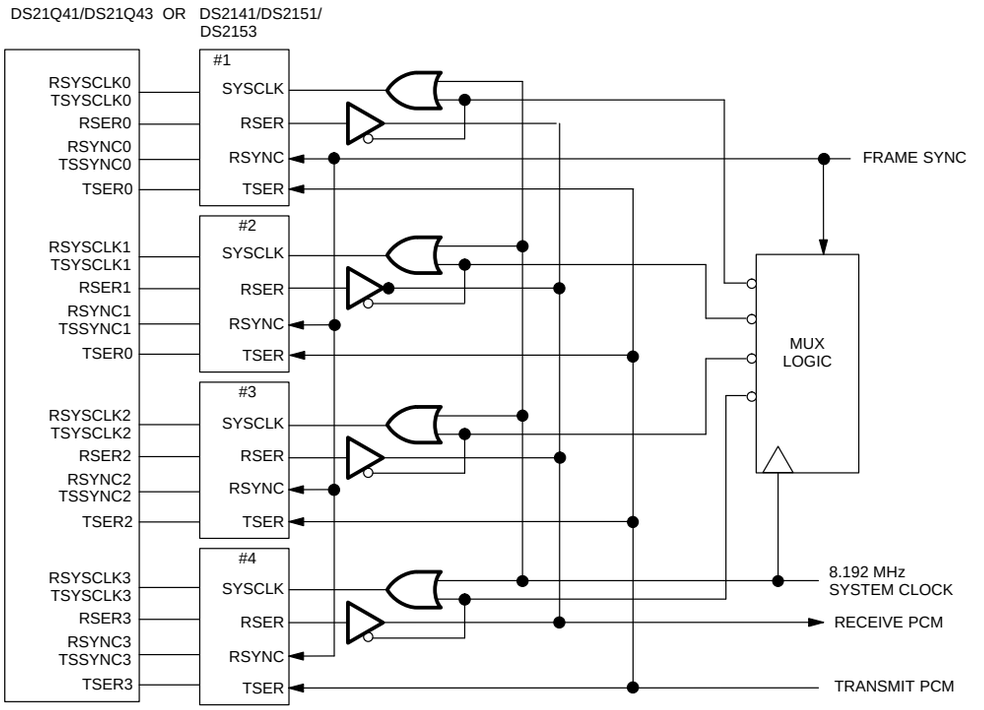
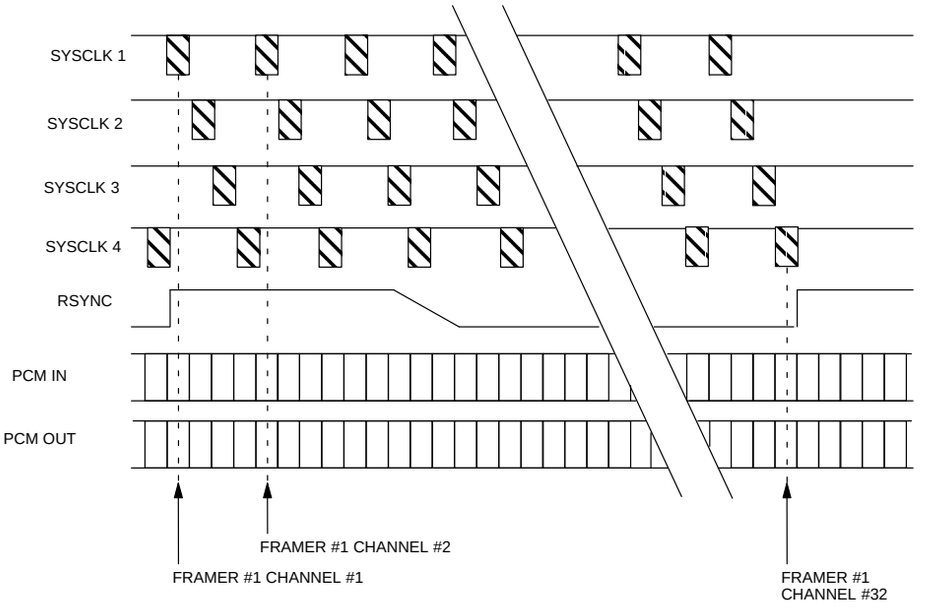
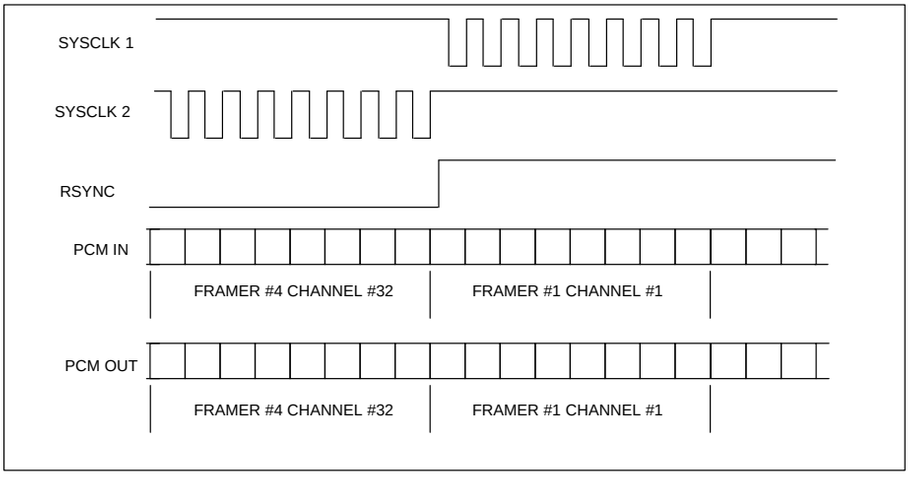


Figure 2


SYSCLK 1
SYSCLK 2
SYSCLK 3
SYSCLK 4
RSYNC
PCM IN
PCM OUT
FRAMER #1 CHANNEL #1
FRAMER #1 CHANNEL #2
FRAMER #1
CHANNEL #32


SYSCLK 1
SYSCLK 2
RSYNC
PCM IN
FRAMER #4 CHANNEL #32
FRAMER #1 CHANNEL #1
PCM OUT
FRAMER #4 CHANNEL #32
FRAMER #1 CHANNEL #1