NOTES:
1. Bt device is programmed for a “framed” input (i.e., Unframed Input control bit = 0).
2. RSYNC is programmed to output a frame sync; TSYNC is programmed to input a frame sync
3. Receive and transmit electric stores are disabled.
4. A “loop–timed” application is shown.
5. Timing is shown below:

RCLK/TCLK/RXCKI/TXCKI

RSYNC/TSYNC/RXSYI/TXSYI

T1 Case:
RSER/TSER/RXDATI/TXDATO

E1 Case:
RSER/TSER/RXDATI/TXDATO

LSB MSB F
Channel 24
LSB
Channel 1
MSB
Timeslot 31
Timeslot 0