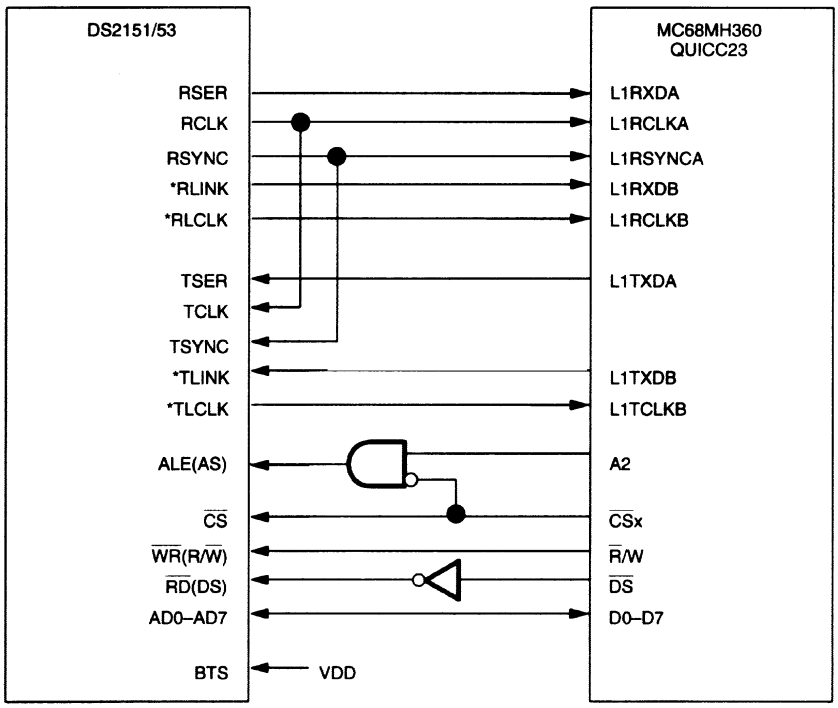
Application Note 318
DS2151, DS2153 PCM Interface, Interfacing to the MC68MH360 QUICC32

Interconnections between the DS2151 or DS2153 and the Motorola MC68MH360 (QUICC32) are shown in Figure 1. The MC68MH360 can be configured as an HDLC controller implementing protocols such as LAPD for both D channel and the FDL. In the configuration Shown, TDM channel A is used for timeslots 0–23 (T1) or 0–31 (E1) and TDM channel B is used for the FDL. For more information see the application note on Interfacing to a Non–multiplex Bus.



*HDLC on the FDL can be implemented either by the second serial input (TDM CHANNEL B) or via the port by the host processor (CPU32 internal to the QUICC32).

DS2151, DS2153 NOTES:

1. Other signals affecting operation of device are not shown.
2. Example circuit has RSYNC in output mode.

MC68360 NOTES:

1. Other signals affecting operation of device are not shown.

2. Use SI mode register to:
   A. Set up transmit and receive frame sync delays (0–3 clocks) to mask the F–Bit in T1 applications. RFSDA = 1 for DS2151, 0 for DS2153.
   B. Set clock edges for transmit on rising edge and receive on falling edge. CEA = CEB = 0.
   C. In the above example, TDM channel A has a common transmit/ receive clock and sync. CRTA = 1.
3. Use the TIMESLOT ASSIGNER to ignore Timeslot 0 for the DS2153.