

Application Note 330 DS2153 SPECIAL MODES

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Special Mode #1:3 State Outputs

When the SYSCLK pin is held high for 256 RCLK periods, all output pins, including the parallel port are 3-stated.

Special Mode #2: Allow Access Between Framer and LIU on Transmit Side

Writing 40hex to the TEST resister will invoke this mode. When enabled, the internal TLINK node is tied to the TSER pin. This access is useful in applications where it is desired to purposely corrupt the data stream before it is to be transmitted out onto the E1 line via TTIP and TRING pins. There is an exact delay from the TSER pin to the bipolar outputs of the formatter so the user has the ability to know when the needed bits appear at RCLK and RLINK pins. This delay is **5 TCLK** periods.

Special Mode #3: Tap the Transmit & Receive Bipolar Data Stream

Setting the 60hex in the TEST2 register will invoke this mode. When enabled, the internal TLINK node is tied to the TSER pin.

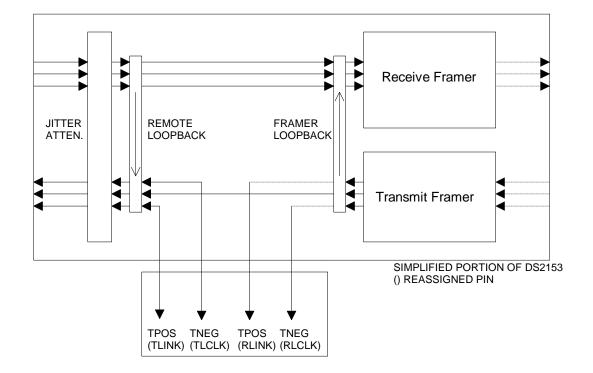
Special Mode #4: Allow Separate Transmit and Receive Backplane Clocks

Setting the CCR3.2-bit in the Common Control Register 3 will invoke this mode.

NOTE: When using Special Mode #4 and polling data on a multi-frame boundary, an external elastic store (DS2175) should be used instead of the transmit side elastic store of the DS2153. The internal elastic store built into the DS2153 can not release data on a multi-frame boundary. A DS2175 has the ability to sync on multi-frame pulses and therefore should be used instead.

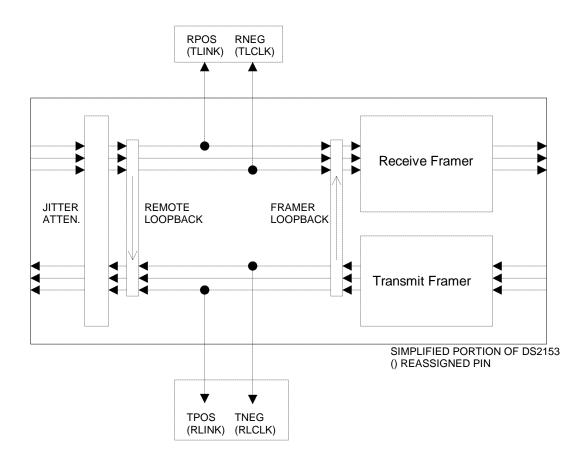
Special Mode #5: LIU Bypass

Setting the 20 hex bit in the TEST2 register will invoke this mode. When enabled, the internal TLINK node is tied to the TSER pin.

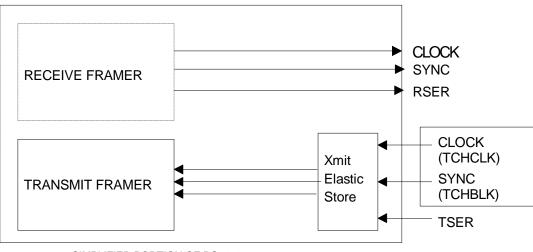


MODE 2: DS2153 Special Mode to Allow Access to Transmit Bipolar Data

MODE 3: DS2153 Special Mode to Tap the Transmit & Receive Bipolar Data



MODE 4: DS2151 SPECIAL MODE TO ALLOW ASYNCHRONOUS BACKPLANE CLOCKS



SIMPLIFIED PORTION OF DS2151 () REASSIGNED PIN

MODE 5: DS2151 Special Mode to Bypass the LIU

