Application Note 331
DS2172 Bit Error Rate Tester, V.54 Modem Test Patterns

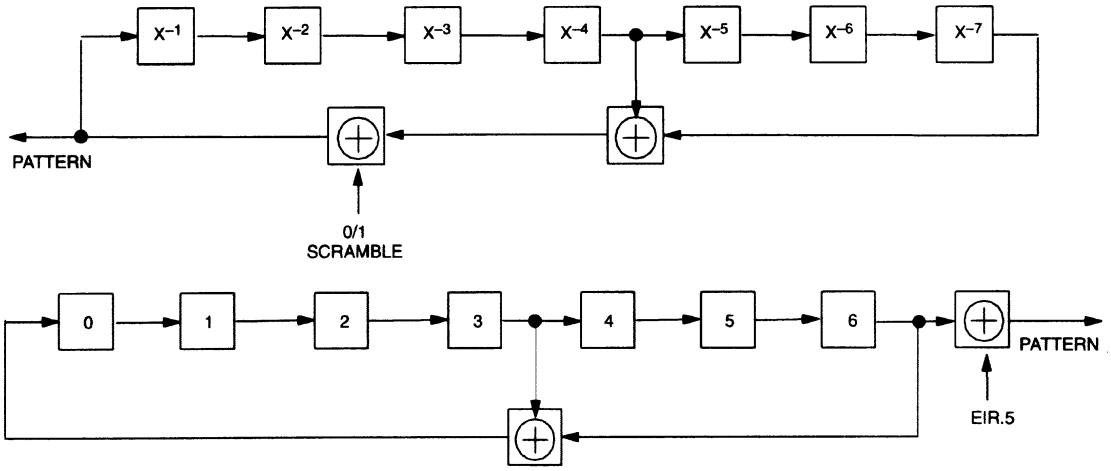
The DS2172 can be used to generate and detect the PREPARATORY, ACKNOWLEDGE, and TERMINATION patterns for V.54 modem testing. Figure 1 shows the pattern generator depicted in V.54. The pattern generator in the DS2172 is shown in Figure 2. With the SCRAMBLE input set to 1 in Figure 1 and the EIR.5 input in Figure 2 set to 1, the DS2172 will generate the same pattern if initialized to all ones, as the V.54 circuit initialized to all zeros. V.54 requires no specific initialization value.

V.54 specifies that each pattern must be N + 100 clocks. This must be handled external to the DS2172.

After the PREPARATORY phase, the initiating DTE must transmit an ADDRESS octet at least 16 times. The DS2172 can also transmit this pattern. The settings for transmitting this repetitive pattern are showing Table 1. The repetition count must be handled externally to the DS23172.

Refer to the initialization values in Table 1 for DS2172 programming.

V.54 CIRCUIT Figure 1



DS2172 INITIALIZATION VALUES Table 1

PATTERN	PLR	PTR	*PSR0	PCR.5	EIR.5	EIR.4	**CLOCK BURST
PREPARATORY	06H	03H	FFH	1	0	0	2055 ± 100
ACKNOWLEDGE	06H	03H	FFH	1	1	1	1955 ± 100
TERMINATE	06H	03H	FFH	1	1	1	8199 ± 100
ADDRESS	07H	00H	ADDRESS	0	0	0	128 MIN

* 7 CLOCKS ADDED TO V.54 SPEC TO ACCOUNT FOR DELAY THROUGH DS2172
** PSR1 = PSR2 = PSR3 = FF