# Application Note 334
## Bit Error Tester, Interfacing to the DS2141, DS2143, DS21Q41, DS21Q43, DS2151, DS2152, DS2153, DS2154

The Circuit in Figure 1 describes a method of interfacing the DS2172 BERT to the Dallas Semiconductor family of T1/E1 Framers and Single Chip Transceivers. The receive side of the DS2172 can be connected directly to the receive data stream of the Framer / SCT. RCHBLK is connected to the Receive Disable (RDIS) pin. RCHBLK and TCHBLK outputs from the Framer / SCT are used to determine the time slot or band in which the BERT is to transmit or receive data. On the transmit side, normal traffic is multiplexed with BERT data. Figure 1 shows the DS2151 or DS2153 with the elastic stores disabled. If elastic stores are enable then the signals RCLK and TCLK on the Framer / SCT will be replace by the appropriate system clock.

**FRAMER / SCT TO DS2172 INTERFACE** Figure 1