Application Note 344
DS21Q41, DS21Q43 Programming, Initialization

GENERAL INITIALIZATION FOR DS21Q41, DS21Q43

After power–up, when supplies and clocks have stabilized, internal registers must be initialized. It is a good idea to clear, set to 00H**, ALL** R/W registers. Certain registers have bits which control special test modes and features which can provide confusing indications. There are some registers containing functions that if not cleared, can cause unexpected conditions on device pins. These registers are;

DS21Q41: **TEST, TCR2**
DS21Q43: **TEST1, TEST2**

Depending on the interrupt structure implemented, it may be a good idea to clear **IMR1** and **IMR2** first. Prior to clearing these two registers however, without an external interrupt disable, there is no way to protect against spurious interrupt signals prior to initialization.

Once the registers have be initialized and set up with the framer's mode of operation, if the transmit or receive elastic store is enabled, the **ESR** bit in **CCR3** should be set then cleared.

SPECIAL INITIALIZATION FOR DS21Q43

TCLK (Transmit Clock) must be present for proper port operation. This clock can be sourced externally from the TCLK pin or internally from RCLK via the LOSS of TRANSMIT CLOCK mux. This mux is enabled by setting CCR2.2 = 1. The following sequence should be used to initialize the **DS21Q43** in which TCLK is not present or TCLK is derived from RCLK (a loop timed system).

- SET **LOTCMC** BIT IN **CCR2** REGISTER
- WAIT 10ms MINIMUM
- WRITE 00H TO ALL OTHER R/W REGISTERS
- WRITE DEVICE CONFIGURATION DATA
- WAIT FOR TSYSCLK AND/OR RSYSCLK TO STABILIZE (IF ELASTIC STORES ENABLED)
- SET **ESR** BIT IN **CCR3** REGISTER HIGH (IF ELASTIC STORES ENABLED)
- CLEAR **ESR** IN **CCR3** BIT.

NOTES:

1. In Loop Timed configurations or when TCLK is not guaranteed to always be present it is recommended that **LOTCMC** in **CCR2** be enabled (= 1).
2. If the RSYSCLK pin (DS21Q41, DS21Q43) is tied high, registers can be initialized (written to), but not read.