DALLAS SEMICONDUCTOR

Application Note 348
DS2154L vs. DS2153Q

1.0 INTRODUCTION

This application note highlights the differences between the DS2154L and the DS2153Q E1 Single Chip Transceivers. The DS2154L is a superset of the DS2153Q. All of the original features of the DS2153Q have been retained and software created for the DS2153Q is transferable to the DS2154L with minimal effort.

2.0 ADDITIONAL FUNCTIONALITY

New Features	Section
• Option for non–multiplexed bus operation	1 & 2
• Crystal–less jitter attenuation	12
• Additional hardware signaling capability – receive signaling reinsertion to a backplane multiframe sync – availability of signaling in a separate PCM data stream – signaling freezing – interrupt generated on change of signaling data	7.2 & 9
• Improved receive sensitivity: 0dB to –43dB	12
• Per–channel code insertion in both transmit and receive paths	8
• Expanded access to Sa and Si bits	11
• RCL, RLOS, RRA, and RAIS alarms now interrupt on change of state	4
• 8.192 MHz clock synthesizer	1
• Per–channel loopback capability	8
• Addition of hardware pins to indicate carrier loss and signaling freeze	1
• Line interface function can be completely decoupled from the framer/formatter to allow: – interface to optical, HDSL, and other NRZ interfaces – be able to tap the transmit and receive bipolar data streams for monitoring purposes – be able to corrupt data and insert framing errors, CRC errors, etc.	1
• Transmit and receive elastic stores now have independent backplane clocks	1
• Ability to monitor DS0 channel in both the transmit and receive paths	6
• Access to the data stream in between the framer/formatter and the elastic stores	1
• AIS generation in the line interface that is independent of loopbacks	1 & 3

- Transmit current limiter to meet the 50mA short circuit requirement 12
- Option to extend carrier loss criteria to a 1 ms period as per ETS 300 233 3
- Automatic RAI generation to ETS 300 011 specifications 3
- Device identification register 3

3.0 CHANGES IN REGISTER DEFINITIONS

When implementing the new features of the DS2154L, a priority was placed on preserving the DS2153Qs register map to facilitate code migration from existing DS2153Q designs. This section highlights register additions and differences found in the DS2154L.

3.1 New Feature Register Usage

Highlights specific registers containing bit locations related to new features. Each item can be found in the data sheet under the listed sections.

3.1.1 DS0 Monitoring (section 6.0)

Register	Description
CCR4	Common Control 4 (bits 4–0)
CCR5	Common Control 5 (bits 4 – 0)
TDS0M	Transmit DS0 Monitor
RDS0M	Receive DS0 Monitor

3.1.2 Hardware Based Signaling (section 7.2)

Register	Description
TS1–TS16	Transmit Signaling Registers 1 – 16
TCBR1–4	Transmit Channel Blocking Registers 1 – 4
TCR1	Transmit Control Register 1
CCR3	Common Control 3 (bits 3 and 2)

3.1.3 Signaling Freeze (section 3.0 and 7.2)

Register	Description
CCR2	Common Control 2 (bits 1 and 0)

3.1.4 Per Channel Loopback (section 8.1.1)

Register	Description
CCR3	Common Control 3 (bit 5)
TIR1 – TIR4	Transmit Idle Registers 1 – 4

3.1.5 Per Channel Code (Idle) Insertion (section 8.0)

Register	Description
TCC1 – TCC4	Transmit Channel Control 1 – 4
TC1 – TC32	Transmit Channels Registers 1 – 32
RCC1 – RCC4	Receive Channel Control 1 – 4
RC1 – RC32	Receive Channels Registers 1 – 32

3.1.6 Device Identification (section 3.0)

Register	Description
IDR	Device Identification

3.1.7 Interrupt on Change of State for RCL, RLOS, RRA, RAIS (section 4.0)

Register	Description
SR1	Status Register 1 (bits 7 and 5)
IMR1	Interrupt Mask Register 1 (bits 7 and 5)

3.1.8 Receive Carrier Loss Alternate Criteria (section 3.0)

Register	Description
CCR3	Common Control 3 (bit 0)

3.1.9 Expanded access to Sa and Si bits (section 11.0)

Register	Description
SR2	Status Register 2 (bit 1)
RSiAF	Receive Si bits in the align frame
RSiNAF	Receive Si bits in the non–align frame
RRA	Receive Remote Alarm
RSa4 – RSa8	Receive Sa bits
TSaCR	Transmit Sa Bit Control Register
TSiAF	Transmit Si bits in the align frame
TSiNAF	Transmit Si bits in the non–align frame
TRA	Transmit Remote Alarm
TSa4 – TSa8	Transmit Sa bits

3.2 Bit Assignment Changes within Existing Registers

Highlights bit locations in the DS2154L which have changed from the DS2153Q.

Register	Bit #	DS2153Q Symbol	DS2153Q Description	DS2154L Symbol	DS2154L Description
RCR2	2	RSCLKM	Receive Side SYSCLK Mode Select	RBCS	Receive Side Backplane Clock Select
TCR1	7	N/A	not assigned	ODF	Output Data Format
TCR2	2	N/A	not assigned	ODM	Output Data Mode
CCR2	1	RLB	Remote Loop Back	RFF	Receive Force Freeze
CCR2	0	LLB	Local Loop Back	RFE	Receive Freeze Enable
CCR3	3	LIRST	Line Interface Reset	RSRE	Receive Side Signaling Re–Insertion Enable
CCR3	2	N/A	not assigned	TSRE	Transmit Side Signaling Re–Insertion Enable

Register	Bit #	DS2153Q Symbol	DS2153Q Description	DS2154L Symbol	DS2154L Description
CCR3	1	TSCLKM	Transmit Side SYSCLK Mode Select	TBCS	Transmit Side Backplane Clock Select
CCR3	0	N/A	not assigned	RCLA	Receive Carrier Loss (RCL) Alter–nate Criteria

3.3 Register Bit Moves

Function	DS2153Q Location	DS2154L Location
LIRST	CCR3.3	CCR5.7
LLB	CCR2.0	CCR4.6
RLB	CCR2.1	CCR4.7

4.0 CHANGES IN DEVICE PIN OUT

4.1 Package types

The DS2154L is offered in a 100 pin 14 x 14 x 1.4 mm LQFP. The DS2153Q is offered in a 44 pin 16.7 x 16.7 x 4.0 mm PLCC. Values listed are for body dimensions.

4.2 Device Pin Differences

4.2.1 Control Port Pins

DS2154L	DS2153Q	DESCRIPTION
INT	INT1, INT2	Flags host controller during conditions and change of conditions in the Status Registers 1 and 2, and the FDL Status Register.
TEST	N/A	Device pin tri–state enable.
MUX	N/A	Multiplexed/non–multiplexed bus operation select.
D0:D7 OR AD0:AD7	AD0:AD7	Multiplexed/non–multiplexed bus.
A0:A6	N/A	Address bus.
A7 OR ALE	ALE	A7 in non–multiplexed bus operation, ALE in multiplexed bus operation.

4.2.2 Line Interface Pins

DS2154L	DS2153Q	DESCRIPTION
MCLK	N/A	A 2.048 MHz TTL clock input used for clock/data recovery and for jitter attenuation.
MCLK, XTALD	XTAL1, XTAL2	2.048 MHz quartz crystal option instead of a TTL level clock at MCLK
8XCLK	N/A	An 8 x 2.048 MHz clock that is frequency locked to either the clock/data recovery block or the TCLKI pin.
LIUC	N/A	Line interface circuitry connect enable.
RPOSO	N/A	Receive line interface RPOS bipolar data output.
RNEGO	N/A	Receive line interface RNEG bipolar data output.
RCLKO	N/A	Buffered recovered clock from the E1 line.

DS2154L	DS2153Q	DESCRIPTION
TPOSI	N/A	Transmit line interface TPOS data input.
TNEGI	N/A	Transmit line interface TNEG data input.
TCLKI	N/A	Transmit line interface clock input.

4.2.3 Transmit Side Digital Pins

DS2154L	DS2153Q	DESCRIPTION
TSYSCLK	N/A	Transmit side elastic store clock.
TSSYNC	N/A	Transmit side elastic store frame or multiframe sync input.
TSIG	N/A	Outgoing signaling data input.
TESO	N/A	Transmit elastic store data output.
TDATA	N/A	Transmit formatter data input.
TPOSO	N/A	Transmit formatter TPOS data output.
TNEGO	N/A	Transmit formatter TNEG data output.
TCLKO	N/A	Buffered clock used to move data through the transmit side formatter.

4.2.4 Receive Side Digital Pins

DS2154L	DS2153Q	DESCRIPTION
RFSYNC	N/A	Receive frame sync.
RMSYNC	N/A	Receive multiframe sync.
RDATA	N/A	Receive side framer data output.
RSYSCLK	N/A	Receive side elastic store clock.
RSIG	N/A	Receive signaling bits output.
RCL	N/A	Receive carrier loss indication.
RSIGF	N/A	Receive signaling freeze indication.
8MCLK	N/A	8.192MHz clock referenced to RCLK.
RPOSI	N/A	Receive side framer positive data input.
RNEGI	N/A	Receive side framer negative data input.
RCLKI	N/A	Receive side framer clock input.