DALLAS SEMICONDUCTOR

Application Note 349
DS2152L vs. DS2151Q

INTRODUCTION

This application note highlights the differences between the DS2152L and the DS2151Q T1 Single Chip Transceivers. The DS2152L is a superset of the DS2151Q. All of the original features of the DS2151Q have been retained and software created for the DS2151Q is transferable to the DS2152L with minimal effort.

ADDITIONAL FUNCTIONALITY

New Features	Section
• Option for non–multiplexed bus operation	1 & 2
• Crystal–less jitter attenuation	14
• Additional hardware signaling capability – receive signaling reinsertion to a backplane multiframe sync – availability of signaling in a separate PCM data stream – signaling freezing – interrupt generated on change of signaling data	7.2 & 9
• Per–channel code insertion in both transmit and receive paths	8
• Full HDLC controller for the FDL with 16–byte buffers in both transmit and receive paths	11
• RCL, RLOS, RRA, and RAIS alarms now interrupt on change of state	4
• 8.192 MHz clock synthesizer	1
• Per–channel loopback capability	8
• Addition of hardware pins to indicate carrier loss and signaling freeze	1
• Line interface function can be completely decoupled from the framer/formatter to allow: – interface to optical, HDSL, and other NRZ interfaces – be able to tap the transmit and receive bipolar data streams for monitoring purposes – be able to corrupt data and insert framing errors, CRC errors, etc.	1
• Transmit and receive elastic stores now have independent backplane clocks	1
• Ability to monitor DS0 channel in both the transmit and receive paths	6
• Access to the data stream in between the framer/formatter and the elastic stores	1
• AIS generation in the line interface that is independent of loopbacks	1 & 3

• Ability to calculate and check CRC6 according to the Japanese standard	3
• Ability to pass the F–Bit through the elastic stores in the 2.048 MHz backplane mode	3 & 15
• Programmable in–band loop code generation and detection	12
• Device identification register	3

CHANGES IN REGISTER DEFINITIONS

When implementing the new features of the DS2152L, a priority was placed on preserving the DS2151Qs register map to facilitate code migration from existing DS2151Q designs. This section highlights register additions and differences found in the DS2152L.

New Feature Register Usage

Highlights specific registers containing bit locations related to new features. Each item can be found in the data sheet under the listed sections.

FULL HDLC & BOC CONTROLLER FOR FDL SUPPORT (SECTION 11.1)

REGISTER	DESCRIPTION
TCR1	Transmit Control Register 1
FDLC	FDL Control
FDLS	FDL Status
FIMR	FDL Interrupt Mask
RPRM	Receive Performance Report Message
RBOC	Receive Bit Oriented Code
RFFR	Receive FDL FIFO
TPRM	Transmit Performance Report Message
TBOC	Transmit Bit Oriented Code
TFFR	Transmit FDL FIFO

DS0 MONITORING (SECTION 6.0)

REGISTER	DESCRIPTION
CCR5	Common Control 5 (bits 4–0)
CCR6	Common Control 6 (bits 4–0)
TDS0M	Transmit DS0 Monitor
RDS0M	Receive DS0 Monitor

HARDWARE BASED SIGNALING (SECTION 7.2 and 9)

REGISTER	DESCRIPTION
RCBR1–3	Receive Channel Block Registers 1 – 3
TCBR1–3	Transmit Channel Block Registers 1 – 3

CCR4	Common Control 4 (bits 7, 6, 2, and 1)

SIGNALING FREEZE (SECTION 3.0 and 7.2)

REGISTER	DESCRIPTION
CCR4	Common Control 4 (bits 4 and 3)

PER CHANNEL LOOPBACK (SECTION 8.0)

REGISTER	DESCRIPTION
CCR4	Common Control 4 (bits 0)
TIR1 – TIR3	Transmit Idle Registers 1 – 3

PER CHANNEL CODE (IDLE) INSERTION (SECTION 8.0)

REGISTER	DESCRIPTION
TCC1 – TCC3	Transmit Channel Control 1 – 3
TC1 – TC24	Transmit Channels Registers 1 – 24
RCC1 – RCC3	Receive Channel Control 1 – 3
RC1 – RC24	Receive Channels Registers 1 – 24

PROGRAMMABLE IN–BAND LOOP CODE GENERATION & DETECTION (SECTION 12)

REGISTER	DESCRIPTION
TCD	Transmit Code Definition
IBCC	In–Band Code Control
CCR3	Common Control 3 (bit 1)
RUPCD	Receive Up Code Definition
RDNCD	Receive Down Code Definition
SR1	Status Register 1 (bits 7 and 6)

DEVICE IDENTIFICATION (SECTION 3.0)

REGISTER	DESCRIPTION
IDR	Device Identification

JAPANESE CRC–6 MODE (SECTION 3.0)

REGISTER	DESCRIPTION
CCR5	Common Control 5 (bit 7)
CCR6	Common Control 6 (bit 7)

INTERRUPT ON CHANGE OF STATE FOR RCL, RLOS, RRA, RAIS (SECTION 4.0)

REGISTER	DESCRIPTION
SR2	Status Register 2
IMR2	Interrupt Mask Register 2

BIT ASSIGNMENT CHANGES WITHIN EXISTING REGISTERS

Highlights bit locations in the DS2152L which have changed from the DS2151Q.

REGISTER	BIT NO.	DS2151Q SYMBOL	DS2151Q DESCRIPTION	DS2152L SYMBOL	DS2152L DESCRIPTION
TCR1	2	TLINK	TLINK Select	TFDLS	TFDL Select
TCR2	0	B7ZS	Bit 7 Zero Suppression Enable	TB7ZS	Transmit Side Bit 7 Zero Suppression Enable
CCR1	3	SCLKM	SYSCLK Mode Select	RSCLKM	RSYSCLK Mode Select
CCR1	4	RLB	Remote Loop Back	TSCLKM	TSYSCLK Mode Select
CCR1	6	LLB	Local Loop Back	ODF	Output Data Format
CCR3	0	LIRST	Line Interface Reset	N/A	not assigned
CCR3	1	TLU	Transmit Loop Up	TLOOP	Transmit Loop Up Enable
CCR3	2	TLD	Transmit Loop Down	ECUS	Error Counter Update Select
CCR3	5	P16F	Function of Pin 16	RLOSF	Function of the RLOS/LOTC Output

REGISTER	BIT NO.	DS2151Q SYMBOL	DS2151Q DESCRIPTION	DS2152L SYMBOL	DS2152L DESCRIPTION
RIR2	2	JALT	Jitter Attenuator Limit Trip	RBLC	Receive Blue Alarm Clear
RIR2	6	RL0	Receive Level Bit 0	LRCLC	Line Interface Receive Carrier Loss Clear
RIR2	7	RL1	Receive Level Bit 1	RLOSC	Receive Loss of SYNC Clear
SR1	1	RCL	Receive Carrier Loss	LRCL	Line Interface Receive Carrier Loss
SR2	0	N/A	not assigned	RSC	Receive Signaling Change
IMR1	1	RCL	Receive Carrier Loss	LRCL	Line Interface Receive Carrier Loss
IMR2	0	N/A	not assigned	RSC	Receive Signaling Change

REGISTER BIT MOVES

FUNCTION	DS2151Q LOCATION	DS2152L LOCATION
JALT	RIR2.2	RIR3.5
LIRST	CCR3.0	CCR6.7
LLB	CCR1.6	CCR5.6
RL0	RIR2.6	RIR3.6
RL1	RIR2.7	RIR3.7
RLB	CCR1.4	CCR7.6

CHANGES IN DEVICE PIN OUT
Package Types

The DS2152L is offered in a 100 pin 14 x 14 x 1.4 mm LQFP. The DS2151Q is offered in a 44 pin 16.7 x 16.7 x 4.0 mm PLCC. Values listed are for body dimensions.

Device Pin Differences

CONTROL PORT PINS

DS2152L	DS2151Q	DESCRIPTION
INT	INT1, INT2	Flags host controller during conditions and change of conditions in the Status Registers 1 and 2, and the FDL Status Register.
TEST	N/A	Device pin tri–state enable.
MUX	N/A	Multiplexed/non–multiplexed bus operation select.
D0:D7 or AD0:AD7	AD0:AD7	Multiplexed/non–multiplexed bus.
A0:A6	N/A	Address bus.
A7 or ALE	ALE	A7 in non–multiplexed bus operation, ALE in multiplexed bus operation.

LINE INTERFACE PINS

DS2152L	DS2151Q	DESCRIPTION
MCLK	N/A	A 1.544 MHz TTL clock input used for clock/data recovery and for jitter attenuation.
MCLK, XTALD	XTAL1, XTAL2	1.544 MHz quartz crystal option instead of a TTL level clock at MCLK
8XCLK	N/A	An 8 x 1.544 MHz clock that is frequency locked to either the clock/ data recovery block or the TCLKI pin.
LIUC	N/A	Line interface circuitry connect enable.
RPOSO	N/A	Receive line interface RPOS bipolar data output.
RNEGO	N/A	Receive line interface RNEG bipolar data output.
RCLKO	N/A	Buffered recovered clock from the T1 line.
TPOSI	N/A	Transmit line interface TPOS data input.
TNEGI	N/A	Transmit line interface TNEG data input.
TCLKI	N/A	Transmit line interface clock input.

TRANSMIT SIDE DIGITAL PINS

DS2152L	DS2151Q	DESCRIPTION
TSYSCLK	N/A	Transmit side elastic store clock.
TSSYNC	N/A	Transmit side elastic store frame or multiframe sync input.
TSIG	N/A	Outgoing signaling data input.
TESO	N/A	Transmit elastic store data output.
TDATA	N/A	Transmit formatter data input.
TPOSO	N/A	Transmit formatter TPOS data output.
TNEGO	N/A	Transmit formatter TNEG data output.
TCLKO	N/A	Buffered clock used to move data through the transmit side formatter.

RECEIVE SIDE DIGITAL PINS

DS2152L	DS2151Q	DESCRIPTION
RFSYNC	N/A	Receive frame sync.
RMSYNC	N/A	Receive multiframe sync.
RDATA	N/A	Receive side framer data output.
RSYSCLK	N/A	Receive side elastic store clock.
RSIG	N/A	Receive signaling bits output.
RCL	N/A	Receive carrier loss indication.
RSIGF	N/A	Receive signaling freeze indication.
8MCLK	N/A	8.192MHz clock referenced to RCLK.
RPOSI	N/A	Receive side framer positive data input.
RNEGI	N/A	Receive side framer negative data input.
RCLKI	N/A	Receive side framer clock input.