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APPLICATION NOTE 119

Embedding the 1-Wire® Master in FPGAs or ASICs

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Abstract: This application note shows how to incorporate the 1-Wire Master (1WM) into a user's ASIC design. It contains excerpts of how to create a 1-Wire Master instance in Verilog. The DS89C200 referred to in this document is a theoretical microcontroller. It is assumed the reader has knowledge of the DS1WM 1-Wire Master and the 1-Wire protocol in general.

Introduction

The DS1WM 1-Wire Master, termed 1WM, was created to facilitate host CPU communication with devices over a 1-Wire bus without concern for bit timing. This application note shows how to incorporate the 1-Wire Master into a user's ASIC design. The DS89C200 referred to in this document is a theoretical micro controller. It is assumed the reader has knowledge of the DS1WM 1-Wire Master and Maxim's 1-Wire protocol. For more detailed information see application note 937, "Book of iButton® Standards" and DS1WM data sheet.

Structure

The 1WM is arranged as a top-level harness that connects four sub-modules together to form a complete unit. There is no HDL code in the toplevel harness. The four sub-module files consist of the one_wire_interface, the one_wire_master, the clk_prescaler and the one_wire_io. For applications that do not need the clock prescaler, this module can be left out if an external 1MHz clock source for the clk_1us signal is supplied (Noted as τ in the DS1WM datasheet, the input clock is specified from 0.8MHz to 1.0MHz).

The one_wire_io module provides the bidirectional signals for the DATA and the DQ signals. In most applications the DQ signal will be an I/O pin. If this is the case, the pad driver for DQ must be an open drain pad with the proper ESD protection (**Figure 1**). Also, if the peripheral devices use a pull-up voltage that is greater than the 1WM supply, then a pad driver must be chosen that can tolerate the extra voltage and diode clamps must not be used. Maxim recommends that the output driver (Q1) of 100Ω and an external DQ pull up of 4.7kΩ to chip V_{CC}. Chip V_{CC} must be greater than VIH of the 1-Wire slave for proper communication.

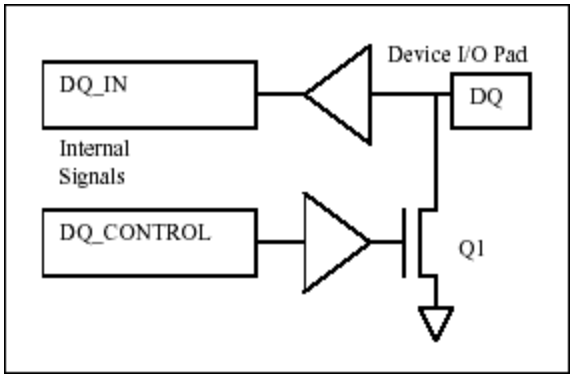

Figure 1. DQ pad driver (one_wire_io).

Libraries

To compile the Verilog source no external libraries are required. The VHDL source version requires both IEEE.std_logic_1164 and work.std_arith libraries.

Connections

The following table lists the wires that needed to be connected for proper operation of the 1-Wire Master.

Pin	Operation
DQ	Open Drain Bi-directional 1-Wire Bus Connection
DATA	Bi-directional 8 Bit Data Bus
ADDRESS	3 Bit Address Bus
ADS-bar	Address Strobe
EN-bar	Instance Enable
RD-bar	Read Data Strobe
WR-bar	Write Data Strobe
INTR	Interrupt Detection
CLK	System Clock
MR	Mater Reset

If no address strobe is available in the system, the ADS-bar may be tied low making the address latch transparent. The EN-bar signal should be generated by address decode logic external to the 1WMaster module. If the 1WM is the only instance on the data bus, EN-bar may be tied low. The system clock wired to CLK must be between 3.2MHz and 128MHz. For detailed operation of all connections see the DDS1WM data sheet.

Instance

The following is an example of how to create a 1-Wire Master instance in Verilog.

```
module DS89C200 (...top level list...);

wire [7:0] DB;
wire [2:0] ADDR;
wire sysclk, read-bar,
     write-bar, master_reset,
     interrupt, addr_strobe;
wire DQ_OUT;

supply1 Tie1;
supply0 Tie0;

cpu xcpu(.CLK(sysclk),
         .DB(DB),
         .EXTRD-bar(read-bar),
         .EXTWR-bar(write-bar),
         .EXTADDR(ADDR),
         .RESET(master_reset),
         .EXTINTR(interrupt),
         .ADDR_ST(addr_strobe),
         ... other I/O signals ...);

onewiremaster xonewiremaster(
         .ADDRESS(ADDR),
         .ADS-bar(addr_strobe),
         .EN-bar(Tie0),
         .RD-bar(read-bar),
         .WR-bar(write-bar),
         .DATA(DB),
         .INTR(interrupt),
         .CLK(sysclk),
         .DQ(DQ_OUT),
         .MR(master_reset) );

... rest of design ...
```

All signals generated by xcpu meet the 1-Wire Master timing requirements. The EN-bar signal is tied low because there is no other addressable logic on the data bus. The DQ_OUT signal is wired directly to an I/O pad.

Synthesis

Synthesis of this design is very straightforward. A bottom up approach is recommended compiling the individual submodules individually and afterwards optionally compiling the top level. Timing constraints need to be placed on the clk_1us signal along with sysclk signal. Further timing constraints may be necessary for some of the asynchronous control signals such as WR-bar, RD-bar, EN-bar, ADS-bar, and MR. Additional constrains may be necessary for clk_1us to keep buffers from being inserted on the clock signal. In most cases will be necessary to have strategy for clock distribution such as a clock tree.

Included with the source code are example synthesis scripts and Makefile to be used with Synopsys design compiler. To use these it is necessary to create a .synopsys_dc.setup file that defines the target synthesis library. In addition, it is necessary to modify the included environment file (named "environment") to specify the device from the target library to be used for specifying output drive strengths and input loads. These example scripts are very generic. The actual scripts and constraint files would be generated by the engineer to meet the timing requirements of the specific design. One thing to keep in mind is that the timing in the 1-Wire Master block is not entirely synchronous by design. The DQ

output is synchronized to CLK, but the bus read/write timing will only be synchronous to CLK if the CPU uses CLK to generate RD-bar, WR-bar, and ADS-bar. See the specification for the timing relationships for these signals.

This example design is fully self contained. It has been successfully compiled to FPGA and ASIC targets with success. When synthesized to a typical ASIC target library, the design uses a total of 1934 2-input NAND gates or 237 slices of a Xilinx® Spartan 3A FPGA.

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Related Parts		
DS1WM	Synthesizable 1-Wire Bus Master	
DS2408	1-Wire 8-Channel Addressable Switch	Free Samples
DS2502-E48	48-Bit Node Address Chip	Free Samples

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