DALLAS SEMICONDUCTOR

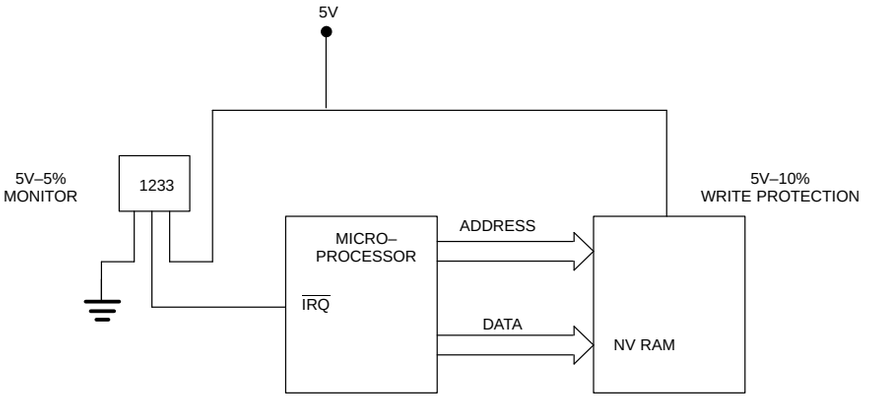
Application Note 51
How to Save Data During a Power Failure Without Corrupting It

For many memory systems requiring nonvolatile memory, Dallas Semiconductor NV SRAMs offer an SRAM's ease of implementation coupled with write protection circuitry and a 10 year information storage capability. NV SRAMs automatically write protect themselves when they detect an out–of–tolerance condition (usually at 10% of V_{CC}), making them a secure receptacle for data to be protected during a power failure.

One issue that is not addressed by the secure write protection strategy of the NV SRAM is this: what happens to the data currently being processed during a power failure? If the voltage has fallen to 10% of V_{CC}, time has already run out to perform any system housekeeping functions such as storing off data and storing the state of the microprocessor. What is required to truly address this need to "save data before write–protecting memory" is a method to detect an impending power failure well before the power supply has fallen to 10% of V_{CC} so that a microprocessor can perform these housekeeping functions.

One way to accomplish this task is to use a second voltage monitoring device. Dallas Semiconductor manufactures the DS1233B, a 5V–5% voltage monitor in a 3–pin TO–92 size package. This 5% monitor drives an active low reset signal, $\overline{RST}$, as soon as it detects an out–of–tolerance condition. This active low signal can be used as an $\overline{IRQ}$ input to a microprocessor, providing the microprocessor with an advanced warning that the power supply is falling, and giving it time to service the interrupt before the system's nonvolatile memory has been write protected. The following diagram illustrates this concept.

5V – 5% $\overline{IRQ}$ GENERATION



You might wonder of what use the time between a 5% and 10% drop in a 5V power supply could possibly be to a microprocessor. After all, don't power supplies fall rapidly when they do go through a hard failure? The answer is, yes, of course they do. But, fortunately, microprocessors can service interrupts and process information even faster. All that is required is that the system's interrupt servicing software be configured so that it quickly identifies and services external interrupts. An example follows of how useful this time can be.

For the sake of this discussion, let's make several assumptions about the conditions that exist inside of the system in question. Let's assume:

1. That the power supply falls quickly, taking only 300 microseconds to fall from 4.75 to 4.0 volts.
2. That the microprocessor in question runs at a relatively moderate clock speed of 25 MHz.
3. That this microprocessor is a common 8–bit device, requiring on the order of six clocks to execute a single instruction.

With this set of givens, how many instructions should the processor be able to execute between the 5% and 10% trip points on a 5V power supply?

1/25 MHz = 40 ns clocks

six clocks/instruction = 240 ns per instruction

(4.75–4.00)/300 µs = 0.0025 V/µs

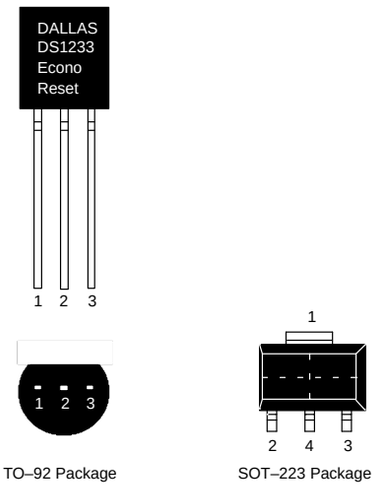
5% – 10% drop = 0.25 V; hence 5%–10% drop = 100 µs

100 µs/ 240 ns per instruction = 416 instructions

Having 416 executable instructions at your disposal versus having none during a power down makes a big difference in saving 256 bytes of information or losing it, or in saving the state machine of the processor or losing it. In addition, the variables can be modified by design to give the processor even more time. The rate of fall of voltage of the power supply during a power failure can be slowed by adding capacitance. Processors requiring fewer than six clocks to execute an instruction can be used. In any case, using a DS1233B in conjunction with your NV SRAM requirements can give you the additional time you need to execute an orderly system shutdown, without corrupting your memory or allowing your microprocessor to run out of control.

ORDERING INFORMATION

DS1233B



TO–92 Package SOT–223 Package

NV SRAM PINOUTS