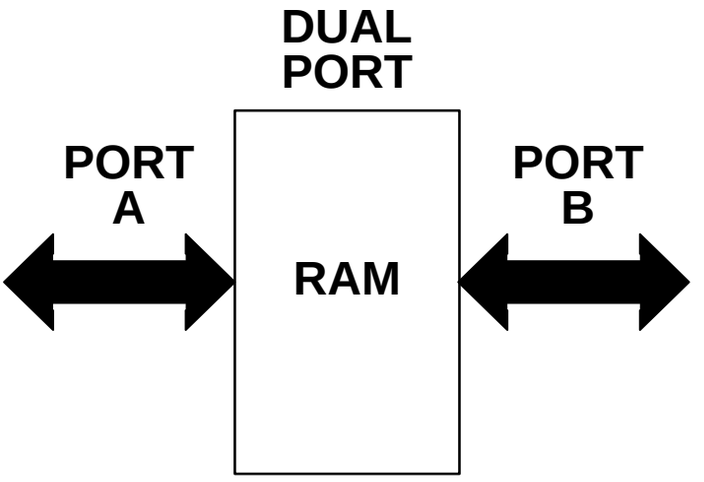
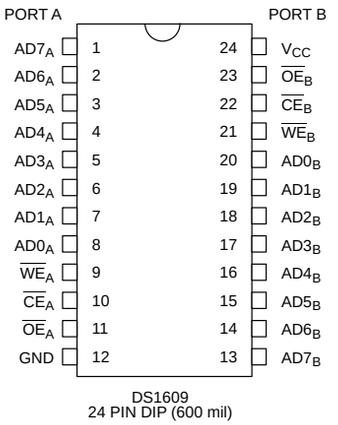
DALLAS SEMICONDUCTOR

Application Note 62
Dual Port RAM

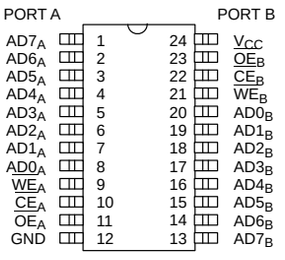


Memory devices and systems are diversifying and becoming more complex out of necessity to support information processing needs. The need to centralize data storage in multiprocessor applications challenges both hardware and software designers. New ways must be found that consolidate system information that is controllable by more than one bus. In addition, systems are becoming more power conscious, particularly portable systems as they typically rely on some kind of rechargeable battery for power. For systems where shared bus access requirements are infrequent, but require many megabytes of memory to be transferred, a shared mass storage device such as a floppy disk drive or networked hard disk drive may suffice. However, for frequent, low density access, media such as hard drives or floppy diskettes are impractical and would greatly slow the rate at which data could be stored and retrieved. The DS1609 Dual Port Ram has been specifically designed to be able to meet high frequency, low volume data storage and retrieval between two asynchronous systems. With its ability to operate at voltages as low as 2.5 volts, the DS1609 also fits easily into any portable application where power availability is limited.

PIN ASSIGNMENT



DS1609
24 PIN DIP (600 mil)



DS1609S
24 PIN SOIC (300 mil)

PIN DESCRIPTION

V_{CC}	+5 VOLT SUPPLY
GND	GROUND
AD0–AD7	PORT ADDRESS/DATA
$\overline{CE}$	PORT ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE

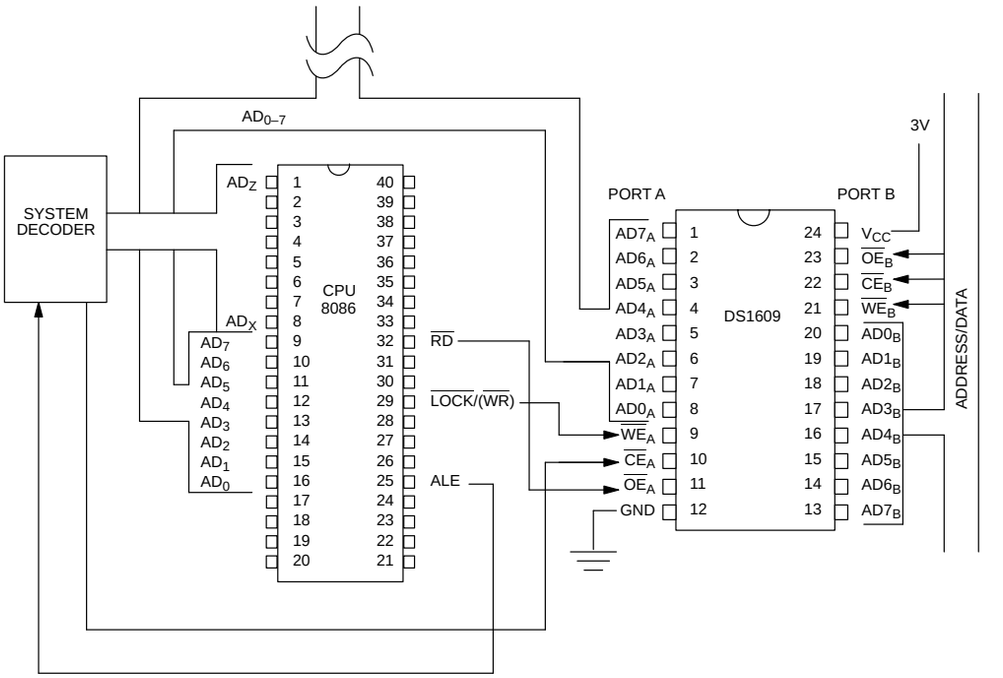
The type of bus which may be connected to either port of the DS1609 is not limited to system level. A multiplexed microprocessor address and data bus can be connected directly to either or both ports of the DS1609. The device can be controlled from either bus port separately by only three signals, $\overline{OE}$, $\overline{CE}$, and $\overline{WE}$. The obvious disadvantage of the multiplexed bus is the slightly reduced system performance because address and data information is being transmitted serially. The equally obvious advantage is the reduced pin count achievable by multiplexing the addressing and data buses.

Read/Write access of either port is transferred as 8 bits address, followed by 8 bits of data. In a read cycle to a port, $\overline{WE}$ is inactive, and the cycle is initiated when $\overline{CE}$ goes active, which with the address latched, data is retrieved under the control of $\overline{OE}$. The rising edge of either $\overline{CE}$ or $\overline{OE}$ terminates the read cycle. For a write cycle, $\overline{OE}$ is inactive, and $\overline{CE}$ becoming active latches the address to be accessed, with $\overline{WE}$ becoming active.

The DS1609 dual port RAM has a special cell design that allows for simultaneous accesses from two ports. Because of this cell design, no arbitration is required for read cycles occurring at the same instant. However, an argument for arbitration can be made for reading and writing the cell at the exact same instant or a write from both ports at the same instant. If a write cycle occurs while a read cycle is in progress, the read cycle will likely recover either the old data or new data and not some combination of both. However, the write cycle will update the memory with correct data. Simultaneous write cycles to the same memory location pose the additional concern that the cell may be in contention causing a metastable state. Depending on the timing of the write cycles of port A and port B, the memory location could be left containing the data written from port A or the data from port B or some combination thereof. However, both concerns expressed above can be eliminated by disciplined system software design. A simple way to assure that read/write contention does not occur is to perform redundant read cycles. Write/write contention needs can be avoided by assigning groups of addresses for

write operations to one port only. Groups of data can be assigned check sum bytes which would guarantee correct transmission. A software arbitration system using a “mail box” to pass status information can also be employed. Each port could be assigned a unique byte for writing status information which the other port would read. The status information could tell the reading port if any activity is in progress and indicate when activity is going to occur.

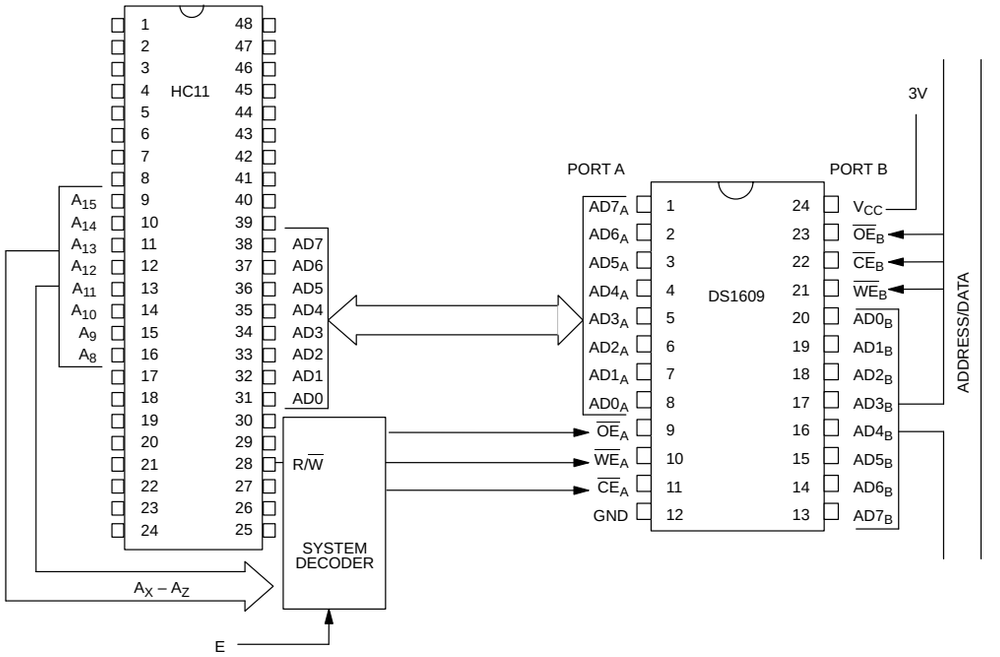
DS1609 DUAL PORT INTERFACE TO INTEL 8086 MICROPROCESSOR Figure 1



The DS1609 is ideally suited for small microprocessor based systems which frequently utilize dedicated 8 bit multiplexed address/data busses the following examples deal with interfacing with the Intel 8086/8088 series and the Motorola HC11 series microprocessors.

For implementation with the Intel 8086/8088 microprocessor family, the address/data pins of either port may be tied directly to the lower 8 address data lines of the Intel 8086 or 8088 microprocessor (Figure 1). The $\overline{RD}$ pin from the microprocessor provides the $\overline{OE}$ input to the port on the DS1609, while $\overline{WR}$ provides the $\overline{WE}$ input to the port. The port's $\overline{CE}$ input may be conditioned by a system decoder, which would require the 8086's ALE output as an input to provide address latching. Several of the unused address/data lines from the 8086 would also be required as inputs to indicate where the DS1609 resides in the system memory map. In applications where multiple DS1609 ports are required, multiple $\overline{CE}$ outputs could be provided from a system decoder using the ALE signal from an Intel 8086/8088 with user specified address lines to generate multiple chip selects (Figure 3).

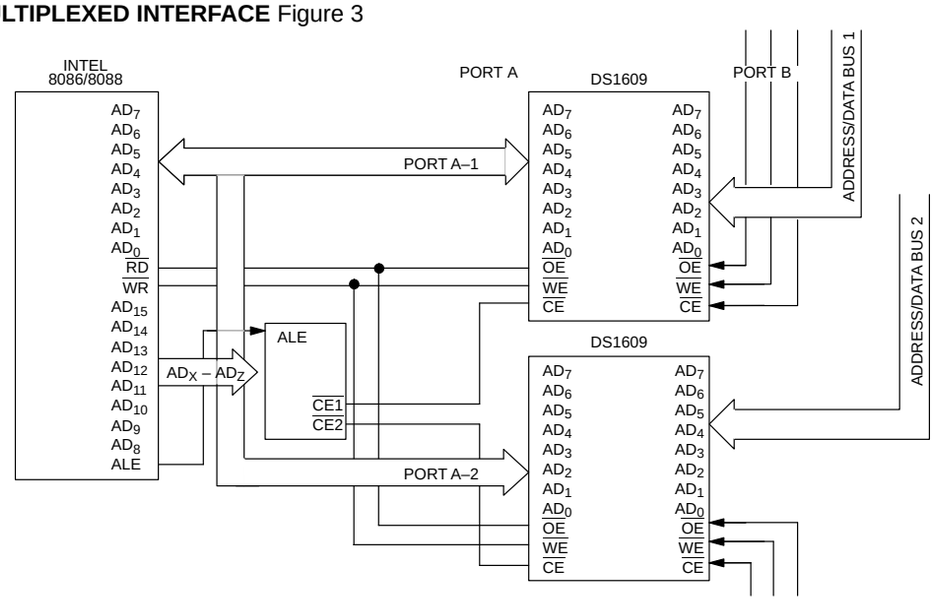
MOTOROLA HC11 EXPANDED MODE Figure 2



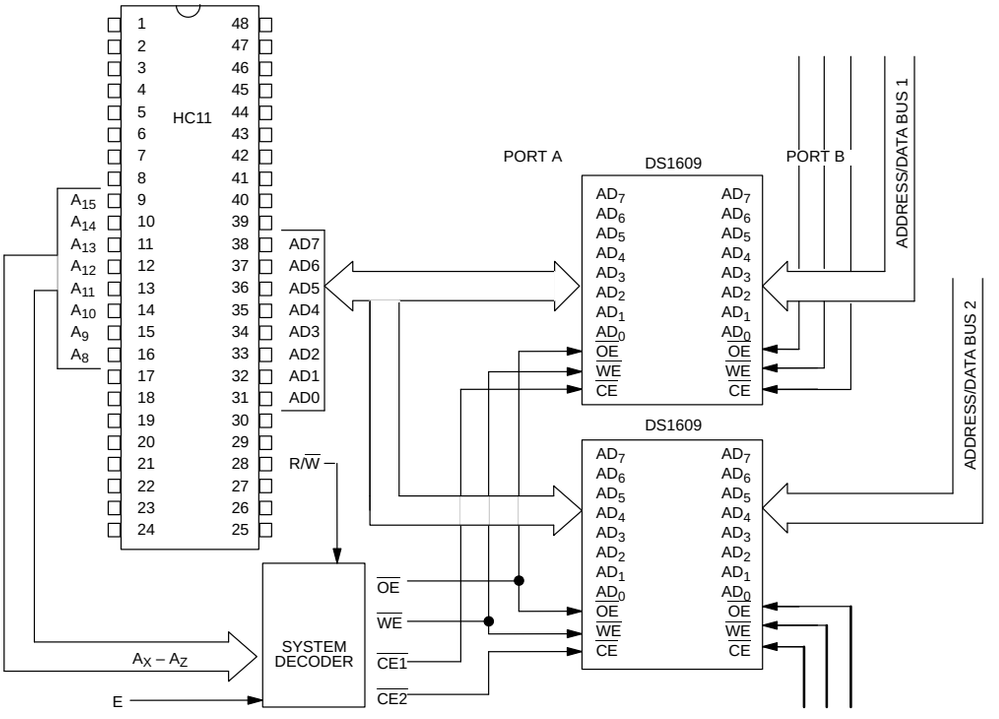
For implementation with the Motorola HC11 microprocessor family, the address/data pins of either port on a DS1609 may be directly ties to port C of an HC11 operating in expanded mode (Figure 2). Address pins from port B of the HC11 ($A_8 – A_{15}$) may be used to provide the DS1609's location in the system memory map. The E signal, which is also an input to the HC11, provides a bus clock to the system decoder indicating whether the HC11 is in an address or data cycle. The R/$\overline{W}$ input to the decoder indicates whether the HC11 is writing or reading data in a data cycle. From these inputs, a system decoder can provide $\overline{OE}$, $\overline{WE}$, and $\overline{CE}$ outputs to DS1609. For applications where more density is required, two DS1609's may be used. The same inputs, including a user selected combination of address lines $A_8 – A_{15}$ can be used to provide $\overline{OE}$, $\overline{WE}$, and multiple $\overline{CE}$ signals for individual DS1609 devices (Figure 4).

The DS1609 may be used with other microprocessors without multiplexed busses, which have a separate address and data bus.

MULTIPLEXED INTERFACE Figure 3

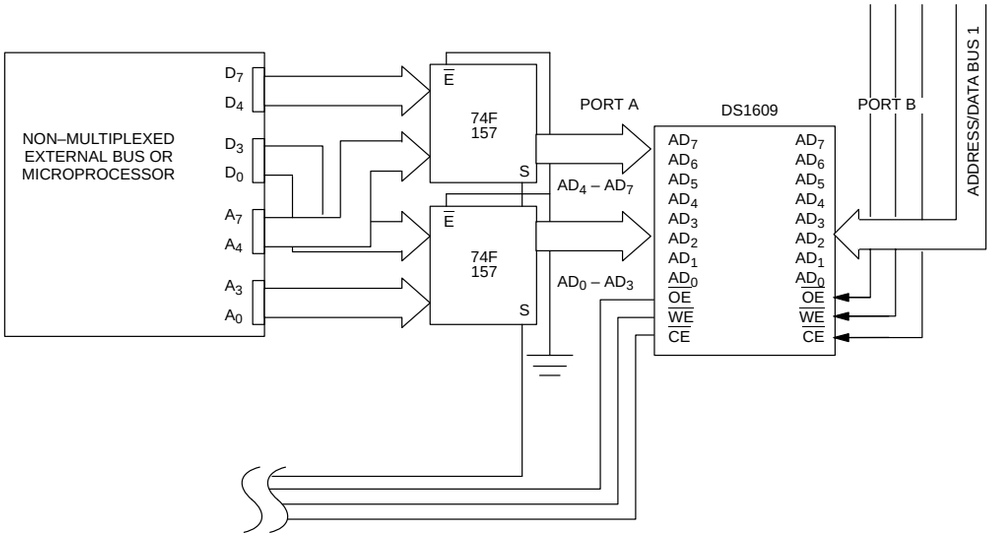


MOTOROLA HC11 EXPANDED MODE MULTIPLE DS1609'S Figure 4



The DS1609 can be used as a go between with non–multiplexed microprocessors such as the Intel 386 or Motorola 68030. Processor cycles to and from a DS1609 must then be multiplexed specifically for the DS1609's address/data/bus. An example implementation is shown below (Figure 5).

SAMPLE IMPLEMENTATION; NON–MULTIPLEXED BUS Figure 5



In this implementation, the lower 8 bits of a microprocessor's address bus and data bus are connected to the multiplexed address and data inputs using two 74F157 quad 2 input multiplexers. Each of the 74F157 devices takes 4 address and 4 data inputs originating from a microprocessor or an external bus master. The 74F157s produce four outputs of multiplexed address/data information which can then be used by a DS1609 port. The $\overline{E}$ inputs of each 74F157 may be tied to ground. The S inputs on the 74F157's become control logic, and direct switching back and forth between passing the address lines or the data lines. Read and write enabling signals must be provided by the microprocessor or external bus master.

IN SUMMARY

The DS1609 Dual Port RAM is tailored for use with 8 bit multiplexed address/data bus microprocessors. The DS1609's unique asynchronous dual port access allows a system design to provide a 256 bytewide registers which may be shared by two independent microprocessors. Multiple DS1609's may be tied together in a system to provide for 3 microprocessors having access to two 256 byte memories. Because of the multiplexed address/data bus, pin count and cost are kept to a minimum while providing for the unique asynchronous access. For systems which do not have a multiplexed address/data bus, minimal logic can convert separate address and data lines into a multiplexed address/data bus usable by the DS1609.

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