DALLAS SEMICONDUCTOR

Application Note 77
DS1585/87, DS1685/87 and DS17x85/87 Accessing Extended User RAM via Software

GENERAL OVERVIEW

The DS1585/87, DS1685/87 and DS17x85/87 include an additional block of extended user RAM. The memory capacity of each device varies as follows; the DS1585/87 provides 65,536 bits organized in an 8K x 8 block, the DS1685/87 provides 1,024 bits organized in a 128 x 8 block, and the DS17x85/87 provides 16,384, 32,768 or 65,536, bits organized in 2K x 8, 4K x 8, or 8K x 8, blocks respectively.

REGISTER PARTITIONING

Figure 1 illustrates how the register blocks have been partitioned into two separate banks, bank 0 and bank 1. A bank select bit, DV0 located in control register 0Ah (bit 4), is used to select which register bank to make accessible. When DV0 is written to a logic 0, bank 0 is selected and an additional 64 bytes of user RAM can be accessed. However, when DV0 is written to a logic 1, bank 1 is selected and the additional features, including the extended user RAM, can be accessed. The real time clock (RTC), control registers, and 50 bytes of user RAM are accessible from either bank, independent of the DV0 bit.

SOFTWARE COMMUNICATION PORTS

The extended user RAM communication ports reside in the bank 1 register block. The extended user RAM address ports are located in registers 50h and 51h, while the extended user RAM data port is located in register 53h. Register 50h contains the LSB address and register 51h contains the MSB address. The DS1685/87 requires only seven bits to address the extended RAM and therefore does not require the MSB address register, 51h. These three bank 1 registers provide the software interface necessary to access the extended user RAM. The steps involved to read from and write to the extended RAM are listed below:

- Write the DV0 bit to a logic 1
- Write the LSB address to register 50h
- Write the MSB address (if required) to register 51h
- Read from or write to the data register, 53h

An automatic address increment feature, available with the DS17x85/87, simplifies the software required to access the extended user RAM. This feature can be enabled or disabled with a single bit, located in extended control register 4Ah, bit 5. This feature simplifies the software required to access consecutive RAM address locations.

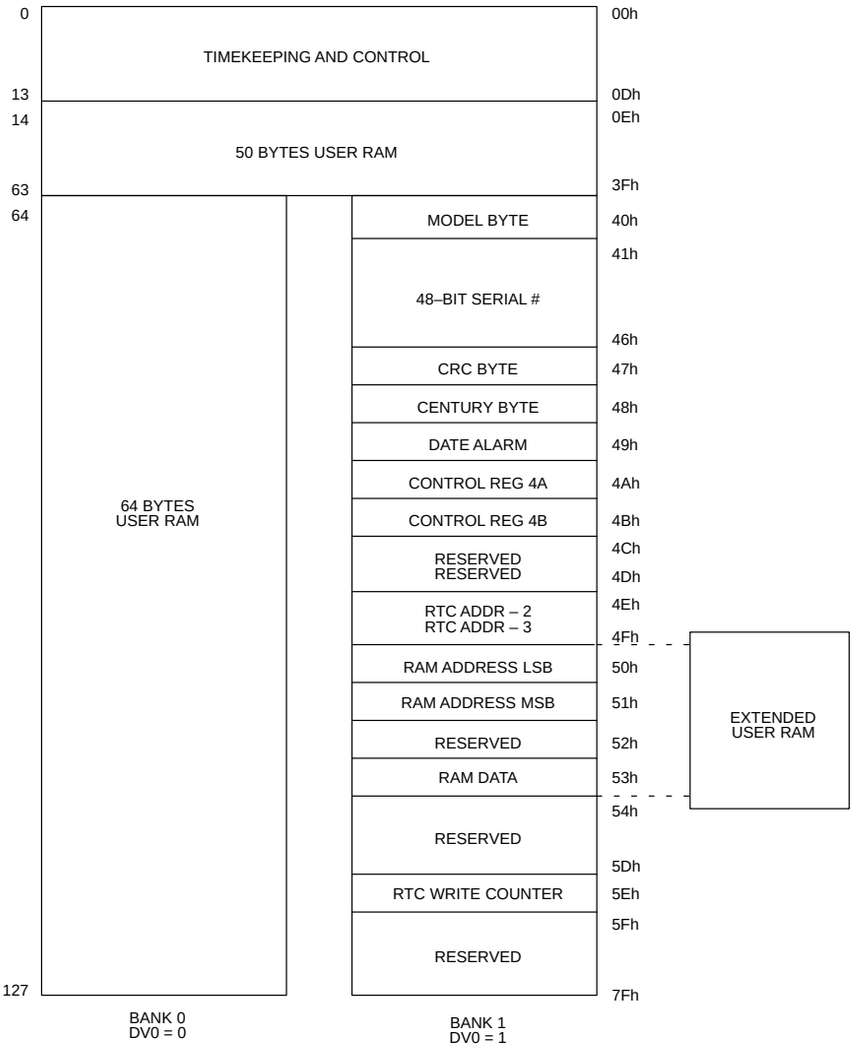
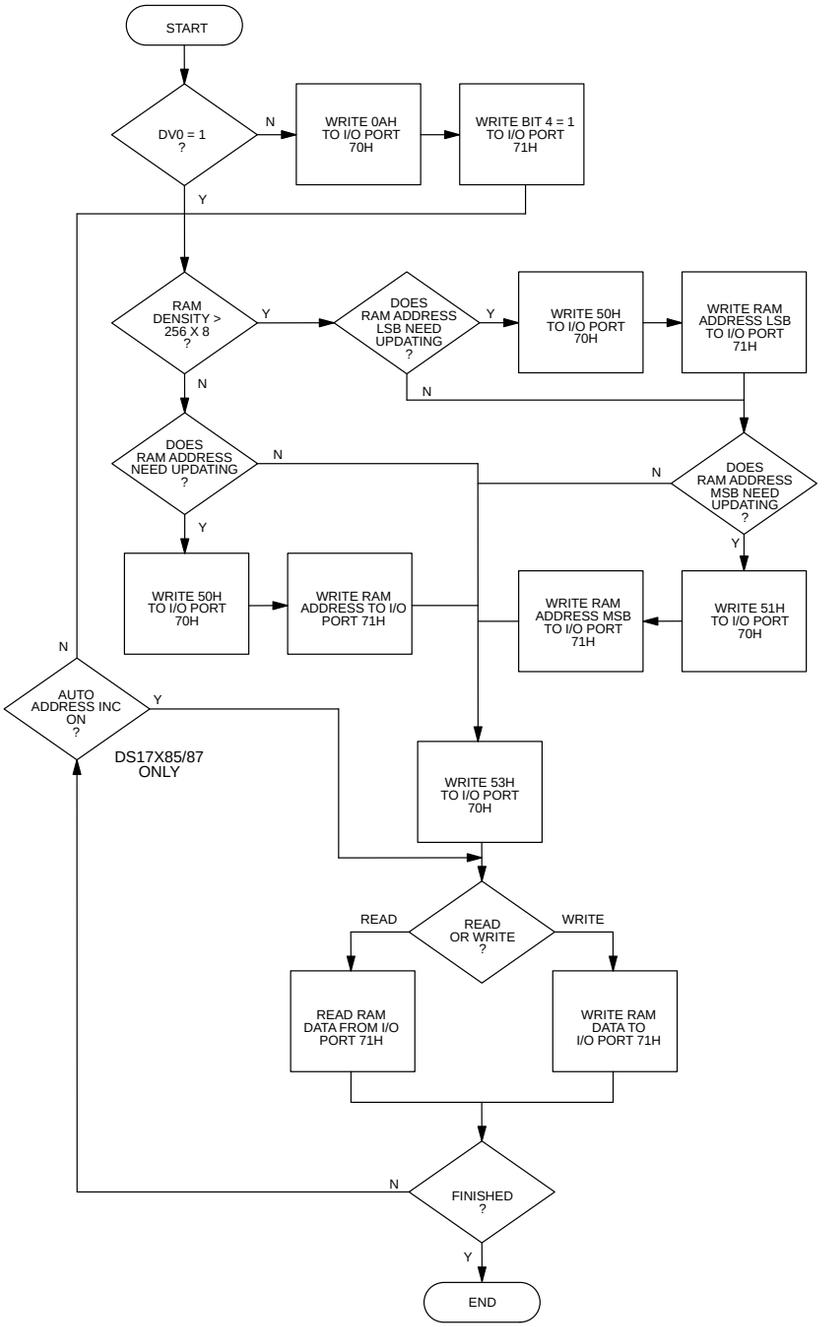
PROTOCOL FOR PC APPLICATIONS

The processor I/O ports used to access CMOS RAM are 70h and 71h. Port 70h is the CMOS RAM address register and port 71h is the CMOS RAM data register. The flow chart shown in Figure 2 illustrates the software protocol for PC applications.

SUMMARY

The DS1585/87 also provides a hardware interface to access the extended user RAM, however, this requires additional hardware to implement. The extended user RAM software access method provides the user with the greatest flexibility when determining which RAM density is needed, without any hardware modifications, for the DS1685/87 and DS17x85/87 (2K, 4K, and 8K) devices.

REGISTER BLOCK PARTITIONING Figure 1



PC SOFTWARE PROTOCOL FLOW CHART Figure 2