Application Note 94
Using the Secure Microcontroller With EPROM/ROM

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OVERVIEW

The Soft Microcontroller family is designed to take advantage of the many features provided by NV RAM technology. Occasionally a designer may wish to use an EPROM or other non-battery backed technology for program storage. While this sacrifices features such as the Bootstrap loader and program encryption, it will still allow a designer to use Soft Microcontroller features such as the power-fail monitor, watchdog timer and the I/O pins made available by the use of the embedded byte-wide bus. This application note addresses considerations when designing such a system using the DS5000FP and DS5001FP Soft Microcontrollers. This application note is not applicable to the DS5002FP Secure Microcontroller as it must use NV RAM to support the encryption features.

USING THE SOFT MICROCONTROLLER WITHOUT A BATTERY

The Soft Microcontroller will work reliably without a battery if a few design precautions are taken. The V_{BAT} input must be tied to V_{SS} if a battery will not be used in the design. A floating V_{BAT} input will cause unreliable device operation and/or a spontaneous reset.

Note that on DS5000FP devices revision D6 or earlier, the power-fail interrupt and power-fail reset will not work properly if V_{BAT} is tied to V_{SS} . On these devices, the V_{BAT} signal is used as a voltage reference to determine the reset trip point and should be approximately 3.0V when V_{CC} > 3.0V. The revision level is marked on each device as follows: xxxxRR-16, where RR is the revision level.

The lack of a battery means that registers that are typically nonvolatile will default to their no V_{LI} reset state. The registers shown in Table 1 should be reinitialized as part of a power-on reset routine to ensure that they are properly set. Note that upon a no V_{LI} reset the DS5001FP will be configured for a partition of 64kB and a range of 32KB. Although this is an invalid setting, the device will operate correctly below the 32kB boundary. The memory configuration of the DS5001FP can only be changed from this setting via the bootstrap loader.

NONVOLATILE REGISTERS Table 1

PCON	87h
MCON	C6h
Encryption Key	N/A
RPCTL	D8h
CRC	C1h

MIXING NV RAM AND ROM MEMORY

Many of the memory interface signals output from the Soft Microcontrollers are battery-backed in data retention mode. This ensures that the memory is write protected in the battery-backed state. While this is beneficial when using NV RAM, it can cause a problem if these signals are connected to memory which will be powered off in data retention mode.

The DS5001FP has a special version of the $\overline{CE1}$ signal that is not battery backed in data retention mode. This signal, $\overline{CE1N}$ can be directly connected to an external memory such as EPROM that will not be battery backed during data retention mode. In addition, $\overline{PE3}$ and $\overline{PE4}$ are not battery backed and can be attached to any kind of peripheral. During data retention mode the address and data lines of the microcontroller are driven to a low state, and so will not be affected by external logic.

Occasionally a design may require the connection of battery-backed signals to logic that will be unpowered during data retention mode. This is often the case if external decode logic is used to bank switch memory devices. In such instances an analog switch such as a 74HC4053 can be used to isolate the signals. Examples of this are contained in Application Note 92: DS5002FP Memory Expansion Techniques.