

Application Note

Wireless Modem Troubleshooting Guide

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Introduction

CML Microcircuits manufactures several different integrated circuits for wireless data applications. Wireless modem designs are typically wrought with many potential technical pitfalls, some of which repeat themselves time and time again. Items such as RF carrier detection, receiver training and frequency response are areas where designers commonly encounter problems.

The purpose of this application note is to provide a systematic method for troubleshooting wireless modem designs, from the perspective of the CML Microcircuits' modem IC. Hardware problems commonly encountered in wireless designs with CML products will be discussed. Detailed treatment of RF and microcontroller issues is beyond the scope of this application note and will not be covered.

NOTE: devices listed in this application note may have the following prefixes:

- "FX" – manufactured by CML Microcircuits (UK)
 - "MX" – manufactured by CML Microcircuits (USA)
 - "CMX" – manufactured in both UK and USA locations of CML Microcircuits
- Unless otherwise stated, parts with an "FX" prefix are electrically identical to those with a "MX" prefix.

For specific applications assistance, please contact the CML Applications Engineering department at: techsupport@cmlmicro.com

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Overview Of CML Wireless Modems

CML Microcircuits is a leader in the narrowband wireless data market with ICs designed for a wide range of wireless data applications:

Part Number	Modulation Scheme	Data Rates Supported	Features	Typical Radio Connection Point	Typical Applications
MX/FX429A	MSK	1200bps – 2400bps	FDX, parallel μ C interface, compatible with MPT1327	Audio path	Professional Trunked Radios
CMX469A	MSK	1200bps – 4800bps	FDX, clock recovery, carrier detection	Audio path	General Purpose
CMX589A	GMSK	4kbps – 200kbps	FDX, selectable BT	Modulator discriminator	General Purpose
CMX909B	GMSK	4kbps – 38.4kbps	HDX, FEC, CRC, interleaving, scrambling, MOBITEX data framing	Modulator discriminator	MOBITEX modems
MX/FX919B	4L-FSK	4.8kbps – 19.2kbps	HDX, RRC filtering, FEC, CRC, interleaving, scrambling, generic data framing	Modulator discriminator	General Purpose
MX/FX929B	4L-FSK	4.8kbps – 19.2kbps	HDX, RRC filtering, FEC, CRC, interleaving, scrambling, RD-LAP data framing	Modulator discriminator	RD-LAP modems
CMX881	MSK	1200bps-2400bps	Interleaving, FEC, CRC, data scrambling	Audio path	Professional Trunked Radios
CMX882	MSK	1200bps-2400bps	Interleaving, FEC, CRC, data scrambling	Audio path	Leisure radios
CMX969	2L and 4L-FSK	4.8kbps and 19.2kbps	HDX, RRC filtering, FEC, CRC, interleaving, scrambling, MOTIENT and MDC4800 data framing	Modulator discriminator	MOTIENT modems
CMX989	GMSK	19.2kbps	Reed-Solomon encode/decode/error correction, CDPD data framing	Modulator discriminator	CDPD modems

Table 1 - CML Wireless Data Products

Abbreviations used in this table:

- MSK - Minimum shift keying
- GMSK - Gaussian pre-filtered minimum shift keying
- 4L-FSK - Four level frequency shift keying
- 2L-FSK - Two level frequency shift keying
- CDPD - Cellular Digital Packet Data
- HDX - Half Duplex
- FDX - Full Duplex
- BT - Bit Rate Bandwidth
- RRC - Root Raised Cosine
- FEC - Forward Error Correction
- CRC - Cyclic Redundancy Check
- BER - Bit Error Rate

CML Wireless Modem Operation

MSK products utilize 'mark' and 'space' frequencies that fall within voice band frequencies (e.g. 300Hz to 3300Hz), so these modems can yield good results when connected to the audio path of a typical voice-grade radio. GMSK and 4L-FSK products must be connected to the radio's modulator and discriminator; they cannot be connected to the radio's audio path. (Note: MSK modem operation at 4800bps utilizes a 'space' frequency of 4800Hz that precludes operation with a radio's audio path; thus, modulator/discriminator access is required for MSK operation at 4800bps.)

In general, MSK modems can be successfully used with low cost 'voice-grade' radios. The higher data rates and specific RF requirements of GMSK and 4L-FSK modems dictate that those applications use higher performance radios than those typically encountered in MSK systems.

Phase noise (e.g. inaccuracy in local oscillator output frequency) can blur the 'decision points' of received digital signals and degrade the received bit error rate (BER). Since GMSK and 4L-FSK modulation schemes directly process digital signals, the radios used with these types of modulations should have local oscillators with low phase noise and precise frequency tolerance (to minimize frequency drift).

GMSK and 4L-FSK are both constant amplitude modulation schemes (carrier amplitude is constant), and this means that power-efficient Class C amplifiers can be used in these types of designs.

Frequency Response

Good low frequency response is critical for GMSK and 4L-FSK modulation schemes. Two areas of circuit design play a large role in this issue:

1. Analogue signal coupling to/from the modem.
2. Phase-locked loop (PLL) based frequency synthesizer.

Ideally, the modem transmit output should be directly coupled to the frequency modulator. In situations where AC coupling must be used, the capacitor value should be chosen so that the high-pass 'rolloff' of the coupling is as low as possible. This will allow more low frequency content of the data signal to pass through the system, and this will enhance the received bit error rate (BER). A rule of thumb for the Tx coupling rolloff frequency is a maximum of 5Hz.

The connection between the radio discriminator and the modem receive input should also be directly coupled if possible. In situations where AC coupling must be used, the capacitor value should be chosen so that the high-pass 'rolloff' is as low as possible. A maximum of 20Hz for the receive coupling roll-off frequency is a good rule of thumb.

Another problem that results from AC coupling is the presence of a step voltage at the discriminator output when the remote transmitter turns on or changes its channel. AC coupling will transform this step voltage into a slowly decaying pulse that is presented to the modem's receive input, and this pulse can confuse the receive circuitry of the modem.

Under normal operation with a coupling capacitor, the data signal will be passed through the coupling capacitor and presented to the CML modem RX input centered around a " V_{bias} " voltage level ($V_{dd}/2$). The CML modem will monitor the excursions of the data signal and use this information to derive optimum DC level "decision thresholds" for the level measuring and clock extraction circuits. The level acquisition and clock extraction circuits work optimally when the data waveform is centered around V_{bias} .

When a DC voltage step is applied to the coupling capacitor, the superimposed AC data signal will follow the decaying pulse until the signal has settled around V_{bias} . The level measuring and clock extraction circuits will be presented with constantly changing signal excursions while the step voltage decays, and this will cause unreliable DC levels to be used for decision thresholds. This will confuse the level measuring and clock extraction circuits and prevent proper "training" from happening.

The time required for this pulse to decay to 37% of its peak value is equal to one 'RC time constant'. Consequently, the coupling components should be selected to minimize this 'RC time-constant' period as much as possible. **The receiver training sequence should not be started until the time required for the step voltage pulse to decay has passed.**

A tradeoff exists when AC coupling is used between the discriminator output and the CML modem. The level acquisition and clock extraction circuits work optimally when the data waveform is centered around V_{bias} . Any voltage step from the discriminator should decay as fast as possible, and this is accomplished by reducing the value of the coupling capacitance.

Unfortunately, the improvement in the discriminator voltage decay rate comes at the expense of greater attenuation of low frequency energy in the data signal; the decrease in coupling capacitance causes an increase in the rolloff frequency of the coupling's high-pass response. This, in turn, will produce degradation in the received BER. Experimentation is required to optimize a particular application.

Phase-locked loop (PLL) based frequency synthesizers present another obstacle to good low frequency response. In applications that use PLL synthesizers, the data signal is injected into the voltage-controlled oscillator (VCO) in a standard 'voice-radio' fashion. This technique works well for voice, but data signals can have considerable energy below 300Hz, and the high-pass frequency response of the PLL can significantly attenuate this low frequency content. One way around this problem is to inject the data signal into a second point in the PLL outside of its feedback loop. A common way to do this is to inject the data signal into the reference oscillator, thereby 'pulling' its frequency slightly. This 'two-point modulation' technique introduces a low-pass frequency response that, when combined with the high-pass response of the VCO injection technique, results in a flatter frequency response across the band of interest. More information on two-point modulation can be found at: http://www.cmlmicro.com/products/applications/two_point_modulation_r1.pdf.

Frequency Response Measurement

As previously mentioned, the frequency response of the Tx-Rx link is of critical importance in wireless designs, and the frequency response of the Tx-Rx link can be easily determined through a simple test.

- Insert a signal generator (SG) at the Tx pin of 'Modem 1' (e.g. lift CML Tx output pin from board and connect SG to other side of broken connection).
- Choose a very low starting frequency (e.g. 5Hz) to represent the lowest expected frequency in the 'real' data signal.
- Set the DC level and peak-to-peak signal amplitude of the test signal to correspond to the expected Tx parameters of the CML device you are working with; see the respective data sheet for more information.
- Inject this signal into the Tx signal path and record the received signal amplitude at the "Modem 2" Rx input.
- Repeat these steps for all frequencies that are expected in the 'real' data signal (i.e. perform a frequency sweep).

Duplicate this testing in the other direction (i.e. from Modem 2-Tx to Modem 1-Rx) and compare the responses. The frequency response in the passband should

(ideally) be flat and is dependent on the data rate and degree/type of filtering applied to the signal.

Distinct differences between these two frequency response plots indicate a problem in one or both sides of the link.

Phase Distortion

Phase distortion is a phenomenon where different frequency components of a signal are subjected to varying amounts of phase shift (e.g. time delay) prior to reception. Phase distortion often causes poor bit-error-rates (BER) in wireless data systems.

Two common causes of phase distortion are:

1. Shifting of the received signal into the edges of the intermediate frequency (IF) filter
2. Inappropriately selected low-pass rolloff frequency for the components external to the CML modem.

The required receiver IF filter bandwidth is determined by several factors, including the data rate, carrier deviation, modulator linearity, and accuracy of the Tx and Rx reference oscillators. The edges of the IF filter can introduce significant phase distortion into the received signal, causing the components of the data signal to arrive at the IF filter output at different times. This signal distortion will confuse the data detection circuitry and thus create a detrimental effect on BER. Consequently, the IF filter bandwidth should be wide enough to accommodate the expected variations in signal bandwidth without allowing the signal to run into the edges of the IF filter. The phase response of the IF filter should be linear in its passband.

The overall frequency response of the transmitter-channel-receiver system will approach that of a low-pass filter, and to varying degrees, the rolloff frequency of this response is adjustable. Attenuation of high frequency energy above that contained in the data signal is desirable, while attenuation of lower frequency energy in the data signal is very undesirable.

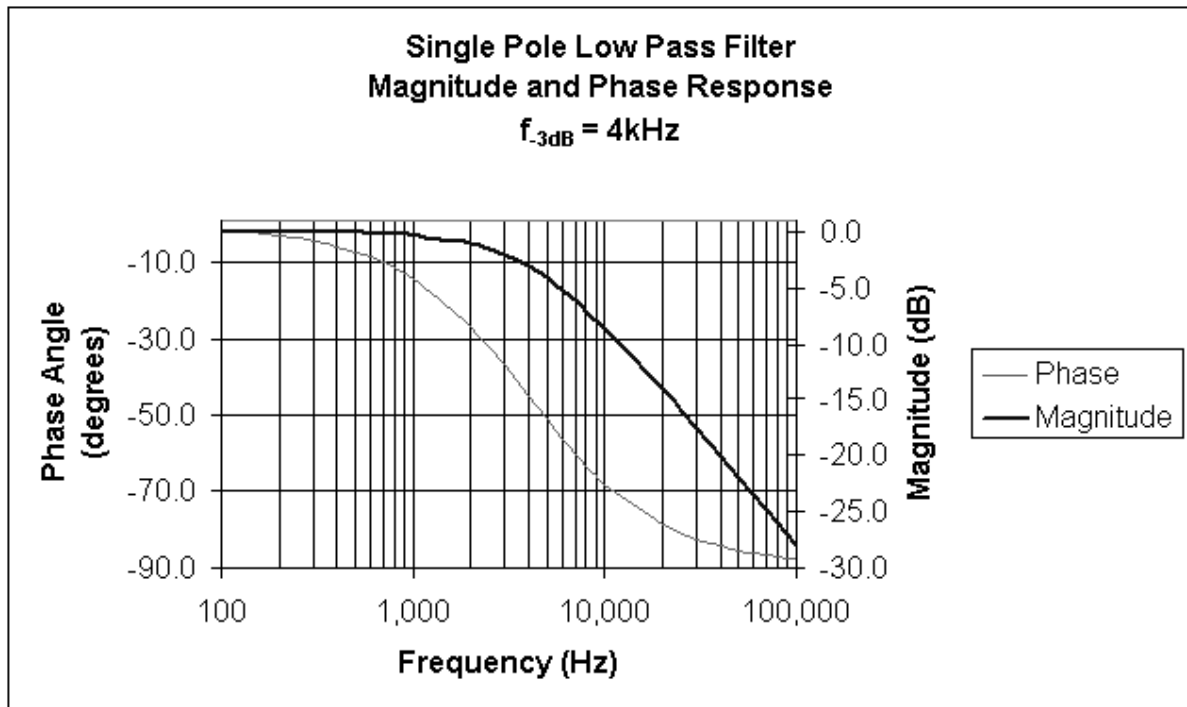
(NOTE: The following explanation utilizes simple approximations to a single-pole low-pass filter system. Phase and magnitude responses in a real system will vary significantly from those illustrated in this example. The reader is cautioned to perform testing to ensure that their design meets intended targets.)

As an example, consider the following scenario:

GMSK with $BT=0.3$
Data rate = 8000bps

The highest fundamental energy component present in this baseband data signal will result from a 1010... pattern. At an 8kbps data rate, the highest fundamental frequency component of this data signal will therefore be 4kHz. An initial assumption could be to manipulate the system components to achieve a low-pass filter "rolloff" frequency of 4kHz, as this will result in passthrough of energy up to 4kHz, with attenuation of all content beyond 4kHz in frequency. This is not necessarily a wise

choice, however, because the system's phase response has not yet been considered.



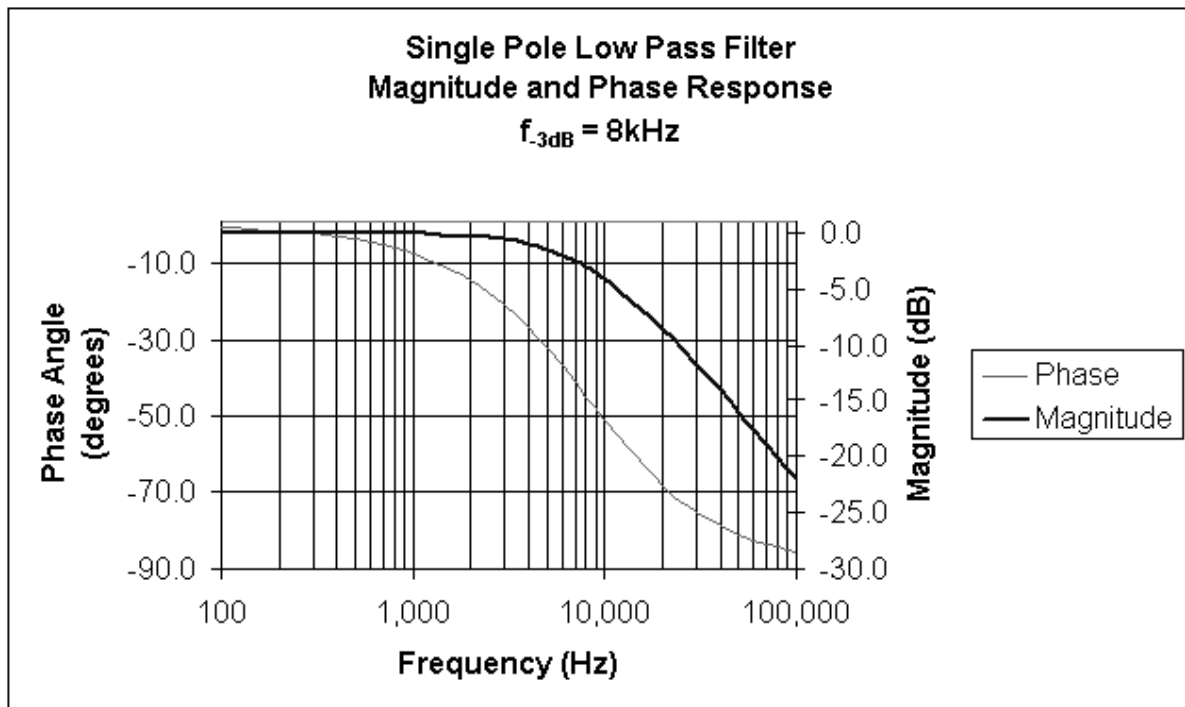
The magnitude response may “break over” at the “3dB rolloff” point, but the phase response has already started to change one decade **below** the 3dB rolloff point. The 4kHz component of the data signal has undergone a 45° phase change.

When compared to a data signal component of 400Hz:

Data Signal Component	Phase Change (degrees)	Time Shift (μs)	Percentage of Bit Time
400Hz	5.7	2.0	1.6%
4kHz	45.0	15.6	12.5%

A good rule of thumb is to keep phase distortion (e.g. time shift) below 10% of a bit time in the passband, so the use of $f_{-3dB}=4\text{kHz}$ violates this guideline.

A more reasonable approach would be to place the 3dB rolloff frequency at 8kHz:



With $f_{3dB}=8\text{kHz}$, the 4kHz signal component phase distortion has improved significantly:

Data Signal Component	Phase Change (degrees)	Time Shift (μs)	Percentage of Bit Time
400Hz	2.9	1.0	0.8%
4kHz	26.6	9.2	7.4%

The higher rolloff frequency provides better phase response than the lower rolloff frequency. As in all aspects of engineering, a tradeoff exists when manipulating the frequency response of the system; improved phase response comes at the expense of additional high frequency energy being allowed into the receiver circuitry.

This example revolved around the use of an extremely simple single-pole low-pass filter; any realistic communication system will have magnitude and phase behavior markedly different from the behaviors illustrated in this example. While this example was based on a crude model, the intention was to demonstrate the impact that phase distortion can have on a system, and to show that both magnitude and phase response need to be considered in the overall system design.

Phase Distortion Detection – Eye Diagrams

Eye diagrams are an effective way to quickly identify the presence of phase distortion in the data signal. An eye diagram is an oscilloscope trace of the baseband signal, taken either at the input to the RF modulator or at the output of the discriminator. The recording of a random data pattern over several bit/symbol times forms the classic eye pattern.

A two-channel analog oscilloscope or digital oscilloscopes with “persistence” adjustments should be used for eye diagram testing. In general, one channel of the oscilloscope should be connected to the signal of interest, such as the Rx input. The other oscilloscope channel should be used for triggering and should ideally be placed on the transmitting modem /IRQ (or bit clock) pin.

The objective is to trigger the oscilloscope display when a new byte/bit has been either transmitted or received. This will allow the triggering to be synchronized with the completion of each transmitted data bit (or byte, depending on the device and trigger location chosen). If this triggering location is not practical, use the receiving modem /IRQ (or bit clock) signal for triggering. Either edge of the /IRQ signal can be used for triggering, but the ‘high-low’ /IRQ transition will yield slightly better results. The oscilloscope timebase should be set to allow about three symbol times to be displayed on the screen. The data stream used for this testing should have a reasonably random structure.

Cleanliness, amplitude and symmetry of the eye opening are key points to look for in an eye diagram. The height of the eye reflects the amount of noise that is present (e.g. more noise, shorter eye), while the width of the eye refers to the amount of jitter in the signal (e.g. more jitter, narrower eye). Typical ‘good’ eye diagrams for different degrees of transmit filtering are provided below (Gaussian filtering used in these examples). The signal illustrated in the BT=0.3 example has received greater high frequency attenuation (low-pass filter cutoff frequency = 0.3 x bit rate) which causes its pulses to be more spread out in the time domain, thus the inner eye opening is reduced in size:

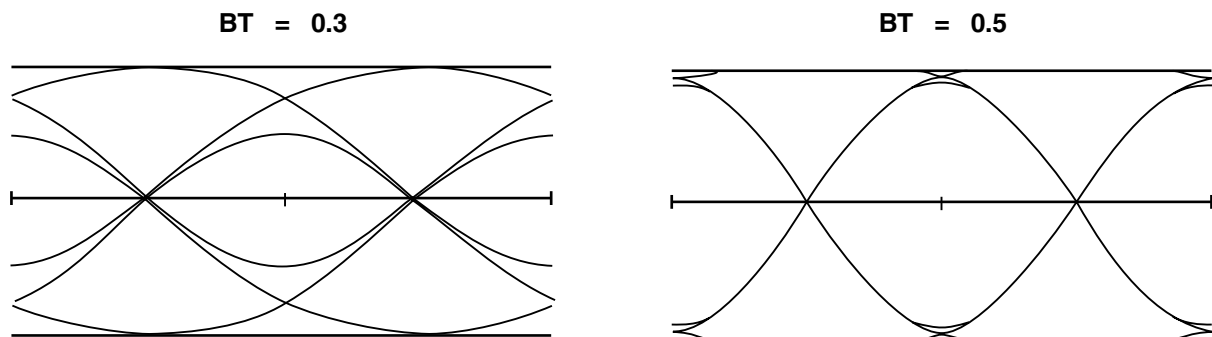


Figure 1: ‘Good’ Eye Patterns with GMSK Modulation

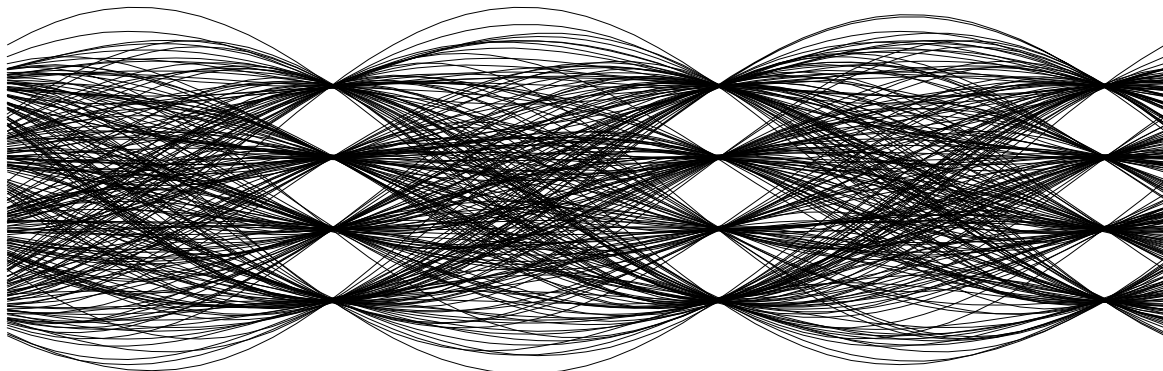


Figure 2: ‘Good’ Eye Pattern with 4L-FSK Modulation

If it is determined that the BER is suffering because of phase distortion, remove all RF-related circuitry and properly connect the Tx path of Modem 1 to the Rx path of Modem 2, and vice versa for the opposite direction. Establish a “baseline” of operation with this modem-to-modem connection and ensure that the eye diagrams and frequency response plots are acceptable. Once this is done, incrementally add RF circuitry back into the data path. Repeat eye diagram and frequency response measurements after each RF circuitry block is added to ensure that the added circuitry is not causing problems. This approach will indicate the portions of the circuit that are problematic from a phase distortion standpoint, and the circuit can be modified accordingly.

CML wireless modems provide different connection points and/or specific register settings in order for the eye diagrams to be viewed. Please review the relevant CML data sheet for specific information on eye diagram measurements, and for further assistance, please contact the CML Applications Engineering department at techsupport@cmlmicro.com

TX Output Pin Loading

CML wireless modems that use GMSK and 4L-FSK modulations have “TX Output” pins that require an external single pole RC filter. This external filter forms an important part of the transmit signal filtering and must be included in the design. With the exception of this single pole RC filter, the Tx Output pin should not be loaded.

Resistive loading of the Tx Output pin can cause DC level shifts (e.g. V_{bias} shifts) when switching between operating modes, and this can result in undesirable shifts in the transmitted carrier frequency. Optimal performance will be achieved when the output of the external RC filter is buffered prior to further signal processing or delivery to the frequency modulator.

V_{bias} Pin Loading

Another frequent cause for DC level shifts in the modem’s transmitted signal are fluctuations in the ‘ V_{bias} ’ signal. The V_{bias} voltage for CML’s wireless modems is developed by a low power internal circuit, and this voltage will shift if the V_{bias} pin is loaded. Since the Tx output driver is referenced to V_{bias} , this can then cause a shift in the DC level of the transmitted signal. Therefore, to minimize DC shifts in the transmitted signal, the V_{bias} voltage should be externally buffered before it is used as a reference voltage elsewhere in the circuit.

Transmit Operation

Device Configuration

Most CML modem ICs must be reset upon power-up to ensure that the device is in a known state before operation is started. Once the device has been reset and its registers are in a known condition (where applicable), the modem IC must be configured for transmit operation.

Data Formatting

CML Microcircuits' wireless modem ICs are synchronous data devices. In order to correctly interpret a received data stream, a synchronous modem must know two things: (1) when to sample the incoming signal and (2) what the expected signal levels are. This information is critical in the determination of what is a 'one' and what is a 'zero'.

A synchronous modem 'learns' the timing and level of the received signal by examining a special data pattern called a 'preamble' sequence. The preamble pattern (e.g. 101010...) conditions the receiver circuits to the zero-crossings and received signal levels so that it can make intelligent decisions regarding the imminent data stream. (Note that the particular preamble pattern for your CML modem may be different than the 101010... pattern mentioned above; consult the CML data sheet for more information.)

The preamble must be added to the front of the transmitted data packet. The length and pattern of the preamble will depend on the device being used and on whether or not the receiver uses RF carrier detection to initiate its training sequence.

Since the first few bits of preamble may have been missed during carrier acquisition, the receiver must "know" when the preamble has ended and the data packet has begun. A 'sync word' is typically appended after the preamble to alert the recipient that the preamble has ended and the data packet is about to begin. The length and pattern of the sync word depends on the device being used and the standard, if any, that defines the system specification. Sync word selection, if permitted, must be performed carefully as it can have a significant effect on system performance.

Once the preamble and sync word have been transmitted, the actual data is then transmitted over the link. Data formatting options are available in some CML products, such as:

- Interleaving can be performed to improve the tolerance of the data stream to 'burst errors'.
- Scrambling can be performed to improve the resistance of the data stream to repetitive pattern biasing (i.e. long strings of 1 or 0 may cause received DC levels to shift).
- Error correction information may be appended to the data to help detect (CRC) and correct (FEC) errors at the receiver, thereby improving the bit error rate (BER).

- Further data formatting (e.g. arranging data into blocks and frames) can be performed, depending on the selected CML device and the defining standard/protocol.

Depending on the data format or protocol being used, a 'hang byte' may be appended to the end of the transmitted packet.

Upon the completion of the data transmission, the RF carrier is dropped and the transmitting device can be placed in a 'sleep' mode to conserve battery power.

Receive Operation

Device Configuration

Most CML modem ICs must be reset upon power-up to ensure that the device is in a known state before operation is started. Once the device has been reset and its registers are in a known condition (where applicable), the modem IC must be configured for receive operation.

MSK modems do not require amplitude information in order to make a decision regarding ones and zeros; zero-crossings alone contain sufficient information to allow interpretation of the received data stream. GMSK and 4L-FSK modems, however, require both amplitude and timing information to enable interpretation of the received data stream. Consequently, the following sections on training sequences deal with GMSK and 4L-FSK modems.

Operation with RF Carrier Detection

The receiving device must 'learn' the timing and amplitude of the incoming signal before it can reliably distinguish between a 'one' and a 'zero'. The preamble portion of the data signal is used to provide this information to the receiver.

In an optimized system, the training sequence will begin very shortly after RF carrier has been detected. The radio's received signal strength indicator (RSSI) or the received S/N indication of the CML modem could be used for this carrier detection, but the response times of these options may be too slow for desired operation.

One possible option for rapid carrier detection is a simple zero-crossing detector. "Hash" will come out of the discriminator when the carrier is not present and zero crossings will happen constantly. The time between zero-crossings can be measured and used to qualify the signal as preamble (e.g. relatively long time between zero crossings indicates preamble is present). Another approach involves configuring the carrier detect circuit to provide its indication only after a certain amount of inactivity. Constant noise and/or zero-crossings would prevent additional

indications, and the lack of indications would tell you that “hash” (and not preamble) is being presented to the modem.

The term hash has been used to describe the Wideband noise present at the discriminator output when no RF carrier is being received.

Once the carrier has been detected, the modem should be configured to train on the preamble. Some CML products provide a facility for an automatic training sequence. Once this feature is activated, the modem automatically adjusts its clock extraction and level acquisition circuits to their most aggressive setting to achieve signal lock in as few bit times as possible. These settings are then automatically relaxed over time as the modem obtains lock on the incoming signal. After enough time has transpired to assure proper timing and level acquisition, the clock extraction and level acquisition circuits are placed in their ‘residual’ settings.

The CMX589A also provides a means for rapid signal training by ‘manually’ strobing device pins at prescribed times. Specific details on CMX589A signal training can be found in its data sheet:

<http://www.cmlmicro.com/products/datasheets/Docs/cmx589ad.pdf>.

After the training sequence is complete, the remainder of the data stream can be reliably processed. Once the data has been received and no retransmission is required, the receiver can be placed in its sleep mode to conserve power.

Operation Without RF Carrier Detection

For systems without RF carrier detection, the receiving modem has no prior knowledge regarding when the preamble sequence will be received. Consequently, it is difficult to know exactly when the training sequence should be initiated.

Another problem; since there will be a large signal transition when the discriminator output changes from ‘hash’ to ‘quiet carrier’ and then to preamble, the modem level and timing acquisition circuits will have to recover from this in order to successfully train on the preamble signal.

These problems require that systems without RF carrier detection use a much longer preamble sequence to increase the likelihood that signal training is successful. Other solutions can be achieved by using data timeslots, these are usually system specific and still require the receiver to latch onto the system timing albeit usually over an extended time period.

Troubleshooting A Problem

The wireless modem design difficulties typically encountered by CML customers are due to firmware and hardware problems. Hardware problems are the focus of this application note. Since the firmware is a function of the microcontroller, development environment and programming language chosen, a detailed treatment of firmware issues is beyond the scope of this application note.

The EV9000 is an invaluable troubleshooting tool for projects utilizing one of the 9x9 series of CML wireless modem devices. The EV9000 allows modem-to-modem testing with radios for realistic BER tests, and this type of testing can significantly reduce design time and enhance time-to-market.

Wireless modem testing should start with direct-wired connections between modems, regardless of whether the final product will use a wired or wireless connection. (NOTE: RF circuitry should only be added AFTER the wired testing has been successfully completed.) Simple data packets, such as “all preamble”, should be used for the initial testing at each stage to minimize complexity and enhance the likelihood of success.

An effective initial test setup involves two CML wireless modem ICs connected ‘back to back’, with the transmit output of one connected to the receive input of the other. In this scenario, a known data packet is transmitted from one modem to the other, and the received data is then transmitted back to the originating modem (i.e. data echoing).

The most commonly encountered problem with wireless modem designs involves the proper timing of receiver training initiation (i.e. when to make the receiving modem IC begin its training sequence).

The key to troubleshooting a problem in a wireless data system is to determine where the fault lies: the transmit side or the receive side. Once that determination has been made, focused efforts to determine the root cause of the problem can be performed.

Some commonly encountered hardware and firmware problems are listed below:

Hardware Problems

- 1) No RF Carrier Detection used to initiate receiver training.
- 2) External circuitry inadvertently causing excessive phase distortion in passband.
- 3) RF circuitry of inadequate quality for desired modulation scheme (e.g. using voice radio for 4L-FSK).
- 4) Transmitting RF circuitry inverts the data signal and the receiving device fails to invert signal to restore original polarity.
- 5) Chip Select line left floating.
- 6) Excessive loading of Tx Output pin.
- 7) Excessive loading of V_{bias} pin causing DC level shift elsewhere in device.
- 8) Bad solder connections of DOC caps introduce noise into circuit.
- 9) Insufficient cleaning/removal of flux around DOC cap connections.
- 10) Inadequate low frequency performance (either by not performing 2-pt modulation or by improper AC coupling of the signal).
- 11) DOC capacitors, Rx input filter capacitor, and/or Tx output filter capacitor of wrong value.
- 12) Microcontroller port not correctly configured for read of CML device.
- 13) Poor power supply conditioning.
- 14) Inadequate crystal stability.
- 15) Breadboarded circuits used for testing instead of PCB.

Firmware Problems

- 1) Preamble and/or sync word not correct (e.g. wrong values loaded for transmission or reception).
- 2) Preamble and/or sync word not consistent between Tx and Rx.
- 3) Preamble not extended when RF carrier detection is not used.
- 4) Preamble not correct for chosen BT (applies only to GMSK devices).
- 5) Microcontroller port not correctly configured for read of CML device.
- 6) Firmware 'state machine' enters infinite loop and can't escape.

The following troubleshooting flow chart is based on the scenario previously mentioned above: two modems connected back-to-back with wires. Troubleshooting typically begins when the data packet transmitted from Modem 1 is not correctly received when 'echoed' from Modem 2. This flow chart is intended to help the reader locate the problem area in this testing scenario.

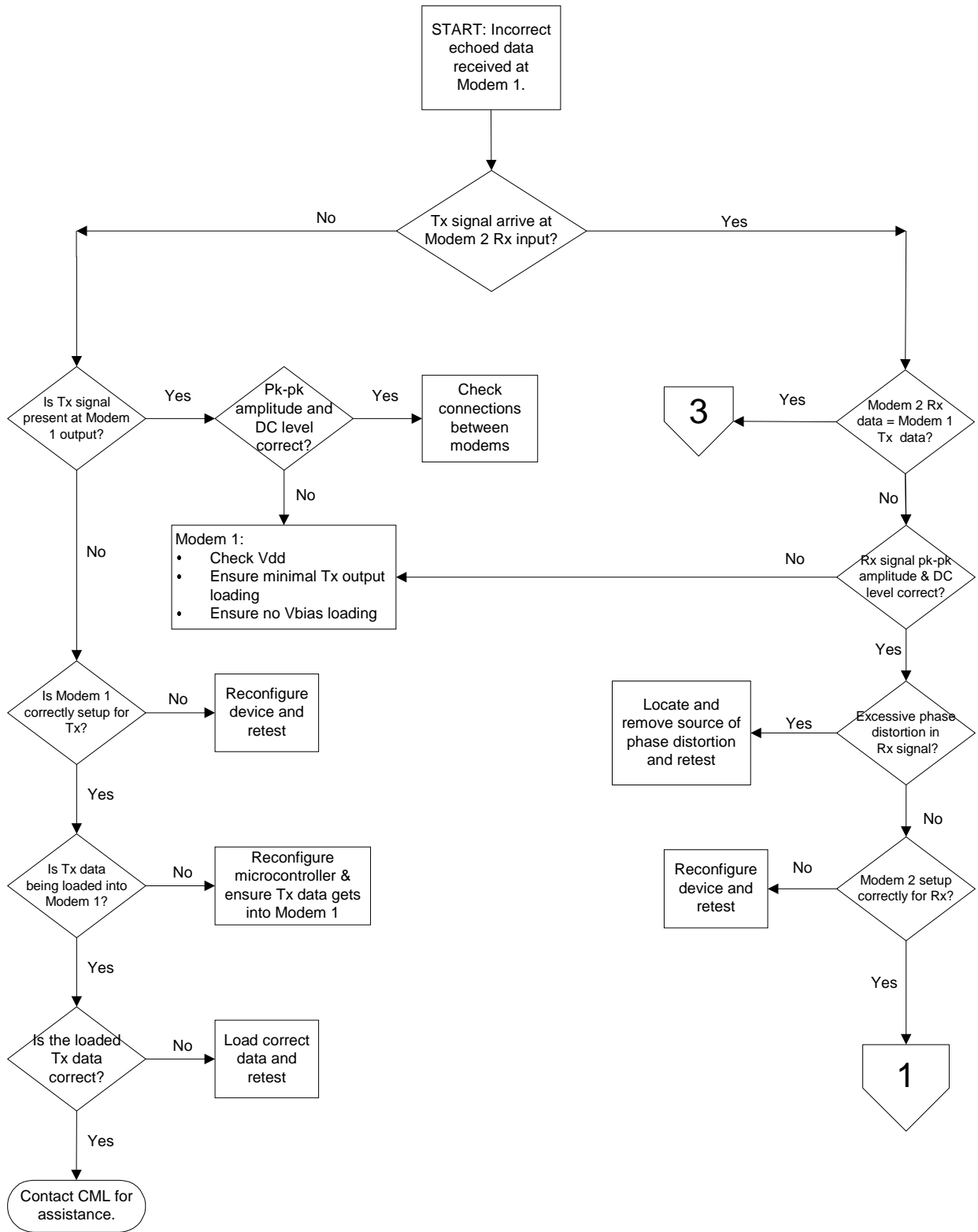


Figure 5: Initial Troubleshooting Flow Diagram

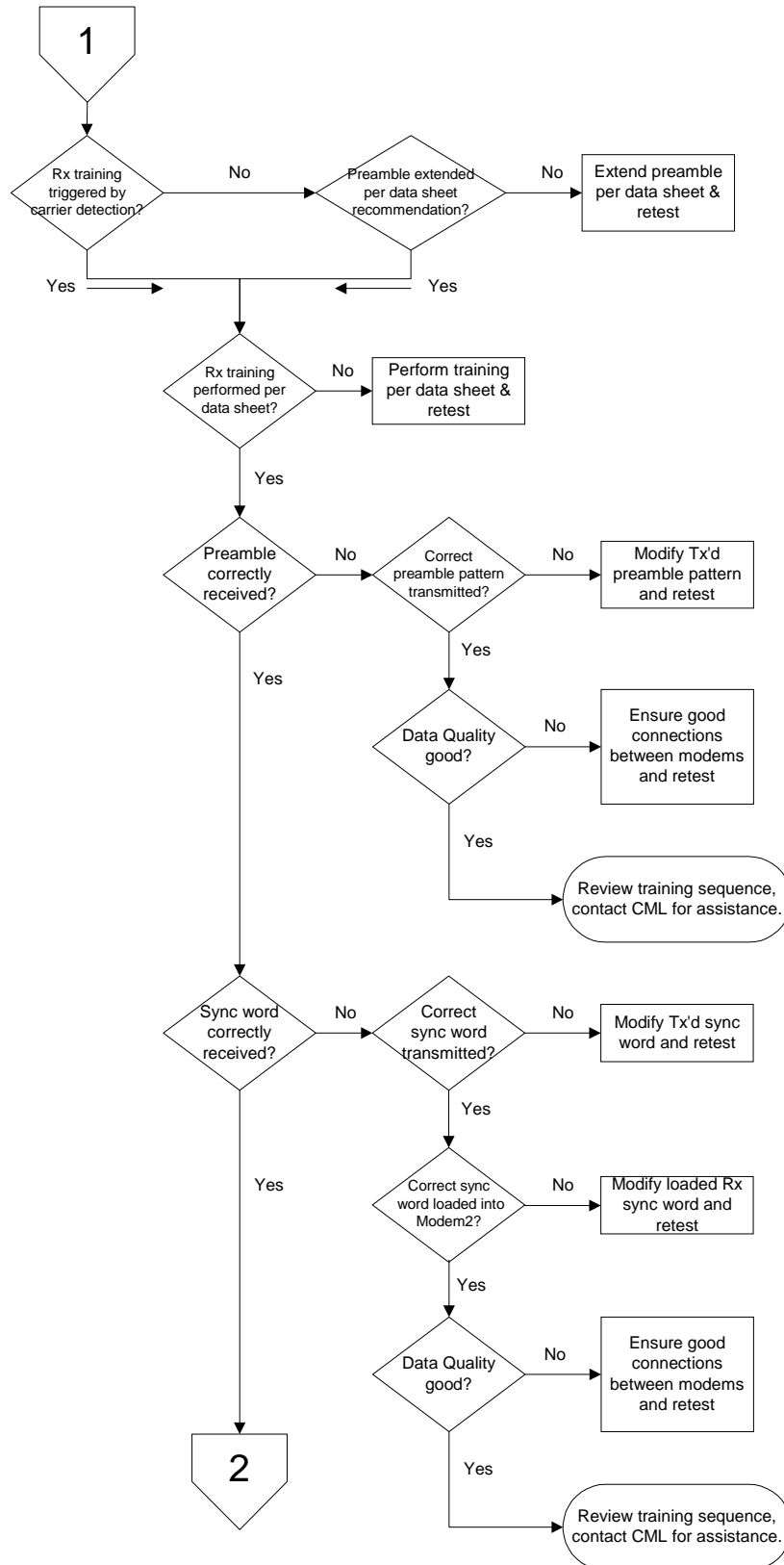


Figure 5: Initial Troubleshooting Flow Diagram (continued)

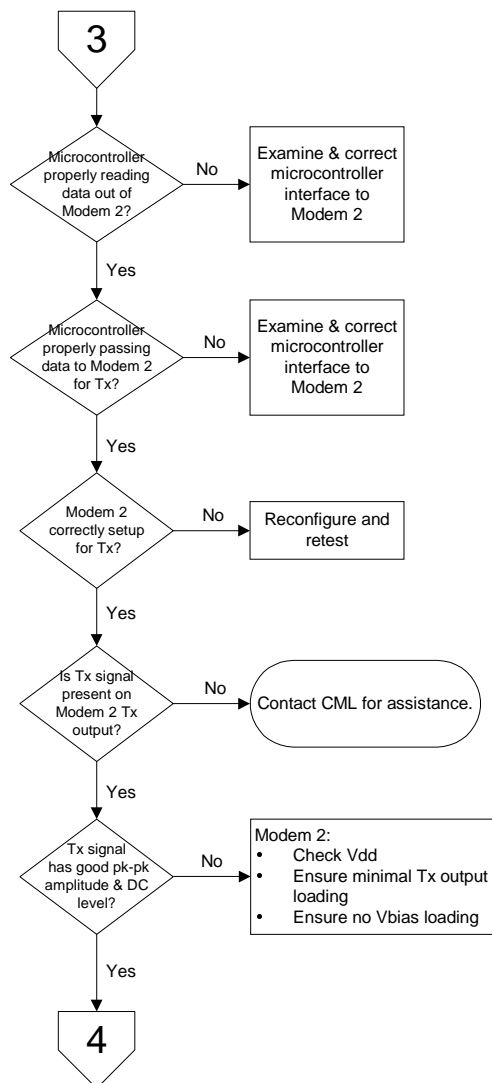
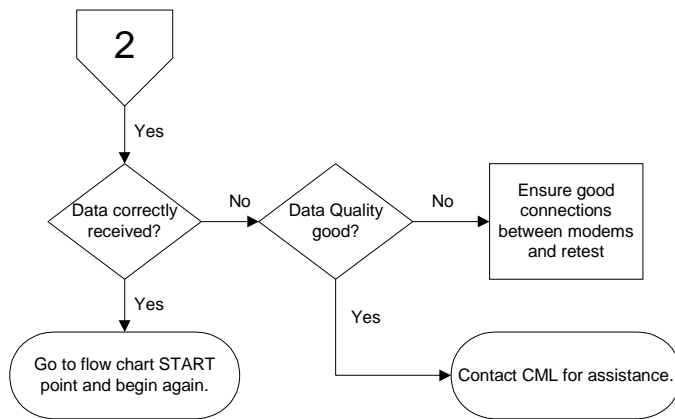


Figure 5: Initial Troubleshooting Flow Diagram (continued)

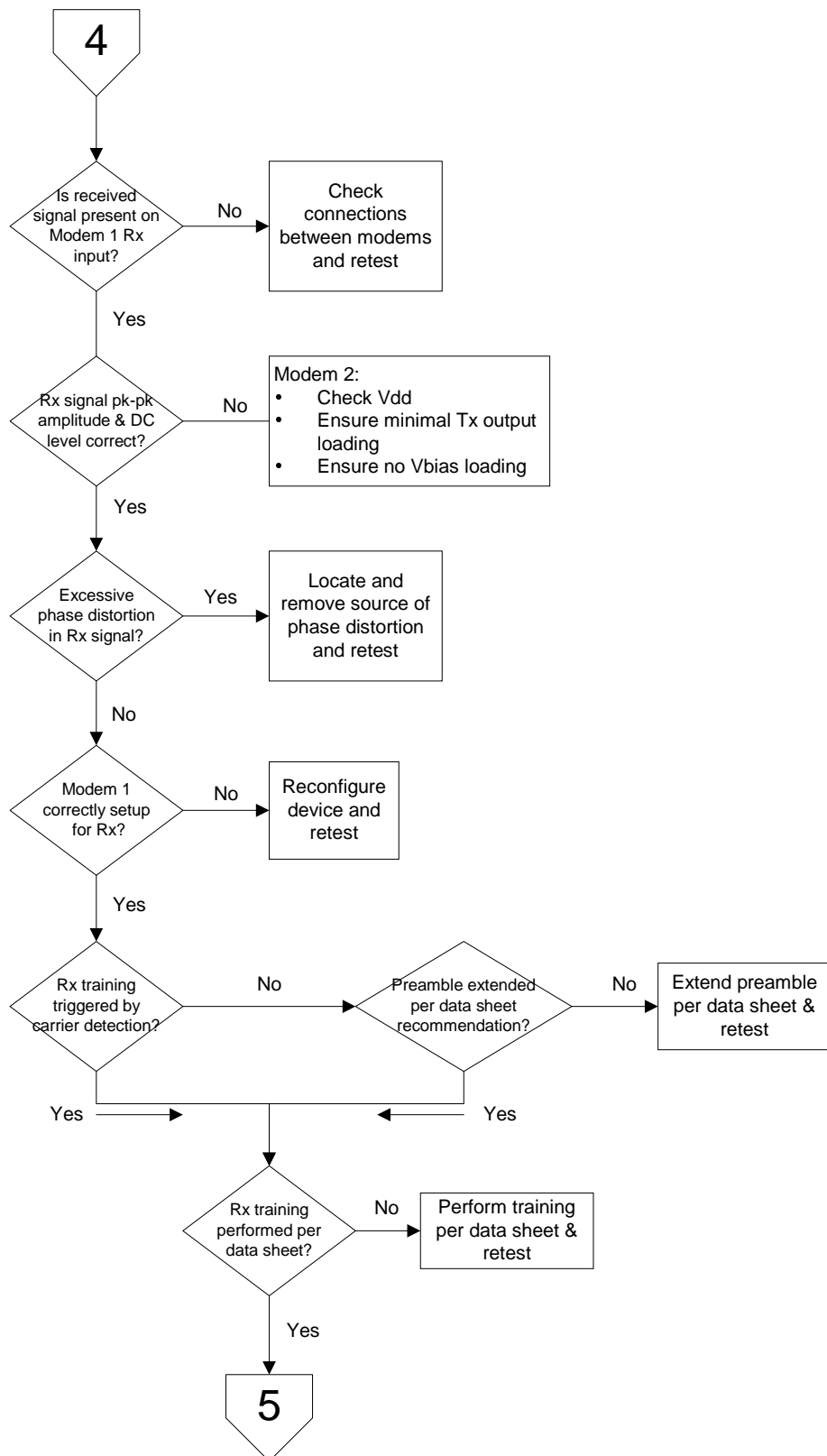


Figure 5: Initial Troubleshooting Flow Diagram (continued)

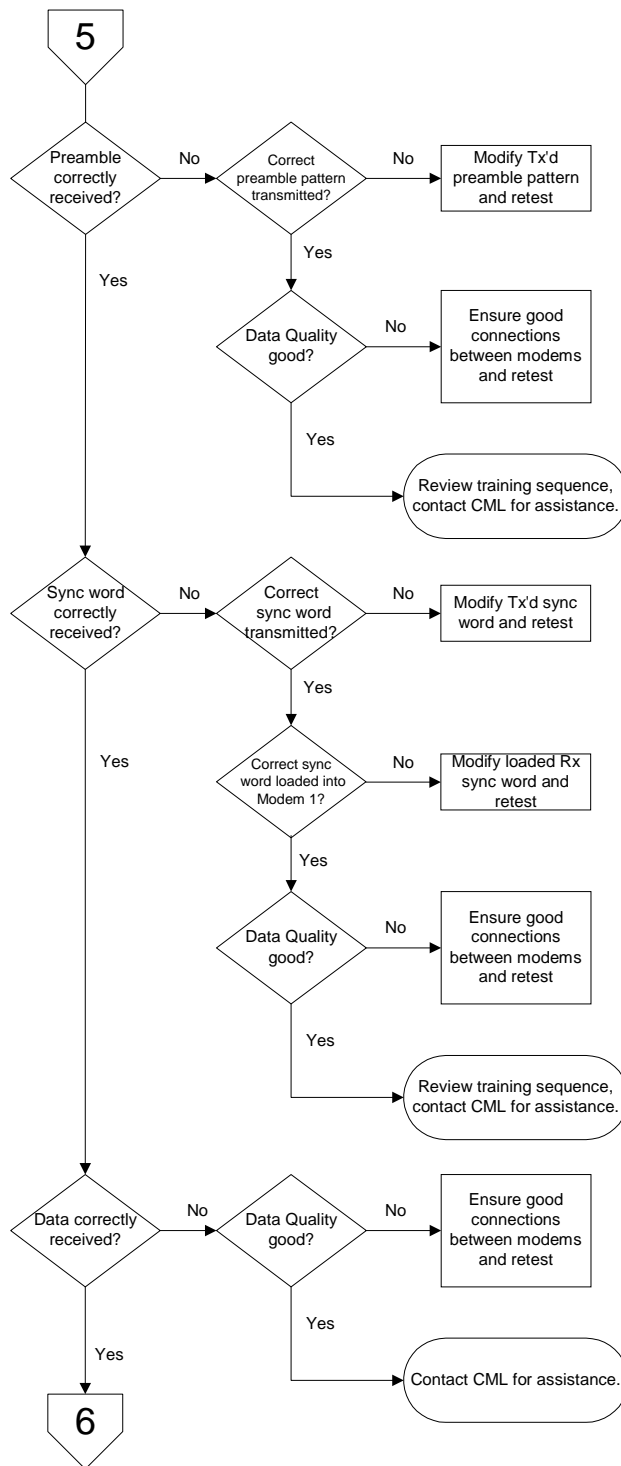


Figure 5: Initial Troubleshooting Flow Diagram (continued)

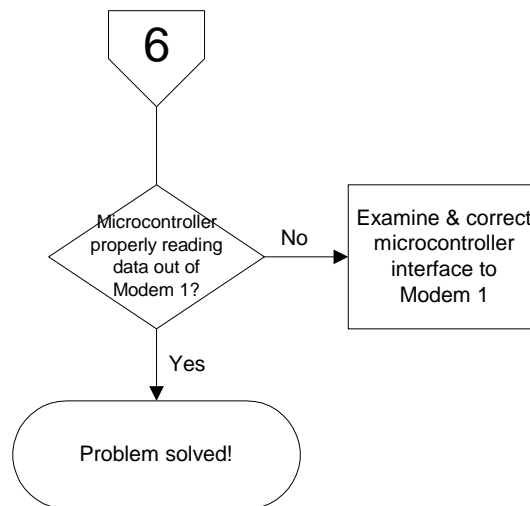


Figure 5: Initial Troubleshooting Flow Diagram (continued)

Conclusion

This paper introduced the portfolio of CML wireless data products and their typical application scenarios. Technical issues commonly encountered in designs with CML wireless modems were presented, and a plan for initial wireless modem troubleshooting was described.

It is hoped that the information in this document will assist the design engineer in designing with CML wireless data products.

References

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