

**GaAs MMIC SMT LOW DISTORTION T/R SWITCH DC - 2.5 GHz**

FEBRUARY 2001

v01.0700

## Features

HIGH THIRD ORDER INTERCEPT: +60 dBm

SINGLE POSITIVE SUPPLY: +3 TO +10V

HIGH RF POWER CAPABILITY

TTL/CMOS CONTROL

## General Description

The HMC154S8 is a low-cost SPDT switch in an 8-lead SOIC package for use in transmit-receive applications which require very low distortion at high signal power levels. The device can control signals from DC to 2.5 GHz and is especially suited for 900MHz and 1.8-2.2 GHz applications. The design provides exceptional intermodulation performance; providing a +60dBm third order intercept at 8 Volt bias. RF1 or RF2 is a reflective short when "Off". On-chip circuitry allows single positive supply operation at very low DC current with control inputs compatible with CMOS and most TTL logic families.



7

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### Guaranteed Performance, $V_{dd} = +5 V_{dc}$ , 50 Ohm System, -40 to +85 deg C

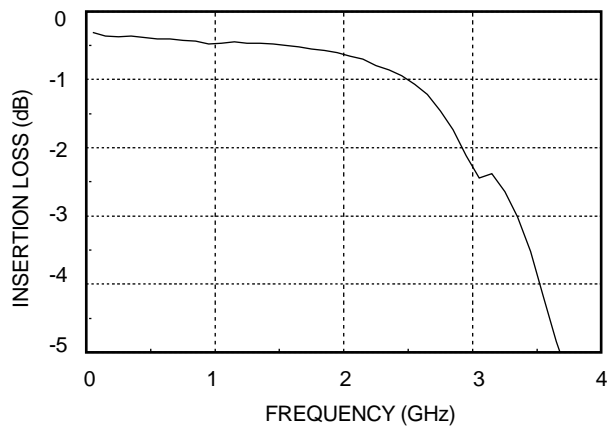
Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	DC - 1.0GHz		0.5	0.7	dB
	DC - 2.0GHz		0.7	0.9	dB
	DC - 2.5GHz		1.0	1.3	dB
Isolation	DC - 1.0GHz	22	25		dB
	DC - 2.0GHz	19	22		dB
	DC - 2.5GHz	15	18		dB
Return Loss	DC - 1.0GHz	20	30		dB
	DC - 2.0GHz	14	18		dB
	DC - 2.5GHz	10	13		dB
Input Power for 1dB Compression	0/8V Control				
	0.5 - 1.0GHz	35	39		dBm
	0.5 - 2.0GHz	34	38		dBm
Input Third Order Intercept	0/8V Control				
	0.5 - 1.0GHz	55	60		dBm
	0.5 - 2.0GHz	54	60		dBm
Switching Characteristics	DC - 2.5GHz				
		tRISE, tFALL (10/90% RF)	10		ns
	tON, tOFF (50% CTL to 10/90% RF)	24			ns

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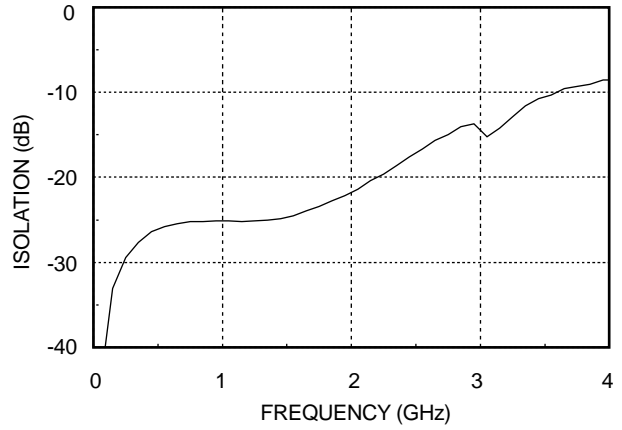
v01.0700

FEBRUARY 2001

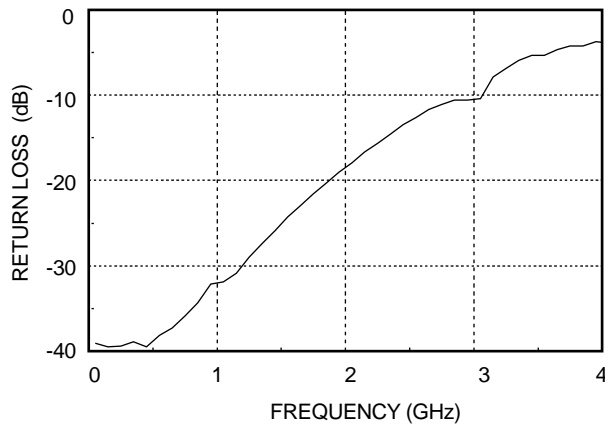
**Insertion Loss**



**Isolation**



**Return Loss**

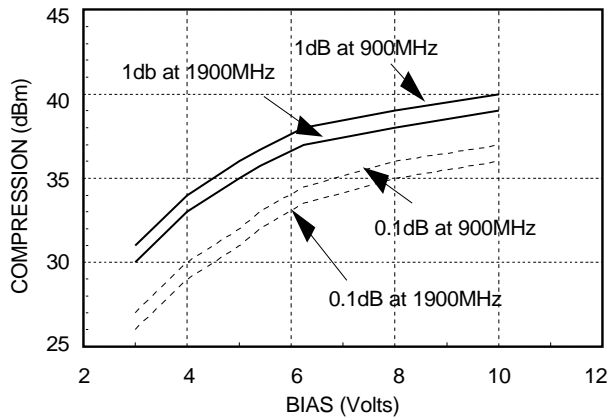


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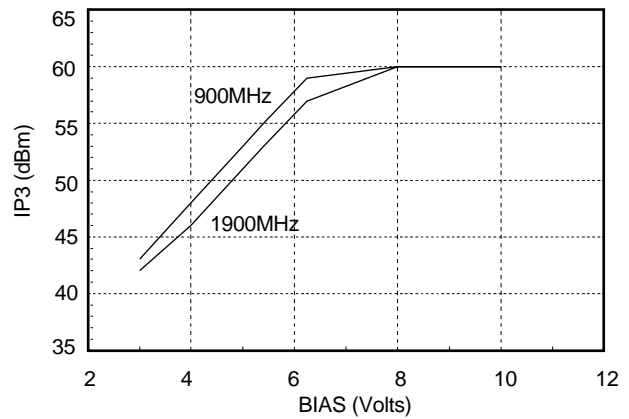
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v01.0700

**Input Power for 0.1 and 1.0 dB Compression vs Bias Voltage**



**Input Third Order Intercept vs Bias Voltage**



7

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**Compression vs Bias Voltage**

Bias Vdd (Volts)	Carrier at 900MHz		Carrier at 1900MHz	
	Input Power for 0.1dB Compression	Input Power for 1dB Compression	Input Power for 0.1dB Compression	Input Power for 1dB Compression
	(dBm)	(dBm)	(dBm)	(dBm)
3	27	31	26	30
4	30	34	29	33
5	32	36	31	35
8	36	39	35	38
10	37	40	36	39

**Distortion vs Bias Voltage**

Bias Vdd (Volts)	1 Watt Carrier at 900MHz			1 Watt Carrier at 1900MHz		
	Third Order Intercept	Second Order Intercept	Second Harmonic	Third Order Intercept	Second Order Intercept	Second Harmonic
	(dBm)	(dBm)	(dBc)	(dBm)	(dBm)	(dBc)
3	43	71	45	42	78	55
4	48	85	55	46	88	65
5	53	90	56	51	87	58
8	60	90	58	60	90	59
10	60	90	59	60	90	60

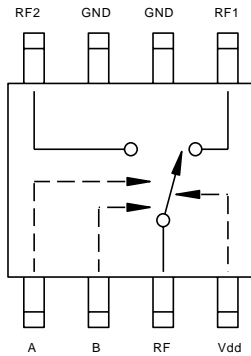
Caution: Do not operate in 1dB compression at power levels above +35dBm and do not "hot switch" power levels greater than +23 dBm (Vdd = +5V).

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v01.0700

FEBRUARY 2001

### Functional Diagram



### Truth Table

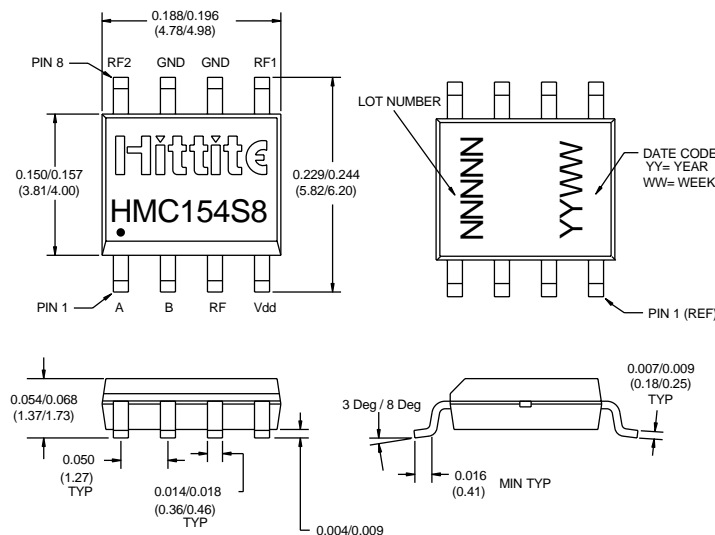
\*Control Input Voltage Tolerances are  $\pm 0.2$  Vdc

Bias Vdc	Control Input*		Bias Current $\mu$ A	Control Current $\mu$ A	Control Current $\mu$ A	Signal Path State	
Vdd (Vdc)	A (Vdc)	B (Vdc)	Ivdd ( $\mu$ A)	Ia ( $\mu$ A)	Ib ( $\mu$ A)	RF to RF1	RF to RF2
3	0	0	30	-15	-15	OFF	OFF
3	0	Vdd	25	-25	0	ON	OFF
3	Vdd	0	25	0	-25	OFF	ON
5	0	0	110	-55	-55	OFF	OFF
5	0	Vdd	115	-100	-15	ON	OFF
5	Vdd	0	115	-15	-100	OFF	ON
10	0	0	380	-190	-190	OFF	OFF
10	0	Vdd	495	-275	-220	ON	OFF
10	Vdd	0	495	-220	-275	OFF	ON
5	-Vdd	Vdd	600	-600	225	ON	OFF
5	Vdd	-Vdd	600	225	-600	OFF	ON

### Absolute Maximum Ratings

Bias Voltage Range (Vdd)	-0.2 to +12 Vdc
Control Voltage Range (A & B)	-0.2 to +Vdd Vdc
Storage Temperature	-65 to +150 deg C
Operating Temperature	-40 to +85 deg C

### Outline



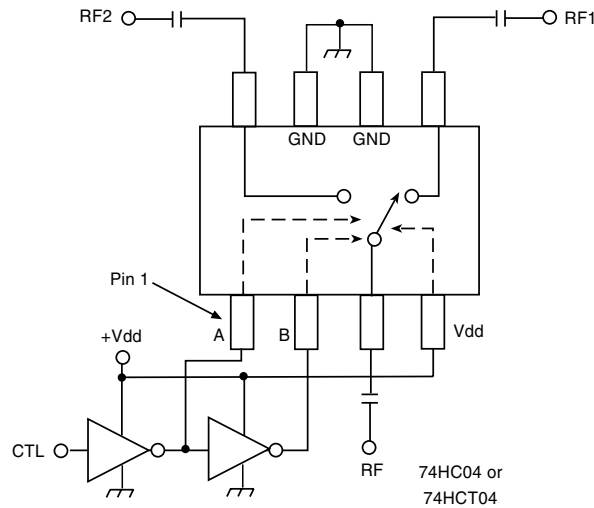
- MATERIAL:  
A) PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED  
B) LEADFRAME MATERIAL: COPPER ALLOY
- PLATING: LEAD-TIN SOLDER PLATE
- DIMENSIONS ARE IN INCHES (MILLIMETERS) UNLESS OTHERWISE SPECIFIED TOLERANCE ARE  $\pm 0.005$  ( $\pm 0.13$ )

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### Typical Application Circuit for HMC154S8



**Notes:**

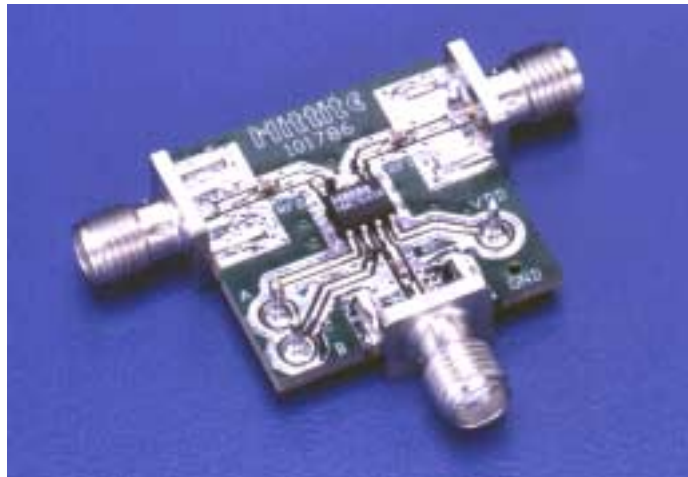
1. Set logic gate and switch Vdd = +3V to +5V and use HCT series logic to provide a TTL driver interface.
2. Control inputs A/B can be driven directly with CMOS logic (HC) with Vdd of 3 to 8 Volts applied to the CMOS logic gates and to pin 4 of the RF switch.
3. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.
4. Highest RF signal power capability is achieved with V set to +10V. The switch will operate properly (but at lower RF power capability) at bias voltages down to +3V.

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### ***Evaluation Circuit Board***



The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown below. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board as shown is available from Hittite upon request.

### ***Evaluation Circuit Board Layout Design Details***

Layout Technique	Grounded Co-Planar Waveguide (GCPW)
Material	FR4
Dielectric Thickness	0.028" (0.71 mm)
50 Ohm Line Width	0.037" (0.94 mm)
Gap to Ground Edge	0.010" (0.25 mm)
Ground VIA Hole Diameter	0.014" (0.36 mm)
Connectors	SMA-F ( EF - Johnson P/N 142-0701-806)

7

SMT SPDT SWITCHES

