MicroWave EMP ©

Adjustable Output Version

$7k

Possible preamp

Pop
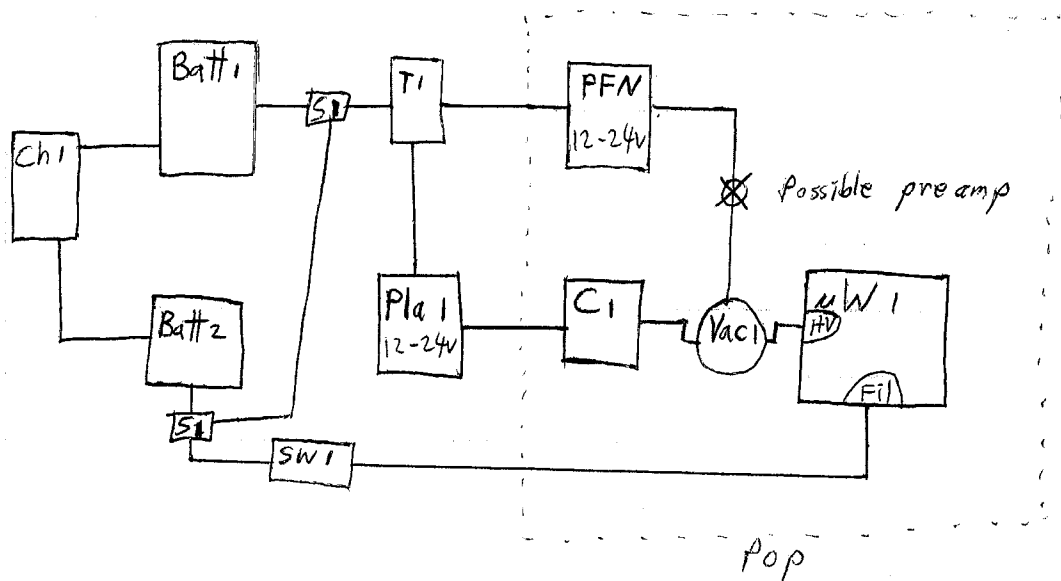
Batt1 = 12 or 24VDC Rechargeable Battery pack.

T1 = Trigger / Relay Trigger Circuit (on/off).

Pla1 = HVDC Plasma Charging Circuit.

C1 = Capacitor Bank (HV Discharge).

PFN = Pulse Forming network (555 Timer).

Vac1 = SPDT Vacuum Relay.

⊗ = Possible Voltage / Current preamp to Trigger vac relay..

uW1 = Magnetron uWave emitter.

Batt2 = 6.3 VDC Regulated Power pack.

Sw1 = SPST 12VDC @ 1A Switch (Toggle).

Ch1 = Battery Charging Circuit.
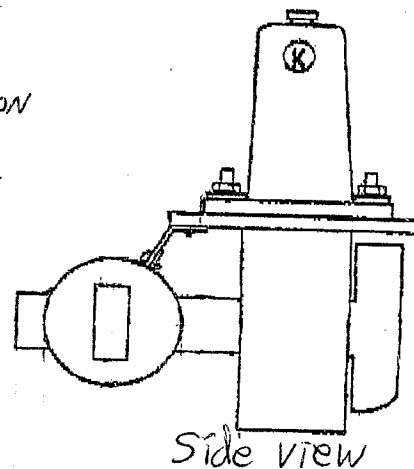
S1 = DPDT Master Switch.

MicroWave EMP ©

Fixed output Version

$5K

POP
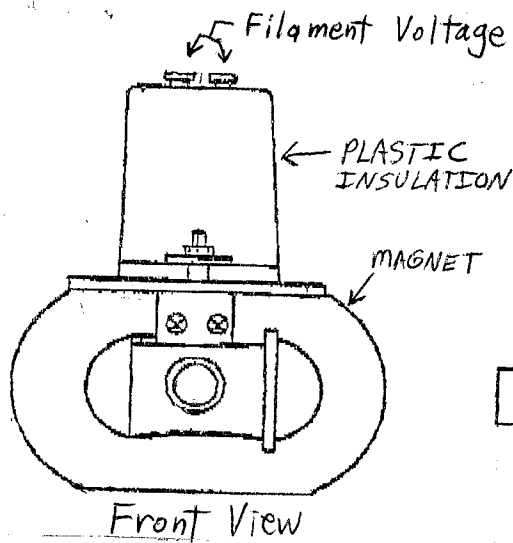(Power output Portion)
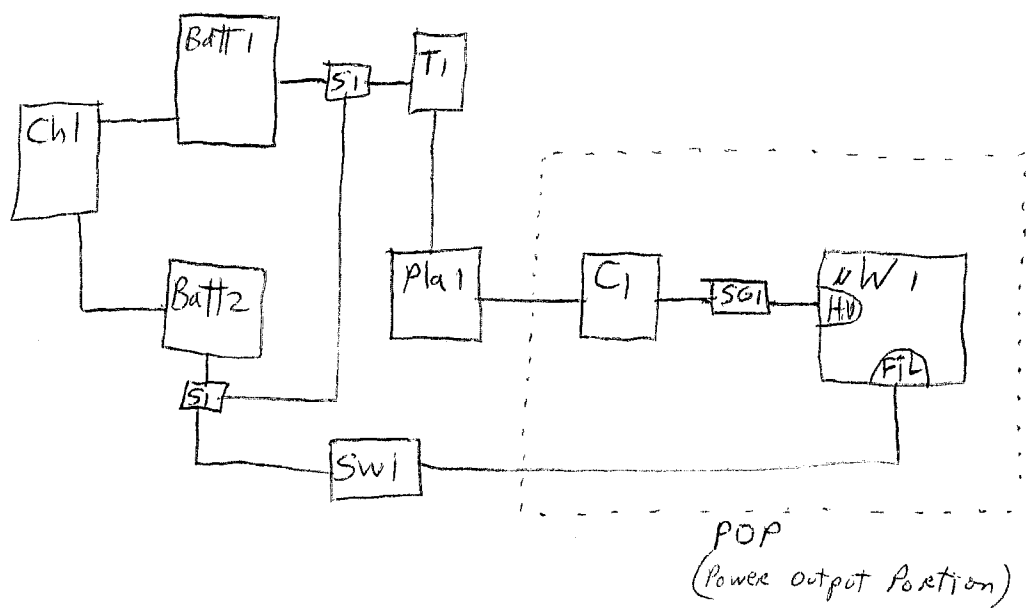
Batt1 = 12-24VDC Rechargeable Battery pack.

Batt2 = 6.3VDC Regulated Battery Pack.

C1 = HV Capacitor Bank.

Ch1 = Battery Charging Circuit.

S1 = DPDT Master power switch.

SW1 = Filament Heater switch 12V@lamp.

T1 = Trigger switch.

SG1 = Sealed Kr 85 spark gap switch 13-14kv.

uW1 = uWave emitter Magnetron.

Pla1 = HVDC Plasma Generator.

BASIC uWave Magnetron

Top View

Mounting Flange

Case is ANODE

← WAVEGUIDE OUTPUT

Filament Voltage

← PLASTIC INSULATION

MAGNET

Front View

Side View
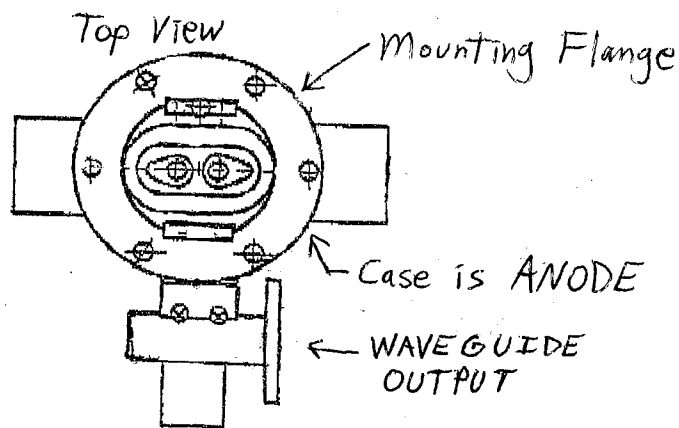
NOT ALL MAGNETRONS LOOK THE SAME, BUT THEY ALL CONTAIN THE SAME BASIC PARTS.

Simple Schematic Diagram

115VAC

VARAC 0-120VAC   TP

100M   10M

100Ω
10W   CAP

9.5KV-16,000V max AC output   S-GAP

CASE

K

Filament
Current Input
6.3VAC

115VAC

MAGNETRON

Best MAG P.S.

2J55 or 2J56A

120VAC

VARAC

HV
xfmr

TO (k) Cathode

TO MAGNETRON CASE
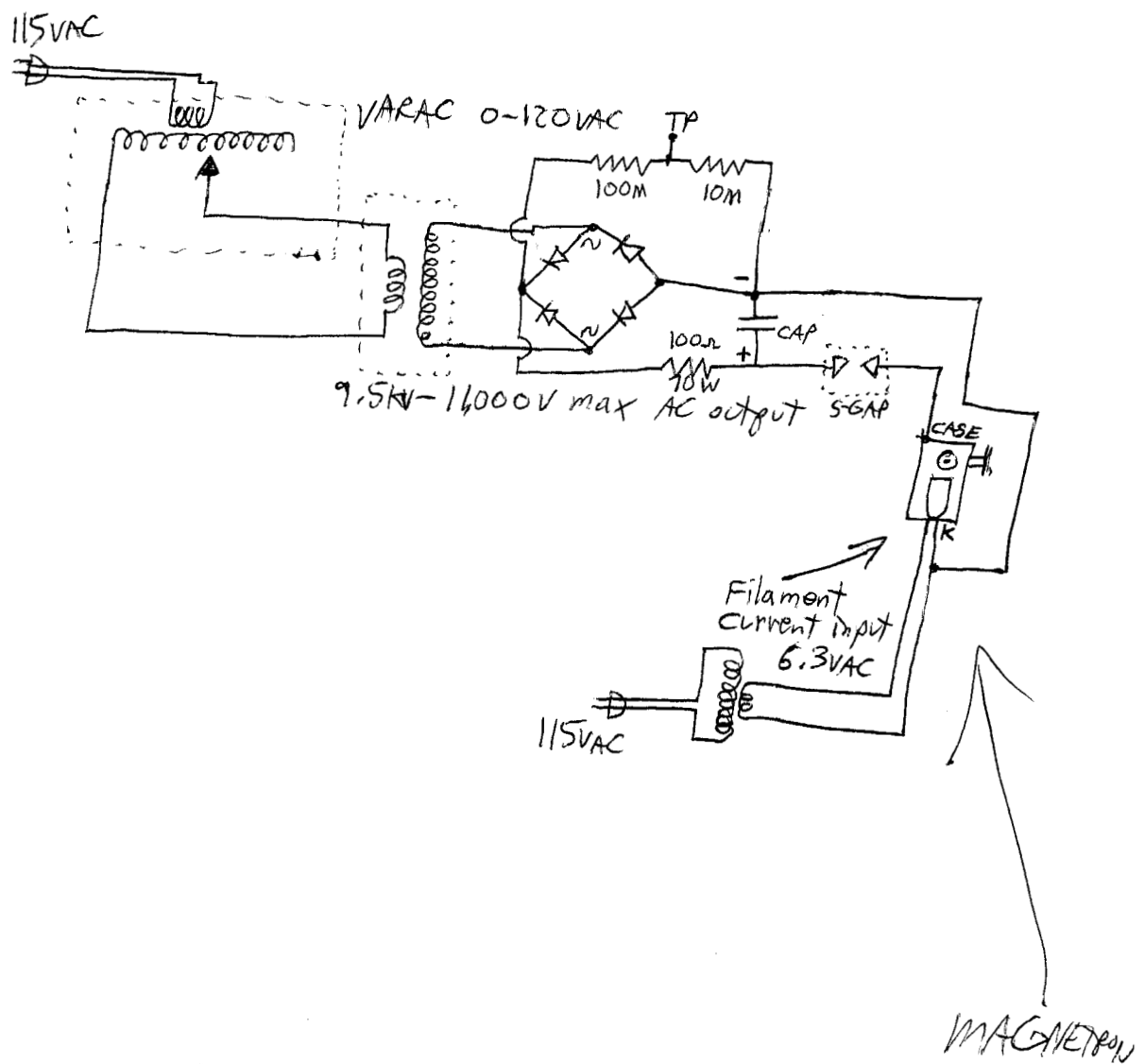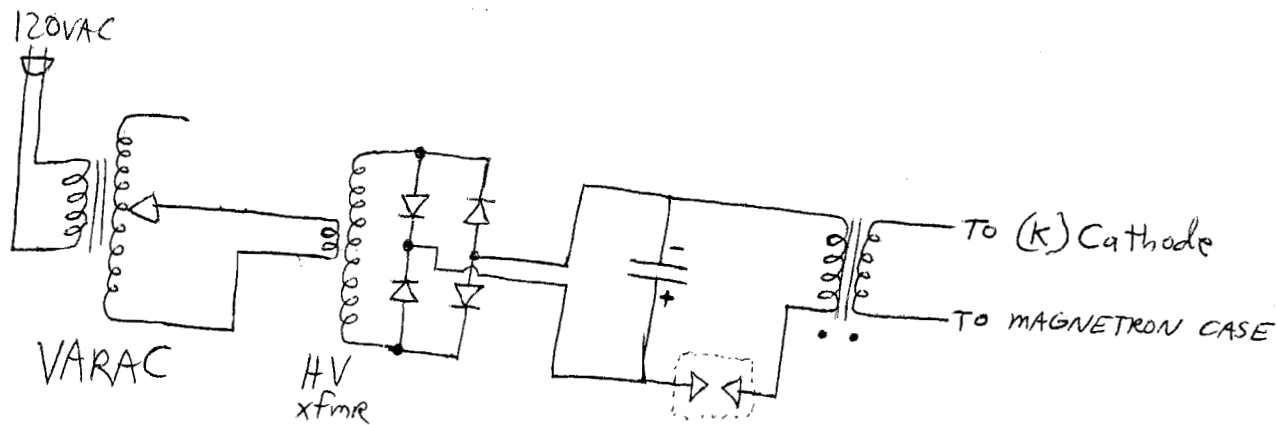
Custom Pulse Transformer

Two Designs will work.

1.) Scratch #1   (Self winded pulse Xfrmr)

insulated #16 wire

teflon insulated #24 wire
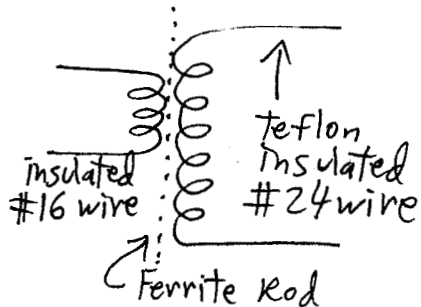
Ferrite Rod

You will use a ferrite rod from 2"L x any diameter to max of 6"L x any diameter.

Coil arrangement: ↓
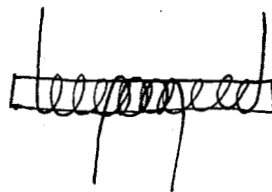
You may also use a toroid and self wind it, but it will take a long time to wrap.
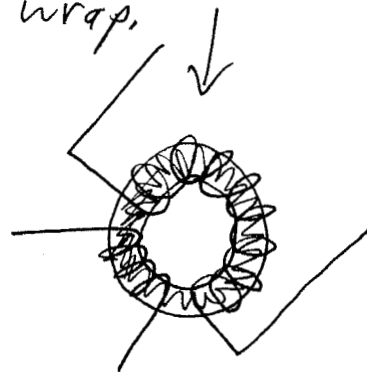
For either design you must use minimum of 20 Turns for the #16 primary winding.

To calculate the # of turns for the secondary:

(S) Turns = Primary # of Turns $\times$ (7.5)

Note: Do not use more than 100 Turns for primary.
Note: The less # of turns you use on the primary — the more Joule energy you will need to power or drive the magnetron.

$60,000 W \times .000001/sec = .06$ Joules

Required Power $\times$ Pulsewidth $=$ Joules

$E = \frac{1}{2} CV^2$ $C =$ capacitance

$E = \frac{1}{2} LV^2$ for an inductor

$E = .06 J$

$V = 15kV$

$L = .0005 uH$ $=$ primary required inductance

Uhepgen
ultra high energy pulse gen
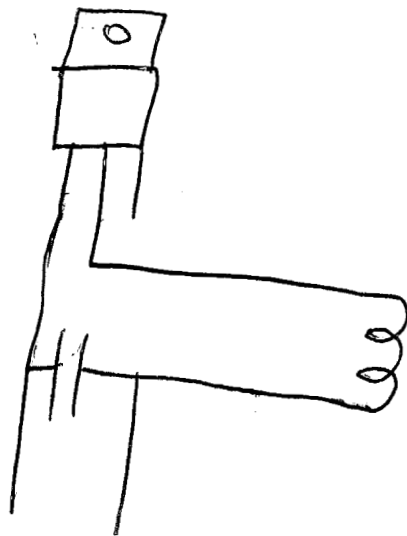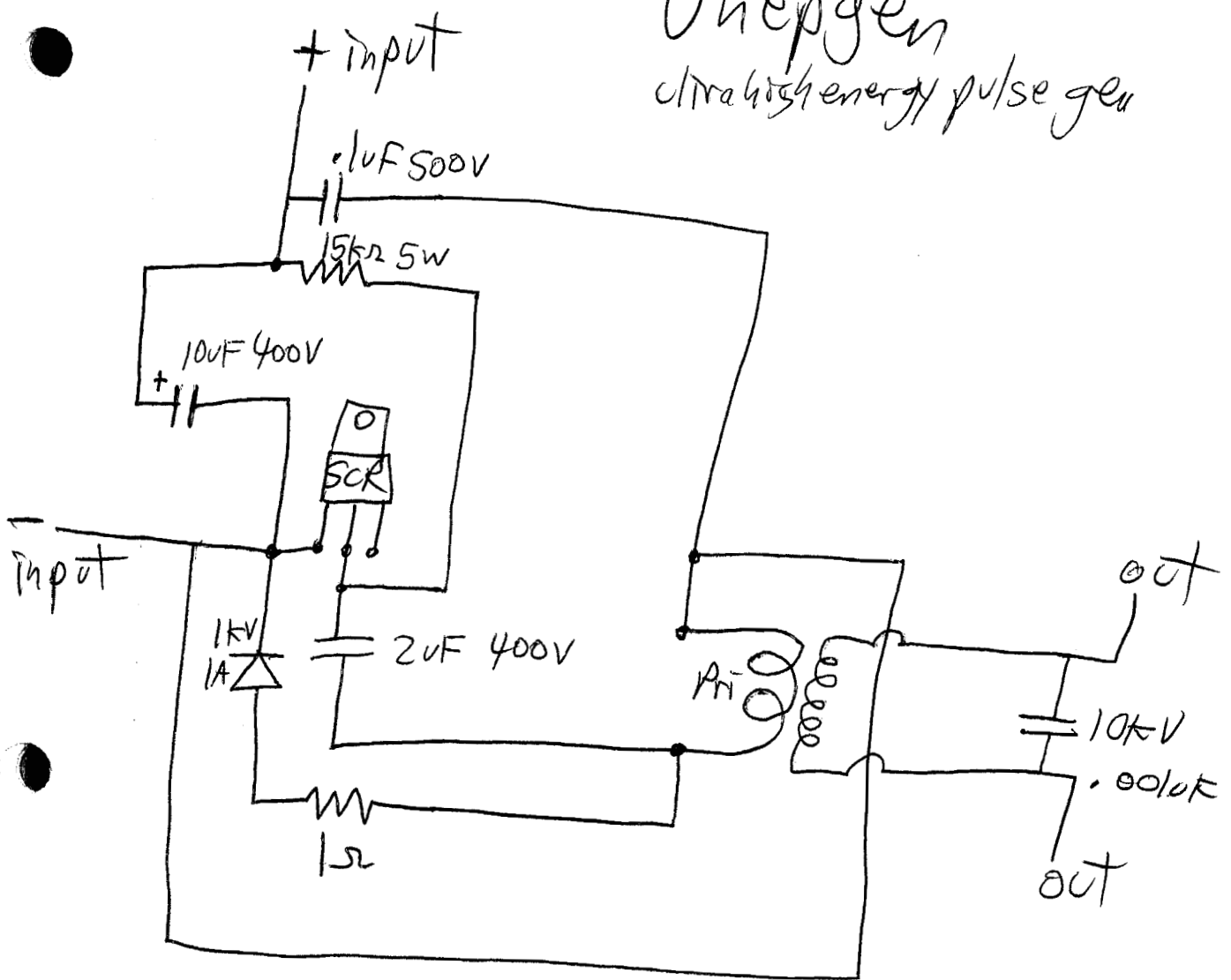
+ input

.1uF 500V

15kΩ 5w

10uF 400V +

SCR

- input

1KV 1A

2uF 400V

1Ω

Pri

out

10KV .001uK

out

Average output power	30 W min.
R.F. bandwidth at ½ power	3.0 MHz max.
Frequency range	9345 to 9405 MHz
Stability (see note 6)	1.0% max.

NOTES:

1. With no anode input power.
    For average pulse input powers less than 150 watts the heater voltage must be reduced within 3 seconds after the application of h.t. according to the following schedule:

    $$Ef = 6.3 \sqrt{1 - \frac{P_i}{180}} \text{ volts}$$

    where P_i = mean input power in watts.

2. The various parameters are related by the following formula:

    $$P_i = i_b \times e_{py} \times Du$$

    where P_i = mean input power in watts

    $\quad\quad i_b$ = peak anode current in amperes

    $\quad\quad e_{py}$ = peak anode voltage in volts

    $\quad\quad Du$ = duty cycle

3. Tolerance ± 10%.

4. Defined as steepest tangent to leading edge of voltage pulse above 80% amplitude. Any capacitance in the viewing system must not exceed 6.0 pf.

5. The anode temperature measured at the point indicated on the outline drawing must be kept below the limit specified by means of a suitable flow of air over the anode body and cooling fins.

6. With the tube operating into a v.s.w.r. of 1.5:1 phased to give maximum instability. Pulse are defined as missing when the r.f. energy level is less than 70% of normal energy level in a 0.5% frequency range. Missing pulses are expressed as a percentage of the number of input pulses applied during the period of observation after a period of 10 minutes.

7. Measured with heater voltage of 6.3 V and no anode input power, the heater current limits are 0.9 A minimum, 1.1 maximum.

8. Design test only. The maximum frequency change with anode temperature change (after warming) is -0.25MHz/°C.

(3)

OUTLINE NOTES

1. Common cathode connection is indicated by letter "K".

2. All metal surfaces except bottom surface of mounting plate and nylon cover shall be painted.

3. Output flange will be concentric with open end of waveguide to within 0.25mm.

4. 31.75 X 15.88 mm external dimension X 1.63mm wall commercial rectangular waveguide.

5. This surface will be free from paint.

6. Heater connection.

7. Cathode connection.

WR 112 waveguide output coupler.

28,5mm X 13mm
internal waveguide output

2J55
Serial# H 4034D
Test cond.
Peak anode Volts = 12.8 kV
Avg power = 55w
Freq = 9389 mHz
Pre heat 6.3V
Avg anode I = 12mA
Pulse = 1 v.Sec   Duty = .001

2J55 *X-Band Magnetron*

GENERAL DESCRIPTION

2J55 is a fixed frequency pulsed type X-band magnetron designed to operate in the frequency range of 9345 to 9405 MHz with a peak output power of 50 kW. It is packaged and waveguide output type and forced air cooled.

GENERAL CHARACTERISTICS

Electrical

Heater voltage (see note 1)	6.3 V
Heater current	1.0 A
Minimum preheat time (see note 9)	120 s

Mechanical

Dimensions	per outline drawing
Net weight	1.9 kg approximately
Mounting position	any
Cooling (see note 5)	forced air
Output coupling	UG-52 B/U

MAXIMUM AND MINIMUM RATINGS (Absoulte)

These ratings cannot necessarily be used simultaneously and no individual ratings should be exceeded.

	Min	Max	Unit
Heater voltage (see note 1)	5.7	6.9	V
Peak anode voltage	—	16	kV
Peak anode current	—	16	A
Peak anode power input	—	230	kW
Average anode power input (see note 2)	—	180	W
Duty cycle	—	0.001	
Pulse duration (see note 3)	—	2.5	μs
Rate of rise of voltage pulse (see note 4)	—	100	kV/μs
Anode temperature (see note 5)	—	100	°C
V.S.W.R. at the output coupler	—	1.5:1	
Pressurizing of waveguide	—	45	lb/in^2
	—	3.2	kg/cm^2

TYPICAL OPERATION

Operational Conditions

Heater voltage	0 V
Peak anode current	12 A
Pulse duration	1.0 μs
Pulse repetition rate	1000 p.p.s.
Rate of rise of voltage pulse	100 kV/μs

Typical Performance

Peak anode voltage	12 kV
Peak output power	50 kW
Average output power	50 W

TEST CONDITIONS AND LIMITS

The tube is tested to comply with the following electrical specification.

Test Conditions	Oscillation 1		Oscillation 2		Unit
Heater voltage (operating)	0		2.5		V
Average anode current	12		8.0		mA
Duty cycle	0.001		0.00065		
Pulse duration (see note 3)	1.0		2.0		μs
V.S.W.R. at the output coupler (max)	1.1:1		1.1:1		
Rate of rise of voltage pulse (max) (see note 4)	100		100		kV/μs

Limits	Min	Max	Min	Max	Unit
Peak anode voltage	11	13	—	—	kV
Average output power	40	—	—	—	W
Frequency	9345	94405	—	—	MHz
R.F. bandwidth at 1/4 power	—	3	—	- 1.25	MHz
Frequency pulling (v.s.w.r. not less than 1.5:1)	—	18	—	—	MHz
Stability (see note 6)	—	0.6	—	0.6	%
Heater current					see note 7
Temperature coefficient					see note 8

LIFE TEST

End of Life Performance (under Test Conditions Oscillation 1)

The tube is deemed to have reached end of life when it fails to satisfy the following:

Average output power	30 W min
R.F. bandwidth at 1/4 power	3.0 MHz max
Frequency range	9345 to 9405 MHz
Stability (see note 6)	1.0% max

NOTES:

1. With no anode input power.
   For average pulse input powers less than 150 watts the heater voltage must be reduced within 3 seconds after the application of h.t. according to the following schedule:

$$Ef = 6.3 \sqrt{1 - \frac{P_i}{150}} \text{ volts}$$

   where P_i = mean input power in watts.

2. The various parameters are related by the following formula:

$$P_i = i_b \times e_{py} \times Du$$

   where P_i = mean input power in watts
   i_b = peak anode current in amperes
   e_{py} = peak anode voltage in volts
   Du = duty cycle

3. Tolerance ± 10%.

4. Defined as steepest tangent to leading edge of voltage pulse above 80% amplitude. Any capacitance in the viewing system must not exceed 6.0 pF.

5. The anode temperature measured at the point indicated on the outline drawing must be kept below the limit specified by means of a suitable flow of air over the anode body and cooling fins.

6. With the tube operating into a v.s.w.r. of 1.5:1 phased to give maximum instability. Pulses are defined as missing when the r.f. energy level is less than 70% of normal energy level in a 0.5% frequency range. Missing pulses are expressed as a percentage of the number of input pulses applied during the period of observation after a period of 10 minutes.

7. Measured with heater voltage of 6.3 V and no anode input power, the heater current limits are 0.9 A minimum, 1.1 A maximum.

8. Design test only. The maximum frequency change with anode temperature change (after warming) is −0.25 MHz/°C.

9. For ambient temperatures above 0°C. For ambient temperatures between 0 and −55°C the cathode heating time is 3 minutes minimum.

PERFORMANCE CHART

PEAK ANODE CURRENT IN AMPERES

PHILIPS

2J 55
2J 56
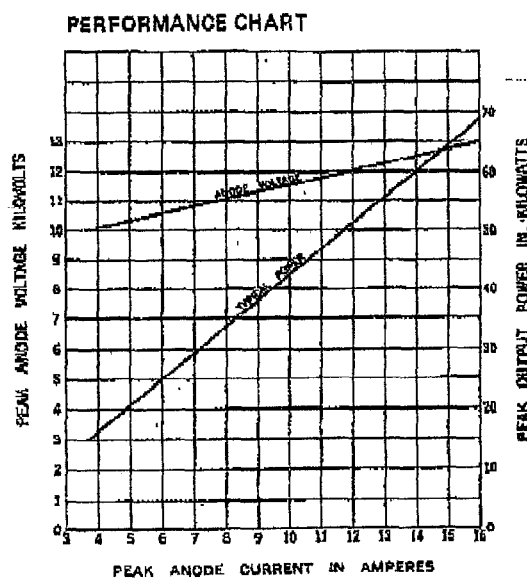
Forced air cooled packaged MAGNETRONS for use as pulsed
oscillators at a fixed frequency in the X-band and
capable of delivering a peak output power of more than
40 kW.
MAGNÉTRONS à refroidissement par ventilation forcée avec
aimant incorporé pour l'utilisation comme oscillateur
d'impulsions à une fréquence fixe dans la bande.X et
capables de fournir une puissance de sortie de crête
de plus de 40 kW.
Druckluftgekühlte MAGNETRONS zur Verwendung als Impuls-
oszillator auf einer festen Frequenz im X-Band mit einer
Ausgangsspitzenleistung von mehr als 40 kW. Magnetron
und Magnet bilden eine Baueinheit.

Type	f
2J55	9375 ± 30 Mc/s
2J56	9245 ± 30 Mc/s

Heating : indirect $\qquad$ V_{fo} $\qquad$ $= 6,3$ V $\pm$ 10 %
Chauffage: indirect $\qquad$ I_f $(V_f = 6,3$ V$)$ $= 1,0 \pm 0,1$ A
Heizung : indirekt $\qquad$

$I_{f\ surge}$ $\qquad$ $= $ max. 6 A
R_f $(V_f = 0$ V$)$ $= $ min. 0,8 Ω
T_W $\qquad$ $= $ min. 2 min.

Remark $\qquad$: V_f must be reduced immediately after applying
the anode power. Please refer to page B.
Observation: V_f doit être réduite immédiatement après
l'application de la puissance anodique. Voir
page B.
Bemerkung $\quad$: Unmittelbar nach dem Anlegen der Anodenleis-
tung muss V_f reduziert werden. Siehe Seite B

Typical characteristics
Caractéristiques types
Kenndaten

V_{ap} $\qquad$ $= $ max. 13,5 kV
$-\dfrac{\Delta f}{\Delta t}$ $\qquad$ $= $ max. 0,25 Mc/s $^{\circ}$C

Δf_p(V.S.W.R. $= 1,5$) $= $ max. 15 Mc/s
C_{ak} $\qquad$ $= $ 9,5 pF

---

[2]) Page 5; Seite 5

V_f must be reduced from 6,3 V to the indicated value
immediately after applying the anode voltage.
V_f doit être réduite à partir de 6,3 V jusqu'à la valeur
indiquée immédiatement après l'application de la
tension anodique
V_f muss sofort nach dem Einschalten der Anodenspannung
von 6,3 V auf den angegebenen Wert reduziert werden

2J55
2J56

PHILIPS

Mounting position: any
Montage: à volonté
Einbau : beliebig

Net weight
Poids net   1,7 kg
Nettogewicht

Shipping weight
Poids brut   4,5 kg
Bruttogewicht

Dimensions in mm
Dimensions en mm
Abmessungen in mm
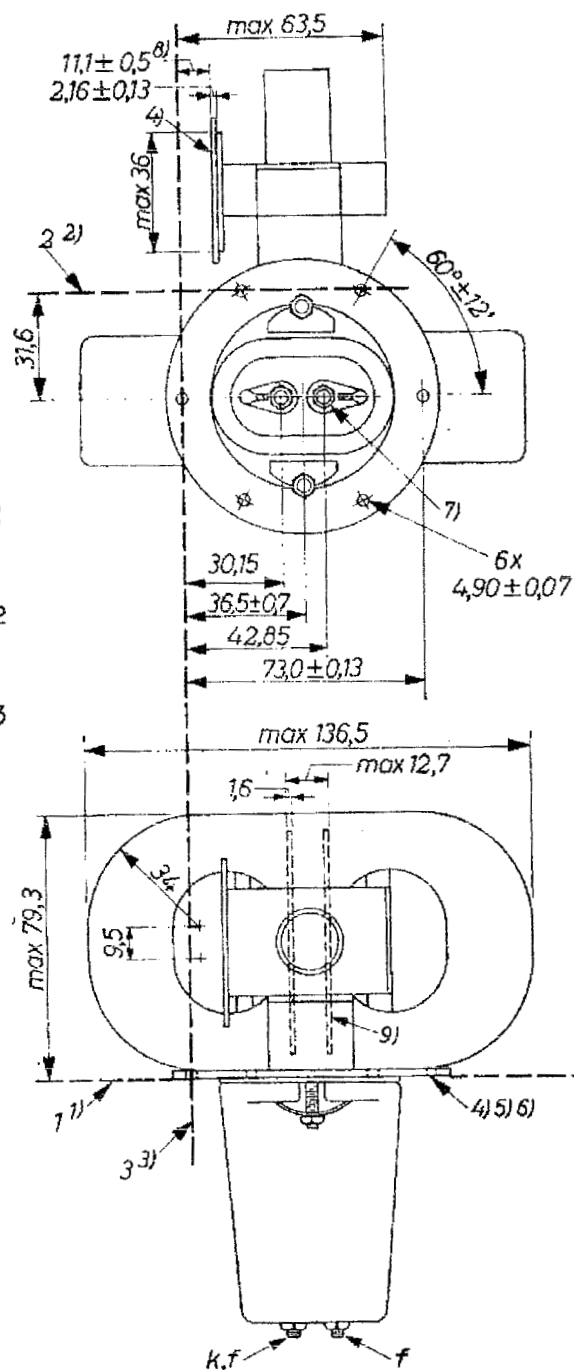
[1]) Reference plane 1
    Plan de référence 1
    Bezugsebene 1

[2]) Reference plane 2
    Plan de référence 2
    Bezugsebene 2

[3]) Reference plane 3
    Plan de référence 3
    Bezugsebene 3

max 63,5
$11,1 \pm 0,5$ [8]
$2,16 \pm 0,13$
4)
max 36
2 2)
31,6
$60° \pm 12'$
30,15
$36,5 \pm 0,7$
42,85
$73,0 \pm 0,13$
7)
6x
$4,90 \pm 0,07$

max 136,5
max 12,7
1,6
max 79,3
3 4)
9,5
9)
7 1)
4) 5) 6)
3 3)
k,f
f

4) All joints in the wave-guide assembly and in the mounting plate are vacuum tight, so that the output flange and the mounting plate may be used to provide hermetic seals.

Tous les joints de l'ensemble du guide d'ondes et de la plaque de montage sont étanches au vide, de sorte que la bride du guide d'ondes et la plaque de montage peuvent être utilisées pour fournir des joints hermétiques.

Alle Verbindungen des Hohlleiters und der Montageplatte sind vakuumdicht, so dass der Flansch des Hohlleiters und die Montageplatte für vakuumdichte Verbindungen gebraucht werden können

5) With the flange resting on a plane surface, the flatness of the mounting plate over a distance of 12.7 mm from the outer edge is such that a 0.25 mm thickness gauge 3 mm wide shall not enter for a distance of more than 6 mm.

Si la bride repose sur une surface plate, la planitude de la plaque de montage sur une distance de 12,7 mm du bord extérieur est telle, qu'un étalon d'épaisseur de 0,25 mm et d'une largeur de 3 mm n'entrera pas plus de 6 mm.

Wenn der Flansch auf einer flachen Unterlage ruht, ist die Flachheit der Montageplatte über einem Abstand von 12,7 mm von dem Aussenrande derart, dass eine 0,25 mm Distanzlehre mit einer Breite von 3 mm nicht mehr als 6 mm zwischengeschoben werden kann.
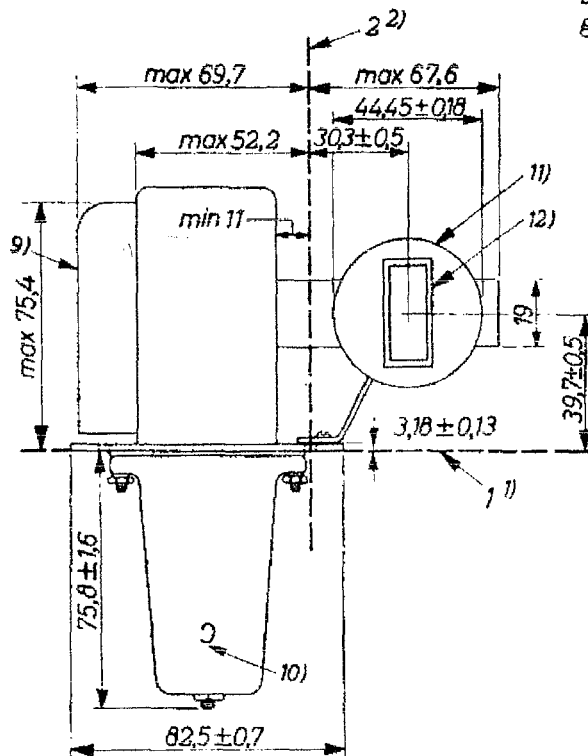
6) 7) 8) 9) 10) 11) 12)
See page 4
Voir page 4
Siehe Seite 4

Dimensions in mm
Dimensions en mm
Abmessungen in mm

6) Any portion of the assembly extending above this surface
is within a 28.1 mm radius of the true centre of the
plate.
Chaque partie de l'ensemble saillante au-dessus de cette
surface est au-dedans d'un rayon de 28,1 mm du centre
de cette plaque.
Jeder Teil der über diese Oberfläche hinausragt befindet
sich innerhalb eines Radius von 28,1 mm vom Mittel-
punkt dieser Fläche.

7) Banana pin jack, 15 mm long hole, 4.29 ± 0.13 mm diameter
Jacks pour fiche banane, profondeur de 15 mm, diamètre
de 4,29 ± 0,13 mm.
Bananensteckbuchsen, Tiefe 15 mm, Durchmesser 4,29 ±
0,13 mm.

8) The tolerance includes the angular as well as the lateral
deviations of the surface
La tolérance comprenne les déviations angulaires et
latérales de la surface.
Die Toleranz umfasst die Winkel- und die seitlichen
Abweichungen der Fläche.

9) Radiator fins
Ailettes du radiateur
Rippen des Radiators

10) The inscription C indicates the common heater-cathode
connexion.
L'inscription C indique la borne commune filament-cathode
Die Markierung C bezeichnet den gemeinsamen Katoden-
Heizfadenanschluss.

11) The output flange is concentric with the open end of
the wave guide to within 0.25 mm
La bride de sortie est concentrique au bout ouvert du
guide d'ondes au-dedans de 0,25 mm
Der Ausgangsflansch ist innerhalb von 0,25 mm konzen-
trisch mit dem offenen Ende des Hohlleiters.

12) Rectangular wave guide with maximum outer dimensions
of 32.5 x 16.5 mm
Guide d'ondes rectangulaire de dimensions extérieures
de 32,5 x 16,5 mm au max.
Rechteckiger Hohlleiter mit Aussenabmessungen von max.
32,5 x 16,5 mm.

Limiting values (Absolute limits)
Caractéristiques limites (Limites absolues)
Grenzdaten (Absolutwerte)

Each limiting value should be regarded independently of
  other values, so that under no circumstances it is per-
  mitted to exceed a limiting value whichsoever

Chaque valeur limite doit être considérée indépendamment
  des autres valeurs de sorte qu'en aucun cas il n'est
  permis de dépasser une limite quelconque

Jeder Grenzwert gilt unabhängig von anderen Werten, so
  dass er unter keinen Umständen überschritten werden darf

T_{imp}	= max.	2,5 µsec	W_{ia}	= max.	180 W
δ	= max. 0,001		T_{rv} [1])	= min. 0,05 µsec	
V_{fo}	= max.	7 V		= max. 0,25 µsec	
$I_{f surge}$	= max.	6 A	V.S.W.R.	= max.	1,5
I_{ap}	= max.	15 A	t_a	= max.	150 °C

$\rightarrow$

Operating characteristics
Caractéristiques d'utilisation
Betriebsdaten

V_f	=	5 [2])	0 [2])	V
T_{imp}	=	0,1	1	µsec
δ	=	0,00033	0,001	
V_{ap}	=	12	12	kV
T_{rv}	=	0,08	0,08	µsec
I_{ap}	=	12	12	A
W_o	=	16,5	50	W
W_{op}	=	50	50	kW

The manufacturer should be consulted whenever it is con-
  sidered to operate the magnetron at conditions substan-
  tially different from those given above

Il faut toujours consulter le fabricant si on veut utiliser
  le magnétron sous des conditions notamment différentes
  de celles indiquées ci-dessus

Es soll immer den Hersteller zu Rate gezogen werden wenn
  man das Magnetron unter wesentlich abweichenden Bedin-
  gungen zu verwenden beabsichtigt

[1]) See "Pulse definitions" page 7
    Voir "Definitions des impulsions" page 10
    Siehe "Impulsdefinitionen" Seite 13

[2]) See page 1; voir page 1; siehe Seite 1

Pages 6-8   in english
Pages 9-11   en français
Seiten 12-14 auf deutsch

MOUNTING

The wave-guide output is designed for coupling to the standard rectangular wave-guide RG-51/U.
Mounting of the magnetron should be accomplished by means of its mounting flange. The tube should in no case be supported by the coupling to the wave-guide output flange alone.
It is required to use non-magnetic tools during installation.
The opening in the output flange should be kept closed by the dust cover until the tube is mounted into the equipment.
Before putting the magnetron into operation, the user should make sure that the output wave-guide is entirely clean and free from dust and moisture.

COOLING

Continuous operation at an anode temperature of 150 $^{\circ}$C involves the risk of somewhat shortened tube life. An anode temperature below 100 $^{\circ}$C is recommended.

PRESSURIZING

The magnetron need not be pressurized when operating at normal atmospheric pressure.
Operation at pressures lower than 52 cm of Hg may result in arcover with consequent damage to the magnetron.
The circular mounting flange and the wave-guide output system of the tube are made so that the magnetron can be used in applications requiring a pressure seal. They can be maintained at a pressure of max. 3.0 kg/cm^2 (43 lbs/$\square$")

LIFE

Magnetron life depends on the operating conditions and is expected to be longer at shorter pulse duration. A load mismatch as low as possible contributes to a longer tube life.

CIRCUIT NOTES

a. The negative high voltage pulse should be applied to the common cathode-heater terminal

CIRCUIT NOTES (continued)

b. If no load isolator is inserted between the magnetron and the transmission line, the latter should be as short as possible to prevent long-line effects. Under no circumstances should the magnetron be operated with a voltage standing wave ratio of the load exceeding 1.5. A ratio kept near unity will benefit tube life and reliability

c. The modulator must be so designed that, if arcing occurs, the energy per pulse delivered to the magnetron does not considerably exceed the normal energy per pulse

d. In order to prevent diode current from flowing during the interval between two pulses and to minimize unwanted noise during the region of the voltage pulse where the anode voltage has dropped below the value required to sustain oscillation, the trailing edge of the voltage pulse should be as steep as possible and the anode voltage should be prevented from becoming positive at any time in the interval between two pulses

e. It is required to bypass the magnetron heater with a 1000 V rated capacitor of minimum 4000 pF directly across the heater terminals.

PULSE CHARACTERISTICS AND DEFINITIONS

The smooth peak value (100 %) of a pulse is the maximum value of a smooth curve through the average of the fluctuation over the top portion of the pulse as shown below

Fig. 1
Voltage pulse

Fig. 2
Current pulse
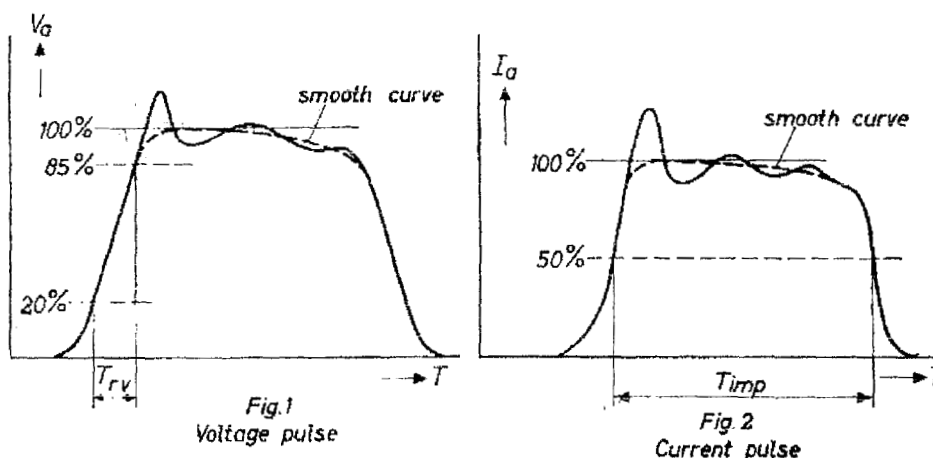
The voltage pulse rise time (T_{rv}) is defined as the time interval between points of 20 and 85 % of the smooth peak value measured on the voltage pulse. Any capacitance used in a removable viewing system shall not exceed 6 pF.

PHILIPS

PULSE CHARACTERISTICS (continued)

The pulse duration (T_{1mp}) is defined as the time interval between the two points on the current pulse at which the current is 50 % of the smooth peak current.

The current pulse must be sensibly square and the ripple over the top portion of the current pulse must be as small as possible to avoid unwanted frequency modulation due to pushing effects.

The spike on the top portion of the pulse must be small to avoid excessive peak pulse current. The leading edge of the pulse must be free from irregularities.

STORAGE, HANDLING

In storage a minimum distance of 15 cm (6 inches) should be maintained between the packaged magnetrons to prevent the decrease of field strength of the magnetron magnet due to the interaction with adjacent magnets.

Magnetic materials should be kept away from the magnet a distance of at least 5 cm (2 inches) to avoid sharp mechanical shocks to the magnet.

Note for page A.

The lower figure of page A shows the variation of W_O as a function of the voltage standing wave ratio for a typical tube.

W_O max. = the output power at the phase adjusted for maximum power

W_O min. = the output power at the phase adjusted for minimum power

W_O = the output power at V.S.W.R. = 1

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2J 55
2J 56

Graph 1: W_{op} (kW) / V_{ap} (kV) versus I_{ap} (A), showing curves V_{ap} and W_{op}.

Graph 2: Δf_p (Mc/s) versus V.S.W.R.

Graph 3: $\dfrac{W_{omax}}{W_o}$ and $\dfrac{W_{omin}}{W_o}$ versus V.S.W.R.

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A

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V_f (V)

W_{ia} (W)

B
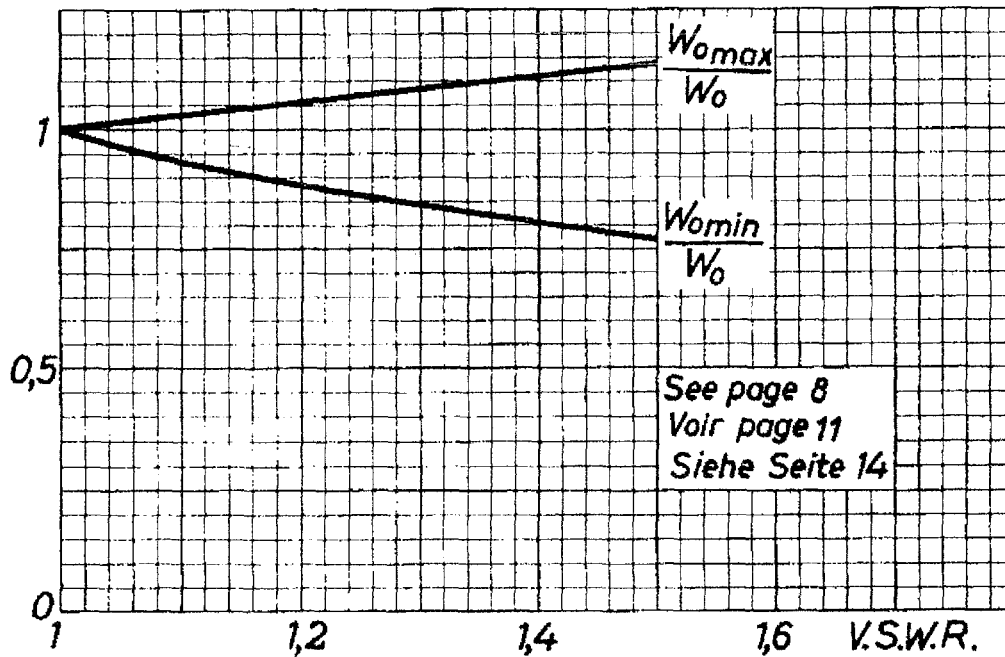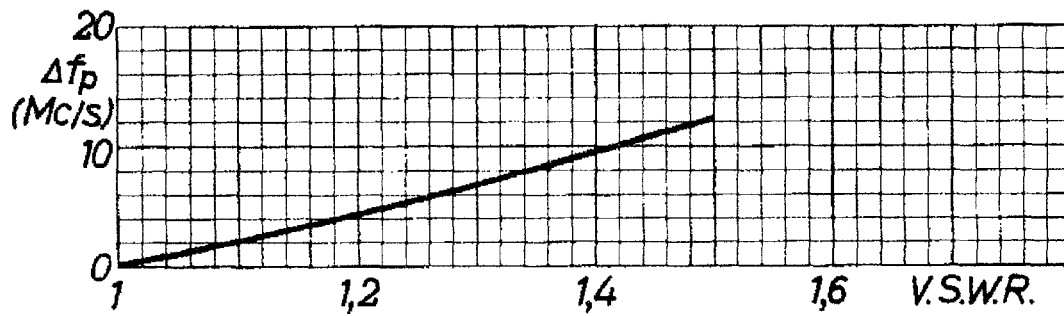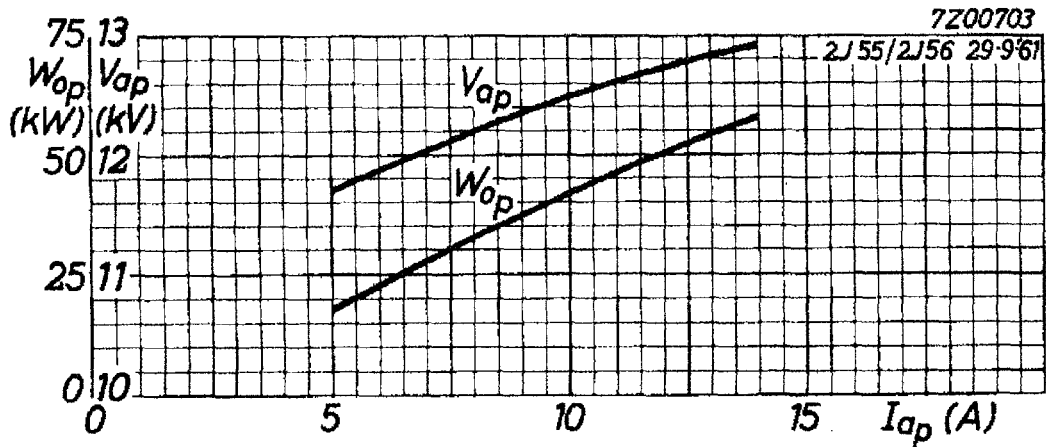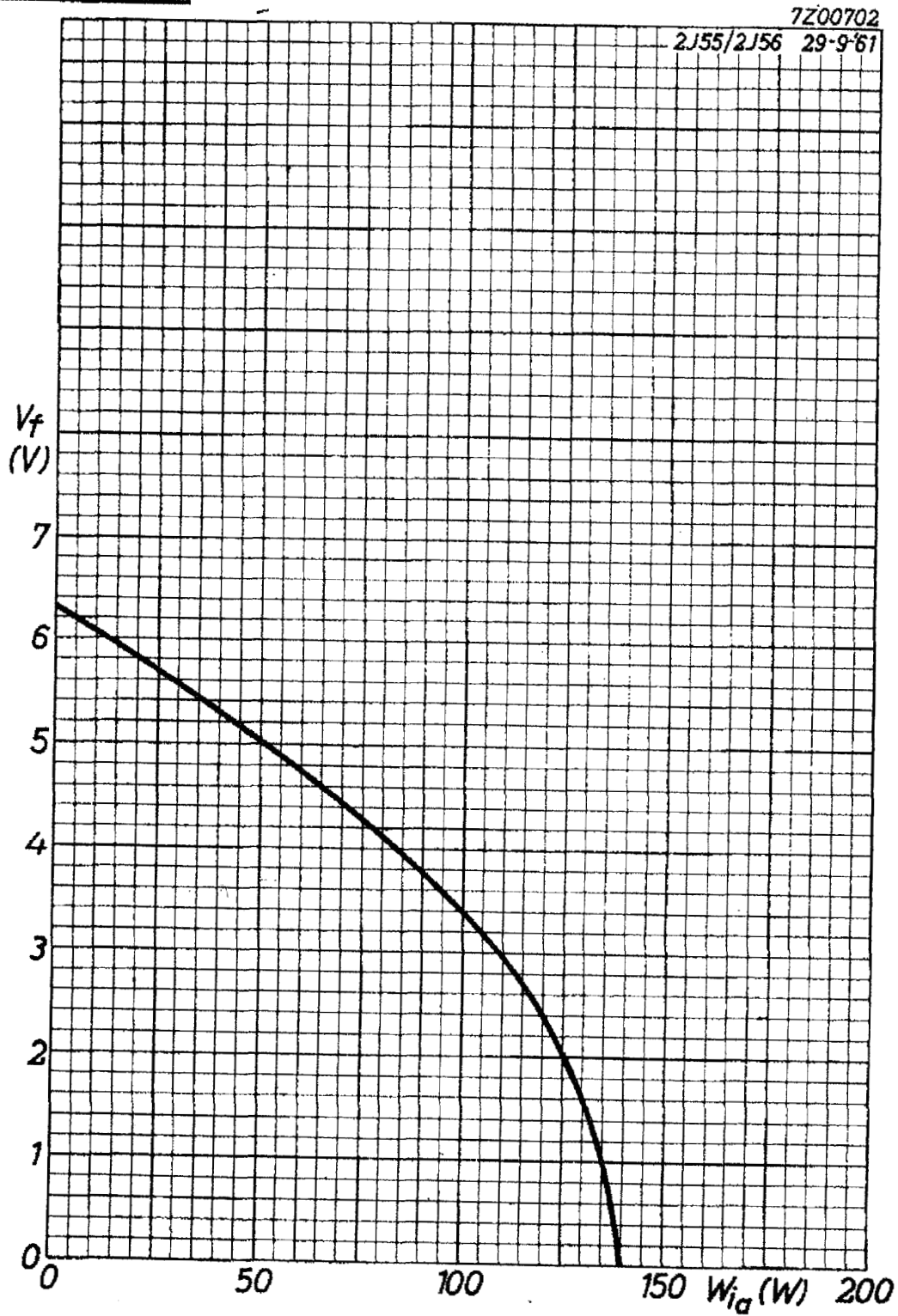
SECTION 4
THEORY OF OPERATION

4.1 INTRODUCTION

In this section is contained an operational analysis of the modulator-transmitter/receivers (MTRs) on two levels; (1) a discussion based on the functional block diagrams in paragraph 4.2 and (2) detailed schematic-level discussions of each subassembly and PCB in paragraph 4.3. Unless otherwise noted, all discussions pertain to all three models of the MTR (25kW, 50kW and 60kW). In cases where the information is different, a separate paragraph will appear bearing the title of the MTR to which it is specifically applicable. In general, the 50kW X-band unit and the 60kW S-band unit are most similar with only a difference in the microwave front end due to operating frequency. The 25kW X-band unit with its lower output power differs from the 50kW and 60kW units mostly in those areas closely related to output power namely, the power supply and the modulator.

4.2 FUNCTIONAL BLOCK DIAGRAM DISCUSSION

4.2.1 50kW and 60kW Unit

Refering to Figure 4-1, the MTR consists of a magnetron oscillator driven by a solid state modulator at three pulse repetition frequencies (PRFs) and three pulse widths, and a receiver which consists of an integrated microwave assembly, a solid state local oscillator and an IF amplifier switchable to either a narrow or wide bandwidth. The MTR has 2 self-contained power supplies which supply all necessary operating voltages.

Input power is supplied to the MTR unit via a surge suppressor assembly and two radio frequency interference (RFI) filters to the high voltage power supply (HVPS A2) and the low voltage power supply (LVPS A3). The switching regulator-type supplies are self-contained and offer excellent power density. All voltages necessary to operate analog and logic circuitry are generated by the LVPS (A3) while the HVPS (A2) provides the high operating potential necessary for the solid state modulator.

Input triggers for the transmitter are normally received from the indicator at the proper PRF for the selected range. For test purposes, an on-board pulse generator (P/O logic and fault PCB, A6) provides the proper repetition rate when local operation is selected with the LOCAL PW SELECTOR switch S5. This allows for complete testing of an MTR without the use of a working display. Two pulse width selector lines from the indicator control a decoder on the logic and fault PCB which determines which of the pulse width solenoids is energized. The solenoids switch certain components into or out of the pulse forming network (PFN) to change the duration of magnetron firing time or pulse width. The PRF trigger pulse is routed through a delay generator in order to allow enough time for the sensitivity time control (STC) generator circuit to begin developing the STC waveform. After the delay period a PRF trigger drive pulse is produced and sent to the snubber driver PCB (in the modulator) which is used to actuate the SCRs.

The solid state modulator is fully self-contained and provides the necessary energy pulses to excite the magnetron oscillator. Consisting of four major circuit areas, the unit operates so as to continually charge and discharge a pulse forming network (or energy storage circuit). Discharge is through a pulse transformer (T1) the secondary of which couples an energy pulse to the magnetron thereby shocking it into oscillation for the duration of the modulator pulse. The four main circuit areas are:

1.   Charging circuits, consisting mainly of the charging SCR PCB A4A1, and the pulse forming network which holds the charge.

2.   Discharge circuits, including the SCR assembly containing 4 SCRs, and the snubber driver PCB which gates the SCRs on or off.

3.   Pulse shaping circuits, comprised of the pulse forming network PCB A4A4 and the tailbiter PCB A4A5 which determine the duration of the pulse coupled to the magnetron.

4.   Magnetron heater scheduling circuits which are contained on the magnetron heater scheduling PCB A4A3. It is on this PCB that the magnetron current is sampled and used to provide an acknowledge pulse output and also to control the magnetron heater voltage circuit.

The magnetron is connected to the microwave assembly (A8) which includes: 1) an integral three-port ferrite circulator with ports for the transmitter, the antenna, and the receiver; 2) a frequency mixer and balanced diode detector; and 3) a Gunn diode local oscillator assembly.

Received signals pass through the circulator and mixer to a logarithmic IF amplifier with electronically switched bandwidths of approximately 4 or 25MHz. During short pulse operation, circuitry on the logic and fault PCB switches the bandwidth of the IF to 25MHz. During medium and long pulse operation, the circuit switches the bandwidth to 4MHz.

Antenna power is applied via an antenna control contactor K1, in the MTR. The antenna contactor can be deenergized by either the ANTENNA switch (mounted on an indicator) or by activating the antenna safety switch at the antenna. Activation of the antenna safety switch shuts off the antenna and the rf but leaves the system in standby. Activating the ANTENNA switch only shuts off the antenna to allow for tuning, and also enables the dimming circuit to prevent CRT burn.

4.2.2   25kW Unit

A functional block diagram for the 25kW unit is shown in Figure 4-2. Referring to this figure, there are a few minor differences in the overall MTR design resulting primarily from the lower power output requirement of this unit. All operating potentials are derived from a single power supply unit (A2) which contains separate low voltage and high voltage output PCBs. The LV output PCB (A2A5) provides all voltages necessary to power analog and logic circuitry within the MTR while the HV output PCB (A2A6) provides the high operating potential necessary for charging and discharging the solid state modulator pulse forming network.

A few differences characterize the 25kW modulator one of which is the deletion of one of the SCRs from the SCR subassembly, the 25kW unit having 3 instead of 4 of these in the assembly. This is a result of less power being switched through the SCR bank. Also in this unit, a despike component board (A4A6) has been added within the modulator and connected to the +800Vdc input line. The purpose of this board is to prevent transients which would occur when the HV on-off transistor (on the HV output PCB A2A6) is initially energized and HV is applied to the completely discharged modulator circuitry. Other than the differences noted here, the overall operation of the 25kW unit does not differ from the 50kW and 60kW units.

4.3 DETAILED THEORY OF OPERATION

The MTR is composed of various subassemblies and PCBs, each designed for a specific functional purpose in the MTR. A schematic level theory of operation for each of the assemblies, as well as their interrelationships where pertinent, is contained in the following paragraphs.

4.3.1 Power Supplies

Power supplies used in the MTRs are of the switching regulator-type which uses 40kHz switching techniques to provide high efficiency and exceptional power density (high power output from a small physical package). The control portion of the supplies is virtually identical in the LVPS (A3) and the HVPS (A2) in the 50kW and 60kW unit and the single power supply (A2) in the 25kW unit which comparison of the schematics in Figures 6-7, 6-9 and 6-50 will reveal. (The control portion of the supply can be said to be that portion of the circuitry on the primary side of the power transformer T1.) The discussion in paragraph 4.3.1.1 is applicable to all three power supply units. A separate discussion follows for each of the three different output sections associated with the power supply units.

4.3.1.1 Input and Control Circuits - The power input (115 Vac, 1φ) is applied through line transient suppressor L1 to a voltage doubler. Voltage doubler action converts the input power to approximately 300Vdc which is supplied to the collector of a step-down power chopper via a current snubber circuit comprising L6, CR7, CR2 and C12. The current snubber is basically a current delay preventing excessive stress on the down-chopper during initial power application. The output of the chopper is a controlled duty cycle, applied through a power filter, inverter circuit and T1 to the output PCB which derives, from the transformer input, the various output voltages needed for MTR operation.

The output is sensed, and compared with a reference voltage. Any difference, or error voltage, is amplified and fed back to the chopper control circuits to change the duty cycle as necessary. Thus a closed loop is achieved, resulting in excellent line/load regulation. Control portions of the circuitry consist of:

1. Pre-Regulator printed circuit board (PCB) A1; a free running, switching regulator which generates system bias voltages.

2. Chopper Duty Cycle Control PCB A2; maintains desired level of power supply output.

3.   Base Driver PCB A3; bias current source for duty cycle control, provides base drive for the power inverter.

Input Circuit - The input is applied through input RFI choke L1 and bridge rectifier CR1 in the full-wave rectifying mode. Input capacitors C2/C3 are in series in the full-wave mode. The input appears as unregulated 250-350Vdc at step-down chopper Q1/Q2 through fuse F2 and RFI choke L6. The chopper establishes the required duty cycle, whose pulse width is controlled by inputs from the A2 chopper control circuit board. Variations in power supply output thus are fed back as error signals to the A2 PCB, processed, and applied to the chopper to vary the duty cycle pulse width. The power filter section, consisting primarily of L4 and C10, averages the duty cycle into a controlled dc level of 120-190 volts depending on the output load requirements.

Pre-Regulator/Bias Supply PCB (A1) - The pre-regulator PCB (Figure 6-11 or 6-51) provides a regulated 150Vdc to the bias inverter on the base driver PCB (A3), and is the source of other bias voltages required by the power supply. An unregulated dc input is processed into a controlled duty cycle pulse which establishes and maintains proper bias voltages. The free-running switching regulator on this PCB is run on a 40kHz clock signal generated by A1U1 and variable by R9. This clock also sets the timing of the supply switching circuits as its output is tapped at the secondary of A1T1 and used as a trigger at J2-2 and J3-1.

Pulse Width Modulator (A1U2)/Chopper (A1Q2) Control - The output of the pulse width modulator (PWM) at pin 3 determines the duty cycle for step-down chopper A1Q2. The PWM operates as follows:

The instantaneous voltage at the threshold input of A1U2 at pin 6 is a function of the (A1) R7/C5 time constant. After being triggered by the 40kHz clock at trigger input pin 2, this voltage begins to increase, until it reaches the level of that at pin 5 (error signal detailed in the following paragraph). This time period sets the "on" time of the duty cycle of A1Q2, and thus the A1T1 primary voltage. The voltage at pin 6 decays until a subsequent trigger at pin 2 repeats the process. As the error voltage at pin 5 varies, so does the "on" time of the duty cycle.

Error Control Amplifier (A1U3) and Bias Control - A section of the primary winding of A1T1 serves two purposes:

1.   Provides a +6.2Vdc trunk line for overall pre-regulator circuit operation.

2.   Establishes the voltage at A1U3 which controls the error signal at A1U2-5.

The voltage across this primary section of A1T1-A senses any variation across the primary winding. This error is applied to error amplifier A1U3, varying the dc level at A1U2-5, and adjusting the duty cycle at A1Q2 as required to maintain 150 Vdc across the A1T1 primary. This regulation effectively maintains the voltage across A1C15 (which functions partly as an LC filter with the A1T1 primary) at a constant 150Vdc. This assures accurate output levels at the remaining A1T1 secondaries.

Potentiometer A1R15 is adjusted to set the output at J3-2 to precisely 5.1Vdc. The remaining bias levels (+16V, ±6.5V, +150V) are dependent on the 5.1Vdc setting.

Chopper Control PCB (A2) - The chopper control PCB (Figure 6-12 or 6-52) contains the circuitry which controls the duty cycle pulse width input to the main power choppers, thus stabilizing the system output level. Three primary circuits contribute to this control:

1.   Voltage error amplifier (A2) U4/U5.

2.   Low voltage sensing (A2) U1-A/U1-E and logic shutdown A2U6.

3.   Current-limiting error amplifier A2U3.

The output of each of these circuits appears as a dc input to an OR gate comprising CR3, CR4 and CR6. The OR gate passes the larger of the three inputs into a constant current comparator circuit. Here it is compared to the relatively constant 40kHz ramp signal (developed by a trigger from the pre-regulator board A1). The comparator outputs are in the form of square-wave pulses, positive for "on" time control, and complementary negative-going turn-off pulses. The resultant output is applied simultaneously to bias drivers at a 40kHz repetition rate.

Base Driver PCB (A3) - Circuit board A3 (Figure 6-13 or 6-53) provides the major functions of base drive to the power switching transistors Q3/Q4 on the main power supply chassis; bias current supply for the chopper driver (A2); and, overvoltage sensing shut off capability.

Power Inverter - The controlled 120-190 volts from the input power choppers establishes the operating voltage for power inverter Q3/Q4/T1 (see overall power supply schematic). Switches Q3/Q4 in the push-pull mode provide a nearly constant (90%) duty cycle to power transformer T1 (with small adjustment for current balance).

4.3.1.2   50kW and 60kW HV Output PCB (A2A5) (Refer to Figure 6-10) - The secondary output of power transformer T1 is fed to the HV output PCB where it is applied to a full wave bridge rectifier comprising CR1, CR2, CR3 and CR4. Output filtering is provided by C6 while a string of ten 10K resistors, R8 through R17, serve a voltage divider function to provide a low voltage indication reflecting fluctuations in the high voltage output. This is used by the logic and fault PCB to sense undervoltage condition in the MTR. In the HV position of the MONITOR switch, this same voltage is used to indicate the relative level of the high voltage. Output of the HVPS is 1kVdc (nominal) regulated.

Circuits allowing the three minute warmup delay of the high voltage are also incorporated on this PCB. When ac is first applied to the MTR, the LVPS supplies +12 volts to the output PCB via CR5 and R18. Zener VR1 sets the input trunk line to +5.1 volts to operate the TTL timer clock circuitry. Frequency of timer clock U1 is determined by components R2, R3 and C2 and can also be increased in frequency by increasing the voltage applied at R2. With a +5.1 volt input the TTL chain will take approximately 3 minutes to produce a TTL low at U3-8, which is connected to one side of relay K1. The other side of relay K1 is connected to the +5.1 volt line so that when U3-8 goes low, the relay is energized providing switch closure to the remote shutdown input of the chopper control PCB (A2A2) thereby turning over control of the HVPS to the logic and fault PCB. When a low is felt at J2-13 and K1 is energized, the HVPS will produce its output.

When time-in has been completed, the low output at U3-8 is used to stop conduction of Q1 on the LVPS output PCB. Transistor Q1 controls the +60 volt output that allows for a fast time-in (restart) if ever the timer circuit should reset after the magnetron has been warmed up. Capacitor C3 on the LVPS output PCB stores the +60 volts and is connected to the +60 volt input on the HVPS output PCB where it is applied through CR6 to the time constant components of U1.

4.3.1.3 50kW and 60kW LV Output PCB A3A5 (Refer to Figure 6-8) - The LV output PCB uses the multi-output T1 secondary to provide the many low voltage operating levels required by the MTR. Among these are the following:

+120Vdc - to the snubber driver PCB A4A2.

+60Vdc - restart output to the HV output PCB.

+12Vdc - fed to a floating, adjustable 8Vdc regulator (U4) on the power supply chassis.

+24Vdc - fused, which provides operating potential to modulator PCBs A4A3, A4A4 and A4A5.

+16.5Vdc - which is the source voltage for the +12Vdc series regulator U1 on the PS chassis.

-16.5Vdc - which is the source voltage for the -12Vdc regulator U2 on the PS chassis.

-9.5Vdc - LO source voltage.

-8Vdc - fed to the tune terminal on the LO as well as to the tune voltage divider in the indicator. In practice, this point can read from -2Vdc to -8Vdc depending on the position of the TUNE control on the indicator.

+9Vdc - which is the source voltage for the +5.1Vdc series regulator U3 on the PS chassis.

4.3.1.4 25kW LV and HV Output PCBs (A2A5 and A2A6) (Refer to Figures 6-54 and 6-55) - The output of A2T1 appears across 4 separate secondary windings, three of which feed the LV output PCB A2A5 and one that feeds the HV output PCB A2A6.

On the LV output PCB comprising a full-wave bridge are rectifiers CR1, CR2, CR3 and CR4 which develop the +120Vdc supply to the snubber driver PCB A4A2. Resistors R2 and R4 isolate another 120Vdc output used to cause fast time-in (restart) of the HV delay circuit on the HV output PCB. These resistors also serve as the collector load for Q1 which is kept in full conduction by a positive voltage applied at its base from the timer circuit on the HV output PCB. After initial warmup is achieved, the timer output goes low, Q1 shuts off causing the full 120Vdc to appear at its collector which in turn is applied to the HV output PCB, and there it causes the time base of the timer circuit to shorten to approximately 10 seconds. The remaining outputs of the 25kW LV output PCB are virtually identical to those described in paragraph 4.3.1.3.

The 25kW HV output PCB contains a HV full-wave bridge rectifier comprising (A2A6) CR1, CR3, CR5, and CR7. The return side of this bridge contains a snubber (L5, CR18 and R30) to protect HV on-off transistor Q1, and a 16 ohm resistor (R5) which is used to provide a sample of the load present on the +800Vdc output.

On-off switching capability of Q1 is afforded by a center-tapped biasing transformer (T1) whose output is rectified, filtered and applied to the emitter-base junction of Q1. The primary's center-tap must be grounded to produce output from the secondary. For this to occur, Q3 must be conducting and a ground must be present at J2-4 which is supplied from the pulse logic PCB in normal operation. Transistor Q3 is driven by the timer circuit and is on whenever the timer has completely cycled through its 3-minute delay period (from turn-on). Transistor Q4 also senses the state of the timer output and provides a signal to the LV output PCB to enable the 120Vdc restart output which is routed back to the HV timer circuit.

Programmable timer U1 is powered by a +12Vdc supply from the LV output PCB. Its time base is set by RC components R8 and C4 which cause its cycle to complete in approximately 3 minutes from turn-on. After the cycle is complete the output drives Q2 into conduction through its emitter resistor network comprising R14, R15 and R16, R17. The value of these resistors cause sufficient positive voltage to appear at the bases of Q3 and Q4 to cause them to turn on.

Reset input to the programmable timer (U1) is at pin 11 which is connected through a 4.7V zener diode to the +12Vdc output of the power supply. An appreciable drop in this input will cause the timer to reset. Once timed in, however, the timer will cycle in only 10 seconds due to the +120Vdc being present at the time base input to U1.

4.3.2   Pulse Former Modulator Theory

The purpose of the modulator is to apply high voltage (approximately 12kV) pulses of the proper duration to the magnetron in order to cause it to produce high power rf pulses.

In the solid state modulator, the high voltage pulses are generated by charging a pulse forming network to a medium high voltage (about 2kV) and then discharging the network rapidly through a pulse transformer. The turns ratio of the transformer provides the required voltage step-up to operate the magnetron.

A simplified version of the modulation system is shown in Figure 4-3 along with an idealized waveform of the voltage changes across the network.
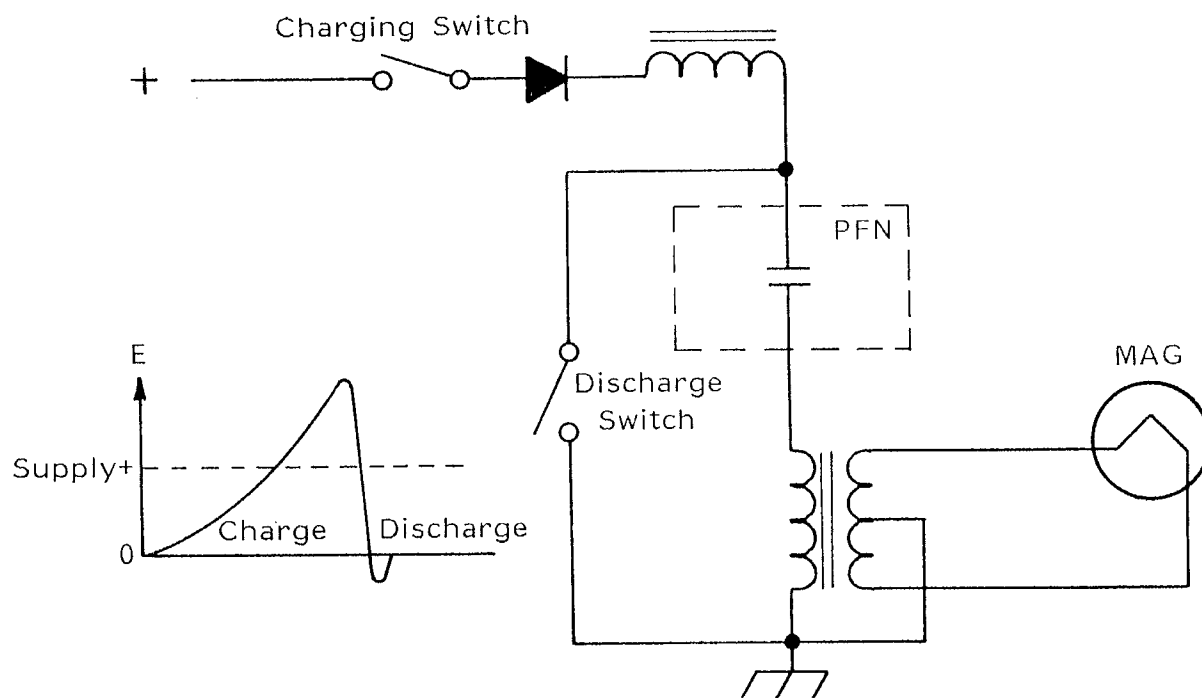
Figure 4-3 Simplified Modulation System

As shown in Figure 4-3, a dc voltage is applied to the pulse forming network (PFN) through a charging switch, an isolation diode, and inductance in series. The negative terminal of the PFN is connected to ground through the pulse transformer. Assume that the components of the PFN (which can be considered as a single capacitor for discussion purposes) are fully discharged. As soon as the charging switch is closed, the PFN will start to charge at a rate that is determined primarily by the value of the series inductance. (Refer to the waveform of Figure 4-3). When the voltage across the PFN is equal to the input voltage, the voltage across the PFN continues to increase, even after it has reached the input level. The extra voltage is obtained from the voltage doubling effect as the magnetic field of the series inductor collapses. The optimum increase in voltage is obtained when the charging switch opens and closes at the frequency at which the series inductance is resonant with the capacitance of the PFN. Under ideal conditions this resonant rise phenomenon will cause the PFN voltage to be twice the input voltage.

At the relatively low charging rate the primary of the pulse transformer appears only as a small resistance and no output is generated. The PFN voltage will remain at the peak charge level because the isolation diode prevents discharge of the network through the charging circuit. In practical circuits, it will leak off due to the finite resistances of the switching circuits.

When the discharge switch is closed, the PFN is connected directly across the primary of the pulse transformer. The circuit is designed so that the characteristic impedance of the PFN matches the primary impedance of the pulse transformer so that the maximum transfer of power takes place. The rapid discharge of the PFN causes very large currents to flow in the pulse transformer primary for a period determined by the values of the various inductors and capacitors which make up an actual PFN. The components within the PFN are connected in such a way that the discharge current remains relatively constant throughout the duration of the pulse and decays rapidly as the pulse ends.

The negative portion of the waveform (Figure 4-3) is caused by an inevitable mismatch (caused by the changes in magnetron impedance as it goes into and out of oscillation). The amount of overshoot is minimized by a diode connected across the transformer primary so that it conducts during the overshoot period.

4.3.3   Solid State Modulator (A4) (Refer to Figure 6-4 or 6-56)

PFN Operation - In the solid state modulator, the PFN consists of five identical inductors, A4A4L1 through A4A4L5 connected in series. PFN capacitance is obtained from A4A4C1 through A4A4C7 which are connected between a common line and the junctions of the inductors. The three pulse widths are selected by solenoids, K1 and K2 which connect the common lines between groups of capacitors as the ranges are changed at the indicator. Note that when the short pulse width (0.05µs) is selected, the PFN consists of C1 only. When medium pulse is selected, C2 through C4 and L1 and L2 are used in addition to C1. Solenoids are used to perform the switching function rather than relays in order to provide a shorter and lower impedance path for PFN discharge current. (Discharge currents are of sufficient amplitude to create voltage drops of greater than 5 volts across a 2-inch length of standard ground strap of 1-inch wide braid).

PFN Charging Circuits - The function of the charging switch (in the simplified schematic) is performed by the circuitry on the charging SCR PCB (see Figure 6-5 or 6-57). Two silicon controlled rectifiers (SCRs), CR1 and CR2 are connected in series to provide the necessary 1000 volt holdoff capability. When triggered, the SCRs provide a low impedance path between the 1000V input and the isolation diode A4CR1. The characteristics of an SCR keep it in the conducting state (after a pulse of some minimum duration has been applied to its gate terminal) until the flow of current from cathode to anode drops to below the holding level. In this circuit, the current drops to zero when the voltage at the PFN increases above 1000 volts.

Timing for operation of the SCRs is developed from the trigger pulse obtained from the indicator. The TRIG IN pulse at A4P11-A1 (Figure 6-4 or 6-56) initiates operation of the first (delay) section of the dual one-shot multivibrator, U1. At the end of the 100µs delay, the second section is triggered. This section applies a positive, 16µs pulse to the base of Q1, which conducts. The resultant negative going pulse at the collector of Q1 causes a positive pulse to be applied between the gate and anode of CR1 and CR2 via T1 and T2. Transformer coupling is used to trigger the two SCRs simultaneously since their anode voltages differ by approximately 500Vdc. Diodes CR1 and CR2 on the charging SCR PCB are triggered into the conducting state by the 16µs pulses and remain in that state until the voltage across the PFN reaches 1000 volts. At that time, the magnetic field across A4L1 (see Figure 6-4 or 6-56) starts to collapse and the resulting increase in voltage reverse biases A4CR1, the isolation diode. The current through A4A1CR1 and CR2 drops to zero and the two SCRs revert to the nonconducting state where they will remain until the next TRIG IN pulse. The voltage across the PFN continues to increase until A4A4L1 is completely discharged. PFN voltage will remain at nearly the peak voltage until the discharge signal is generated since the leakage path is greater than 3M ohms.

PFN Discharge Circuits - The positive going TRIG IN signal (derived from the indicator trigger pulse) is amplified and shaped by A4A2Q1 (Refer to Figure 6-4 or 6-56, snubber driver PCB, A4A2) to produce a negative going 12 volt pulse at Q1-C. This signal turns on Q2 which in turn produces a positive pulse of current through the emitter-base junction of Q3. The voltage at the base of Q3 is limited to less than 1 volt by the action of the transistor junction. The collector voltage at the base of Q3 drops to approximately 1 volt for the duration of the TRIG IN signal. This causes a negative going pulse of 120 volts amplitude to be applied to the series connected primaries of A4A2T1 through T4. The series connection divides the total voltage swing so that each transformer sees a negative 30 volt pulse. The simultaneous pulses at the transformer secondaries are used to trigger the discharge SCRs A4A2CR2 through CR5. As in the charging SCR circuit, the series connected SCRs are used to increase the overall voltage holdoff capability of the circuit. Resistors R4, R7, R10, and R13 are connected in parallel with the SCRs to insure that the voltage drops across the individual SCRs are equal since the forward leakage current of the semiconductor devices may vary slightly from unit to unit. An RC network is also connected across each of the SCRs to compensate for variations in turn-on time of the devices.

When the SCRs are first triggered into conduction, the majority of the PFN voltage is dropped across the saturable reactor, A4L2. As the current increases, L2 reaches the point where its core is saturated and its reactance drops to nearly

zero. The result of the inclusion of L2 in the discharge path of the PFN is that the voltage across the primary of the magnetron pulse transformer, A4T1 rises much more rapidly than it would if it received the total PFN voltage continuously.

The two bi-filar wound secondaries of A4T1 allow a low dc filament voltage to be applied to the magnetron filament terminals along with the high voltage pulse output of T1 without having the pulse voltage difference between the two secondary windings. Each of the two secondaries is tapped so that either the X-band magnetron or the S-band magnetron can be used with the same transformer. Operation of the magnetron heater scheduling circuit which varies the magnetron filament voltage to compensate for duty cycle changes is described further on in this section.

The voltage between the positive terminal of the PFN and ground is applied to a sensing network comprising C10, R24, R25 and CR17 on the snubber driver PCB. The voltage across R24 is applied to the logic and fault PCB for fault detection purposes. Whenever the average voltage at the pick-off point increases above a fixed threshold higher than normal, it indicates that the PFN is not being discharged at the proper rate.

It should be noted that the timing of the charging and discharging cycles is such that the discharge circuit is triggered before the charging circuit operates (100μs delay between reception of the TRIG IN signal and triggering of the charging SCRs). As a result, the discharge cycle is completed long before the PFN is charged. A secondary result is that the first TRIG IN signal (when the indicator control is first set to TX ON) will not produce an rf output. Since the PFN will be charged before the second TRIG IN pulse, all subsequent triggers will produce outputs.

In the S-band MTR, the tailbiter circuit (A4A5) is used to prevent stretching of the short (0.05μs) pulse width by the S-band magnetron. The X-band unit does not exhibit the pulse stretching characteristic. When it is put into the circuit by energizing solenoid A4A5K1, the tailbiter circuit connects the high voltage output pulse from A4T1 to ground through A4A5R1, R3 and the saturable reactor, A4A5L1. The characteristics of L1 allow the full voltage of the pulse to be applied to the magnetron during the period before the core of L1 becomes saturated (approximately 0.05μs) and then be reduced to a low level which effectively shorts the magnetron input to ground. The rf output of the oscillator is cut off and the tube is prevented from being retriggered by reflections.

Magnetron Heater Scheduling Circuits (Refer to Figure 6-6 or 6-58) - Filament voltage for the magnetron is obtained from a floating (non-grounded) source in the LVPS. The source provides approximately 8Vdc which is connected to the magnetron through the magnetron heater scheduling PCB, where transistor A4A3Q3 is connected in series with the positive (cathode) line. The resistance of Q3 is varied by controlling its bias in the following manner. During each transmitter pulse a small positive pulse is felt at terminal 9 of A4A3. The positive going pulse is applied to A4A3Q4 and through R6, to rectifier, CR2 through saturable reactor, L1, and to meter rectifier, CR4.

The positive voltage rectified by CR2 is filtered by C2 to provide a dc level which is proportionally related to transmitter duty cycle, i.e. a change from short to medium pulse length causes the voltage across C2 to increase. The voltage across C2 is applied to the voltage divider (R1, VR2 and R2). A portion of this voltage is picked off at the arm of potentiometer, R1. Capacitor C1, connected across R1 removes the effect of the input signals which appear at the filament output terminal.

The voltage at the arm of R1 controls the conduction of Q1 which in turn controls Q2 and ultimately determines the resistance of Q3. Resistors R1 and R2 form a feedback path which causes the average filament voltage to be proportional to the voltage level stored on C2.

The positive transmitter pulses appearing at the base of Q4 are inverted and amplified to form negative pulses at Q4-C. These pulses are inverted by Q5 and decreased in amplitude by VR1 to produce the positive 15 volt acknowledge pulses which trigger the indicator timing circuits.

The pulses are also rectified by CR4 to produce a dc voltage which is stored by a filter capacitor, C8. The average dc level thus produced is converted to a current proportional to the magnetron duty cycle by R14 and applied to the monitor panel meter when the MAG I position is selected.

If for any reason the voltage across C8 should drop to less than about +1 Vdc, Q6 will cut off and the low level XMIT ON signal will go high. The removal of the ground (via Q6) will enable the flasher circuit on the logic and fault PCB, which in turn will cause the status indicator LED on the indicator to flash at a rapid rate.

25kW Variations - Operation of the 25kW solid state modulator is virtually identical to that of the 50kW and 60kW unit except for the following variations. Due to the lower power output of the 25kW unit, the maximum operating potential applied to the PFN circuits is +800Vdc. This in turn requires less holdoff capability in the discharge switch and so only three SCRs are used. Additionally, a despiker component board is added on the +800Vdc input line the purpose of which is to prevent transients which would occur when the HV on-off transistor (on the HV output PCB A2A6) is initially energized and HV is applied to the completely discharged modulator circuitry.

4.3.4   Logic and Fault Detection Circuits (A6)

The logic circuits which are used to determine the individual circuit conditions that must be set to match selected indicator control settings are located on the logic and fault PCB (A6). Refer to Figure 6-3 or 6-59 for a schematic diagram of this PCB.

Pulse Length Selection - Pulse length requirements are received from the indicator on two lines. They are both open circuited (short pulse) or individually grounded (medium or long pulse). The condition of the two lines is decoded to provide a low level (logic 0) enabling signal at the A input terminal of one of the three lockout pulse one-shot multivibrators, (A6U2-2, U5-1 and U5-2) and in parallel, places a low level at the data (D) input of one of the three data transfer latches (U9-1, U9-2, and U9-3). The same low level also appears at one input on each of three exclusive OR gates, U8-1, -2, and -3.

Assume that the short pulse has just been selected for the following circuit explanation:

The low at U8-1, pin 1 combined with the high at U8-1, pin 2 (due to the previously selected pulse length) causes the output at U8-1, pin 3 to go high. (Exclusive OR action causes the output to be high if the two inputs are different and low if the inputs are the same - either high or low.) The high at pin 1 of U10-1 causes its output to go low, setting the R-S latch, U4-2 and U4-3. Integrated circuit U4-2, pin 6 goes high and remains until a low is placed on the latch reset input, pin 10 of U4-3. The latch output is used in three places: (1) It activates the XMIT ENABLE OUT signal line through the OR gate U10-2 and Q14; (2) through U10-2 and U7-3 it allows the voltage at pin 5 (modulation input terminal) of the astable multivibrator, U12, to go high, (This allows the MV to operate at a higher frequency when it is enabled by a fault detection circuit.); (3) it enables operation of the 3Hz oscillator. The oscillator consists of the two one-shot multivibrators, U11-1 and U11-2. The two devices are timed to produce output pulses of 150ms each and are connected so that the termination of the output of one device triggers the other one-shot. A low level at pin 3 of U11 prevents operation of the circuit, but when the signal at this pin goes high it enables the circuit and provides a trigger (through an internal connection).

Operation of the 3Hz oscillator also requires that the signal at U11, pin 1 be low. This point is normally low when the MTR is being operated under control of the radar indicator. However, when the local control panel is being used (for test and alignment), U2-1 is the source of PRF trigger pulses and the signal at U11-1 goes high during the pulses. In this event, the trailing edge of the trigger will initiate action of the first 150ms one-shot.

The voltage transition from low to high at pin 5 of U11-1, which occurs at the start of the second 150ms period acts as a clocking signal for the latch, U9. At this time all data present at the D inputs (low at pin 13, high at pins 4 and 5) are latched into the device and appear at the Q output. Pin 15 therefore goes low and since the low applied to pin 2 of U8-1 matches the low at pin 1, the output at pin 3 goes low. The set signal is thus removed from U4-2, pin 4. In synchronysm with the latch clock, the signal at U11, pin 12 goes low which provides a reset signal to the R-S latch, U9-3.

During the second 150ms period of the oscillator, the XMIT ENABLE OUT signal is disabled by a signal through pin 9 of U10-2. The transmitter is therefore held off for 300ms after the initiation of a pulse width change. This allows for operation of the pulse width solenoids with no voltage applied to the PFN of the modulator and eliminates the chance of false triggering of the transmitter with the consequent damage to the high voltage circuits. Actual operation of the solenoids is performed by inverting the latch output signals by three sections of U7 and allowing this buffer inverter (U7) to control the current (on or off) through the driver transistors, Q11, Q12 and Q13. A high level at the base of a transistor biases the device into saturation and the resultant current flow energizes the solenoid which is connected to the collector of the particular transistor. When long pulse is selected, it is necessary to energize both A4A4K1 and A4A4K2 on the PFN PCB. This is accomplished by A6CR16 which allows current flow through the medium pulse solenoid, A4A4K1, to be conducted to ground through A6Q13. Diode action prevents A4A4K2 from being energized by A6Q12. The short pulse solenoid, A4A5K1, is only used in the S-band MTR.

<u>Trigger Pulse Generation</u> - Timing of the transmitter trigger pulses (PRF) is controlled by either the output of the local PRF generator (for test and alignment) or from the PRF generation circuits in the indicator (normal operation). The source of timing pulses is selected by the LOCAL PW SELECTOR switch on the MTR control panel.

When the LOCAL position is selected, and a jumper connected between A6E1 and A6E2, delayed positive feedback from pin 2 to pin 1 of U1-1 causes that device to oscillate. Variable resistor R2 is adjusted to set the oscillation frequency to 3.6kHz. Each positive going transition of the local oscillator for signal triggers the one-shot, A6U2-1. Timing components C3 and R4 cause the device to produce a 1.4µs pulse for each trigger. The signal at the pin 19 of the A6 PCB is a train of negative going 1.4µs pulses at a rate of 3.6kHz if the local (SHORT) position is selected. In the REMOTE position, the pulse rate is a function of the range selected at the indicator. A trigger pulse at pin 19 is differentiated by A6C4 and R5 and the positive going transition triggers the SCR gate drive one-shot, A6U3-1.

This device produces a 1µs (adjustable by R6) positive pulse at pin 5 which is applied to the three lockout one-shots and to the AND gate, U4-4. This gate is normally enabled unless a voltage fault is detected (refer to fault detection paragraph) and the resultant low at pin 11 causes Q1 to conduct. The 1µs positive pulse developed across the collector load of Q1 (R10) is applied to the snubber driver PCB in the modulator as a trigger. It is also connected to the MTR control panel as a sync pulse for test and alignment purposes.

The triggering pulse applied to the lockout one-shots will cause one of the devices to operate. Only one of these devices is enabled at a time by the decoded pulse length selection signals (see pulse length selection paragraph). The enabled device produces a negative going pulse at its complement ($\overline{Q}$ at pin 4 or 12) output terminal which inhibits operation of U3-1 (through the active low OR gate, U6-1) for a period which is appropriate to the PRF. This action prevents retriggering of U3-1 at a frequency greater than that designed for the particular pulse length.

<u>STC Pulse Generation</u> - The input trigger at pin 19 of the A6 PCB is also applied through inverter U1-6 to the STC one-shot, U3-2. This device produces a positive pulse at pin 13 which is less than 1µs in width. The exact width is adjustable by R22. The pulse output is inverted by U7-1 to bias Q3 into saturation for the duration of the pulse. The conduction of Q3 allows C20 to charge fully during the pulse period. (Asterisk components [*] not present on log [-2] version of this PCB.) At the termination of the pulse, the capacitor discharges through R27 and the STC control network (Q7 and associated components). The rate of discharge is determined by the setting of R40. The voltage waveform across the capacitance is inverted and amplified by Q4. The output of Q4 is applied to the receiver to reduce the gain during the early part of the receive period and thus reduce clutter due to nearby returns.

<u>Fault Detection Circuits</u> - Several critical points within the MTR are monitored by fault detection circuits which warn the operator (by flashing the transmit status indicator on the display indicator) and in some cases inhibit transmission until the fault has been cleared.

The current drawn from the high voltage power supply (LATCH I SENSE) and the current drawn during PFN discharge (SHUNT I) are monitored as the cathode voltage of SCR, Q9. If this voltage drops below the 11 volt level (set by VR2) the SCR goes into conduction and the lowered anode voltage places a logic 0 level at the input to inverter U6-2. The resultant high at pin 8 of U6 causes a low at the output of OR gate U10-1. The low at this point forces a high at the output of U4-2. Under either of these fault conditions the completion of a pulse length change cycle (refer to pulse length selection paragraph) will not cause the latch to reset until the fault has been cleared. The high voltage will be removed from the modulator (XMIT ENABLE OUT goes high) and the transmit status indicator LED will flash.

The voltage level of the HVPS is monitored at the VOLTAGE SENSE input (pin 6) and NAND gate U4-4. If the monitored voltage drops below the logic 1 threshold level, the voltage at U4-4, pin 11 will remain high and inhibit transmission of SCR drive pulses to the modulator until the fault has been cleared.

4.3.5   IF Amplifier and Mixer Assembly (A9)

The IF assembly is enclosed in a single shielded enclosure (see Figure 6-15 or 6-60). One end of the module accepts the balanced 45MHz IF signal from the X or S-band front end. The IF consists of a log amplifier providing sufficient gain to drive a video detector. The detected video is amplified and fed out of the module through 75 ohm coax cable to drive radar indicator circuits. Specifications for the IF amplifier assembly are as follows:

Noise Figure:	
IF	3.1dB
Overall	9.3dB
Bandwidths: (switchable)	25.6 MHz and 4.4 MHz
IF Center Frequency:	45.5 MHz
Tuning:	Narrowband is fixed tuned, wideband is synchronous with the narrowband.
Gain:	93 mV in wideband 75 mV in narrowband
Overload Recovery:	No paralysis or loss of linearity for 70dB overdrive.

Input Stage - The IF amplifier (refer to Figure 4-4 for simplified diagram) utilizes a cascode front end (Q1 and Q2) to provide low noise amplification with sufficient gain to mask the noise contribution of the following stages. Q1 exhibits a noise figure of less than 2dB at 45MHz.

Variable inductor L4, provides impedance matching between the mixer and Q1 and is adjusted to optimize the 25MHz receiver bandwidth.

IF Logging - The output of the cascode stage drives the input to the log IF section of the receiver. The log IF section consists of five identical stages followed by a sixth stage. The sixth stage differs from the others in order to effect bandwidth switching.

Figure 4-5 shows a typical log stage. Transistor Q1 is used as a common-emitter amplifier with a shunt-peaked collector load. Inductor L2, shown as an 8.8μH coil, consists of three and a half turns of wire on a ferrite bead core. Above 30MHz this coil is essentially resistive, i.e., it looks like a 400 ohm resistor. Inductor L2 provides a load resistor with low dc resistance with L3 providing the peaking. This L2, L3 combination in parallel with the input impedance of the following stage presents a 300 ohm load to Q1.

The small-signal gain of the stage is set by R2 in parallel with the series-connected R1, CR1 and CR2. The large-signal incremental gain, unity, is determined by R2 alone. Gain switchover from small-signal to unity gain occurs when the input signal swings positive or negative enough to turn-off CR1 or CR2 respectively. Note that the large signal output of such a stage is larger than the input signal. This is due to the summation in Q1 of current flow through R1 and the diodes with the current flow through R2. A cascade of such stages provides a logarithmic transfer characteristic.

Bandwidth Switching - Bandwidth switching can be accomplished either ahead of or after the logging. However, if a constant noise level and log slope are to be retained, any gain changes must be made ahead of the log section. A gain change after logging changes the log slope.
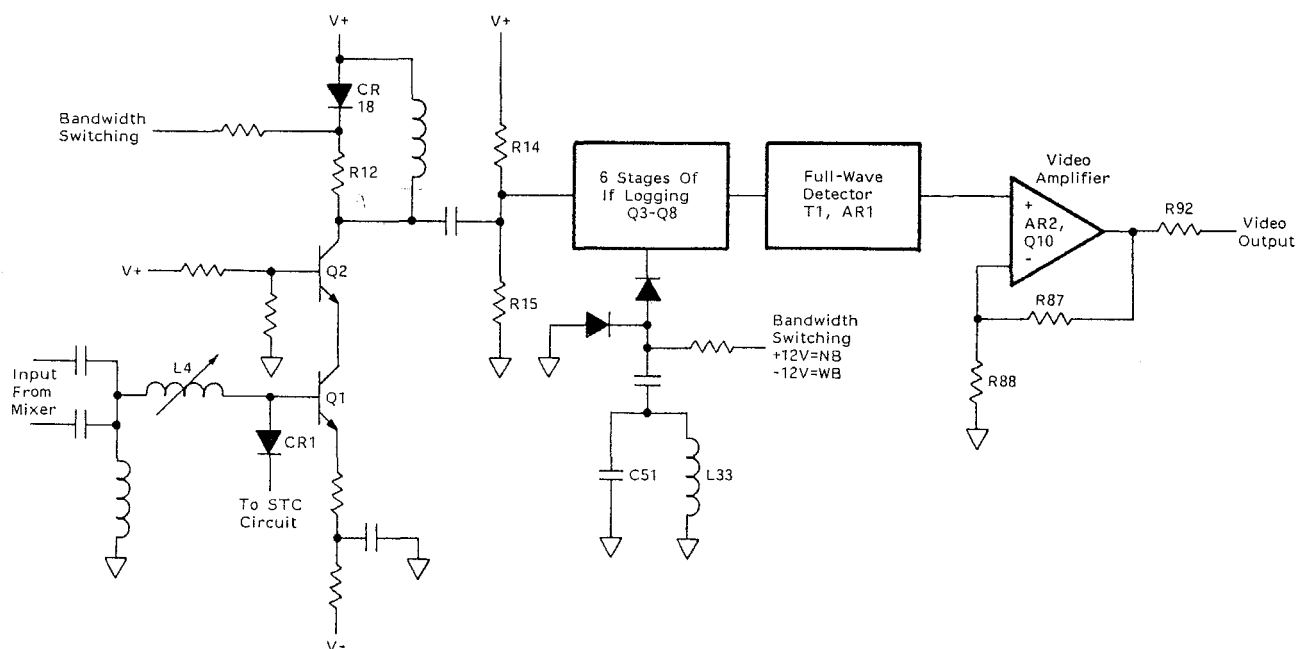
Figure 4-4 IF Amplifier Simplified Diagram

R2

R6
FULLY CCW

TRIGGER JACK
J5

+4V-

0V-

|←——→| SHORT
278μs

|←————→| MED
555μs
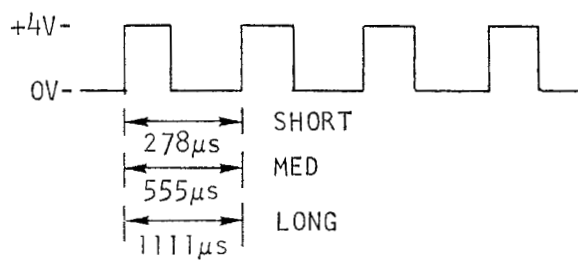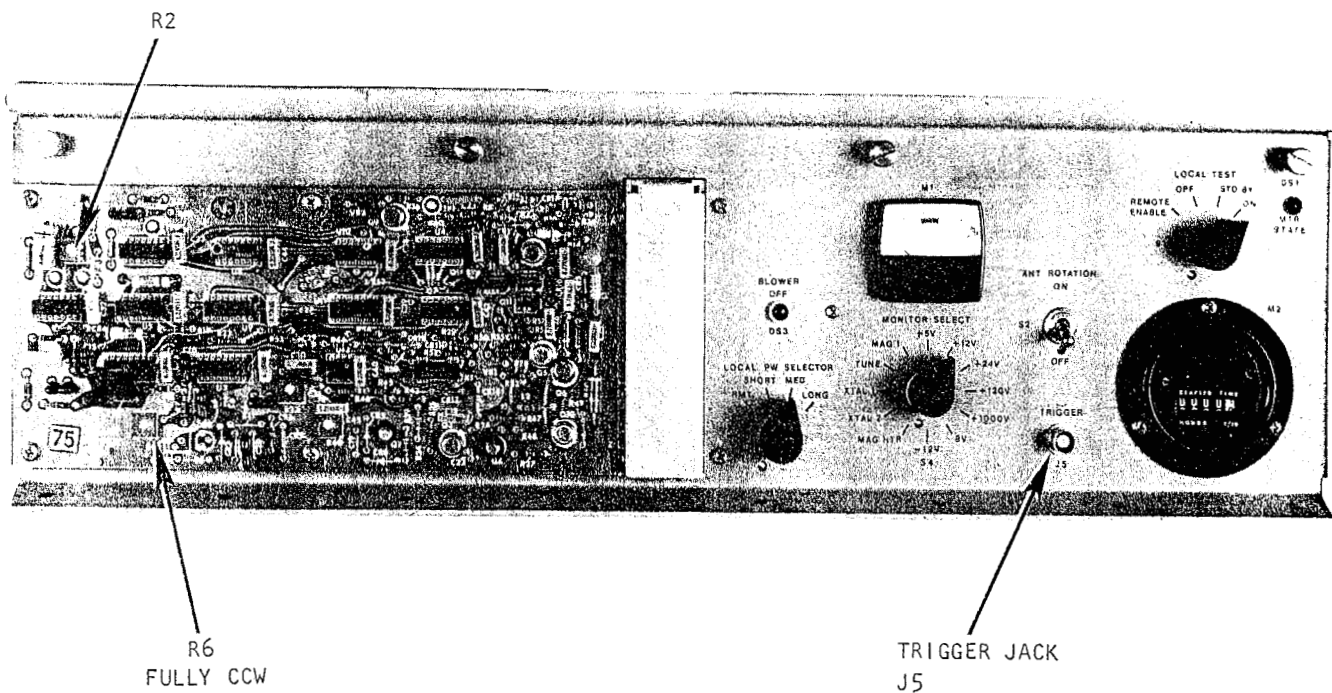
|←————————→| LONG
1111μs

Figure 5-10 Local PRF Adjustment (50kW and 60kW MTR)

5.7.3.4 Magnetron Current (Mag I) and Magnetron Heater Scheduling PCB
         Adjustment - Proceed as follows: (Refer to Figure 5-11)

1. Set LOCAL PW SELECTOR switch to LONG.

2. Set MONITOR SELECT switch to MAG I.

3. Adjust R23 on the HVPS mother PCB (A2A4) to obtain an indication
    in the upper portion of the green zone on meter M1.

4. Connect multimeter between TP1 (positive) and TP2 (negative) on mag-
    netron heater scheduling PCB (A4A3). Reading should be:

	New Magnetron	Aged Magnetron (1000-2000 Hrs.)
S-Band	4.2Vdc	4.6Vdc
X-Band	2.4Vdc	2.8Vdc

5. If necessary, adjust R1 on the magnetron heater scheduling PCB to
    obtain the specified reading.

6. Upon completion of this adjustment, reset HVPS A2A4 R23 to obtain a
    MAG I indication in the lower portion of the green zone on meter M1.
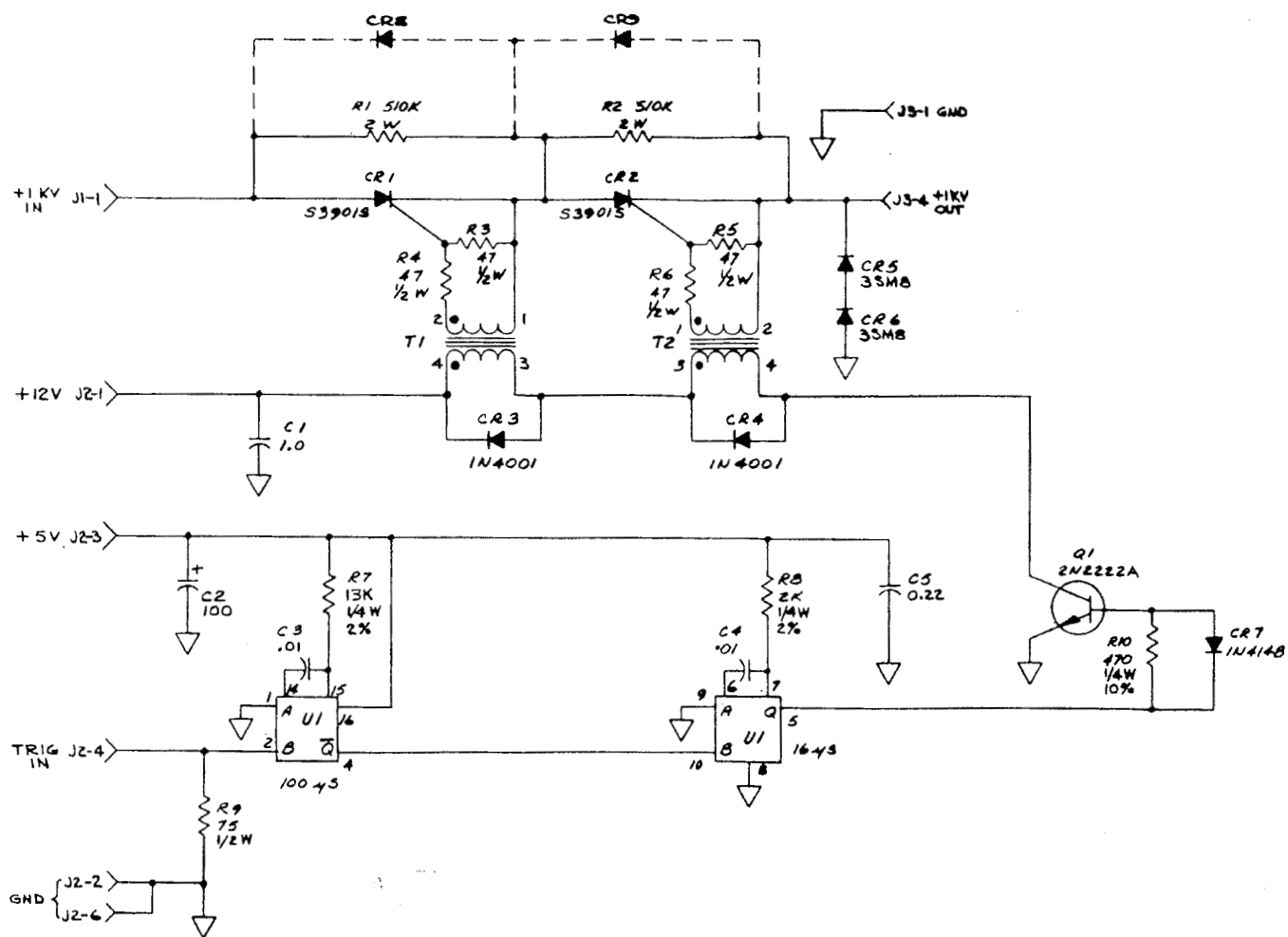
NOTES:
1. UNLESS OTHERWISE SPECIFIED—
   A. ALL RESISTORS ARE IN OHMS, 5%
   B. ALL CAPACITORS ARE IN MICROFARADS

C169268 Rev 3
Parts List: Table 6-24
Assy. Dwg.: Fig. 6-35

Figure 6-5   Charging SCR PCB A4A1
Schematic Diagram

Assy. Dwg.: Fig 6-37
Parts List: Table 6-26
C168803 Rev B

Figure 6-6   Magnetron Heater Scheduling
PCB A4A3
Schematic Diagram

NOTES:

UNLESS OTHERWISE SPECIFIED :
A - ALL RESISTORS ARE 1/4W ± 5%.
B - ALL CAPACITORS ARE IN MICROFARADS.

⚐ DESIGNATES SEPARATE GROUND PLANE.

SNUBBER-DRIVER ASSY A2
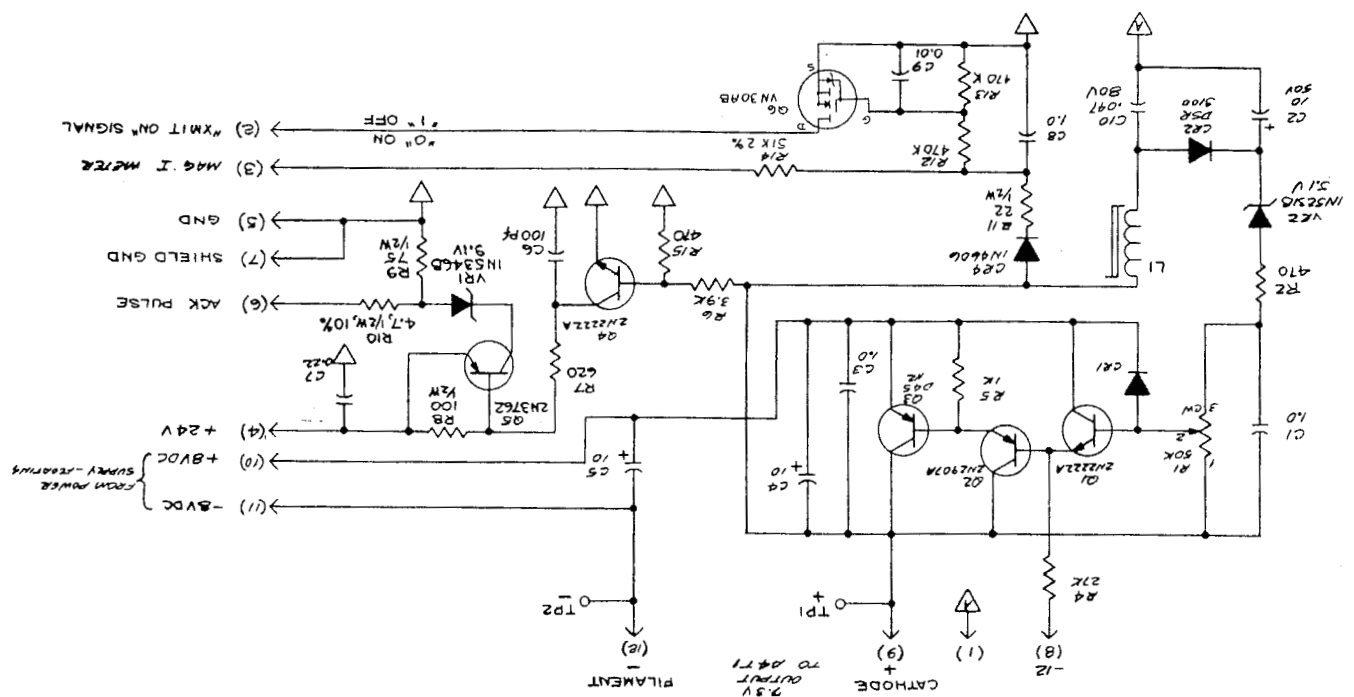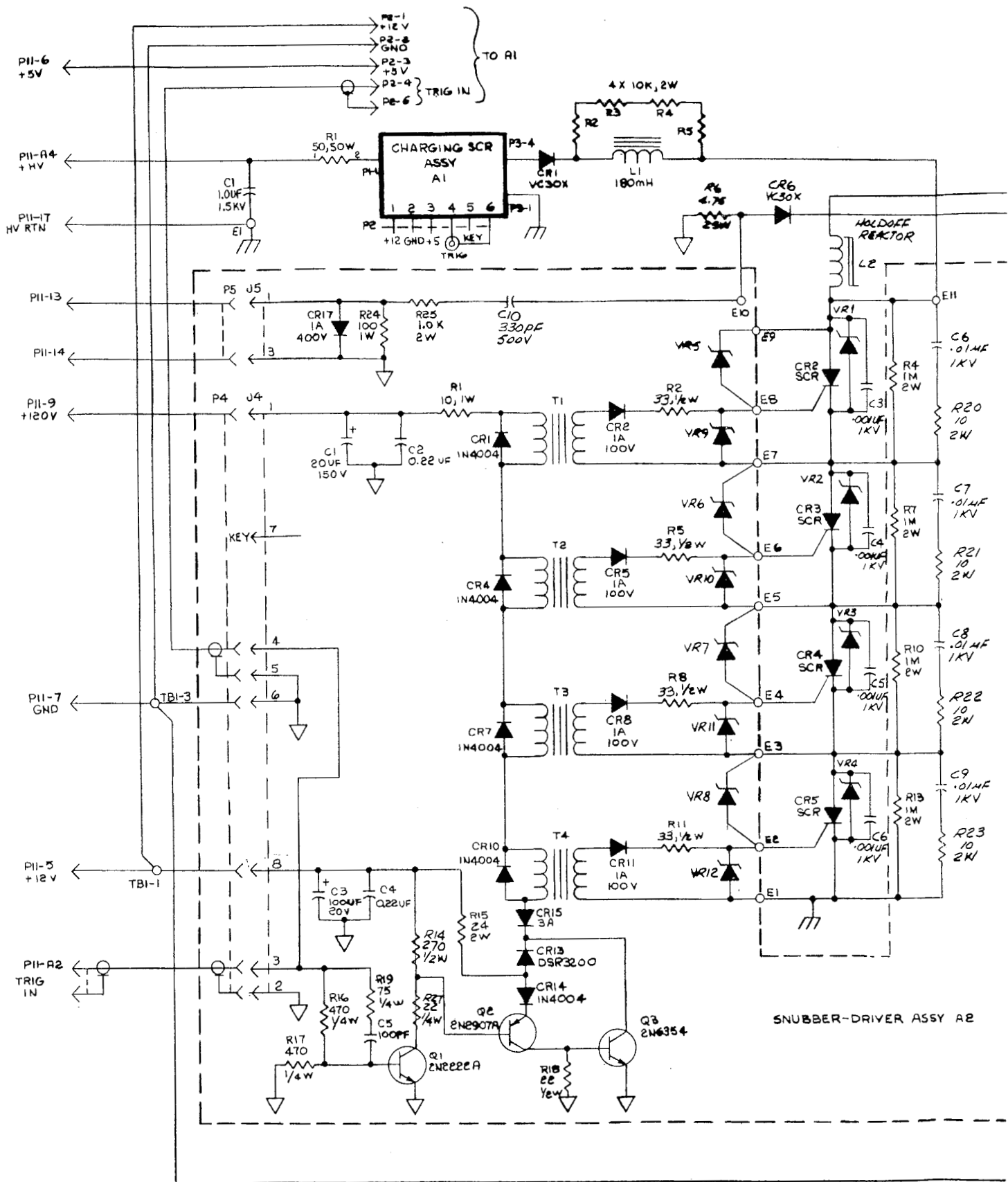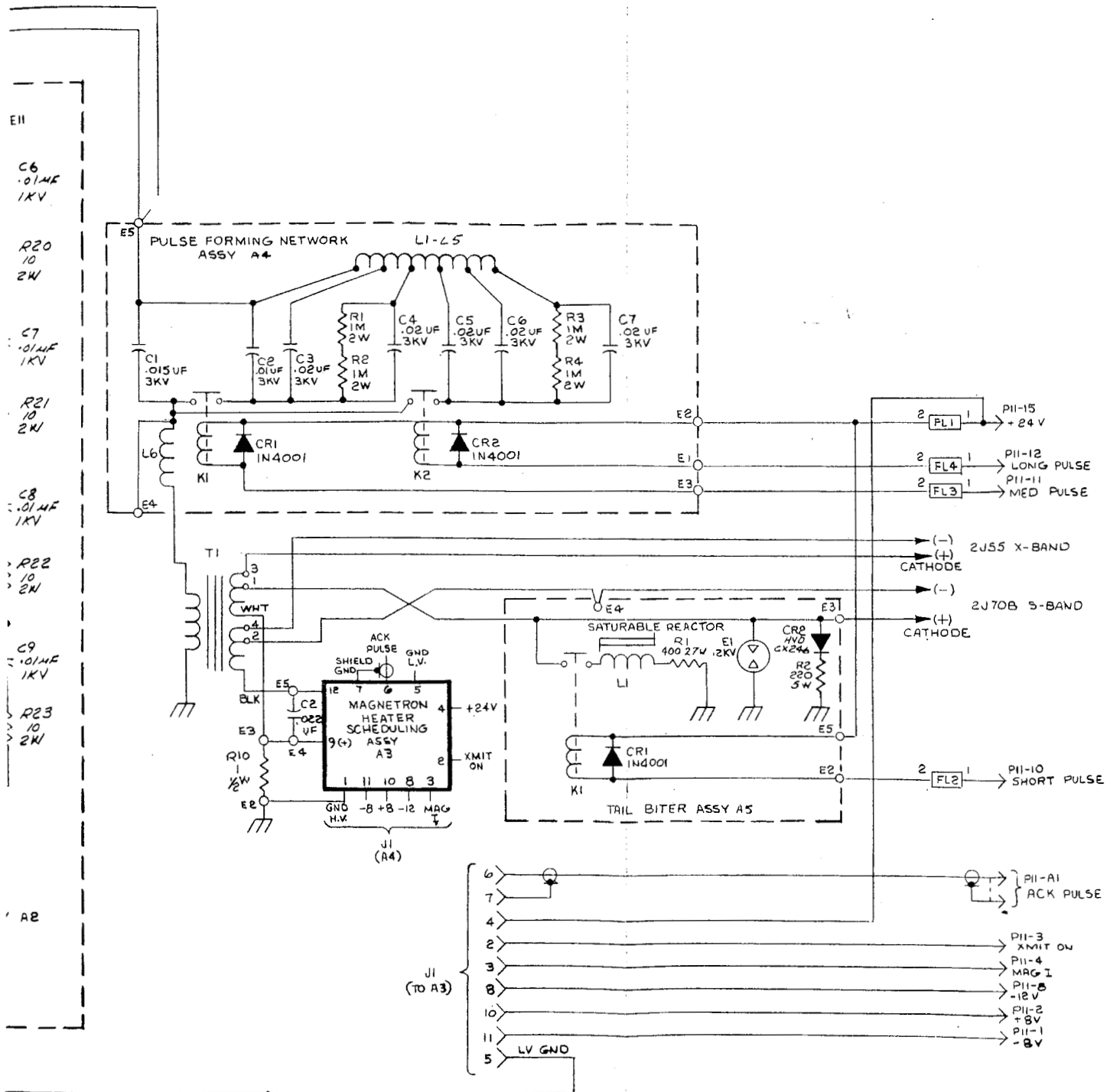
Figure 6-4   Solid State Modulator (SSM)
A4 Schematic Diagram

E169636 Rev E
Parts List: Table 6-22
Assy. Dwg.:   Fig. 6-33

RESOLVER DRIVE   FROM INDICATOR
→ RESOLVER DRIVE
PCB A10

NOTES:

1. THE MINUS SIGN (-) INDICATES
ACTIVE LOW SIGNAL

MTR STATE
(TO INDICATOR)

DS1

STC

BANDWIDTH SWITCHING (+12VDC NARROW
-12VDC WIDE BAND. SHORT PULSE)

MP ENABLE-

LP ENABLE-

SP SC
MP SC
LP SC

LOGIC & FAULT PCB A6

FROM INDICATOR

PRF
TRIGGER

LOCAL PW
SELECTOR
SWITCH
S5

TRIGGER

LOGIC
FAULT

P/O SNUBBER DRIVER
PCB A4A2   SHUNT

LOCAL
PRF

SHUNT I

TRANSMIT

ENABLE-

CHARGING SCR PCB
A4A1

P/O
LOCAL
TEST
SWITCH S1

SAFETY
INTERLOCK
S6

800VDC

CR1

100μs   16μs

120VDC

HV OUTPUT PCB A2A6

TRIGGER

SC
GA
DR

115VAC

800VDC

P/O SNUBBER
DRIVER PCB A4A2

FROM
RADAR
POWER

115VAC

POWER CONTROL
A1

POWER
SUPPLY
A2

DESPIKE BOARD A4A6

SYSTEM
ENABLE

TO/FROM

SYSTEM ENABLE
RETURN

INDICATOR

LV OUTPUT PCB A2A5

120VDC TO A4A2

6VDC FLOATING TO A4A3

24VDC TO A4A3, A4A4, A4A5

P/O
LOCAL
TEST
SWITCH S1

+12VDC & -12VDC TO ANALOG CIRCUITRY

+5.1VDC TO DIGITAL CIRCUITRY

-9.5VDC TO LO

TUNE CONTROL (-2 TO -8VDC) TO LO, TO INDICATOR

-16.5VDC & -15VDC TO PERFORMANCE MONITOR OPTION A12

NORMALIZED RESOLVER DRIVE (TO ANTENNA PEDESTAL)

)LVER DRIVE
'CB A10

X-AXIS & Y-AXIS RESOLVER SIGNAL (FROM ANTENNA PEDESTAL)

4

X-AXIS & Y-AXIS RESOLVER SIGNAL (TO INDICATOR)

4

VIDEO AMP
A11
(CONNECTED IN
DUAL SYSTEMS
OR SINGLE SYSTEMS
WITH HARD-WIRED
SLAVES)

VIDEO
TO
INDICATOR

X   X

LO

MIXER

LOG IF CAN ASSY A9

12VDC NARROW BAND, MEDIUM & LONG PULSE;
' PULSE)

MICRO
WAVE
ASSY
A8

SP SOLENOID ENABLE-
MP SOLENOID ENABLE-
LP SOLENOID ENABLE-

TAILBITER PCB
A4A5

RF
TO/FROM
ANTENNA

)RIVER
IUNT

CR6

CURRENT
SAMPLE

R6

CR PCB
A4A1

CR1   L1   L2
HOLDOFF
REACTOR

PFN PCB A4A4

16µs

SCR
GATE
DRIVE

CR2
THRU
CR4

T1

MAGNETRON
OSCILLATOR
M5039

MAG DRIVE

ER
B A4A2

MAG
FILAMENT
SAMPLE

MAG HEATER
SCHEDULING
PCB   A4A3

ACKNOWLEDGE PULSE (TO INDICATOR)

)ARD A4A6

R10

SOLID STATE
MODULATOR A4

TUNE TO
LO

ICATOR

TUNE TO
INDICATOR

? OPTION A12

Figure 4-2   25kW Solid State MTR
Block Diagram

Theory of Operation

Rev- (8/81)   4-4

RESOLVER DRIVE   FROM INDICATOR ───▶ **RESOLVER DRIVE PCB A10**

NOTES:

1. THE MINUS SIGN (-) INDICATES
   ACTIVE LOW SIGNAL
2. IN THE S-BAND MTR (60KW) THE LO
   IS SUPPLIED WITH ±12VDC.

MTR STATE
(TO INDICATOR)

DS1

STC
BANDWIDTH SWITCHING (+12VDC NARRO⹁
-12VDC WIDE BAND, SHORT PULSE)

MP ENABLE-

LP ENABLE-

LOGIC & FAULT PCB A6

SP S⹁
MP S⹁
LP S⹁

LOGIC FAULT

P/O SNUBBER DRIVER
PCB A4A2   SHUNT

PRF TRIGGER

LOCAL PW SELECTOR SWITCH S5

TRIGGER

LOCAL PRF

SHUNT I

CHARGING SCR PCB A4A1

CR1

TRANSMIT ENABLE-

P/O LOCAL TEST SWITCH S1

1000VDC

100µs   16µs

LATCH I
UNDER VOLTAGE SENSE
TRANSMIT ENABLE-

120VDC

HVPS A3

SAFETY INTERLOCK S6

1000VDC

TRIGGER

S⹁
G⹁
DR⹁

115VAC

P/O SNUBBER DRIVER PCB A4A2

FROM RADAR POWER

115VAC

POWER CONTROL A1

SYSTEM ENABLE

TO/FROM

SYSTEM ENABLE RETURN

INDICATOR

60VDC RESTART
60VDC RESTART ENABLE
+12 VDC TIMER SUPPLY

SOLID STATE MODULATOR ⹁

P/O LOCAL TEST SWITCH S1

115VAC

LVPS A2

120VDC TO A4A2
8VDC FLOATING TO A4A3
24VDC TO A4A3, A4A4, A4A5
+12VDC & -12VDC TO ANALOG CIRCUITRY
+5.1VDC TO DIGITAL CIRCUITRY
-9.5VDC TO LO (X-BAND ONLY) [2]

CONTACTOR CONTROL

TUNE CONTROL (-2 TO -8VDC) TO LO, TO INDICATOR

FROM SHIP'S POWER

CONTACTOR K1

TO ANTENNA PEDESTAL

NORMALIZED RESOLVER DRIVE (TO ANTENNA PEDESTAL)

X-AXIS & Y-AXIS RESOLVER SIGNAL (FROM ANTENNA PEDESTAL)

X-AXIS & Y-AXIS RESOLVER SIGNAL (TO INDICATOR)

LVER DRIVE
CB A10

VIDEO AMP
A11
(CONNECTED IN
DUAL SYSTEMS
OR SINGLE SYSTEMS
WITH HARD-WIRED
SLAVES)

VIDEO
TO
INDICATOR

LOG IF CAN ASSY A9

LO

MIXER

MICRO
WAVE
ASSY
A8

RF
TO/FROM
ANTENNA

VDC NARROW BAND, MEDIUM & LONG PULSE;
PULSE)

SP SOLENOID ENABLE-
MP SOLENOID ENABLE-
LP SOLENOID ENABLE-

TAILBITER PCB
A4A5

RIVER
INT

CR6

CURRENT
SAMPLE

R6

R PCB
A4A1

CR1   L1   L2
HOLDOFF
REACTOR

PFN PCB A4A4

16µs

SCR
GATE
DRIVE

CR2
THRU
CR5

T1

MAG DRIVE

MAGNETRON
OSCILLATOR
2J55 X-BAND
2J70B S-BAND

A4A2

MAG
FILAMENT
SAMPLE

MAG HEATER
SCHEDULING
PCB   A4A3

ACKNOWLEDGE PULSE (TO INDICATOR)

R10

ODULATOR A4

TUNE TO
LO

ATOR

TUNE TO
INDICATOR

Figure 4-1   50kW and 60kW Solid State
MTR Block Diagram

Theory of Operation