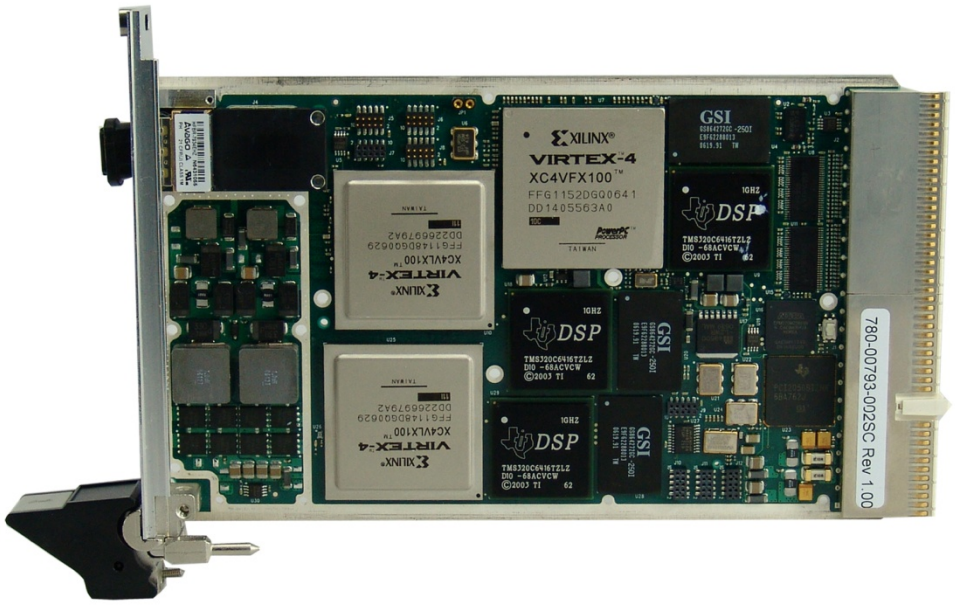
Digital Receiver Technology, Inc.

Approved for Public Release

WPM3
Wireless Processor Module 3



DESCRIPTION

The WPM3 processes wideband digital IF signals, producing audio and narrowband IF data streams for further processing. The WPM3 occupies one 3U CompactPCI slot of the DRT1000C system. The WPM3 can receive up to eight channels of wideband digital IF data from the J2 backplane connector. The WPM3 can simultaneously receive up to four additional channels of wideband digital IF data and/or transmit up to four channels of wideband digital IF data through a front-panel quad optical transceiver. The WPM3 independently tunes/processes narrowband IF channels using dynamically reconfigurable Field Programmable Gate Arrays (FPGAs).

The maximum bandwidth the WPM3 can process in any one narrowband channel is dependent on the sample rate selected. The WPM3 can also act as a signal generation platform for transmit applications. The DSP control processor has a built-in PCI bus interface. Normally, the WPM3 will provide demodulated audio data and other information to a system wide TDM ScBus. The WPM3 ScBus controller is implemented within an FPGA for maximum flexibility. The WPM3 generates all required non-standard voltages. Only the standard +3.3V and +5.0V CompactPCI voltages are needed at the backplane connectors.

Various power-down modes are available, scalable with the application and requirement.

Features

- High-Performance Fixed-Point Digital Signal Processors (TI C6416T), each running at 1 GHz, with an external 64M bit SBSRAM operating at 133MHz. Built-in Viterbi and Turbo decoder coprocessors.
- Large banks of SDRAM provide for advanced exploitation features. The control FPGA has a pair of 2G bit SDRAMS, FPGAA and FPGAB each have a 1G bit SDRAM device attached. The SDRAMS are all 16 bits wide and are operated at DDR 200 MHz.
- Large FPGAs (Xilinx XC4VLX100-11FFG1148I) provide an unprecedented capability to perform various intensive signal processing functions, including application-specific Digital Down Conversion (DDC) and Digital Up Conversion (DUC), flexible sample rates (polyphase filter-based resampler), matrix inversion, FFT processing, high speed spectral processing and other applications
- Configurable FPGA switch (Xilinx XC4VFX100-11FFG1152I) allows extremely flexible routing of wideband digital IF data streams. Route up to eight wideband digital IF data streams to/from J2 backplane connector. Route up to eight wideband digital IF streams (four in, four out) to/from front-panel optical transceiver at up to 3.125Gbps, including encoding overhead.
- CompactPCI (Rev 2.1) compliant interface.
- Optional 4-channel optical transceiver. Each channel provides a full duplex, 3.125 Gbps path for 8B/10B encoded data. Useful for IF data extraction for external data processing. Optical interface is a standard MTP/MPO ribbon fiber interface.
- On-board temperature measurement and built-in test capability.
- Future enhancements possible via propitiatory Mezzanine interface.

Physical/Environmental

• **Operating Temperature Range***	0°C to +60°C (+32 to +140°F) inlet air temperature of any DRT system in which the module is installed
• **Size**	Single-slot: 0.8” (20.32 mm) wide 3U: 3.9” x 6.2” (100 mm x 160 mm)
• **Weight**	~700g (1.56 lbs)
• **Power Consumption**	<25 Watts (typical), <40 Watts (custom applications)

*Consult factory for extended temperature range.

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