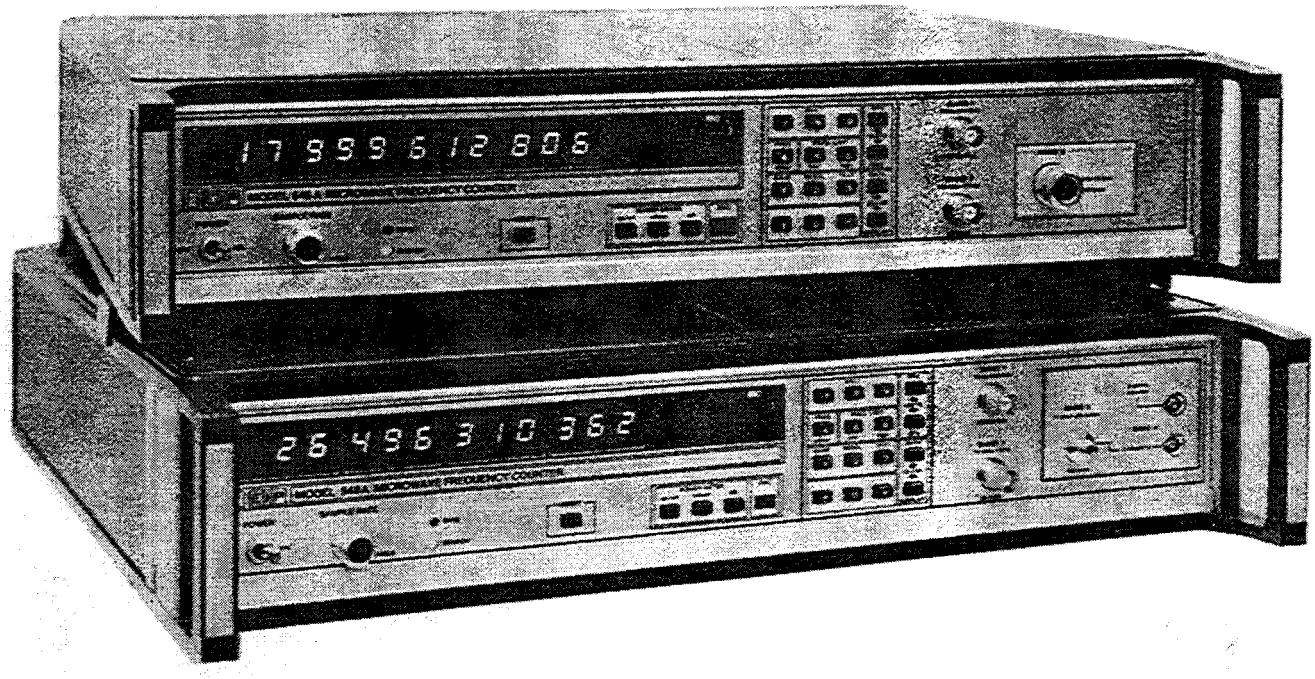

Models 545A & 548A
Microwave Frequency Counters

EIP Microwave, Inc.
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Manual Part Number: 5580021-04
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List of Effective Pages

This List of Effective Pages gives the most recent date on which the technical material on any given page was altered. If a page is simply rearranged due to a technical change on a previous page, it is not listed as a changed page. Within the manual, changes are marked with an arrowhead in the margin.

Pages	Effective Date
FIRST EDITION	*April 1981*
SECOND EDITION	*April 1983*
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FIRST EDITION ..... *April, 1981*

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FOURTH EDITION..... ..... *August 1986*

FIFTH EDITION..... *October 1986*

SIXTH EDITION..... *January 1987*

SEVENTH EDITION ..... *June 1987*

Certification

EIP Microwave certifies that this instrument was thoroughly inspected and tested, and found to be in conformance with the specifications noted herein at time of shipment from factory.

Warranty

EIP Microwave warrants this counter to be free from defects in material and workmanship for one year from the date of delivery. Damage due to accident, abuse, or improper signal level, is not covered by the warranty. Removal, defacement, or alteration, of any serial or inspection label, marking, or seal, may void the warranty. EIP Microwave will repair or replace at its option, any components of this counter which prove to be defective during the warranty period, provided the entire counter is returned PREPAID to EIP or an authorized service facility. In-warranty counters will be returned freight prepaid; out-of-warranty units will be returned freight COLLECT. No other warranty other than the above warranty is expressed or implied.

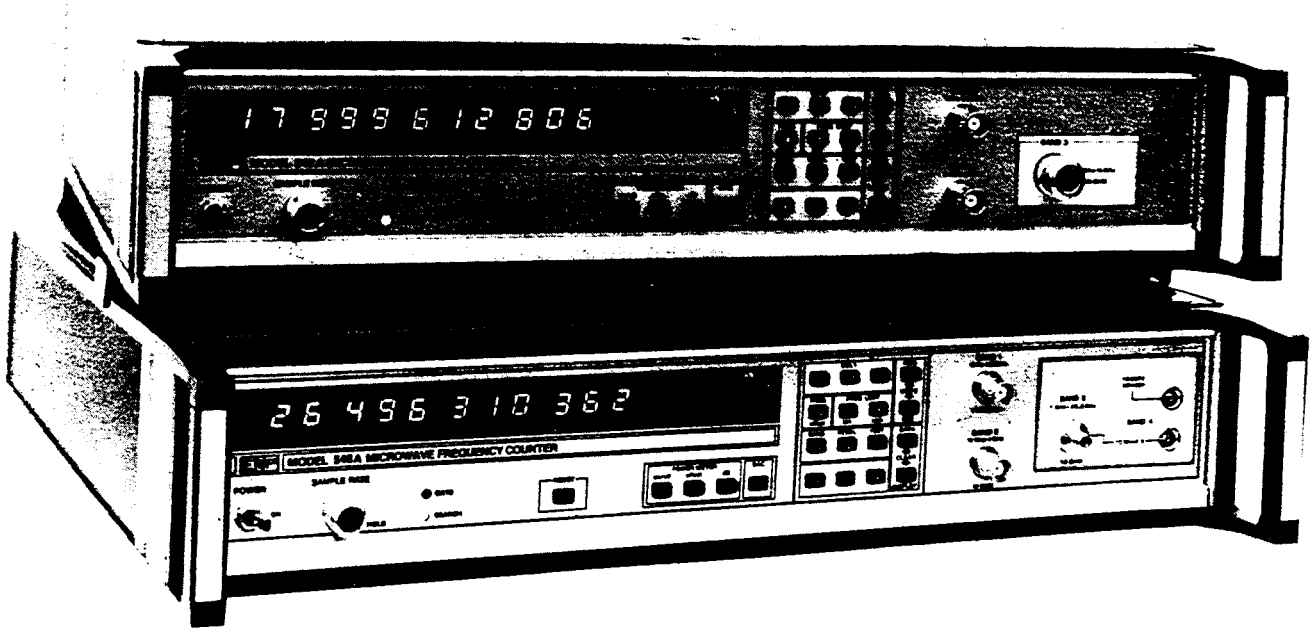
Table of Contents

Table of contents, continued

List of Illustrations

List of Illustrations, continued

Section 1
General Information



DESCRIPTION

The 54XA series counters are microprocessor-based heterodyne instruments. The 545A and 548A span the frequency range from 10 Hz to 18 GHz and 10 Hz to 26.5 GHz, respectively. The model 548A, when equipped with frequency extension capability (Option 06), is used in conjunction with a remote sensor (See Model 590) to measure up to 110 GHz.

Using keyboard control, the 54XA series counters provide frequency offsets and frequency selectivity. Options include Power Measurement, full Systems capability via GPIB or BCD/Remote Programming and D/A Converter output.

Full frequency range is covered in three bands. Band 1 is a high impedance input (1 M ohm/20 pF), and spans a 10 Hz to 100 MHz range, with a sensitivity of 25 mV RMS. Band 2 has an input impedance of 50 ohms, a 10 MHz to 1 GHz range, with a sensitivity of −20 dBm. Band 3 has an input impedance of 50 ohms nominal over a range of 1 GHz to 18 (or 26.5) GHz, and a sensitivity to −30 dBm. For frequencies above 26.5 GHz a remote sensor, with an appropriate waveguide input, is called Band 4.

Measurements are presented on a 12 digit LED display that is sectionalized to read GHz, MHz, kHz, and Hz. When the optional power measurement function is activated, the digits on the far right display power in dBm with .1 dB resolution, and frequency resolution is limited to 100 kHz.

SPECIFICATIONS

BAND 1	
RANGE	10 Hz to 100 MHz
SENSITIVITY	25 mV rms
IMPEDANCE	1 MΩ/20 pF
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	120 V rms *
DAMAGE LEVEL	150 V rms *
	* (Above 1 KHz max. input will decrease at 6 dB/octave down to 3.0 V rms.)

BAND 2	
RANGE	10 MHz to 1 GHz
SENSITIVITY	-20 dBm
DYNAMIC RANGE	30 dB
IMPEDANCE	50Ω Nominal
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	+10 dBm
DAMAGE LEVEL	+27 dBm
ACQUISITION TIME	< 50 msec

BAND 3		
RANGE	1 GHz to 18 GHz (26.5 GHz for model 548A)	
SENSITIVITY	-30 dBm: 1.0 GHz to 12.4 GHz -25 dBm: 12.4 GHz to 18 GHz	-20 dBm: 18 GHz to 22 GHz -15 dBm: 22 GHz to 26.5 GHz
DYNAMIC RANGE	1 GHz to 12.4 GHz, 37 dB 12.4 GHz to 18 GHz, 32 dB	18 GHz to 22 GHz, 27 dB 22 GHz to 26.5 GHz, 22 dB
IMPEDANCE	50Ω Nominal	
CONNECTOR	Model 545A - Precision type N, (female) Model 548A - APC - 3.5 (female)	
MAX. INPUT LEVEL	+7 dBm	
DAMAGE LEVEL	5 Watts (+37 dBm)	
ACQUISITION TIME	~ 250 msec Independent of frequency	
AUTO AMPLITUDE DISCRIMINATION	(Automatic amplitude discrimination of two frequencies) 10 dB	
FM MODULATION	20 MHz P-P up to 10 MHz rate	
VSWR	< 2.5:1 typical	
FREQUENCY LIMIT	Keyboard control of desired limits (standard). Counter will measure largest signal within programmed limits. Signal outside operating band must be separated by at least 100 MHz from either limit. For signals more than 10 dB above desired signal, separation is typically 200 MHz	

TIME BASE	
FREQUENCY	10 MHz TCXO
AGING RATE	$< \lvert 1 \times 10^{-7} \rvert$ per month
SHORT TERM	$< \lvert 1 \times 10^{-9} \rvert$ rms for one second averaging time.
TEMPERATURE	$< \lvert 1 \times 10^{-6} \rvert$ 0° to + 50°C
LINE VARIATION	$< \lvert 1 \times 10^{-7} \rvert \pm 10\%$ change.
WARM UP TIME	NONE
OUTPUT FREQUENCY	10 MHz, square-wave, 1 V p-p minimum into 50 ohms.
EXT. TIME BASE	Requires 10 MHz, 1 V p-p minimim into 300 ohms.

SPECIFICATIONS, continued

GENERAL	
RESOLUTION	Front panel keyboard input select 1 Hz to 1 GHz
MEASUREMENT TIME	1 msec for 1 KHz resolution 1 sec for 1 Hz resolution
DISPLAY	12 digit LED sectionalized
ACCURACY	± 1 count ± time base error
TEST	Front panel selected diagnostics
SAMPLE RATE	Controls time between measurements variable from 100 msec typ. to 10 sec. Switchable Hold position holds display indefinitely.
RESET	Resets display to zero and initiates new reading
OFFSETS	Keyboard control of frequency offsets (standard) and power offsets (standard with power measurement Option 02). Displayed frequency (power) is offset by entering value to 1 Hz resolution (0.1 dB power).
OPERATION TEMP.	0°C to 50°C
POWER	100/120/220/240/VAC ± 10% (selectable) 50 to 60 Hz, 60 VA typical
WEIGHT, NET	~ 26 lbs. (11.8 kg)
WEIGHT, SHIPPING	~ 32 lbs. (14.5 kg)
DIMENSIONS (HWD)	3.5" x 16.75" x 14.0" (89 mm X 425 mm X 356 mm)
ACCESSORIES FURNISHED	Power Cord and Manual

BAND 4
Used with 578/06 Counter and 590 Frequency Extension Kit

OPTION	91	92	93	94	95	96
SELECT BAND	41	42	43	44	42 or 43	41 or 42
Waveguide Band	Ka	U	E	W	V	Q
Range	26.5–40 GHz	40–60 GHz	60–90 GHz	90–110 GHz	50–75 GHz	33–50 GHz
Sensitivity (typ)	-25dBm (-20 dBm min)	-25 dBm	-25 dBm	-25 dBm	-25 dBm	-25 dBm
Waveguide Size	WR-28	WR-19	WR-12	WR-10	WR-15	WR-22
Waveguide Flange	UG-599/U	UG-383/U	UG-387/U	UG-387/U	UG-385/U	UG-383/U
Max. Input (typ)	+5 dBm	+5 dBm	+5 dBm	+5 dBm	+5 dBm	+5 dBm
Damage Level	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+10 dBm
Aquisition Time (typ)	<2.5 sec	<2.5 sec	<2.5 sec	<2.5 sec	<2.5 sec	<2.5 sec

EXAMPLE: If desired measurement is 60 - 90 GHz, the required equipment is:

Model 578 with Option 06 - Extended Frequency and
Model 590 - Extended Frequency Cable Kit with Option 93 - Remote Sensor

SPECIFICATIONS, continued

OPTIONS **See Section 10 for detailed information.**

01 D TO A CONVERTER
DAC will convert any three consecutively displayed digits into an analog voltage output on rear panel.

02 POWER METER
1 to 18/26.5 GHz will measure sine wave amplitude to 0.1 dBm resolution from sensitivity to -10 dBm; from -10 dBm to overload and display 0.2 dBm resolution simultaneously with frequency.
Power offset to 0.1 dB resolution, selectable from front panel.
Option will not degrade the basic performance of the counter.

TIME BASE OSCILLATOR OPTIONS:

	03	04	05
AGING RATE/24 HOURS (After 72 hour warm-up)	$< \lvert 5 \times 10^{-9} \rvert$	$< \lvert 1 \times 10^{-9} \rvert$	$< \lvert 5 \times 10^{-10} \rvert$
SHORT TERM STABILITY (1 second average)	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms
0°to +50°C TEMPERATURE STABILITY	$< \lvert 6 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$
± 10% LINE VOLTAGE CHANGE	$< \lvert 5 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$

06 EXTENDED FREQUENCY CAPABILITY –548A
Use in conjunction with models 590 Frequency Extension kit

07 REMOTE PROGRAMMING/BCD OUTPUT

08 GPIB – Provides programming and output capability per IEEE 488-1978.

09 REAR INPUT

10 CHASSIS SLIDES

Section 2
Installation

SAFETY

The Model 545A/548A Microwave Counter is a Safety Class I instrument. This instrument has been designed and tested according to international safety requirements. This manual contains information, cautions, and warnings that must be followed by the service person to ensure safe operation and to retain the instrument in safe condition.

SAFETY SYMBOLS

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure or practice which, if not correctly performed or adhered to, could result in personal injury.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure or practice which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

OVERALL SAFETY CONSIDERATIONS

WARNING

Before this instrument is switched on, the protective earth terminals of this instrument must be connected to the protective conduction of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective earth (grounding) conductor.

WARNING

Only fuses with the required rated current, voltage, and specified type should be used. Do not use repaired fuses or short-circuited fuse holders. To do so could cause a shock or fire hazard.

WARNING

Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

WARNING

All protective earth terminals. extension cords, autotransformers, and devices connected to this instrument should be connected to a socket outlet provided with a protective earth contact. Any interruption of the protection will cause a potential shock hazard that could result in personal injury.

INSTALLATION

No special installation instructions are required. The counter is a self-contained bench or rack mounted unit and only requires connection to a standard 100/120/220/240V 50-60 Hz power line for operation.

CAUTION

Check current rating of counter fuse and setting of rear panel VAC selector switch before applying power to counter.

COUNTER IDENTIFICATION

This counter is identified by two sets of numbers, the model number 545A or 548A and a serial number that is located on a label affixed to the rear panel. Both numbers must be mentioned in any correspondence regarding this counter.

SHIPPING

Should it be necessary to ship the counter, wrap it in heavy plastic or kraft paper and repack in original container if available. If the original container cannot be used, use a heavy (275-pound test) double-walled carton with approximately four inches of packing material between the counter and the inner carton. Seal the carton with strong filament tape or strapping. Mark the carton to indicate that it contains a fragile electronic instrument.

STORAGE

The instrument should be stored in an environment that is protected from sand, dust, and other contaminants at an altitude of less than 12,000 m (40,000 ft) and should not be exposed to temperatures beyond the range of -40° C to 75° C, humidity above 95 ±5% (75 ±5% above 30°C, 45 ±5% above 30°C), dripping water, or vibration shock of greater than 2 g.

PERFORMANCE CHECKOUT PROCEDURE

The following procedure can be performed without special tools or equipment.

1. Turn counter power switch off. Check fuse rating and setting of AC POWER switch on rear panel.
2. Connect power cord to 100/120 or 220/240 V, 50-660 Hz single-phase power source. The ground terminal on the power cord plug should be grounded.
3. Turn POWER switch on. Dashes will be displayed for about one second, followed by all 0's. This indicates that automatic self-check has been completed.
4. Press TEST 0 1. Display should read 200 000 000 ±1.
5. Press TEST 0 2. Display should read all 8's and all annunciators should be lit.
6. Press TEST 0 3. Each display segment should light in turn.
7. Press TEST 0 4. Each digit should light in turn.
8. This completes the performance checkout procedure.

Section 3
Operation

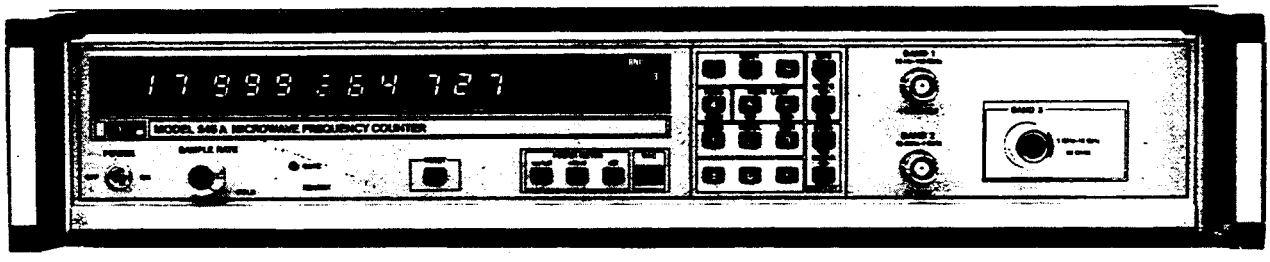


Figure 3-1. Front Panel, Model 545A

FRONT PANEL CONTROLS AND INDICATORS

DISPLAY

- The 12 digit LED display provides a direct numerical readout of a measurement or of an input frequency. The frequency readout is displayed in a fixed position format that is sectionalized in GHz, MHz, kHz and Hz. Power information is displayed in dBm to 0.1 dB resolution, on the three right-most digits. When both power and frequency are displayed, frequency resolution is limited to 100 kHz.

- POWER switch turns counter on.

- SAMPLE RATE/HOLD varies time between measurements from 0.1 to 10 seconds (nominal). (Gate time is added to sample time, thus the minimum reading for 1 Hz resolution is 1.1 seconds.) The last reading is retained indefinitely in HOLD.

- GATE lights when the signal gate is open and a measurement is being made.

- SEARCH lights when the counter is not locked to an input signal.

- RESET manually over-rides all controls, resets the counter and converter, and initiates a new reading.

OPERATING STATUS

The operating status of the counter is indicated by a series of LEDs. When the counter is displaying input data, instead of a measurement, the appropriate LED status indicator will flash.

- REMOTE lights to indicate that front panel controls are disabled, and that the counter is being controlled by the GPIB option (08), or by the BCD/Remote Programming option (07).

- EXT REF lights to indicate the counter is set to an external time base reference.

CAUTION

When EXT REF lights it does NOT indicate that correct signal level has been applied.

- dBm lights to indicate that the Power Meter option (02) is active.

- FRQ LMT, LOW/HIGH lights when frequency limits for Band 3 operation have been selected.

- OFFSET, PWR/FRQ lights when power and/or frequency offsets are stored in the counter memory.

- Band 1, 2, 3, 41, 42, 43, 44 light to indicate which operating range has been selected. When any Band 4 annunciator is lit it indicates that the Extended Frequency Capability option (06) has been selected (Available on 548A only).

- DAC lights to indicate that the Digital-to-Analog Converter option 01 is active.

- MLT lights to indicate the multiplier function is active.

POWER METER/DAC OPTION KEYBOARD

Four keys control the operation of these options.

- ON/OFF push button activates/deactivates power meter .

- OFFSET push button activates the power offset function.

- dB pushbutton acts as a terminator for the input of power offsets.

- DAC pushbutton, followed by two digits (00-12), activates the DAC option. The number keyed in will select the most significant digit (00 = OFF, 01 = 1 Hz, 12 = 10 GHz).

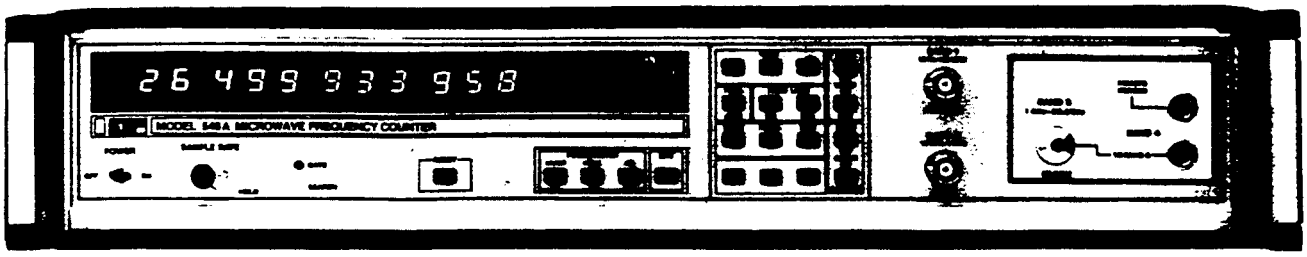


Figure 3-2. Front Panel, 548A

SIGNAL INPUT

- Band 1 input connector (BNC female) has a nominal input impedance of 1 Meg ohms, shunted by 20 pF. It is used for measurements in the range of 10 Hz to 100 MHz.
- Band 2 input connector (BNC female) has a nominal input impedance of 50 ohms. It is used for measurements in the range of 10 MHz to 1 GHz.
- Band 3 input connector on the model 545A is a precision type N female. It is used for counter operation in the range of 1 GHz to 18 GHz. Model 548A has an APC-3.5 female connector that is used for operation in the range of 1 GHz to 26.5 GHz.
- Band 4 is used in conjunction with the Extended Frequency capability option (06), the Model 590 Frequency Extension Cable kit and a remote sensor. Remote sensors are options to the Model 590 and cover waveguide bands from 26.5 to 110 GHz.

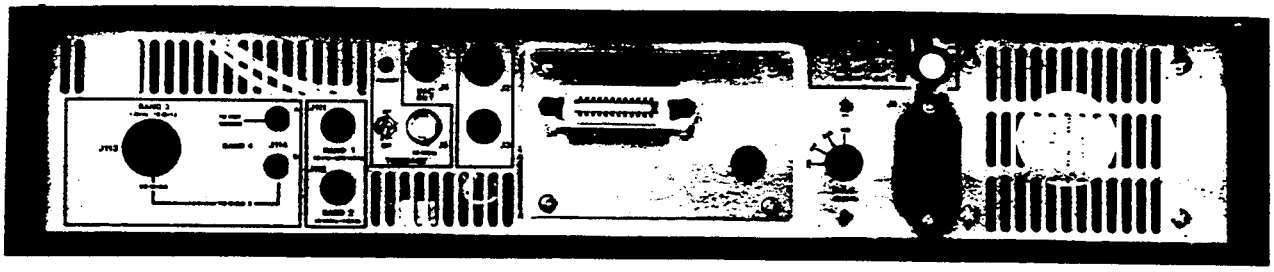


Figure 3-3. Rear Panel

REAR PANEL CONTROLS AND CONNECTORS

- Spaces labeled BAND 1, BAND 2, BAND 3, BAND 4, and TO REMOTE SENSOR are used for those connectors in instruments equipped with Option 09, Rear Panel Input.
- TIME BASE ADJUST control is used with options 03, 04, or 05 only. Screwdriver adjustment allows precise setting of the internal ovenized crystal oscillator.
- TIME BASE INT/EXT switch selects either the internal time base or an external 10 MHz reference.
- TIME BASE connector (BNC female) allows monitoring of internal 10 MHz time base, or input of an external 10 MHz reference.
- DAC OUT connector provides a voltage analog to any specified three digits of frequency displayed, in instruments equipped with Option 01, D to A Converter.
- GPIB connector is used with the IEEE 488 - 1978 General Purpose Interface Bus.
- FUSE provides overload protection. Use a 1 amp slow-blow MDL type fuse for 100/120 V operation. Use a .50 amp slow-blow FST type fuse for 220/240 V operation.
- VAC SWITCH sets the operating voltage of the counter to match power line. There are 4 settings: 100, 120, 220, and 240 VAC. Counter will operate at voltages within ±10% of selected line voltage, at frequencies of 50 to 60 Hz.

CAUTION

Switch setting and fuse rating must match power line voltage.

- AC POWER connector accepts the power cord supplied with the counter.

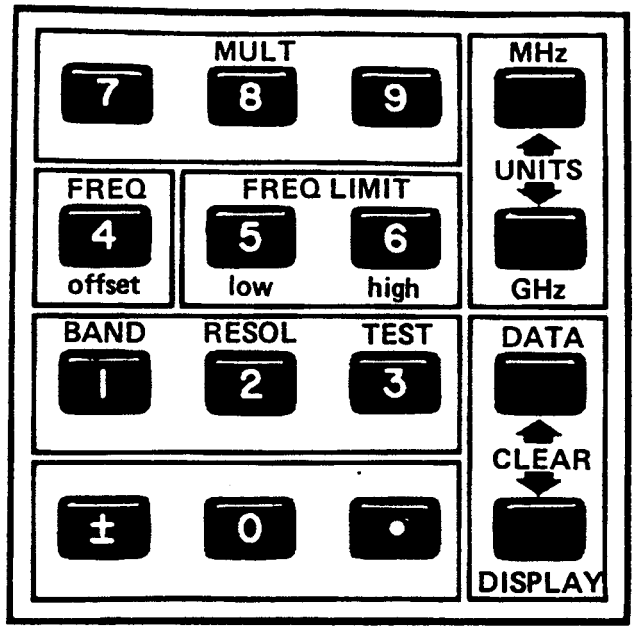


Figure 3-4. Keyboard

KEYBOARD

The keyboard consists of 16 pushbuttons that control major functions of the counter. Twelve keys are used for numerical data entry, the digits 0 through 9, the decimal point and the minus sign. Two keys (MHz and GHz) act as terminators for the input of frequency offset or frequency limits. The CLEAR DATA and CLEAR DISPLAY keys are used to clear stored or displayed data. Seven of the numerical keys are also used to select the band, resolution, test function, frequency offset, frequency limits, and multiplier function.

UNITS (MHz/GHz)

PRESS: MHz Completes Entry Sequence

PRESS: GHz Completes Entry Sequence

CLEAR (DATA/DISPLAY)

PRESS: DATA CLEAR Return "STORED" data of selected function to Power On state. Clears Limits (Low/High), Offsets, DAC, and multiplier operations.

PRESS: CLEAR DISPLAY Clears display. Does not affect stored data. Restores counter to measurement mode.

BAND SELECTION

To select one of three standard operating bands on the model 545A or 548A .

PRESS: BAND [1] or BAND [2] or BAND [3]

Notice annunciator flash and selected band number will light when chosen. This feature allows multiple inputs to be connected and selected in turn.

The "BAND" KEY followed by a numeric key enables the following band selection.

PRESS: BAND [1] 10 Hz - 100 MHz Input

PRESS: BAND [2] 10 MHz - 1 GHz Input

PRESS: BAND [3] 1 GHz - 18 GHz (Model 545A) 26.5 GHz (Model 548A)

On the model 548A equipped with option 06, a 590 cable kit and appropriate optional remote sensor, Band 4 is selected by:

PRESS: BAND [4] [X]

For example, with the 91 Sensor you will press: BAND [4] [1]

MULTIPLY FUNCTION:

In the multiply function the measured frequency is multiplied by an integer up to 99. The result is displayed to 1 KHz resolution. If the results of the multiplications are too big for the front panel to display, the front panel will show F's.

EXAMPLES: PRESS [MULT] AND KEY IN TWO DIGIT NUMBER

EXAMPLE [MULT] [0] [2] FOR MULTIPLIER = 2

NOTE: When "MULT" key is pressed the annunciator "MLT" will flash until the sequence is completed. The two digit multiplier (m) will be displayed as the numbers are entered.

To clear the multiplier function the following operation is performed.

PRESS [MULT] [CLEAR DATA] or PRESS [MULT] [0] [1]

This sequence clears the multiplier function and multiplier (m).

mX ± b

By using the frequency offsets and multiply functions the counter can automatically perform mX ± b calculations.

The equation for the function performed is:

Displayed Reading = mX ± b where m = Multiplier (up to 99) entered from keyboard.

X = Input frequency.

± b = Frequency offset entered from the keyboard.

TO DO mX ± b CALCULATION FOR m = 2, b = -70 MHz

PRESS [MULT] [0] [2] AND [FREQ OFFSET] [±] [7] [0] [MHz]

FREQUENCY LIMITS

Frequency limits can be entered to 10 MHz resolution .

PRESS: [FREQ LIMIT / low] Notice flashing annunciator.

PRESS: [#] Number keys corresponding to desired frequency low limit to 10 MHz resolution.

PRESS: [MHz] or [GHz] To terminate input sequence. Notice FRQ LMT LOW annunciators solidly lit.

PRESS: [FREQ LIMIT / high] Notice flashing annunciator

PRESS: [#] Key numbers corresponding to desired freq. Hi limit.

PRESS: [MHz] or [GHz] To terminate input sequence. Notice FRQ LMT Hi annunciator solidly lit.

To recall stored limits.

PRESS: [FREQ LIMIT / low] and [CLEAR / DISPLAY] then [FREQ LIMIT / high] and [CLEAR / DISPLAY]

To clear data memory and remove frequency limits.

PRESS: [FREQ LIMIT / low] and [DATA / CLEAR] then [FREQ LIMIT / high] and [DATA / CLEAR] Vary Source. Notice selected limit(s) are erased. Also notice "FRQ LMT LOW HI" annunciators are out.

NOTE: High and low limits should be separated by at least 100 MHz.

TEST SELECTION

The following tests will verify proper operation of most functional areas of the counter. At the initial turn on the counter performs a RAM and PROM check. During this check dashes are displayed until the check has been completed.

RAM and PROM

The processor writes a sequential bit pattern to each RAM location, then independently reads that pattern. Thus each bit in each location is checked. If the RAM check fails the display will show all "E's". This indicates that the RAM or the RAM decoding is faulty.

The PROM check verifies the PROM bit pattern. If the PROM check fails an error message will be displayed. This indicates that the PROM's or the PROM decoding is faulty. See Section 6.

If both RAM and PROM check are good the counter will begin normal operation about one second after turn on. The counter will now display all 0's.

200 MHz SELF TEST

PRESS: TEST [ ] [0] [1]

Notice display is 200 MHz. This verifies operation of the time base reference and it's associated circuits, the signal selection, the count chain, and the local oscillator.

LED TEST

PRESS: TEST [ ] [0] [2]

Notice all LED segments and yellow annunciators are lit. This verifies operation of all visual indicators

LED SEGMENT TEST

PRESS: TEST [ ] [0] [3]

Notice each segment of each display digit is lit in turn. The sample rate pot will change the rate, and may be adjusted. This checks the segment drivers.

DISPLAY DIGIT TEST

PRESS: TEST [ ] [0] [4]

Notice all segments of each digit are lit in turn to verify that each digit operates independently.

The sample rate pot will change the rate, and may be adjusted.

KEYBOARD TEST

PRESS: TEST [ ] [0] [5]

Notice display is 05. Press any key and display will indicate a two digit number showing the position of that key within the matrix thus checking keyboard operations. See Figure 6-5 for coordinates.

TO EXIT TESTS

PRESS: CLEAR DISPLAY [ ] to exit a test and return to normal operation.

To exit tests 1 through 4, 6 and 7 you can press any function key. This will exit the test and enter the function selected.

Tests 6 through 10 are used for calibration and troubleshooting. See Pages 6-6 and 6-7.

SET-UP FOR BASIC FREQUENCY MEASUREMENT

Choose the input band by pressing [BAND] and a number key corresponding to the band. Choose resolution by pressing [RESOL] and a number key corresponding to required resolution. The signal coupled to the selected input Band Connector will be automatically displayed to the resolution chosen.

NOTE: When pressing the RESOL key the display will go blank for approximately 1/4 second.

FREQUENCY OFFSETS

Frequency OFFSETS can be added or subtracted from the measured value. These OFFSETS can be entered via the front panel keyboard to 1 Hz resolution:

PRESS: [FREQ] [OFFSET] Notice the flashing annunciator.

PRESS: Number keys corresponding to desired frequency OFFSETS. If OFFSET is to be subtracted press [±] and notice polarity sign indicator at far left of display.

PRESS: [MHz] or [GHz] to integrate programmed OFFSET into actual frequency measurement. Notice solidly lit annunciator indicating instrument memory is loaded.

PRESS: [FREQ] [OFFSET] Recalls OFFSET to display, FRQ and OFFSET annunciators flashing.

PRESS: [CLEAR] [DISPLAY] Notice frequency displayed includes OFFSET; annunciators are lit continuously.

PRESS: [FREQ] [OFFSET] Recalls OFFSET to display; FRQ and OFFSET annunciators flashing.

PRESS: [CLEAR] [DATA] Clears data memory and clears offset.
FRQ and OFFSET annunciators are out.
Display is actual frequency without offset.

DISPLAY ERROR MESSAGES

When an error occurs the error number will be displayed. The probable cause of each error is listed below.

OPERATOR ERRORS

The following error messages indicate an operator error.

01 Illegal Key Sequence.

02 A resolution number was not entered.

03 A band number was not entered; or the number entered was too large.

04 No power reading in current band.

05 Frequency limit high > 18.5 GHz, 27 GHz (548A).

06 (Freq Limit HI) – (Freq Limit Lo) < Min. (100 MHz) difference.

07 Frequency Limit Low < .95 GHz (545A/548A).

08

09 Illegal test mode key sequence.

10 Illegal DAC key sequence.

11 Illegal Multiplier key sequence.

12

13 Option not installed.

COUNTER ERRORS

The following error messages indicate a malfunction within the counter.

31	Check sum error	Section 1 PROM	D0000 - DFFF	A105, U13
32	Check sum error	Section 2 PROM	E000 - EFFF	A105, U17
33	Check sum error	Section 3 PROM	E000 - FFFF	A105, U15
34	Check sum error	Power Meter PROM	4000 - 47FF	A107, U20
35	Check sum error	Band 4 PROM	C000 - C7FF	A105, U14
36	Check sum error	GPIB or BCD/Remote PROM	C800 - CFFF	A105, U16

Section 4
Theory of Operation

GENERAL

The 545A and 548A counters automatically measure and display the frequency of an input signal within the range of 10 Hz to 18 GHz for the 545A, and 10 Hz to 26.5 GHz for the 548A. In both models the frequency is divided into three bands.

BAND 1 operates from 10 Hz to 100 MHz. An impedance converter provides an input impedance of 1 M ohm, shunted by 20 pF.

BAND 2 operates from 10 MHz to 1 GHz, using a heterodyne down converter which converts the input signal into an output signal with a range of 10 MHz to 190 MHz.

BAND 3 operates in the microwave range of 1 to 18 GHz (or 26.5 GHz) and uses a YIG tuned heterodyne converter to translate the input frequency downward to an intermediate frequency (IF) of 125 MHz.

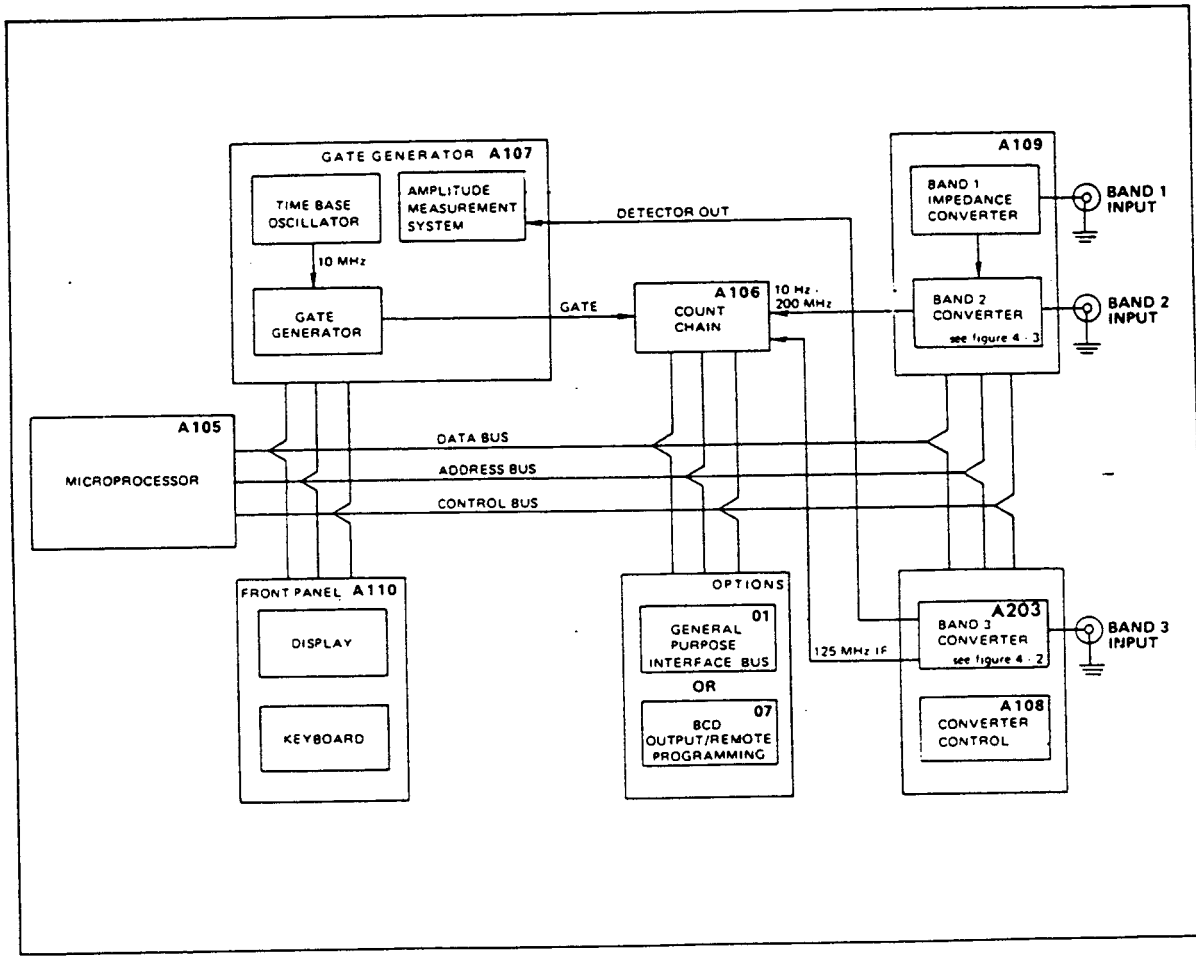


Figure 4-1. Counter Block Diagram, Simplified

BASIC COUNTER

Overall operation is controlled by the Microprocessor Assembly A105. This assembly contains an eight bit microprocessor, its control logic, and the system memory. It communicates with all other assemblies in the instrument by means of a triple bus system: the data, address, and control bus. On each assembly there is a Peripheral Interface Adaptor (PIA) which provides the interface between the bus system and the instrument hardware.

Frequency measurements are performed by comparing an unknown signal to a reference frequency, namely the time base. A 10 MHz crystal oscillator is used as the internal reference and is a part of the Gate Generator Assembly A107. For increased accuracy and stability, ovenized oscillator options are available, or the user may select an external 10 MHz reference.

A frequency measurement is made by generating a time interval (Gate Time) consisting of a number of cycles of the reference. This Gate Time is then used as an interval during which the input signal is counted by the Count Chain Assembly A106.

Initially, the microprocessor selects one of several available inputs to the Count Chain Assembly and the appropriate Gate Time based on user input information; band selection, resolution, etc. The microprocessor then initiates the measurement cycle by resetting the Count Chain to zero and allowing a gate to be generated. During the gate interval, the Count Chain accumulates the number of cycles of the input signal. At the end of the gate time, the microprocessor reads the stored information in the Count Chain and performs any required calculations necessary to convert the measurement into a direct reading of the unknown frequency. The front panel display is then updated with the new measurement results. Figure 4-1 shows a simplified block diagram of the counter.

BAND 2 CONVERTER

An input signal is applied to the mixer along with an appropriate local oscillator (L.O.) to generate an IF frequency in the range of 10 MHz to 190 MHz. This signal is filtered and amplified to a level suitable for direct measurement by the Count Chain.

The L.O. frequency is generated by the Voltage Controlled Oscillator (VCO) of the Band 3 Converter. This frequency is phase locked to the counter's time base and controlled by the microprocessor. A VCO multiplier serves to either pass along the signal directly or double it. It can also turn off the signal and pass only a DC bias to the mixer.

Two detectors provide outputs proportional to the amplitudes of both the applied RF signal and the resulting IF signal. These outputs are compared in the Signal Comparator, which provides a digital output when the IF amplitude exceeds the RF amplitude.

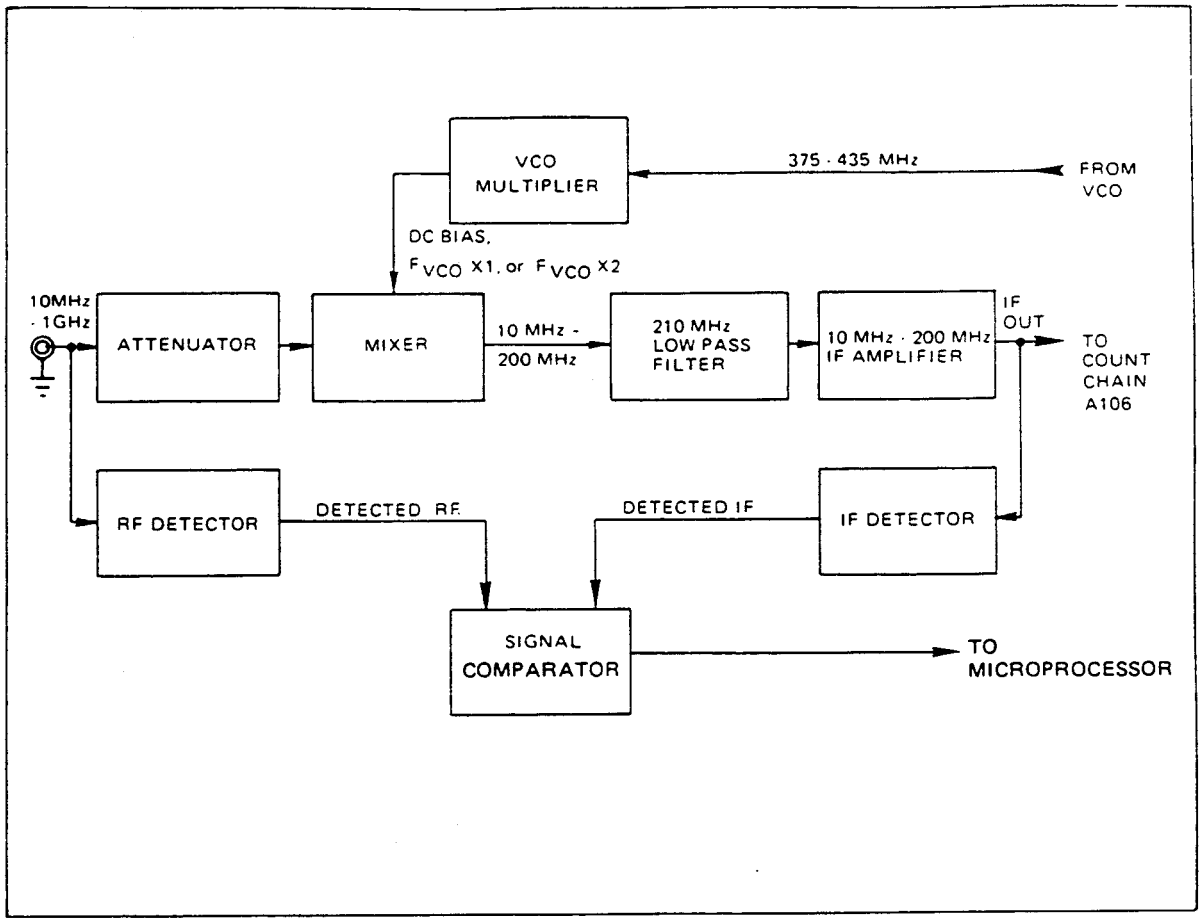


Figure 4-2 Band 2 Converter Block Diagram, Simplified

The output frequency of the system is the difference between the input signal and the L.O. applied to the mixer. Since the L.O. frequency is a harmonic (N) of the VCO frequency, the unknown input frequency can be expressed as $F_{IN}=N\ F_{VCO} \pm F_{IF}$. There are three primary functions of the software operating the converter:

- To select the appropriate harmonic number N.
- To select an appropriate VCO frequency.
- To determine whether the IF frequency is added to, or subtracted from the L.O. frequency.

These functions are accomplished by selecting N and F_{VCO} and looking for an IF signal of the appropriate amplitude and frequency. Overall system gain is such that whenever the correct L.O. frequency is applied, the IF power will exceed the RF power. This is the primary information used in determining the correct VCO frequency and harmonic number. Once an IF is obtained, the harmonic number is verified and the +/- sign in the equation is determined by shifting the VCO frequency and observing the magnitude and direction of the resulting IF shift. Converter operation is diagrammed in figure 4-3.

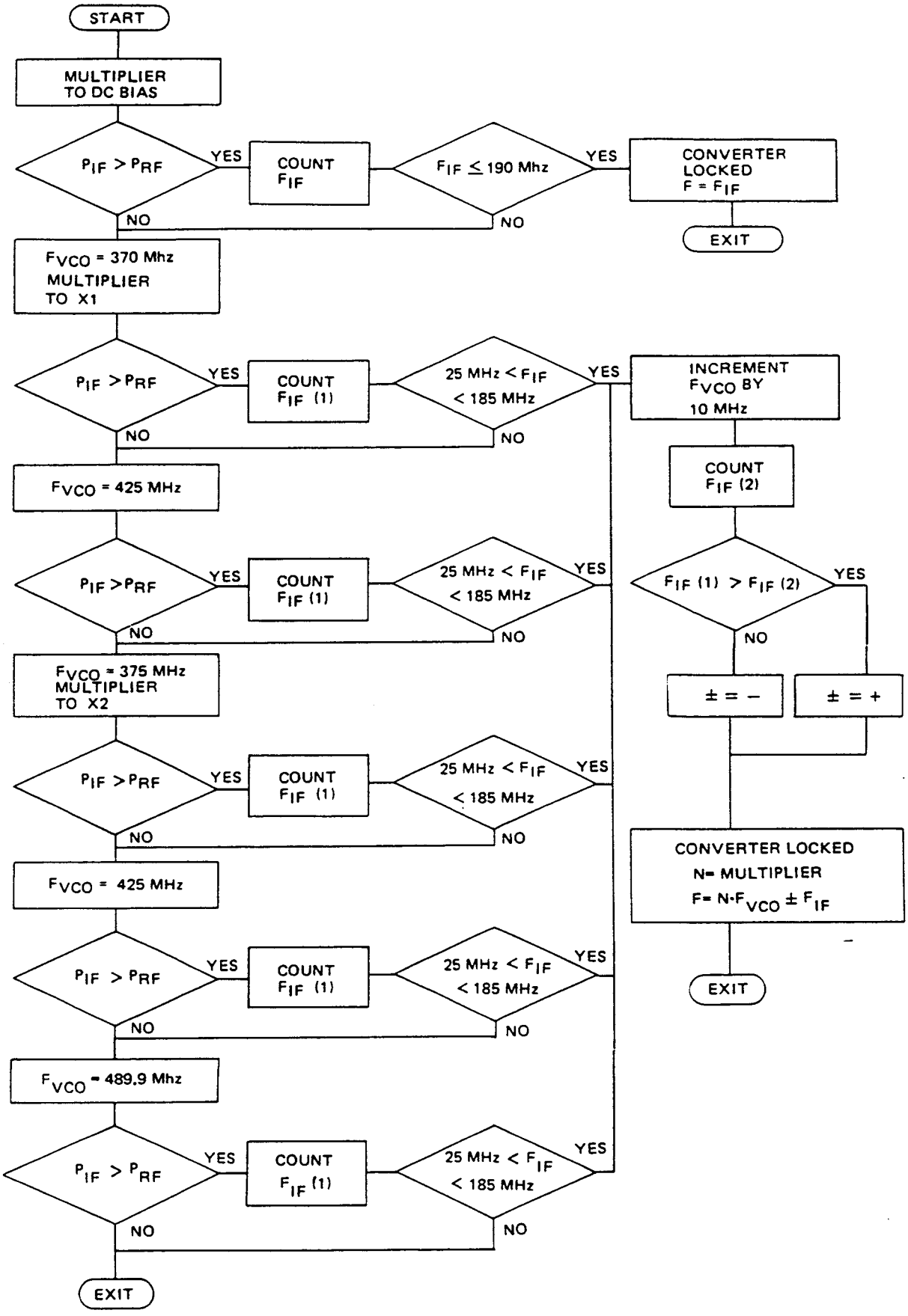


Figure 4-3. Band 2 Converter Operation

The L.O. frequencies being used, except the range of direct counting (< 190 MHz), have been selected so only IF frequencies from 25 MHz to 185 MHz are required. Since the counter can count signals less than 10 MHz, the restricted operating range provides margin for frequency modulation on the input signal, and for incrementing the VCO frequency.

Figure 4-4 shows the operating ranges for the various harmonics and VCO frequencies used.

Input Frequency Range F_{IN}(MHz)	VCO Frequency F_{VCO}(MHz)	Harmonic Number N	IF Frequency Range F_{IF}(MHz)
10 - 190	–	0	10 - 190
185 - 345	370	1	185 - 25
345 - 400	425	1	80 - 25
400 - 560	375	1	25 - 185
560 - 610	425	1	135 - 185
610 - 725	375	2	140 - 25
725 - 825	425	2	125 - 25
825 - 935	375	2	75 - 185
935 - 1035	425	2	85 - 185
1035 - 1164.8	489.9	2	55.2 - 185

Figure 4-4. Band 2 Operating Ranges

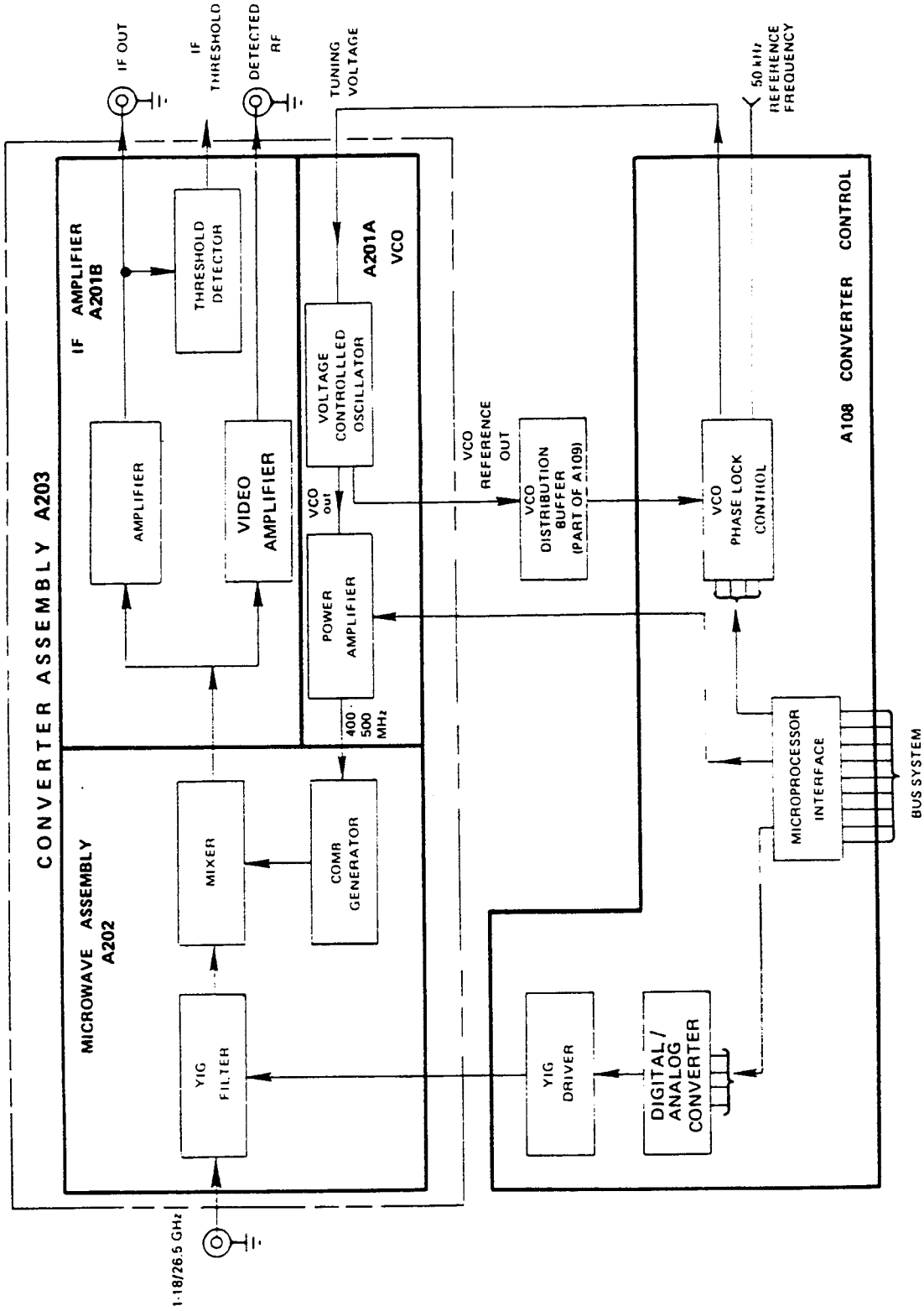


Figure 4-5 Band 3 Converter, Simplified.

BAND 3 CONVERTER

Measurement of a signal in Band 3 is accomplished by down converting from the microwave range to approximately 125 MHz. This is accomplished by mixing the input signal with a known reference frequency which is found by selecting a VCO harmonic in the range of 400 to 500 MHz. The VCO frequency can be selected in 50 kHz increments by using a microprocessor controlled phase lock system, while retaining the accuracy and stability of the counter's time base reference.

A simplified diagram of the Band 3 converter is shown in figure 4-5. There are two major assemblies. The Converter Control assembly (A108) and the Converter Assembly (A203).

CONVERTER CONTROL A108

The Converter Control assembly contains the interface between the microprocessor bus system and the Converter (A203). A digital-to-analog converter and a precision current (YIG) driver provide a 2 MHz frequency resolution for setting the YIG filter of A202.

A108 also contains the programmable VCO phase lock control system. This system lets the microprocessor interface select any VCO frequency between 400 and 500 MHz, in increments of 50 kHz.

CONVERTER A203

The Converter assembly consists of three subassemblies.

- A201A, Voltage Controlled Oscillator (VCO) Assembly
- A201B, IF Amplifier Assembly
- A202, Microwave Assembly (yig)

The A202 Microwave Assembly contains the YIG filter, mixer and comb generator.

The input signal (1 GHz - 18 GHz/26.5 GHz) passes through a YIG filter on A202. The filter is an electronically tunable bandpass filter, with an operating frequency proportional to its tuning current. This filter determines the approximate frequency of the input signal, and filters out any undesired signals, making it possible to count a signal at one frequency even if a larger signal is present at another frequency.

When tuning the YIG filter to the input signal, the mixer is used as an RF detector, and its output is amplified in the video amplifier on the IF assembly .

The output of the Video amplifier is maximum when the YIG filter is tuned to the input signal. In the case of multiple input signals, the video amplifier output determines which signal is largest.

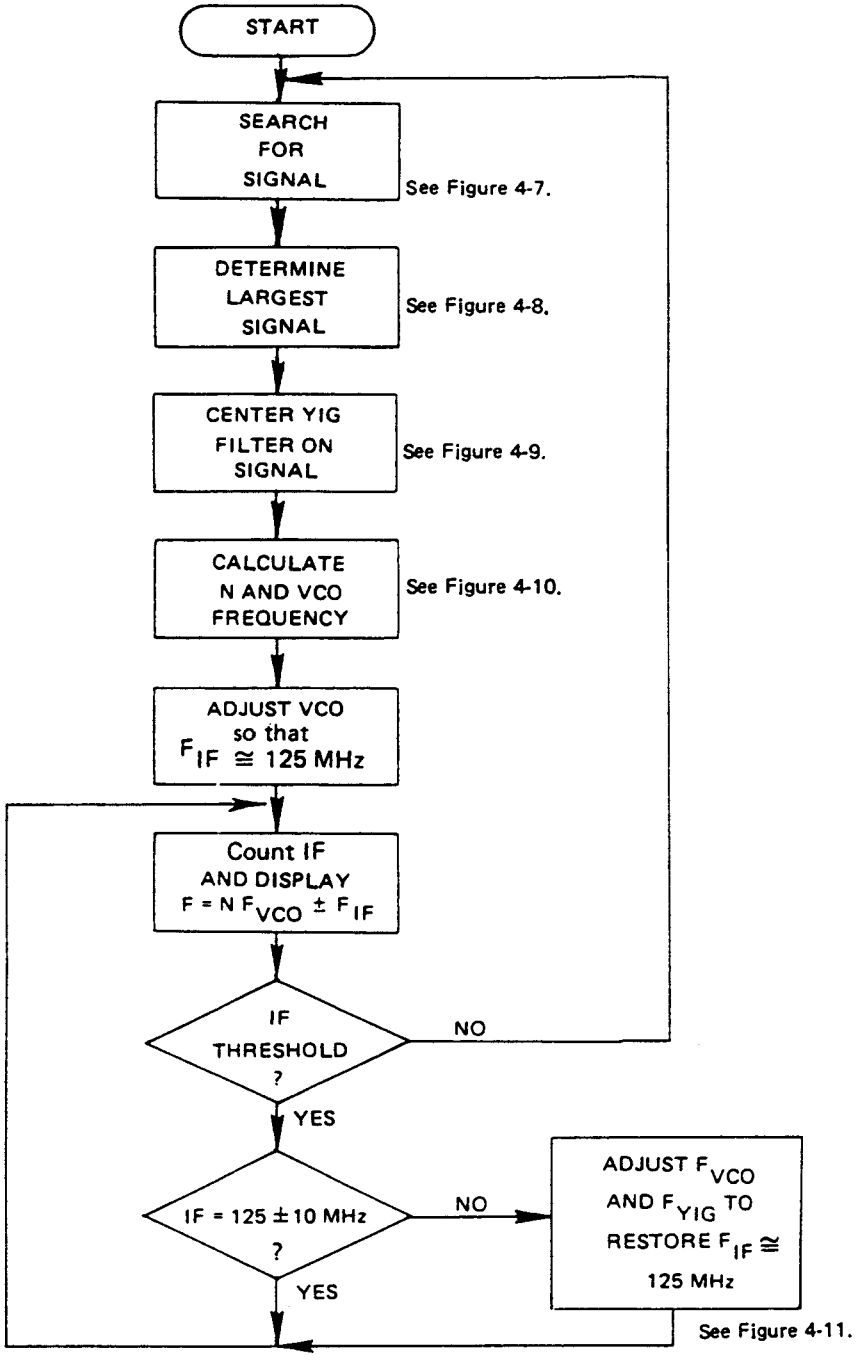


Figure 4-6. Band 3 Operation, Simplified.

On units equipped with the Power Measurement Option (02), accurate frequency correction factors are stored in the counter's memory. This allows absolute power calibration of the video amplifier output.

Once the YIG filter is tuned to the input signal, the appropriate harmonic number (N) and VCO frequency (F_{VCO}) are selected to produce an IF frequency (F_{IF}) at approximately 125 MHz. An approximation of the input signal is found by using:

$$F_{IN} = N F_{VCO} \pm F_{IF}$$

The IF frequency produced in the mixer is amplified by the high gain IF amplifier and sent to the count chain (A106). The IF threshold detector (A201B) insures sufficient IF amplitude for count accuracy.

OPERATION

First the YIG filter is stepped, (in 64 MHz steps), from its low to high limits. During this search the RF detected output is fed, through a microprocessor controlled step attenuator to a threshold detector. After each step the threshold detector is checked. If triggered, the search mode is halted until the amplitude of the signal is determined. This is done by stepping the filter back and forth through the signal and stepping the attenuator until the signal is attenuated below the threshold. The counter then returns to the search mode to look for any larger signals. After searching the entire frequency range, it returns to the largest signal and begins to center the YIG filter precisely on the input frequency. See Figure 4-6 for a simplified diagram of Band 3 operation. For more detailed descriptions of Band 3 operation see Figures 4-7 through Figure 4-11.

The centering process consists of slowly stepping the YIG filter down (in 2 MHz increments) until a level of 3-6 dB below the peak is reached. This frequency is stored and the process is repeated from the other side by stepping the filter up in 2 MHz steps. The average of the two frequencies obtained is the center of the passband. This is the frequency which is used to determine the N and F_{VCO}.

After centering, N is determined from $N = \frac{F_{YIG} - 125}{500}$ and then rounded up to the next highest integer. From this, F_{VCO} is calculated using $F_{VCO} = \frac{F_{YIG} - 125.}{N}$ Should this yield $F_{VCO} < 400$ MHz, then F_{VCO} is recalculated using $F_{VCO} = \frac{F_{YIG} + 125.}{N}$

Since F_{YIG} is only approximately equal to F_{IN}, the IF frequency will not be exactly 125 MHz. Therefore, the next step in operation is a VCO frequency adjustment to shift F_{IF} into the middle of the IF passband.

VCO frequency correction is achieved by counting F_{IF} and changing F_{VCO} by $\pm \frac{F_{IF} - 125.}{N}$ If the error is large enough to be outside the IF passband (IF threshold is not triggered) then a series of steps (shifting the IF in ± 20 MHz increments) are taken until the signal falls within the passband.

Once the VCO corrections have been made, the converter has acquired the signal and the counter is ready to count and display the input frequency.

After each measurement, the frequency of the IF is examined. If the input frequency has shifted more than 10 MHz, new frequencies for the YIG and VCO are calculated to restore the IF to 125 MHz. This method provides rapid tracking of a signal being tuned.

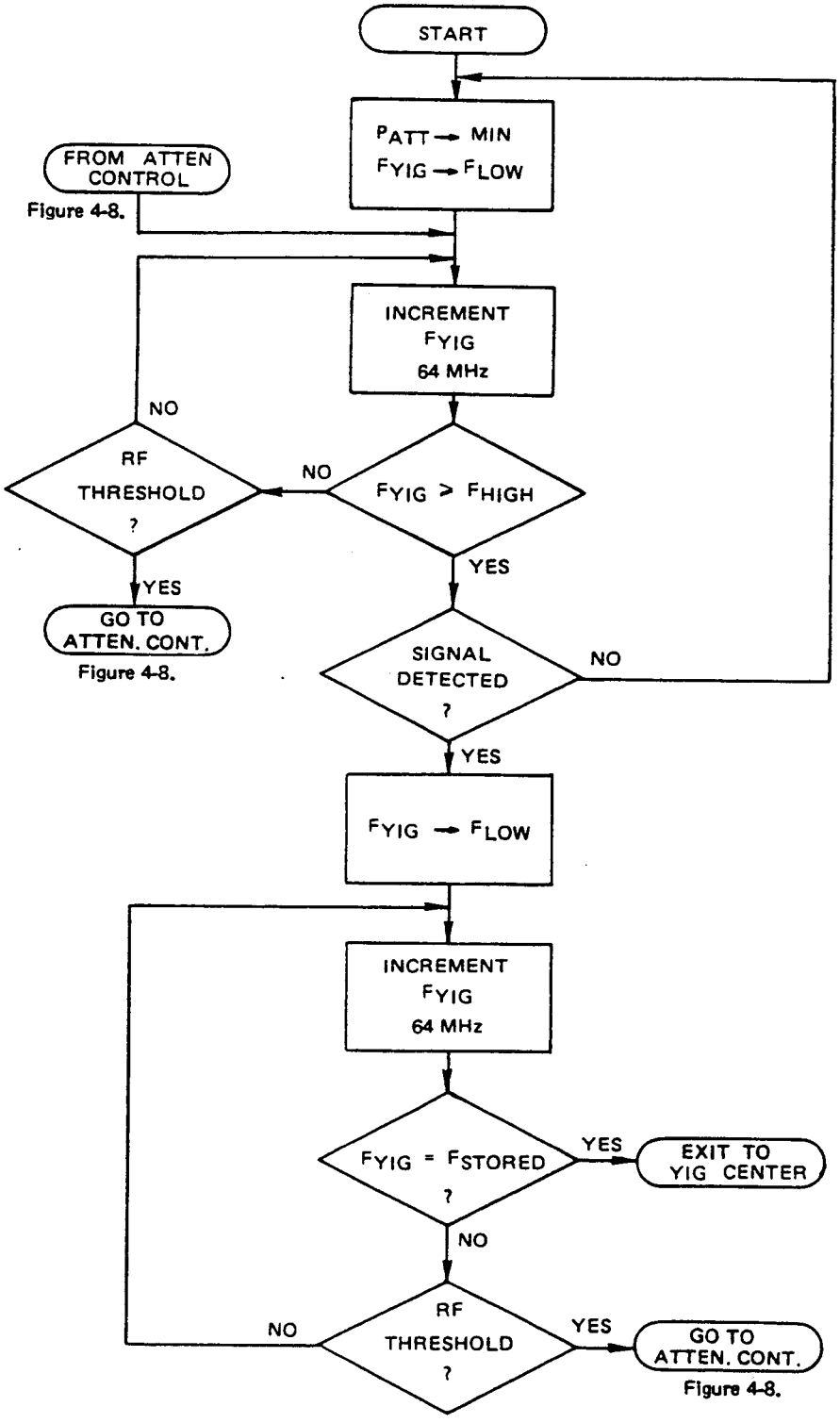


Figure 4-7. Band 3 Search For Signal

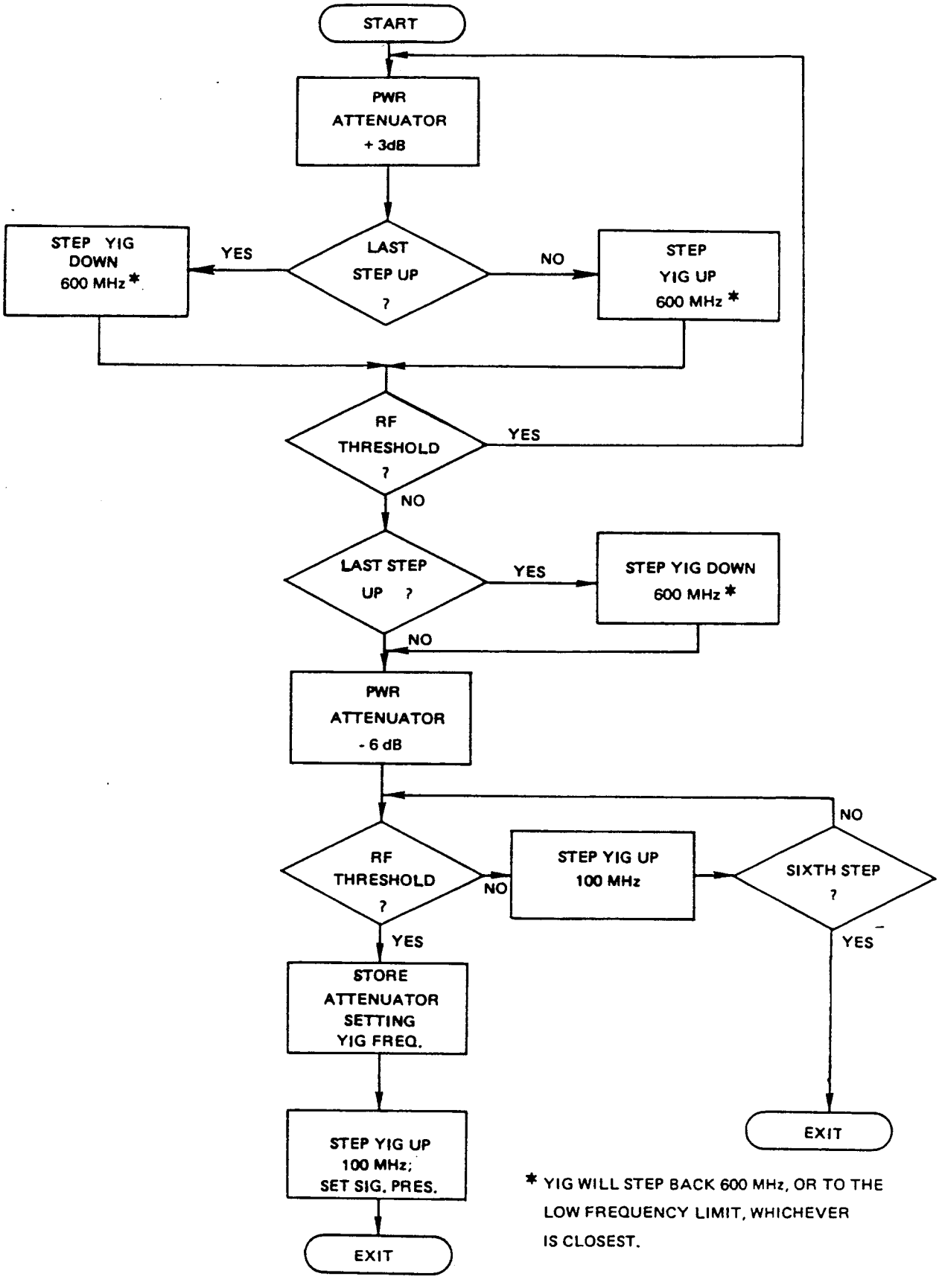


Figure 4-8. Determine Largest Signal

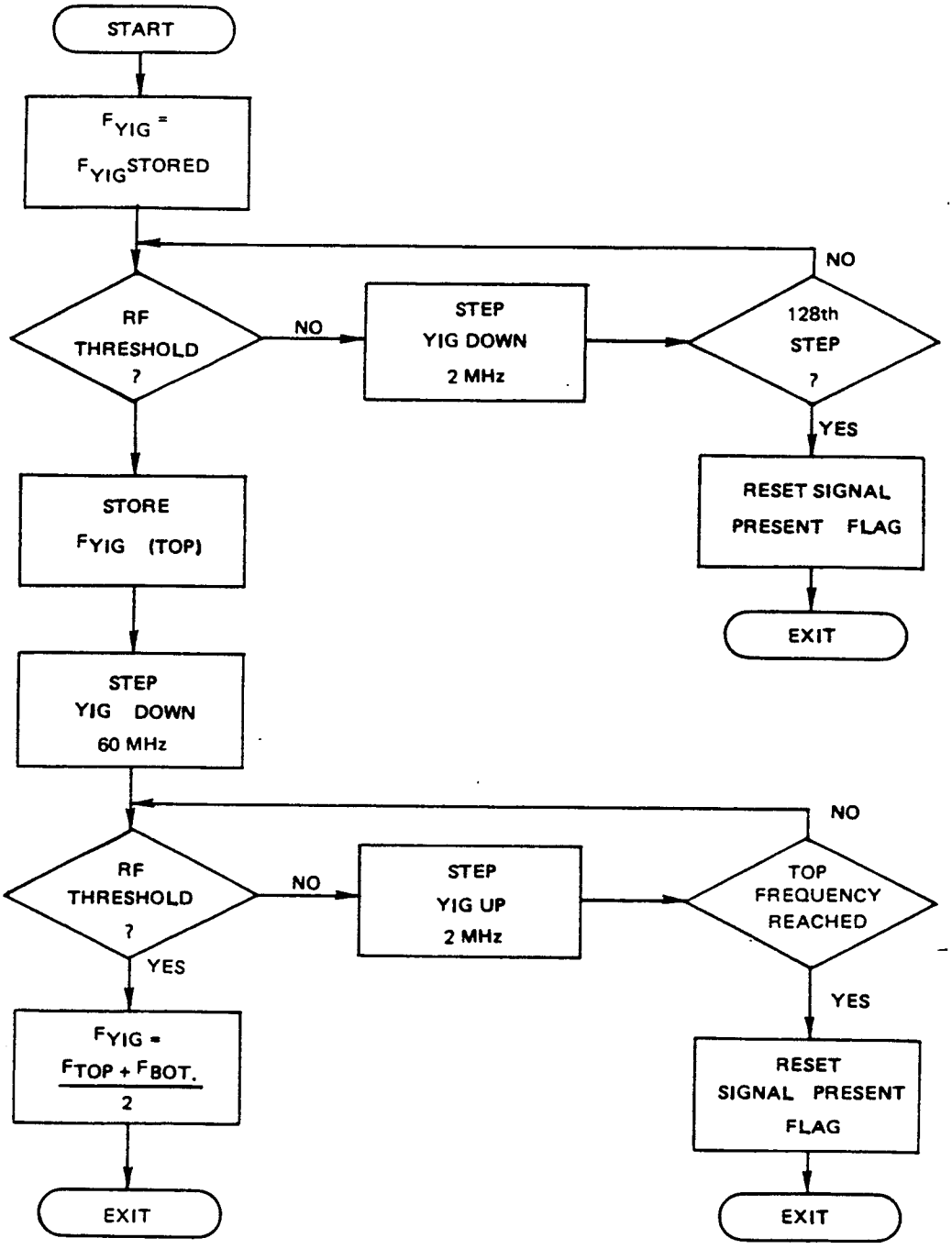


Figure 4-9. YIG Centering

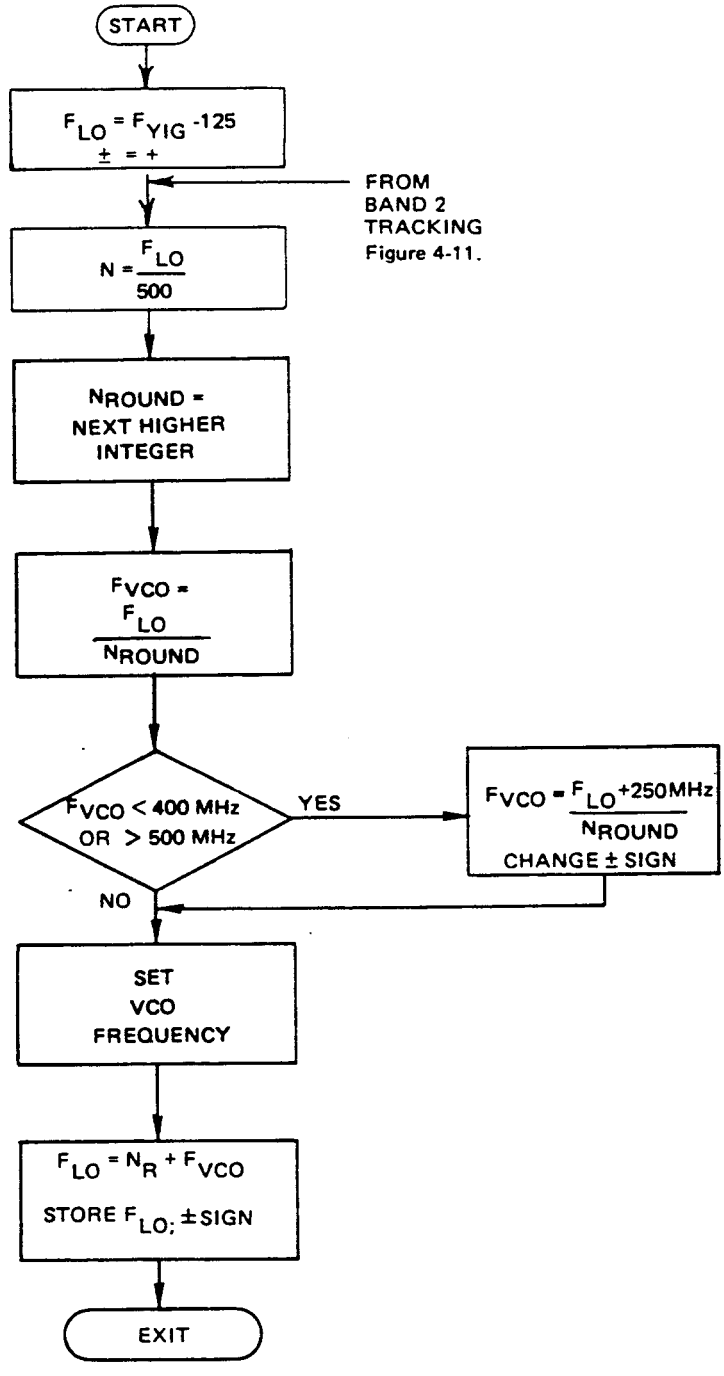


Figure 4-10. Calculate N and VCO Frequency

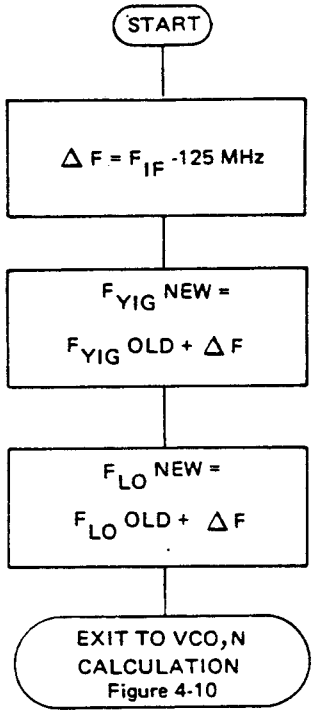


Figure 4-10

Figure 4-11. Band 3 Signal Tracking

Section 5
Maintenance and Service

This section contains information about your counter and instructions for performing maintenance and service.

MAINTENANCE

FUSE REPLACEMENT

The Model 545A/548A Microwave Counter uses one fuse; it is located on the rear panel next to the voltage select switch.

- For 100/120 Vac operation use a 1.0-A slow-blow MDL-type fuse.
- For 220/240 Vac operation use a 0.50-A slow-blow FST-type fuse.

The voltage select switch should be set to the proper line voltage.

WARNING

Be sure the counter is disconnected from the power line.

1. With a flat-edged screw driver, rotate the voltage select switch until the arrow points to the desired line voltage.
2. Change to a fuse with the value specified for the line voltage selected.

WARNING

Only fuses with the required rated current, voltage, and specified type should be used. Do not use repaired fuses or short-circuited fuse holders. To do so could cause a shock or fire hazard.

CAUTION

Always be sure that the voltage select switch is set to correspond to the ac power input voltage, or the counter may be damaged.

AIR CIRCULATION

Air circulates through the vents in the rear panel of the counter. These vents must not be obstructed or the temperature inside the counter may increase enough to reduce counter stability and shorten component life.

PERIODIC MAINTENANCE

No periodic maintenance is required. To maintain accuracy, it is recommended that the counter be recalibrated every six months.

If the following assemblies are repaired or replaced, the counter may require recalibration for proper operation.

- o Power Supply (A101)
- o Gate Generator (A107)
- o Converter Control (A108)
- o Microwave Converter (A102)

Care should be taken when removing any assemblies to prevent damage to components or cables.

CAUTION

Do not attempt repair or disassembly of the Microwave converter (A203) or Time Base Oscillator (A204)assemblies. Opening the sealed covers of these assemblies voids the warranty on the counter. Contact EIP or your sales representative.

SERVICE

DISASSEMBLY, REPAIR, REPLACEMENT, AND REASSEMBLY

GENERAL INSTRUCTIONS

To perform repairs on the 545A/548A printed circuit boards listed in the procedures below, you will need to open the counter by removing the top and/or bottom covers. The top cover may be removed by loosening the six screws that secure it to the counter frame. The bottom cover is held in place to the bottom of the frame by four screws.

Refer to Figure 5-1, Counter Assembly Locations, on page 5-9, for the names and locations of parts and assemblies described in this procedure. Numbers referred to in brackets [ ] in these procedures are keyed to the numbers in Figure 5-1. Cables are referred to by their reference designators (W-) so that they can be located in Figure 5-1. Cables are further identified by their EIP part numbers (2040XXX-01) because these part nmbers are printed on the cables themselves. The format in which socket J1 on the A101 baord is referred to as A101J1 is used throughout this procedure.

WARNING

Before proceeding with any further disassembly, be sure the counter is disconnected from the ac power source. Voltages as high as 230 Vac may exist in the counter. Serious injury or DEATH may result from contact with these potentials.

A101 POWER SUPPLY

Disassembly

1. To remove the A101 board, both top and bottom covers must be removed. Take off the top cover by removing the six screws that secure it to the counter frame [1]. Turn tecounter over and take off the bottom cover by loosening the four screws that hold the bottom cover to the frame.
2. With the counter still up side down, unscrew the four screws that hold the A101 board to the Main Interconnect board (A110).

3. Return the counter to the upright position. Disconnect from J1 on the A101 board the connector attached to the W6 cable from the transformer (T1).

4. Lift the board extractors [2] away from the center of the board to unlock the board from the card guides [3] and remove the board from the counter.

Reassembly

1. To reassemble, thread the board into the card guides [3], and press it down about an inch.

2. Attach the connector for the W6 cable to A101J1.

2. Press the board down the rest of the way until it is seated.

3. Flip the board extractors [2] down to lock the board into position.

4. Screw in the four screws that attach the A101 board to the Main Interconnect (A100) board from the bottom.

A102 (OPTION 08, GPIB)

If your instrument is equipped with Option 08, GPIB programming capability, the GPIB board will be present in the A102 slot.

Disassembly

1. Lift the board extractors [2] away from the center of the A102 board to unlock it from the card guide [3].

2. Slide the board up and remove from the counter.

Reassembly

1. To reassemble, thread the board into the card guides [3], and press it down until it is seated.

2. Flip the board extractors [2] down to lock the board into position.

A105 MICROPROCESSOR

Disassembly

1. Lift the board extractors [2] away from the center of the A105 board to unlock it from the card guide.

2. Slide the board up and remove from the counter.

Reassembly

1. To reassemble, thread the board into the card guides [3], and press it down until it is seated.

2. Flip the board extractors [2] down to lock the board into position.

A106 COUNT CHAIN

Disassembly

1. Lift the board extractors [2] away from the center of the board to unlock it from the card guide.

2. Slide the board up about an inch until the cables can be disconnected.
3. Disconnect from A106J1 the connector for the W15 cable (2040210-01) from A109J5.
4. Disconnect from A106J2 the connector for the W14 cable (2040172-01) from A201J1.
5. Lift the board up and out of the instrument.

Reassembly

1. To reassemble, thread the board into the card guides [3], and lower it about an inch.
2. Reconnect cable 2040210-01 to A106J1.
3. Reconnect cable 2040172-01 to A106J2.
4. Press the board the rest of the way down until it is seated.
5. Flip the board extractors [2] down to lock the board into position.

A107 GATE GENERATOR

Disassembly

1. Lift the board extractors [2] away from the center of the board to unlock it from the card guide.
2. Slide the board up until the cables can be disconnected.
3. Disconnect from A107J1 the connector for the W8 cable (2040173-01) from A201J4.
4. Disconnect from A107J3 the connector for the cable (2040227-01) from A108J3.
5. If your instrument is equipped with Option 03/04/05, Time Base Oscillator, disconnect from A107J2 the connector for the W30 cable (2040179-01) from A114,the optional time base oscillator and J6 (not shown) on the Main Interconnect (A100) board) .
6. Lift the board up and out of the instrument.

Reassembly

1. To reassemble, thread the board into the card guides [3], and lower it about an inch.
2. Reconnect cable 2040173-01 to A107J1.
3. Reconnect cable 2040227-01 to A107J3.
4. Reconnect cable 2040179-01 (if present) to A107J2.
5. Press the board the rest of the way down until it is seated.
6. Flip the board extractors [2] down to lock the board into position.

A108 CONVERTER CONTROL (BAND 3)

Disassembly

1. Lift the board extractors [2] away from the center of the board to unlock it from the card guide.
2. Slide the board up about an inch until the cables can be disconnected.

3. Disconnect from A108J1 the connector for the W6 cable (2040208-01) from A109J3.
4. Disconnect from A108J2 the connector for the W9 cable (2040174-01) from A201J3.
5. Disconnect from A108J3 the connector for the cable (2040227-01) from A107J3.
6. Lift the board up and out of the instrument.

Reassembly

1. To reassemble, thread the board into the card guides [3], and lower it about an inch.
2. Reconnect cable 2040208-01 to A108J1.
3. Reconnect cable 2040174-01 to A108J2.
4. Reconnect cable 2040227-01 to A108J3.
5. Press the board the rest of the way down until it is seated.
6. Flip the board extractors [2] down to lock the board into position.

A109 BAND 2 CONVERTER

Disassembly

1. Lift the board extractors [2] away from the center of the board to unlock it from the card guide [3].
2. Lift off clip [10] that is attached to card cage edge from A109 board.
2. Slide the board up about an inch until the cables can be disconnected.
3. Disconnect from A109J1 the connector for the W17 cable (2040175-01) from A201J2.
4. Disconnect from A109J3 the connector for the W16 cable (2040208-01) from A108J1.
5. Disconnect from A109J4 the connector for the W11 cable (2040166-01) from J112 (Band 2 input on the front panel).
6. Disconnect from A109J5 the connector for the W15 cable (2040210-01) from A106J1.
7. Disconnect from A109J6 the connector for the W10 cable (2040165-01) from J111 (Band 1 input on the front panel).
8. If the instrument is a 548A equipped with option 06, Extended Frequency (Band 4), disconnect from A109J2 the connector for the W27 cable (2040213-01) from P1 on the Option 06 (Band 4 Converter) assembly.
9. Lift the board up and out of the instrument.

Reassembly

1. To reassemble, thread the board into the card guides [3], and lower it about an inch.
2. Reconnect cable 2040175-01 to A109J1.
3. Reconnect cable 2040208-01 to A109J3.
4. Reconnect cable 2040166-01 to A109J4.

5. Reconnect cable 2040210-01 to A109J5.

6. Reconnect cable 2040165-01 to A109J6.

7. If present, reconnect cable 2040213-01 to A109J2.

8. Press the board the rest of the way down until it is seated.

9. Flip the board extractors [2] down to lock the board into position.

A111 FRONT PANEL LOGIC

Disassembly

1. With top cover off, remove two screws [8] holding front black bracket (5210235-01) [4] to front edge of counter frame.

2. Remove two more screws [9] that hold front panel assembly (consisting of front panel overlay [5], Front Panel Display and Keyboard A110 board, and Front Panel Logic A111 board) to front edge of frame.

3. With the bottom cover off, remove four screws (in positions corresponding to the top screws) that hold front panel assembly to bottom of front edge of counter frame.

4. Loosen eight screws [6] (two on top of right corner post, two on top of left corner post, two on bottom of right corner post and two on bottom of left corner post) that hold front panel board to side panels.

5. Pull side panels [7] apart slightly and pull boards forward and free of side panels so that cable connectors can be disengaged.

6. Disconnect from A11J5 the W19 cable (2040168-01) from transistor U14 on support bracket [8].

7. Disconnect from A111J4 the W20 cable (2040168-00) from R101 (Sample/Hold control) on front panel.

8. Disconnect W1 cable (2010189-01) from power switch assembly (S101) on front panel.

9. Disconnect *at A109/Band 2 Converter board end* W10 cable (2040165-01) for Band 1 from J6A109 and W11 cable (2040166-01) for Band 2 from J4A109. *These cables must stay with the A111 board.*

10. Disconnect from A111P2 the W7 cable (2040169-01) from J1 on A100 (Main Interconnect board).

11. If instrument is a 548A equipped with Option 06, extended frequency, disconnect *at A204 Band 4 Converter end* the W28 cable (2040231-01) from J1A204 and the W29 cable (2040232-01) from J2A204. *These cables must stay with the A111 board.*

A110 FRONT PANEL DISPLAY AND KEYBOARD

To gain access to the A110 (Front panel Display and Keyboard) board, it is necessary to separate the Front Panel Logic (A111) board from the Front Panel Display (A110) board.

1. Unscrew the eight screws (four on the upper edge and four on the lower edge) that hold the A110 and A111 boards and the front panel overlay together and lift the boards from the front panel.

2. Then unscrew a ninth screw (about halfway down on the left side of the boards) that holds the A110 and A111 boards together.

3. Gently separate the two boards.

Reassembly of A110 to A111

1. To reassemble Front Panel Logic (A111) board to Front Panel Display and Keyboard (A110) board and front panel overlay, replace A111 on A110 as it was when removed from the counter.

2. Secure with screw at center of left edge of both boards.

3. Secure both boards to front panel overlay with eight screws (four on upper edge and four on lower edge).

Reassembly of A110, A111, and Front Panel Overlay to Counter

1. To reassemble front panel assembly to counter, position the front panel assembly just outside of its normal position in the counter so that the cables can be reattached.

2. Reconnect W20 cable 20401342-01 to A111J4.

3. Reattach W19 cable 2040168-01 to A111J5.

4. Reconnect W1 cable 2040167-01 to S101.

5. Reconnect W10 cable 2040165-01 to A109J6.

6. Reconnect W11 cable 2040166-01 to A111J1.

7. Reconnect W7 cable 2040169-01 to A100J1.

8. If the instrument is a 548A with Option 06, reconnect W28 cable (2040231-01) and W29 cable (2040232-01) from Band 4 Converter to A111J1 and A111J2 respectively.

9. Spread the side panels [7] slightly to allow the front panel assembly to be inserted in its proper position.

10. Tighten the two screws [6] on the top of the left corner post, the two screws [6] on the top of the right corner post and the two screws each on the bottom right and left corner posts that hold the front panel boards to the side panels.

11. Secure front panel assembly (consisting of front panel overlay, front panel display and keyboard board and front panel logic board) to top of front edge of frame with two screws [9].

12. Secure black bracket [4] (5210235-01) to front panel assembly with two screws [8].

13. Secure front panel assembly to bottom of front edge of counter frame with four screws in positions corresponding to screws in top of frame.

FACTORY SERVICE

If the counter is being returned to EIP for service or repair, be sure to include to include the following information with the shipment. Pack the counter for shipping per instructions in Section 2.

1. Name and address of owner.

2. Model and complete serial number of counter.

3. Complete description of the problem (Under what conditions did the problem occur? What was the signal level? What equipment was attached or connected to the counter? Did that equipment experience failure symptoms?).

4. Name and telephone number of someone familiar with the problem who may be contacted by EIP for further information, if necessary.

5. Shipping address to which the counter is to be returned. Include any special shipping instructions.

FIELD SERVICE

EIP has an assembly exchange program. All plug-in assemblies, modules, and the front panel assembly may be exchanged.

After you have identifed a faulty assembly, call EIP with the assembly number and shipping information. A replacement can be shipped within 24 hours. After you have received the replacement assembly, return the faulty assembly to EIP for credit.

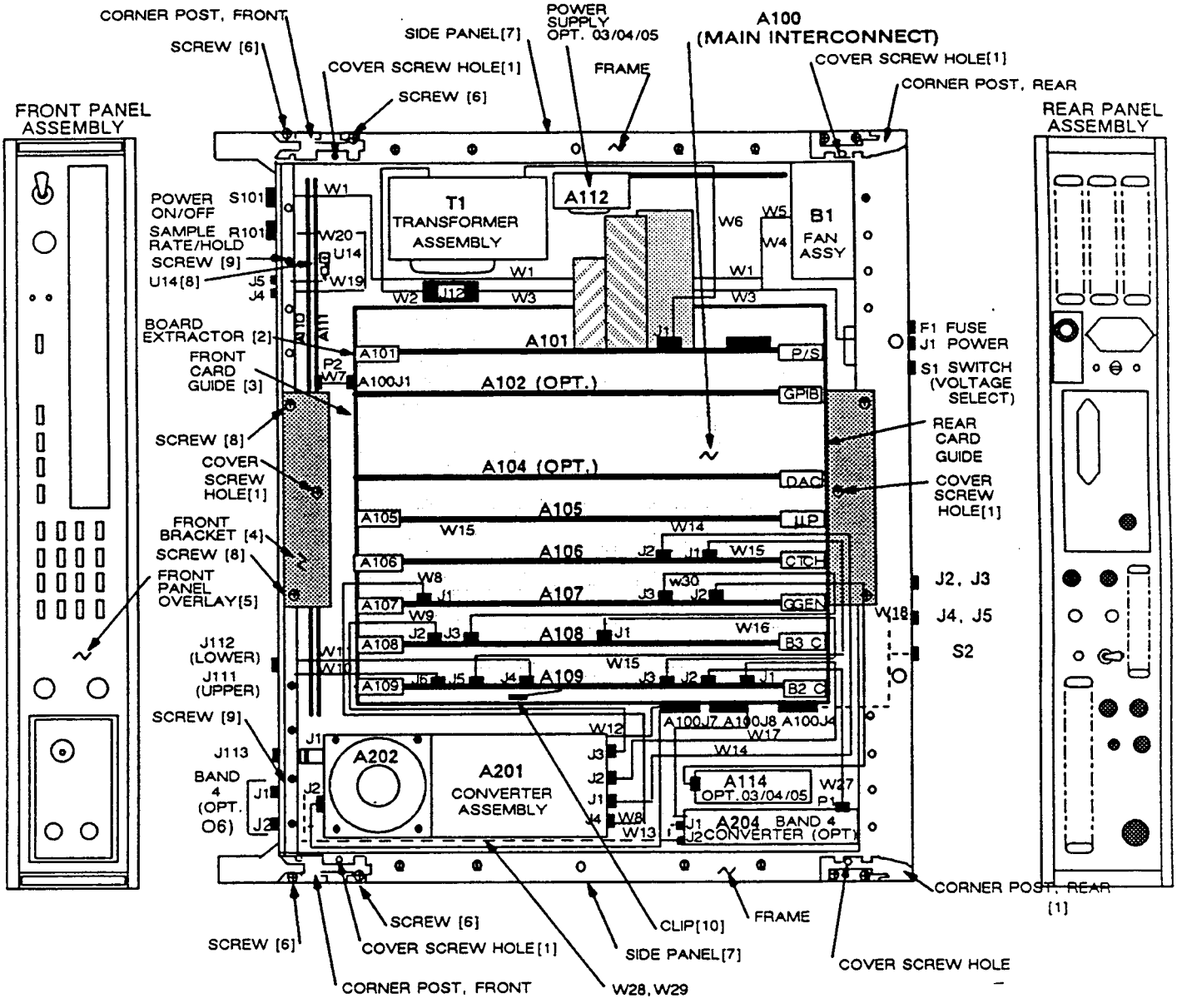


Figure 5-1. Counter Assembly Locations

Section 6
Troubleshooting

This section defines troubleshooting aids that are incorporated in the 5345A/548A counter. They are:

- Signature analysis
- Self diagnostics
- Keyboard controlled circuit tests

The procedures and tables are provided for troubleshooting to a functional circuit level.

SIGNATURE ANALYSIS

Signature analysis is a technique used to troubleshoot complex logic circuitry. It uses data compression to reduce any data pattern to a 4 character alpha-numeric word.

The start and stop inputs define the measurement window. Each time a transition within the measurement window occurs on the clock input, the probe is sampled, and the logic level is shifted into the analyzer. This information is used to generate a signature unique to that data string. That signature can then be compared to a reference signature, taken from a known good product, to determine if the data string is correct. The counter implements signature analysis in either a free running or program controlled manner.

FREE RUNNING

This mode of signature analysis is essential for troubleshooting problems that could prevent the program from running. A CLRB instruction can be forced by breaking the data bus at A105 JMP1 and grounding A105 TP5, effectively "free running" the microprocessor. "Free running" means forcing a simple instruction (such as NOP or CLRB) on the data bus, which the microprocessor sees at every address location. This causes the microprocessor to continually cycle through its entire address range, accessing everything on the address bus as it does. By strategically placing the start and stop connections the entire bus system can be probed for bad signatures.

	START	STOP	CLOCK
CONNECTIONS	A105 TP2	A105 TP2	A105 TP8
BUTTONS	IN	IN	IN

LINE	SIGNATURE	LINE	SIGNATURE
A0 (P1 Pin 54)	UUUU	U8 Pin 8	9UPO
A1 (P1 Pin 54)	FFFF	12	755P
A2 (P1 Pin 53)	8484	U11 Pin 2	9UP1
A3 (P1 Pin 51)	P763	4	4FCA
A4 (P1 Pin 50)	1U5P	6	37C5
A5 (P1 Pin 49)	0356	8	7791
A6 (P1 Pin 48)	U759	11	6321
A7 (P1 Pin 47)	6F9A	13	6U28
A8 (P1 Pin 46)	7791	15	4868
A9 (P1 Pin 45)	6321	17	00001
A10 (P1 Pin 44)	37C5	U12 Pin 2	U759
A11 (P1 Pin 43)	6U28	4	1U5P
A12 (P1 Pin 42)	4FCA	6	8484
A13 (P1 Pin 41)	4868	8	UUUU
A14 (P1 Pin 40)	9UP1	11	FFFF
A15 (P1 Pin 39)	00001	13	P763
U1 Pin 5	0003	15	0356
U2 Pin 9	75HA	17	6F9A
U4 Pin 2	6U2C	U18 Pin 4	6H4C
8	9UP3	5	0994
10	9UP2	6	U3H7
12	0002	7	P257
U5 Pin 6	755F	9	854F
8	PACU	10	H602
12	0003	11	25P6
		12	9F14

+ 5V 0003, phase 2 0003 *

* Due to the synchronous qualities of the signature analyzer, phase 2 will read the same as + 5V but the logic probe will be flashing. Likewise, anything gated with phase 2 may have the same signature as the ungated signal.

Figure 6-1. Microprocessor Free Running Signatures

	START	STOP	CLOCK
CONNECTIONS	A105 TP14	A105 TP15	A105 TP8
BUTTONS	IN ↓	OUT ↑	IN ↓

NODE	SIGNATURE		NODE	SIGNATURE	
	C1	C2		C1	C2
A105 JMP1 Pin 9	8HU1	46H8	A105 JMP1 Pin 13	C38U	A095
A105 JMP1 Pin 10	7068	424H	A105 JMP1 Pin 14	CU8P	U155
A105 JMP1 Pin 11	F439	12A5	A105 JMP1 Pin 15	7096	A44U
A105 JMP1 Pin 12	U774	FP59	A105 JMP1 Pin 16	3H73	1F0H
+5V	1817	1817			

Figure 6-2. Signatures, Basic PROM Set

PROGRAM CONTROLLED

If the counter is working sufficiently to access the test functions, program controlled signature analysis can be used. In program controlled signature analysis the start and stop (and therefore the signature) are controlled by software. This allows the signature analyzer to be used, in many cases, to troubleshoot the hardware outside the bus system.

SELF DIAGNOSTICS

At turn-on, the counter performs several internal diagnostic checks, checking the RAM, PROM, and the associated decoding circuitry. The display shows dashes during these checks. If the counter passes the tests it then enters the normal operating mode. If it fails RAM check, the display will show all Es and a unique signature will be generated. If the counter fails any of the PROM checks, an error message will be displayed, and a signature will be generated. Please refer to figure 6-3.

The counter generates PROM error signatures only during the power up diagnostics check. It is necessary to turn the power off, and then on again, while the signature analyzer is connected, to get a signature.

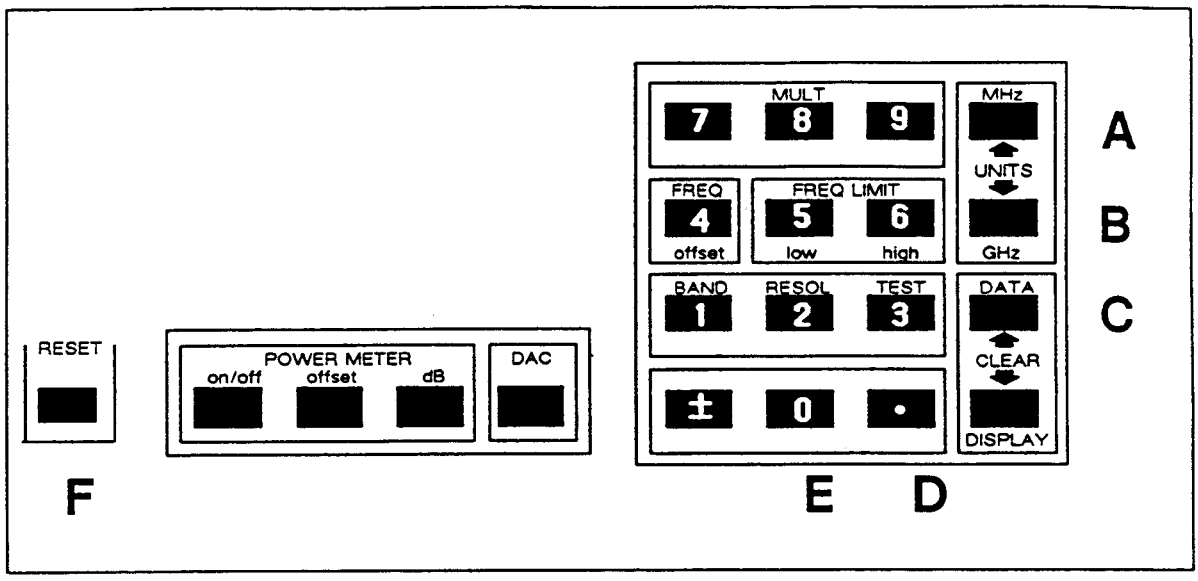
	START	STOP	CLOCK	PROBE
CONNECTION	A106 TP5	A106 TP5	A105 TP8	A105 TP6 (+5V)
BUTTONS	OUT ↑	IN ↓	IN ↓	

PROBLEM	ERROR	SIGNATURE
Ram Bad	All E's	007U
A105 U13 (Basic Program) Bad	31	1UFP
A105 U17 (Basic Program) Bad	32	U399
A105 U15 (Basic Program) Bad	33	P672
A107 U2 (Power Meter) Bad	34	9FA8
A105 U14 (Band 4) Bad	35	2A2C
A105 U17 (GPIB or BCD/RMT) Bad	36	8AFH

Figure 6-3. Self Diagnostic Error Indications

KEYBOARD CONTROLLED CIRCUIT TESTS

There are 11 keyboard controlled circuit tests (01 thru 11). All tests are accessed by pressing TEST and then the two digit test number. Tests which do not require keyboard inputs to function (tests 01, 02, 03, 04, 06, 07, 11) can be exited by pressing any key. The counter will exit the test and enter the functions selected. Tests which use the keyboard in their operation (tests 05, 08, 09, 10) can be exited by pressing any key not used by the test. All tests can be exited by pressing CLEAR DISPLAY. The counter will return to normal operation. Some tests require hexidecimal coded keyboard inputs (tests 08, 09, 10). For those tests the keyboard is defined in figure 6-4.



KEY	HEX EQUIV.	KEY	HEX EQUIV.
0	0	9	9
1	1	MHz	A
2	2	GHz	B
3	3	CLR DATA	C
4	4		
5	5	•	D
6	6	+/–	E
7	7	RESET	F
8	8	CLR DISPLAY	EXITS TEST

Figure 6-4. Keyboard Configuration For Tests Requiring Hexadecimal Inputs.

	START	STOP	CLOCK	PROBE
CONNECTION	OUT ↑	IN ↓	IN ↓	
BUTTONS	A106 TP5	A106 TP5	A105 TP8	A105 TP6 (+5V)

BUTTON	COORDINATES	SIGNATURE
Reset	47	U68C
Power Meter ON/OFF	46	U7HA
Power Meter Offset	36	20P6
dB	16	U2F9
DAC	26	811P
7	41	A19C
8	42	66PU
9	43	CCH7
MHz	44	U5PU
4	31	PUPH
5	32	UC70
6	33	HF3A
GHz	34	OPA2
1	21	APH1
2	22	C45H
3	23	1766
CLR DATA	24	H9C8
+/–	11	375U
0	12	H7PC
•	13	UAHH
CLR DISPLAY	EXIT TEST	C75U

Figure 6-5. Keyboard Test Coordinates and Signatures.

TESTS

01 **200 MHz Self Test** This test sets the VCO to 400 MHz, divides it by two, and counts the 200 MHz output from the divider. It checks the count chain, VCO and VCO phase lock circuitry, and the gate generator.

02 **8's Test** This will light all LED's, annunicators, and decimal points. It checks that everything on the display is lit, the intensity of the display, and the alignment of the LED's and annunciators.

03 **Display Segment Test** This lights one segment of each digit, and one annunciator at a time, cycling through all segments. The cycle rate can be adjusted with the sample rate pot. It verifies that each segment of the display, segment drivers and display multiplexer operate properly and independently.

04 **Display Digit Test** This lights one entire digit, and its decimal point, at a time. It cycles through all digits and annunciators. The cycle rate is determined by the sample rate pot. It checks each digit and digit driver independently, and verifies operation of the display multiplexer.

05 **Keyboard Test** This will display the coordinates of each key as it is pressed. It also generates a unique signature for each key, so the keyboard can be checked without the display. Test 05 may be entered by keyboard or by momentarily tying A108 TP1 to A105 TP6. This makes it possible to enter the keyboard test for troubleshooting even if the keyboard is not operating well enough to enter the test in a normal manner. Test 05 checks the keyboard, keyboard interrupt, and keyboard decode circuitry. The coordinates and signatures for each key are shown in figure 6-5.

06 **Converter Ramp Test** Test 06 continuously ramps the Band 3 Converter DAC from 0 to 27 GHz, in 2 MHz (LSB) steps. It also generates a signature for each of the inputs to the DAC. (See figure 6-6). It can be used to test the yig DAC, yig drivers, yig, and Band 3 RF level circuits.

	START	STOP	CLOCK
CONNECTIONS	A106 TP5	A106 TP5	A105 TP8
BUTTONS	OUT ↑	IN ↓	IN ↓

NODE	SIGNATURE	NODE	SIGNATURE
A108 U4 Pin 2	9U78	A108 U4 Pin 9	7763
A108 U4 Pin 3	9946	A108 U4 Pin 10	HP8A
A108 U4 Pin 4	8F62	A108 U4 Pin 11	P45A
A108 U4 Pin 5	89U9	A108 U4 Pin 12	80A8
A108 U4 Pin 6	833F	A108 U4 Pin 13	77U6
A108 U4 Pin 7	U9CC	A108 U4 Pin 14	7245
A108 U4 Pin 8	FCA6	A108 U4 Pin 15	28U9
+ 5V	49P4		

Figure 6-6. Converter Ramp Test Signatures

07 **VCO Test** This test cycles the VCO frequency from 400 to 500 MHz, in increments of 50 kHz. The cycle rate can be adjusted by the sample rate pot. 07 tests the VCO and the phase lock circuitry.

08 **Power Meter Offset Test** This makes it possible to set the power meter zero DAC to any setting. The setting is entered as a four digit hexidecimal number (figure 6-6). The first two digits are used to program the course offset DAC, and the last two digits program the fine offset DAC. Test 08 enables the power meter zero DAC to be tested, and can provide a DC level signal to aid in testing the power meter circuit.

09 **Power Meter Gain Test** This makes it possible to set the power meter sensing circuit to any number. The number is entered as a five digit hexidecimal number (figure 6-6) in the following format.

1st digit	A107 U10 bits 4-7
2nd digit	A107 U10 bits 0-3
3rd digit	A107 U12 bits 4-7 (Power Meter Option only)
4th digit	A107 U12 bits 0-3 (Power Meter Option only)
5th digit bit 0	Sets Amp marked "15 dB Gain" to high gain
5th digit bit 1	Sets Amp marked "30 dB Gain" to high gain

Digit 5 is a 2 bit number, so any number entered for digit 5 will be justified to a number from 0-3. Test 09 checks the RF level and power meter circuits.

10 **Information Read/Alter Routine** Test 10 can read any microprocessor address and, if that address is RAM or I/O, change its contents. The desired address is entered as a 4 digit hexidecimal number (see figure 6-6). When the 4th digit is entered the counter will display the contents of the desired address. The contents are then changed by entering a two digit hexidecimal number.

NOTE

Test 10 can change any temporary storage in the counter, including locations that are essential to the operation of the counter. Changing the wrong location will not damage the counter permanently, but it can cause improper operation. To return the counter to proper operation turn the counter off then back on.

11 Test 11 for the DAC option 01 is described in Section 10.

SIGNIFICANT ADDRESSES, I/O PORTS

If an I/O bit is configured as an output, the number read by test 10 will be the same number that is programmed. If an I/O bit is configured as an input, the number read by test 10 will be the input signal level on the I/O line. Therefore, if an I/O port is programmed, and then read, the number displayed may not correspond to the number programmed because some bits of the I/O port may be configured as inputs.

DESCRIPTION	ADDRESS OF PA PORTS	ADDRESS OF PB PORTS
PIA on Count Chain (A106)	AC00	AC02
PIA on Gate Generator (A107)	9900	9902
Frequency Control PIA on Converter Control A108	9840	9842
Programmable Counter PIA on Converter Control (A108)	9820	9822
PIA on Band 2 Converter (A109)	9880	9882
PIA on Front Panel Logic (A111)	9808	980A
PIA on BCD/Remote (A102)	9A00	9A02
PIA on DAC Board (A103)	A820	A822

DESCRIPTION	ADDRESS
GPIB Address Switch	9C04

Figure 6-7. I/O Addresses.

Two important I/O port locations are the yig frequency control (address 9840, 9842) and the VCO frequency control (address 9820, 9822).

To convert from the desired yig frequency to the PIA program number:

1. Round the desired frequency to a multiple of 2 MHz (The yig DAC resolution is 2 MHz).
2. Divide the desired frequency in MHz by 2 (F/2).
3. Convert F/2 from decimal to hexidecimal.
4. The two most significant digits are programmed to address 9842, and the two least significant digits are programmed to address 9840.

To convert from the desired VCO frequency to the PIA program number:

EXAMPLE (420. 75 MHz)

1. Round the desired frequency to a multiple of 50 kHz
   (The resolution of the VCO frequency is 50 kHz).
2. Multiply the desired frequency (in MHz) by 5. . . . . 420. 75 X 5 = 2103.75
3. If the result contains no fractional part, go to step 8.
4. Multiply only the fractional part by 16 . . . . . .75 X 16 = 12
5. Add the result to the most significant digit from step 2. . . . . .MSD of 2103.75 = 2 - 2 + 12 = 14
6. Convert the result to hexidecimal . . . . . $14_{10} = E_{16}$
7. Replace the MSD from step 2 with the result from step 6
   and drop the fractional part. . . . . .2103.75 → E103
8. The two most significant digits are programmed to address 9822, and the two least significant digits are programmed to address 9820.

SIGNIFICANT ADDRESSES, RAM

All storage in RAM are in the following formats.

REGISTER FORMAT, FREQUENCY STORAGE			REGISTER FORMAT, POWER STORAGE		
ADDRESS	SIGN (00 = +, FF = –)		ADDRESS	SIGN (00 = +, FF = –)	
ADDRESS + 1	100 GHz	10 GHz	ADDRESS + 1	NOT	USED
ADDRESS + 2	1 GHz	100 MHz	ADDRESS + 2	NOT	USED
ADDRESS + 3	10 MHz	1 MHz	ADDRESS + 3	NOT	USED
ADDRESS + 4	100 KHz	10 KHz	ADDRESS + 4	NOT	USED
ADDRESS + 5	1 KHz	100 Hz	ADDRESS + 5	100 dB	10 dB
ADDRESS + 6	10 Hz	1 Hz	ADDRESS + 6	1 dB	. 1 dB

REGISTER	ADDRESS
L.O. frequency	01A8
I.F. frequency	023F
Frequency output to display	01B8
Frequency limit low	025B
Frequency limit high	0254
Frequency offset	0246

Figure 6-8. Frequency Storage Registers

REGISTER	ADDRESS
Power output to display	01BF
Power offset	024D

Figure 6-9. Power Storage Registers

TROUBLESHOOTING TREES

Troubleshooting trees are intended only as a guide, and do not describe every possible failure situation. Turn power off before removing or installing any P.C. boards or connectors. If the following assemblies are repaired or replaced, recalibration of the counter will be necessary.

- A101 Power Supply
- A107 Gate Generator
- A108 Converter Control
- A203 Converter Assembly

CAUTION

Do not attempt to repair or disassemble
the A203 hybrid assembly.

TEST EQUIPMENT REQUIRED

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
Tektronix	475	Oscilloscope	100 MHz min. Bandwidth
Fluke	8050A	D.V.M.	4½ digit resolution
H.P.	182C, 8559A	Spectrum Analyzer	125 MHz
H.P.	5004A	Signature Analyzer	
H.P.	651B	Signal Generator	10 Hz - 10 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
EIP	928	Microwave Source	1 GHz - 18.6 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz - 26. 5 GHz

Figure 6-10. Troubleshooting Test Equipment (Or Equivalent).

To use the troubleshooting trees:

1. Refer to the main troubleshooting tree.

2. Step through the main troubleshooting tree, performing all necessary checks, until the failure mode is noted.

3. Refer to the appropriate troubleshooting tree for that failure mode.

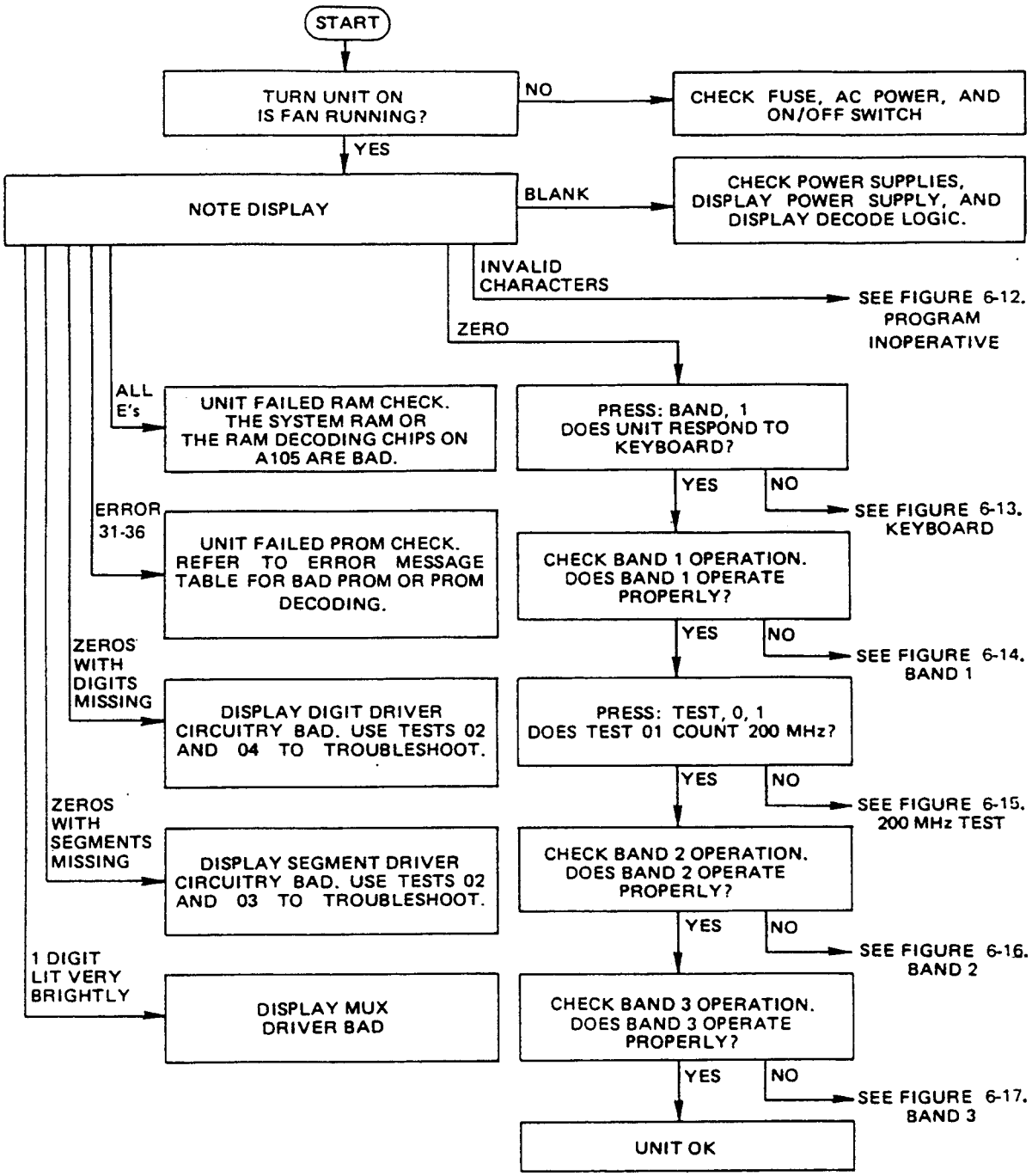


Figure 6-11. Main Troubleshooting Tree

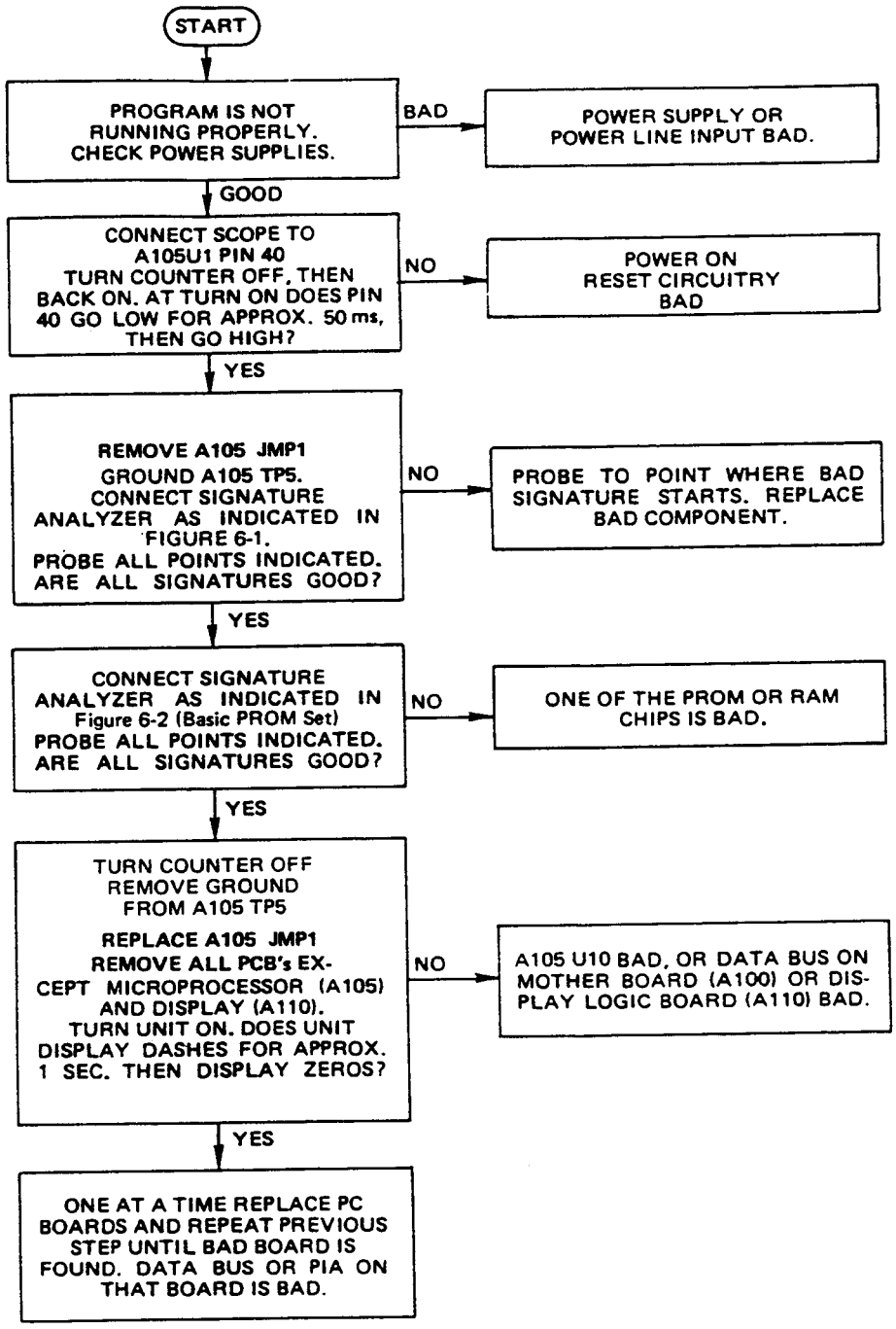


Figure 6-12. Program Inoperative

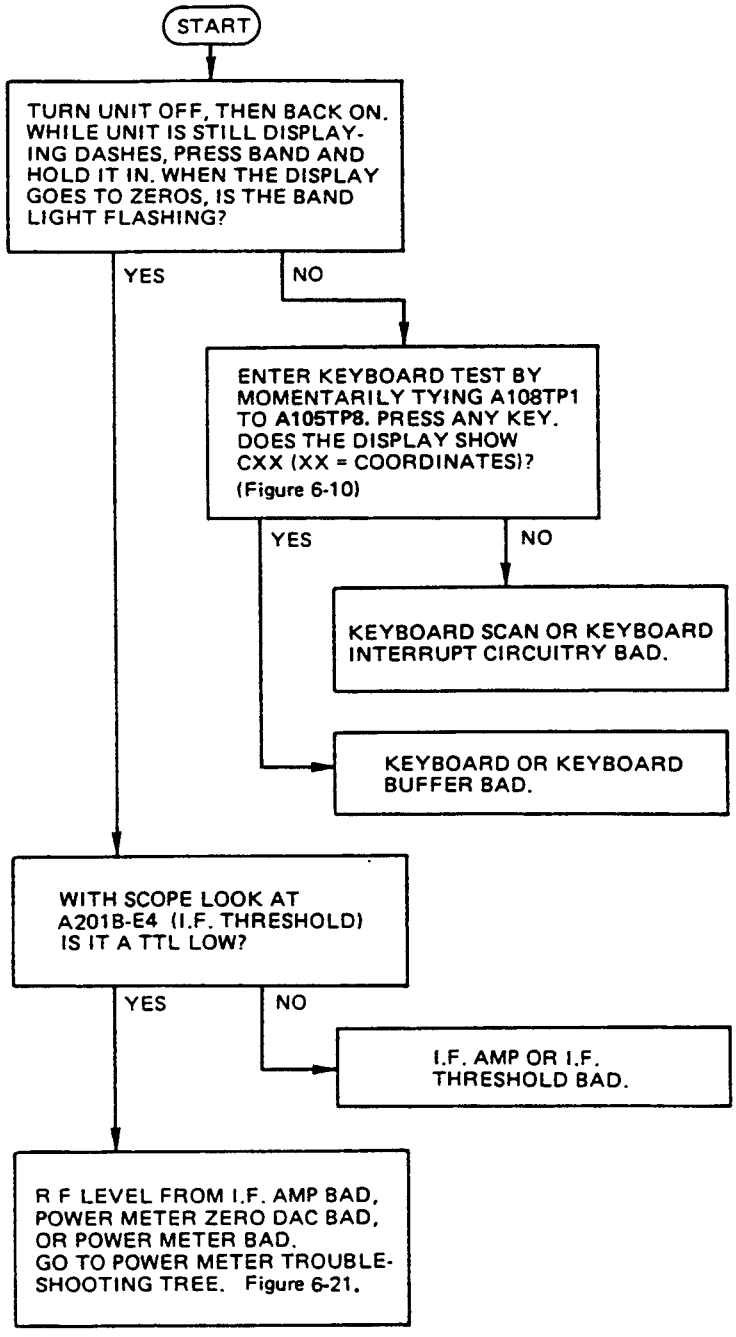


Figure 6-13. Keyboard

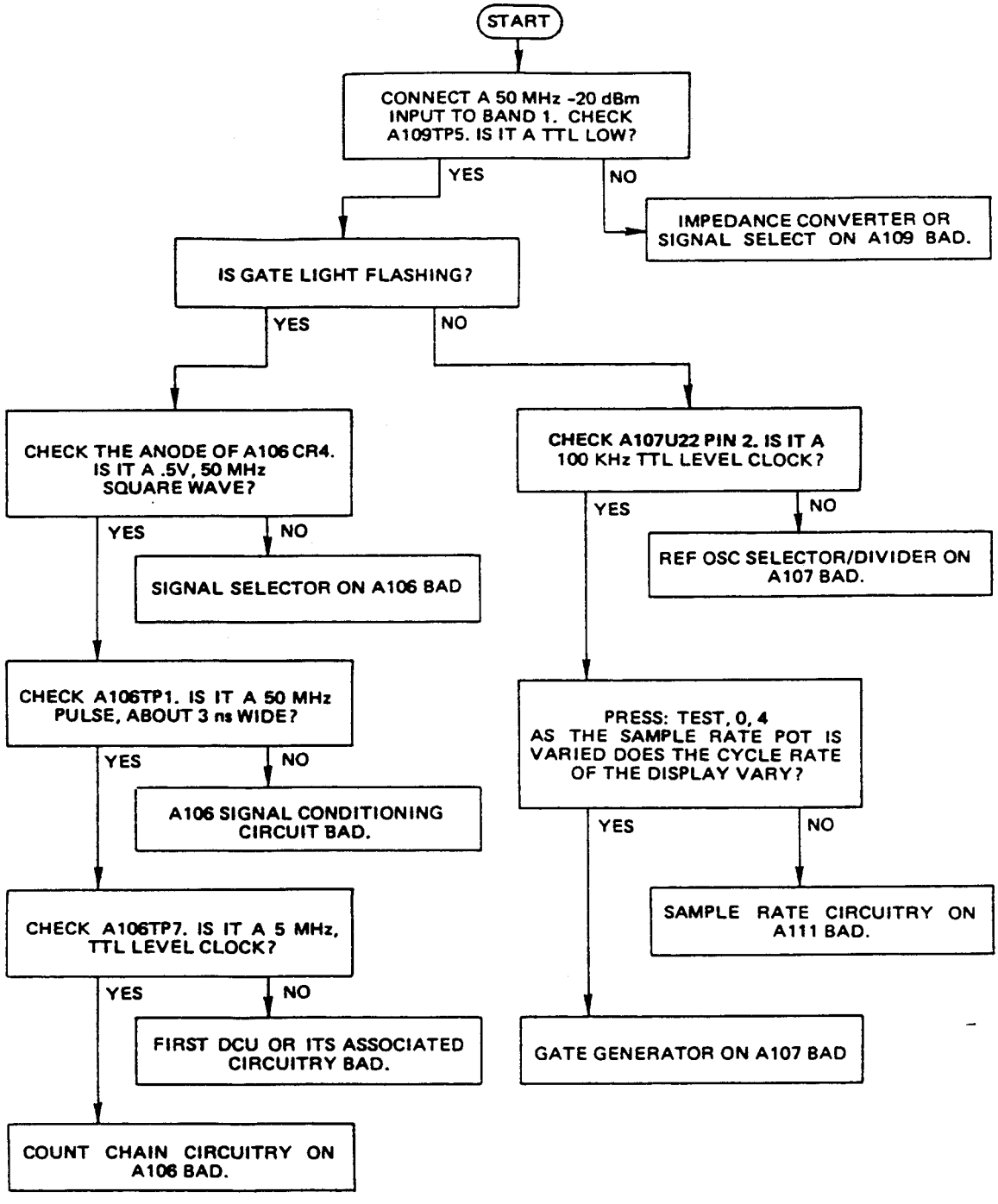


Figure 6-14. Band 1

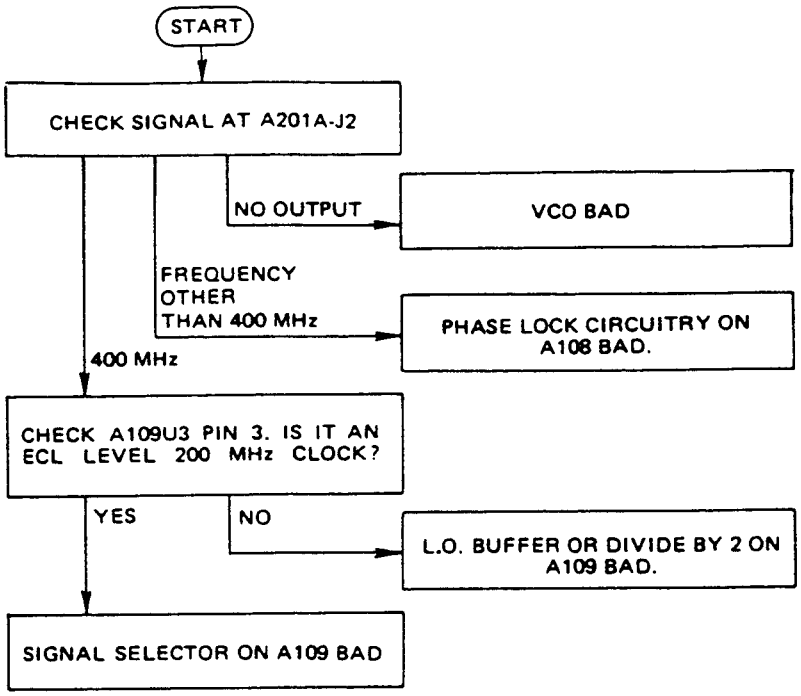


Figure 6-15. 200 MHz Test

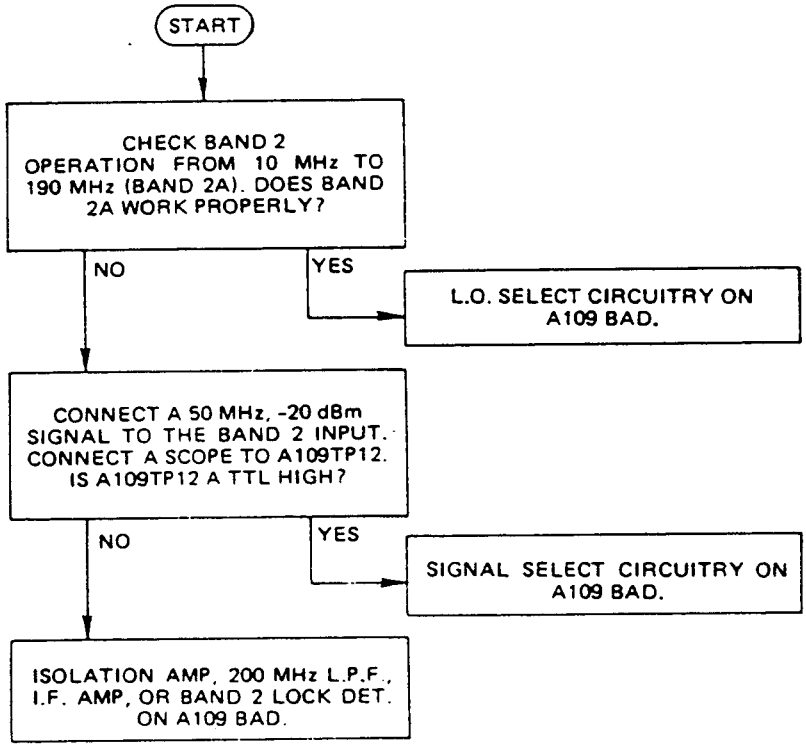


Figure 6-16. Band 2

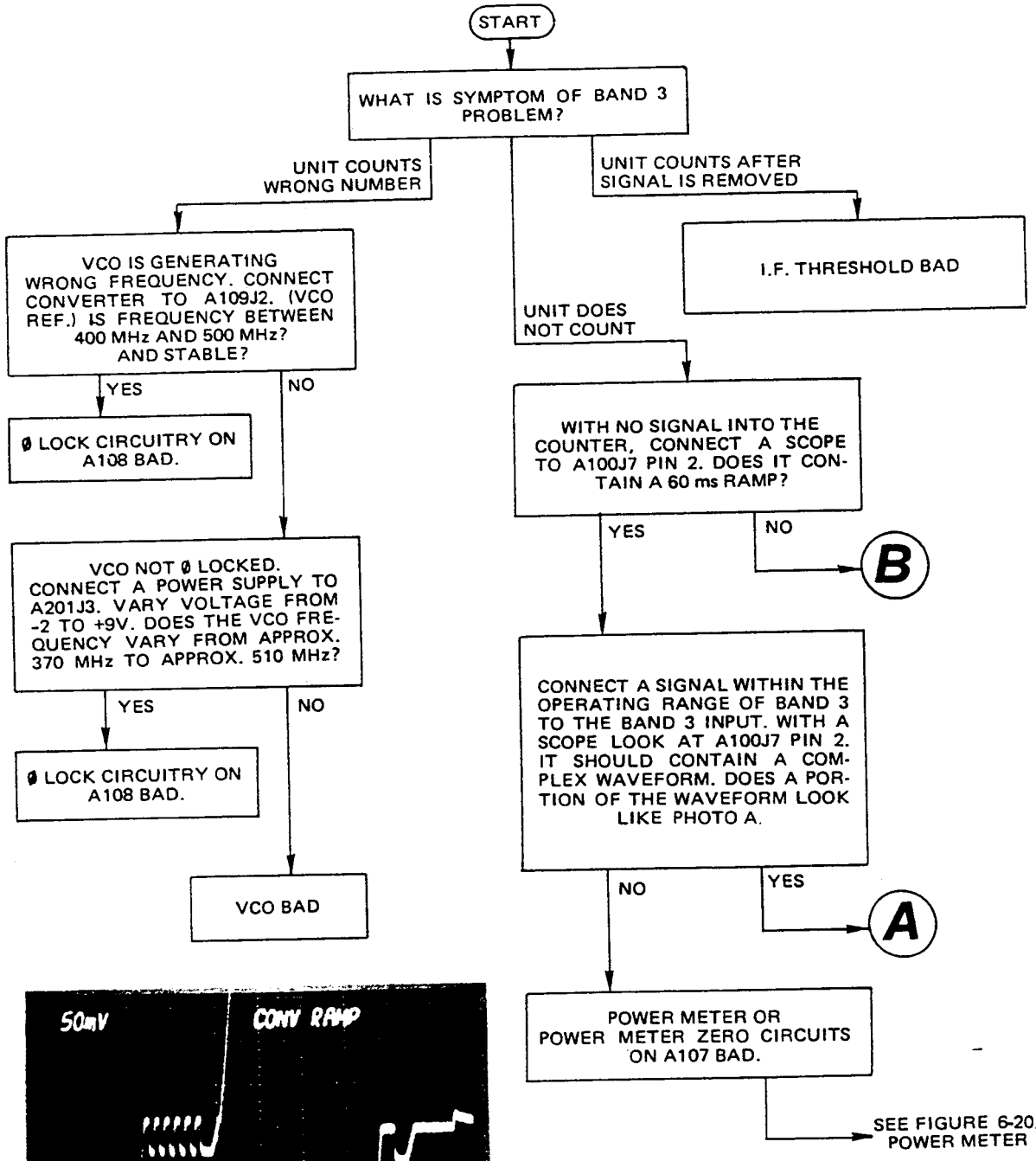


PHOTO A.

Figure 6-17. Band 3

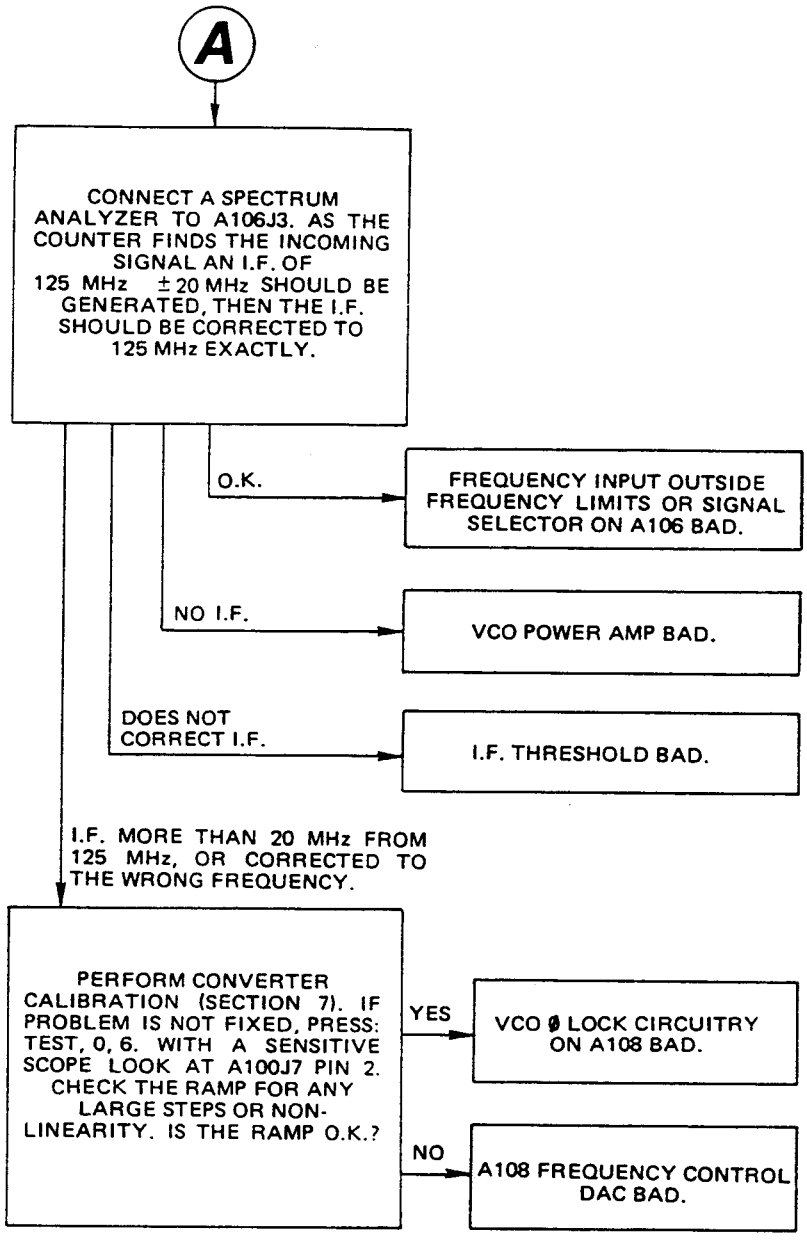


Figure 6-17. Band 3, continued

CONVERTER CONTROL BOARD CALIBRATION

COARSE ADJUSTMENT

1. Press: BAND [ ] [3], TEST [ ] [1] [0],
   [9] [8] [4] [2] [0] [3]
   [9] [8] [4] [0] [±] (E) [8]

2. Set the Wavetek microwave sweeper at 2.00 GHz ± 10 MHz, about -10 dBm.

3. Connect the sweeper output to Band 3 input connector of the counter.

4. Connect the oscilloscope to A201B (IF Amplifier Board) E5 (RF level).

5. Adjust A108 (Converter Control) R10 until A201B-E5 is at maximum positive voltage.

6. Set the sweeper to 15.00 GHz ± 10 MHz.

7. On the counter press: [9] [8] [4] [2] [1] [•] (D)
   [9] [8] [4] [0] [4] CLEAR [ ] DATA (C)

8. Adjust A108R6 until A201B-E5 is at maximum positive voltage.

9. Set the sweeper to 2.00 GHz ± 10 MHz.

10. On the counter press: [9] [8] [4] [2] [0] [3]
    [9] [8] [4] [0] [±] (E) [8]

11. Adjust A108R10 until A201B-E5 is at maximum positive voltage.

12. On the counter press: CLEAR [ ] DISPLAY

FINE ADJUSTMENT

1. Set the source to 1.0 GHz, and connect to Band 3 input of counter.

2. Connect the spectrum analyzer to A106J3 (IF output) of the counter.

3. The counter should be counting the incoming signal. The spectrum analyzer should be displaying the IF (125 MHz).

4. On the counter press RESET. When the converter finds the incoming signal, an IF is generated which is near 125 MHz at first, then shifts to exactly 125 MHz (see Figure 7-2). If the first IF is more than 5 MHz from 125 MHz, adjust A108R10 until the first IF (at an input frequency of 1 GHz) is 125 MHz ± 5 MHz.

5. Slowly tune the microwave sweeper from 1 to 26.5 GHz (to 18 GHz for 545A), while pressing RESET on the counter.

6. Every time the converter finds the incoming signal, the first IF should be 125 MHz ± 20 MHz. If not, adjust A108R6 until the first IF is always 125 MHz ± 20 MHz.

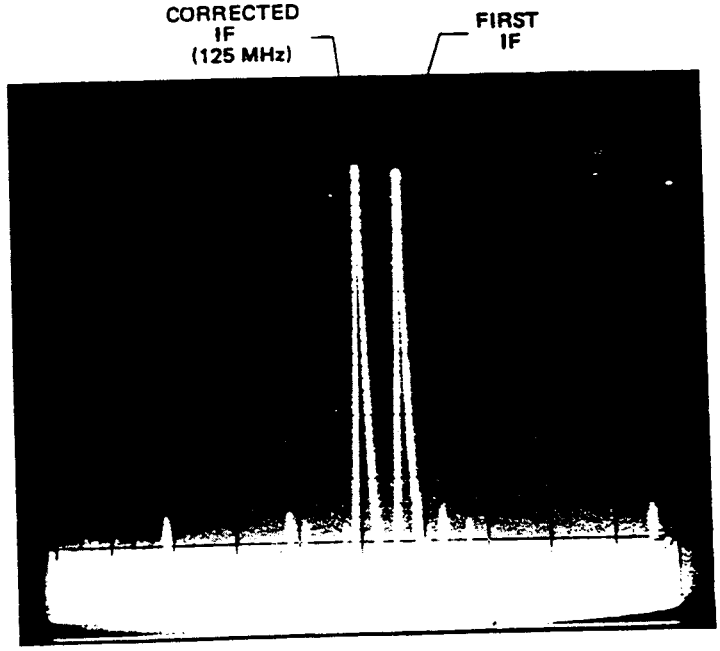


Figure 7-2. IF Signal.

A100
COUNTER INTERCONNECT
(202180)

FUNCTIONAL
DESCRIPTION
NOT REQUIRED

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A100 COUNTER INTERCONNECT ASSY

2020180 - G

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A100	Counter Interconnect Assy	2020180	1	EIP	34257
J1	Header, Str, 26 pin	2620078	1	3429 - 2302	76381
J2	Header, Str, 50 pin	2620081	2	3433 - 2302	76381
J3	J2				
J4	Friction Lock, 4 pin	2620061	1	09 - 65 - 1049	0000A
J5	Friction Lock, 6 pin	2620090	1	09 - 65 - 1069	"
J6	Header, Str, 7 pin	2620186	1	09-64-1071	"
J7	Header, Str, 10 pin	2620187	1	09-64-1101	"
J8	Friction Lock, 4 pin	2620068	1	640456-4	AMP
XA101	Conn, 11 position	2620183	1	5193-442-1	AMP
XA102	Conn, 50 position	2620185	1	5193-442-3	"
XA103 thru XA109	Conn, 30 position	2620184	7	5193-442-2	"
	Key Plug	50001030	10	530286 - 2	"

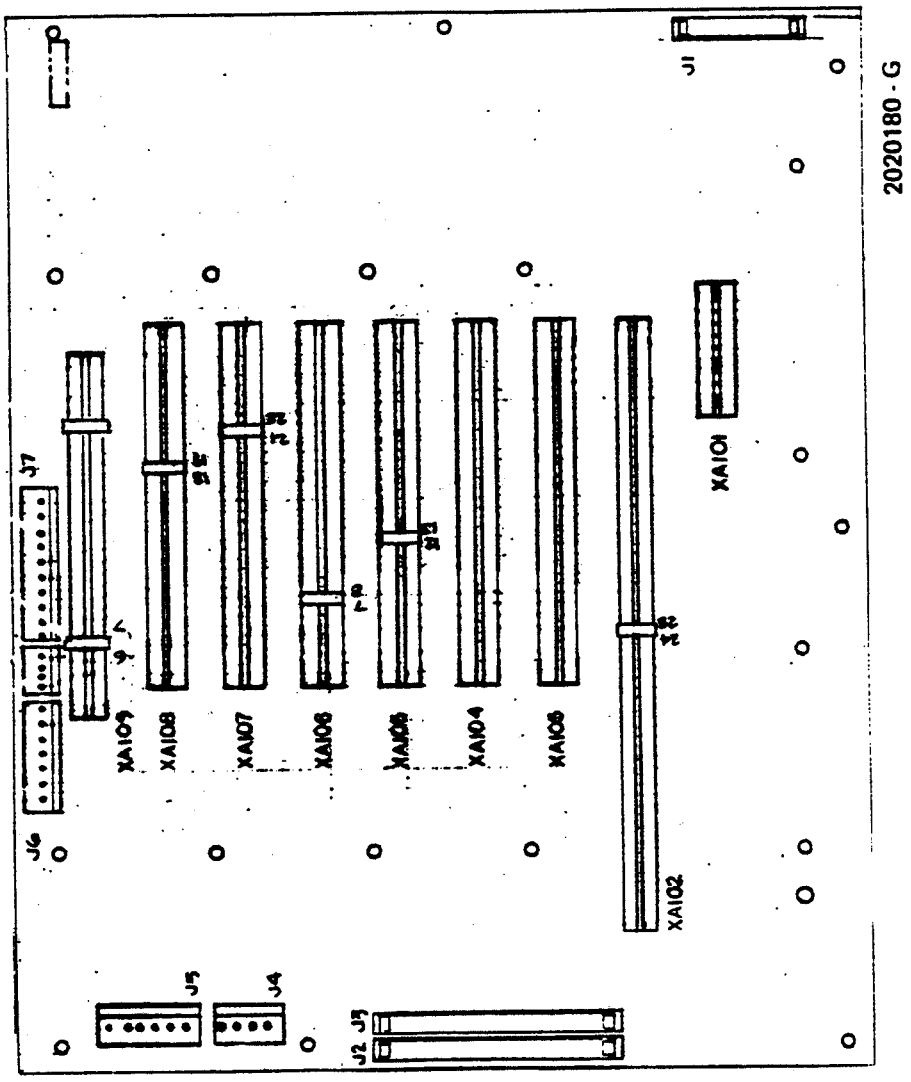

Figure 100-1. Counter Interconnect Component Locator

A101
POWER SUPPLY
(2020131)

The power Supply furnishes all basic operating voltages required by the counter. The supply consists of two basic sub-assemblies.

- PC Board (A101), containing the rectifiers, filter capacitors, and regulator circuitry.
- Chassis mounted components consisting of the power transformer (T1), primary wiring, F1 fuse; (100/120V), the 220/240V power programming switch; and the on/off power switch (S101) mounted on the front panel.

The basic voltages required by the counter are unregulated +18V, regulated +5V, −5.2V, +12V and −12V.

The input AC voltage is full wave rectified and filtered to produce DC voltages of ± 9V and ± 18V.

The unregulated +18V is used directly as one supply voltage. The +18V is regulated to a +12V by the action of LM305, a series pass transistor (MJE3055), and foldback current limiting circuitry. The −18V is regulated to a −12V by LM304, a series pass transistor, and foldback current limiting circuitry.

The +9V is regulated to +5V by a three terminal regulator containing thermal and current shutdown circuitry. The −9V current is also regulated to −5.2V by a three terminal regulator that contains thermal and current shutdown circuitry.

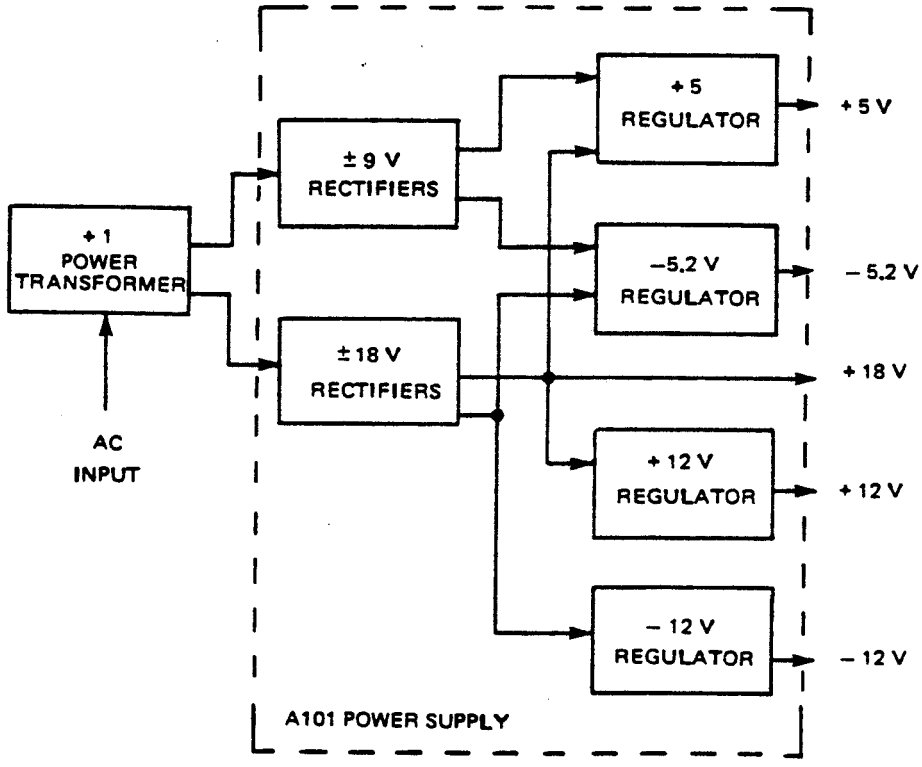

Figure 101-1. Power Supply Functional Diagram

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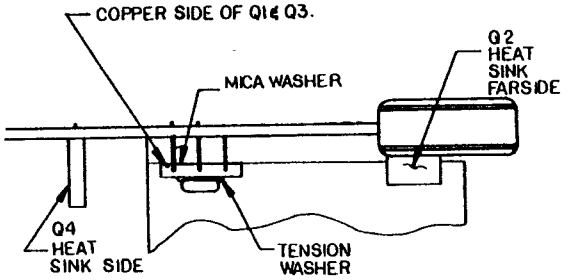
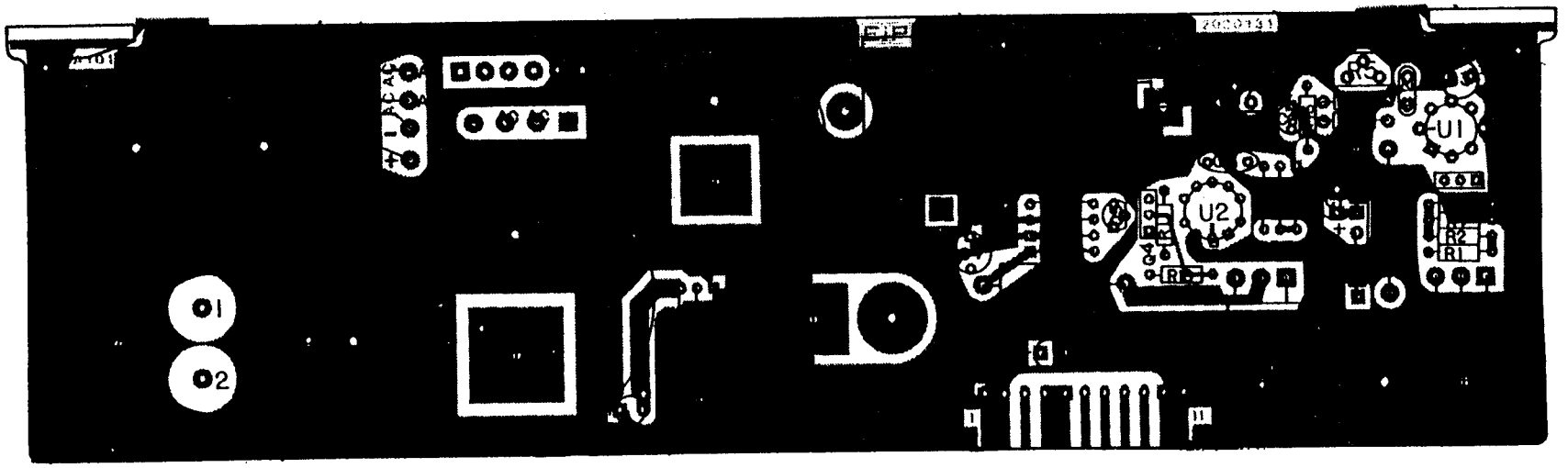
A101 POWER SUPPLY ASSY

2020131-L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A101	Power Supply Assy	2020131	1	EIP	34257
C1	Tant. 10μF. 20%, 25V	2300029	3	TAG 20 - 10/25(M)	14433
C2	Mica, 47 pF, 5%, 500V	2260004	1	DM10 - 470J	72136
C3	C1				
C4	Tant, 33μF, 20%, 20V	2300023	1	TAG 20 - 33/20 - 20	14433
C5	Cer, .001μF, 20%, 20V	2150001	1	5GA - D10	56289
C6	Tant, 1.0μF, 20% 35V	2300008	2	TAG 20 -1.0/35 - 50	14433
C7	Elec, 14,000μF, 25V	2200017	1	3110HB143U025	80031
C8	Elec, 9,500μF, 15V	2200016	1	3110HA952U025	80031
C9	Elec, 32,000μF, 15V	2200019	1	3110RB323U015	80031
C10	Elec, 4,900μF, 15V	2200020-00	1	3050JJ4920U15JM	80031
C11	C6				
C12	C1				
CR1 thru CR4	Rectifier	2704001	4	IN4001	07263
CR5	Zener, 12V	2720963	1	IN963A	04713
CR6	Rectifier Brdg	2710029	1	MDA970 - 1	04713
CR7	Rectifier, Brdg	2710028	1	MDA990 - 1	04713
J1	Conn, 6 pin (FRCTN Lock)	2620157	1	640445-6	0000A
Q1	NPN Power	4710001	2	MJE3055	04713
Q2	PNP Power	4710002	2	MJE370	04713
Q3	Q1				
Q4	Q2				
Q5	PNP, General Purpose	4704126	1	2N4126	04713
R1	Comp, 68 ohms, 5%, 1/4 W	4010680	2	RC07GF680J	81349
R2	Met Ox, 36 ohms, 2%, 1/4 W	4130360	1	C4/2%/36	24546
R3	Wire Wound, 0.66 ohms, 3%, 4W	4110012	2	RS - 2	91637
R4	Prec, 14.7K ohms, 1%, 1/8 W	4061472	1	RN55D1472F	81349
R5	Var. Cer., 500 ohm	4250014	1	72XR500	73138
R6	Prec, 2.26K ohms, 1%, 1/8 W	4062261	1	RN55D2261F	81349
R7	Met Ox, 820 ohms, 2%, 1/4 W	4130821	2	C4/2%/820	24546
R8	R7				
R9	R3				
R10	R1				
R11	Comp, 100 ohms, 5%, 1/4 W	4010101	1	RC07GF101J	81349
R12	Met Ox, 910 ohms, 2%, 1/4 W	4130911	1	C4/2%/910	24546
R13	Met Ox, 12K ohms, 2%, 1/4 W	4130123	1	C4/2%/12K	24546
R14	Prec, 2.43K ohms, 1%, 1/8 W	4062431	1	RN55D2431F	81349
R15	Prec, 4.7K ohms, 2%, 1/4 W	4130472	1	C4/2%/4.7	24546
R16	Met Ox, 1K ohms, 2%, 1/4 W	4130102	1	C4/2%/1K	24546
R17	Var, Cer, 2K ohms	4250016	1	72XR2K	73138
U1	Voltage Regulator	3040305	1	LM305	0000X
U2	Voltage Regulator	3040304	1	LM304	0000X
U3	+5VDC Regulator	3057805-01	1	UA78H05A	07263
U4	-5.2 V Regulator	3057905	1	MC7905.2 CT	04713





2020131-01-L

Figure 101-2. Power Supply Component Locator

A105
MICROPROCESSOR
(2020195)

In the normal fetch and execute cycle, the microprocessor executes the command sequence stored in the PROMs and, coupled with its I/O capability, obtains complete control over the counter.

The Microprocessor assembly (A105) is divided into four functions as follows:

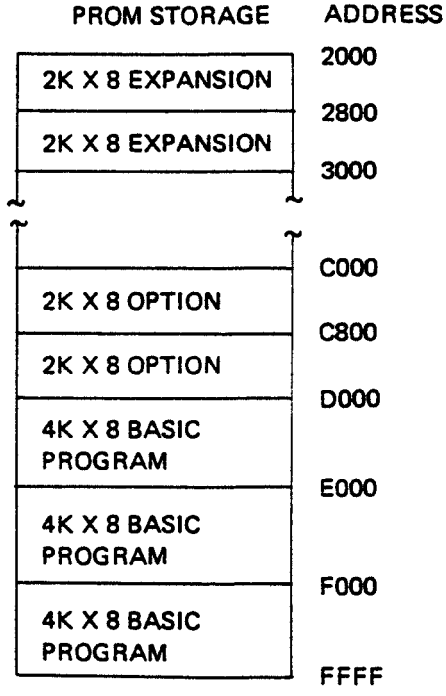
1. Microprocessor
2. Memory elements
3. Power-up reset circuit
4. Control logic and buffers

MICROPROCESSOR

The MCM6802 microprocessor (U1) is used as the main controlling element for the counter. It is driven by a 4 MHz crystal and controls all counter functions by means of a stored program in PROM.

MEMORY ELEMENTS

The memory elements consist of two 1K X 4 RAMs (U6, U7) that are configured to give a total of 1K X 8 storage locations. The basic program for the counter is stored in three 4K X 8 PROMs (U13, U15, U17). Option programs are stored in two 2K X 8 PROMs (U14, U16) and expansion PROMs U19, U20 give the microprocessor board the capability of 20K X 8 total locations for program storage. The memory map for the PROMs is as follows :



POWER-UP RESET CIRCUIT

The power-up reset circuit consists of comparator U3 and its associated components. Resistor R5 provides hysteresis action for the circuit while CR1 provides a path for fast decay time of capacitor C4.

CONTROL LOGIC AND BUFFERS

The I/O select line is used to enable I/O chips associated with the processor system. The equation for the selection of I/O is :

$$\text{I/O SEL} = \text{VMA} \cdot \text{A15} \cdot \overline{\text{A14}}$$

The three buses which are brought out of the microprocessor board are the 16 bit address bus, the 8 bit data bus, and the 6 bit control bus. Buffer/Driver chips U9, U10, U11, U12 provide drive current that is sufficient to drive the external bus.

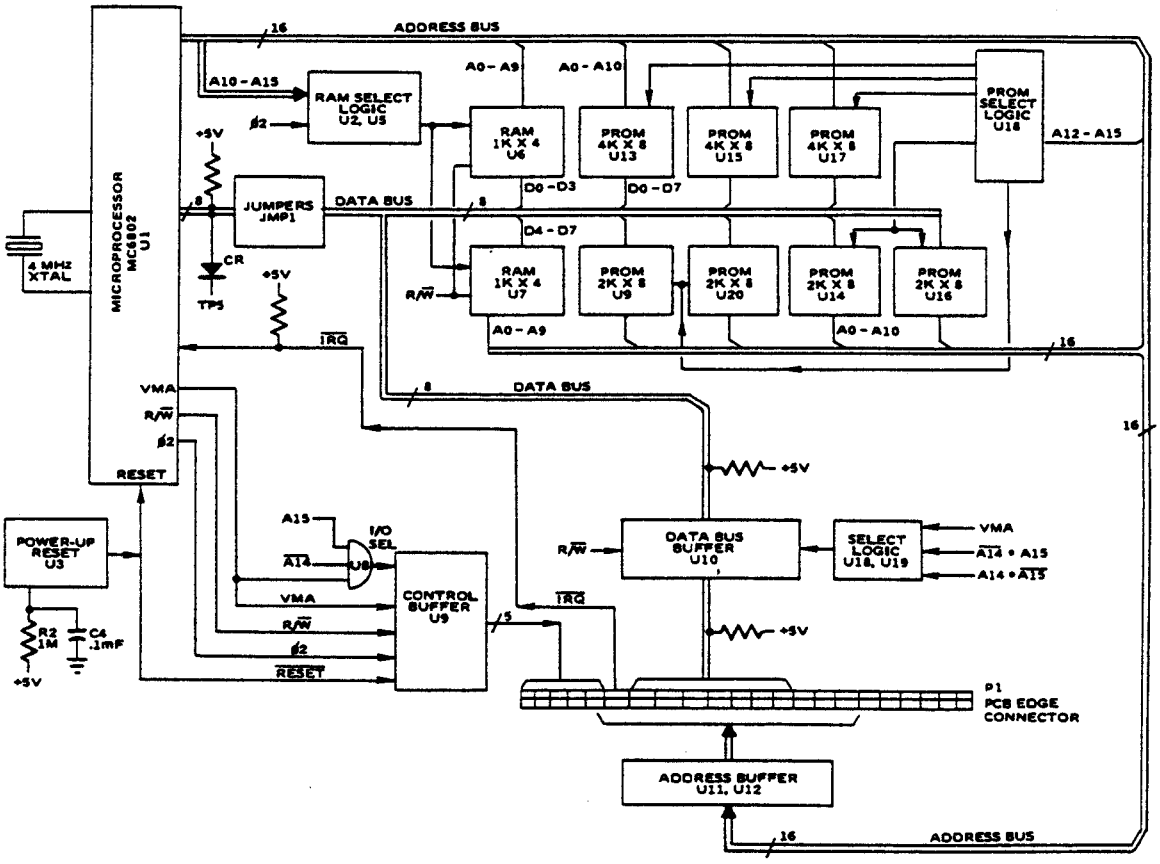


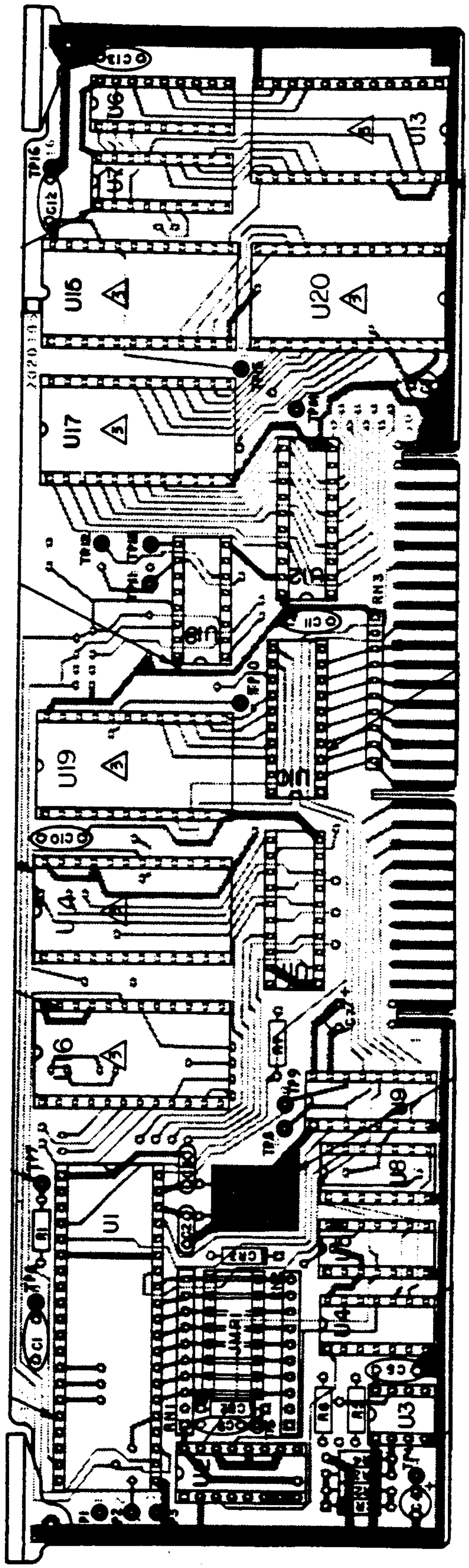
Figure 105-1. Microprocessor Assembly A105

A105 MICROPROCESSOR

2020195 - E

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A105	Microprocessor Assy	2020195	1	EIP	34257
C1	Cer, .01μF, 20%, 100V	2150003	7	TG - S10	56289
C2	Mica, 12pF, 5%, 500V	2260013	1	CD10CD120J03	72136
C3	Mica, 15pF, 5%, 500V	2260014	1	CD10CD150J03	72136
C4	Tant, 0.1μF, 20%, 35V	2300020	1	TAPA 0.1M35	14433
C5	C1				
C6	Not used				
C7	Tant, 33μF, 20%, 10V	2300015	2	TAPA 33M10	14433
C8	C7				
C9 thru C13	C1				
CR1 thru CR3	Hot Carrier	2710004	3	FH 1100	07263
R1	Comp, 10K, 5%, 1/8W	4010103	2	RC07GF103J	81349
R2	Comp, 1M, 5%, 1/8W	4010105	1	RC07GF105J	81349
R3	R1				
R4	Comp, 4.3K, 5%, 1/8W	4010432	1	RC07GF432J	81349
R5	Comp, 22K, 5%, 1/8W	4010223	1	RC07GF223J	81349
R6	Comp, 4.7K, 5%, 1/4W	4010472	2	RC07GF472J	81349
RN1 thru RN3	Network, 10K	4170003	3	785-1-R10K	80740
TP1 thru TP16	Conn, Pin, .04D, Gold	2620032	16	460-2970-02-03	71279
U1	MPU W/CLK-RAM	3056802	1	MC6802	04713
U2	6 Bit Comparator	3078136	1	DM8136	27014
U3	Voltage Comparator	3050311	1	LM311N	0000X
U4	Hex Inverter	3087404	1	DM74LS04	0000X
U5	3-INP NAND Gate	3087410	1	DM74LS10	0000X
U6	1K x 4 Bit RAM	3052114	2	2114	EM&M
U7	U6				
U8	3-INP AND Gate	3087411	1	DM74LS11N	0000X
U9	Hex Bus Driver/Buffer	3084365	1	SN74LS365N	01295
U10	Octal Bus Transceiver	3084245	1	SN74LS245N	01295
U11	Line Driver/Octal Buffer	3084244	2	SN74LS244N	01295
U12	U11				
U13	PROM, Basic 2	2060010-01	1	6500010-01	
U14	Not Used				
U15	PROM Basic 4	2060010-01	1	6500010-03	
U16	PROM Basic 1	2060010-01	1	6400010-01	
U17	PROM Basic 3	2060010-01	1	6500010-02	
U18	2–4 Lie Decoder/DE Mult.	3084139-01	1	SN74LS139N	01295
U19	PROM GPIB Option	2060010-02	Ref.	6400010-03	01295
Alt. U19	PROM BCD Remote Option	2060010-05	Ref.	6400010-04	
U20	PROM Band 4 Option	2060010-06	Ref.	6400010-02	
	4 MHz Crystal	2030015	1	MP1PR400	

PROMs installed at basic counter assembly. See page 9-4.



⚠4 REWORK INSTRUCTIONS FROM REV B TO REV C (USING FAB 5260195 AT REV A) PER ECN 3069.

⚠3 INSTALLED AT ABASIC COUNTER ASSY.

2020195-E

Figure 105-2. Microprocessor Component Locator

A106
COUNT CHAIN
(2020136)

The Count Chain Assembly receives IF signals from the Band 3 IF Amplifier (A201B) and the Band 2 Converter (A109). It also receives a gate signal and a 100 kHz reference signal from the Gate Generator (A107). The count chain assembly selects the appropriate IF signal, gates it, and counts it to produce a BCD output that represents the input frequency. It also produces one or two IF output signals to be used for options at J3 and J4.

The A106 board receives two IF input signals on J1 and J2. The appropriate input is selected by enabling one of two differential amplifiers (U1A or U1B). Enabling of the appropriate amplifier is achieved by turning on a transistor switch (Q11 or Q12). The appropriate transistor is turned on by the output of an open collector inverter (U7C or U7A) driven by a TTL signal from the PIA (U10).

The output of the input selector differentially drives a squaring circuit. The squaring circuit consists of a differentially driven current mirror (Q1) driving a tunnel diode (CR5). The voltage across the tunnel diode changes abruptly between two states (approximately 0.2V and 0.5V). The signal across the diode drives the pulse forming circuit. This circuit begins with a high speed differential amplifier (Q2 and Q3). The output of this amplifier drives Q4 which is a current switch. The square wave current, from Q4's collector, drives an inductor (L1). The voltage across the inductor is a series of pulses; a positive pulse when Q4 turns on and a negative pulse when Q4 turns off. Diode CR5 tends to remove the negative pulses and increases the damping to improve the amplitude of the positive pulses. The positive pulses from the generator drive a pulse inverter (Q6). The pulse inverter is a high-speed zero bias amplifier that is biased at cut off by diode CR6.

The output of the pulse inverter (Q6) drives the input to the first decade counter (U2). The bias for the U2 input is established by a tracking bias supply (U3, Q7). The voltage at TP2 is equal to the voltage on U2 pin 1, plus a fixed DC offset selected by R45. The BCD outputs from U2 are slew-rate limited, and can only be seen after the counting ends and comes to rest. The carry output on pin 9 is an ECL level U2 signal, and is always visible.

The ECL output of U2 drives an ECL to TTL converter (Q8, Q9 and Q10). This converter is a differential amplifier with a cascode output buffer (Q8). The response of Q8 is improved by inductive peaking provided by L2. The output of Q8 drives a decade counter (U4) which in turn drives a third decade counter (U5). The BCD outputs of U4 and U5 are connected to a 6 decade counter (U6) which derives its clock information directly from the BCD outputs of U5. When counting is finished, 8 decades of BCD data are read by the microprocessor (through the PIA U10) from U6 by a time multiplex process. The multiplexer (set to the first digit by the end of the previous reset clock) loads the multiplex latches with the $\overline{\text{Latch Load}}$ clock, and steps to the remaining 7 digits with 7 pulses on the $\overline{\text{Scan Clock}}$ line. The first decade of BCD data from U2 is read directly from the PIA.

A single reset line is used to reset all count stages to zero before the next count cycle begins.

A real-time clock (U8, U9) is also on the count chain assembly. This circuit takes the 100kHz reference signal, that is coming from the Counter Interconnect Assembly (A100), and divides it by 10,000 to give a 10Hz (100ms) clock. The output from this clock is fed to the PIA to allow the microprocessor to gather time information at a 10Hz rate for timing functions within the program.

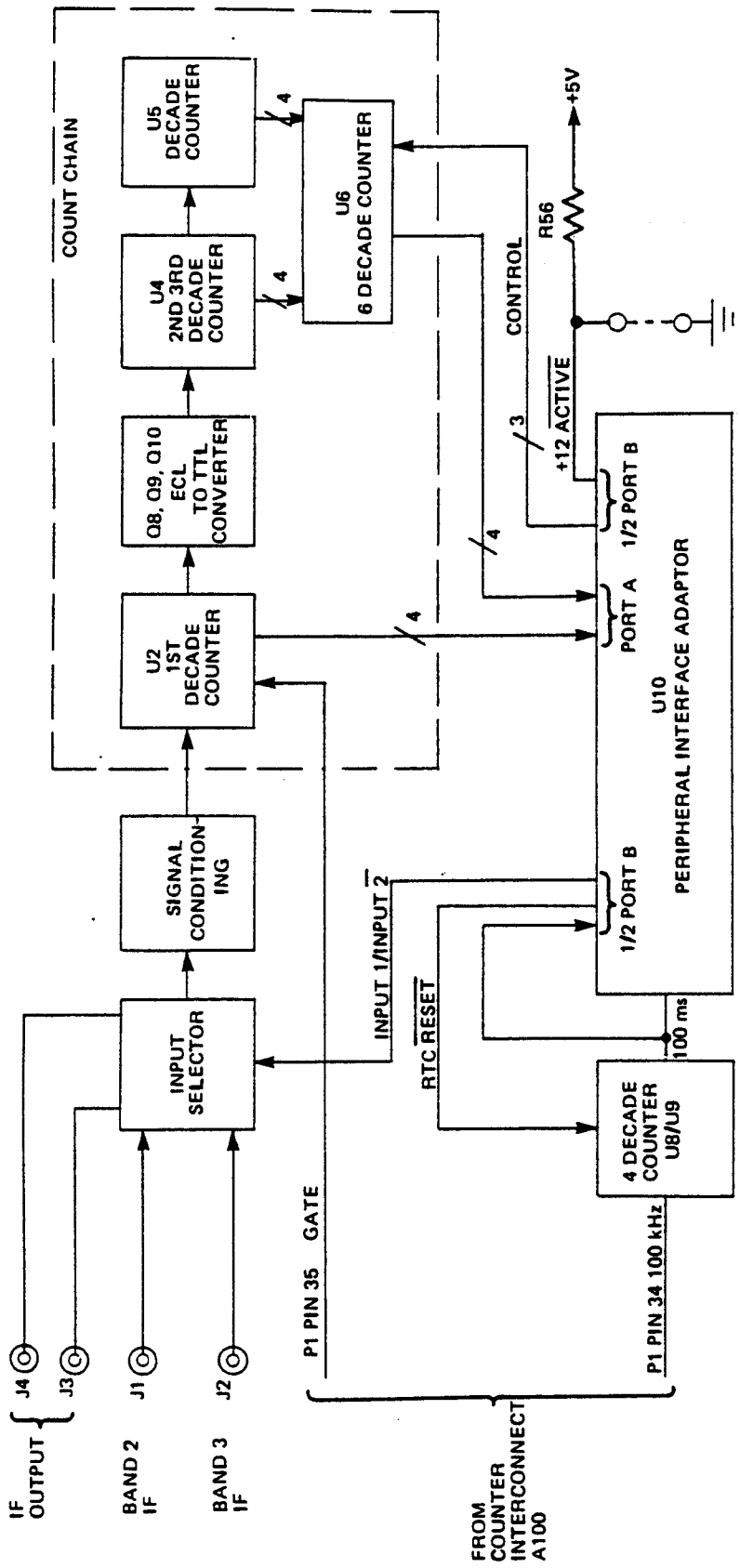


Figure 106-1. Count Chain Functional Diagram

A106 COUNT CHAIN ASSY

2020136 - S

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A106	Count Chain Assy	2020136	1	EIP	34257
C1	Tant, 33μF, 20%, 10V	2300015	5	TAG 20 - 33/10 - 50	14433
C2	Cer., .01μF, 20%, 100V	2150003-00	17	TG - S10	56289
C3	C2				
C4	C1				
C5	Mica, 10pF, 5%, 500V	2260012	1	CD100J03	72136
C6	Tant, 10μF, 20%, 25V	2300029	4	DF106M259	72136
C7	C2				
C8	C2				
C9	Cer., .001μF, 20%, 1KV	2150001	3	5GA - D10	56289
C10	C2				
C11	Not used				
C12	C9				
C13	C2				
C14	C6				
C15	C6				
C16	C2				
C17	C9				
C18	Not Used				
C19	Not Used				
C20	C1				
C21	C2				
C22	C1				
C23	Not Used				
C24 thru C28	C2				
C29	C1				
C30 thru C33	C2				
C34	C6				
CR1	Diode: Fast Sw	2704148	3	IN4148	07263
CR2	Zener, 6.2V	2705234	1	IN5234	04713
CR3	CR1				
CR4	Tunnel, Switching	2710033	1	G00010C	20754
CR5	Hot Carrier	2710004-00	1	5082 - 2835	28480
CR6	CR1				
L1	Part of Board				
L2	Inductor, 1μH	3510003	1	DD 1.0	72259
Q1	PNP, RF	4704959	1	2N4959	04713
Q2	NPN, RF SW	4710017	3	MMT 3960	04713
Q3	Q2				
Q4	PNP, RF	4710010	1	MPS - H81	04713
Q5	PND, RF GRADED	4710013	1	2N5179	34257
Q6	NPN, RF	4710026	1	NE73432B	0000S
Q7	Q2				
Q8	NPN, RF	4705179	3	2N5179	04713
Q9	Q8				
Q10	Q8				
Q11	PNP, General Purpose	4704126	2	2N4126	04713
Q12	Q11				

A106 COUNT CHAIN ASSY, continued

2020136-S

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1	Comp., 1.5K, 5%, 1/4 W	4010152	2	RC07GF152J	81349
R2	Comp., 6.2K, 5%, 1/4 W	4010622	2	RC07GF622J	81349
R3	Comp., 51 ohm, 2%, 1/4 W	4130510-00	2	C4/2%/51	24546
R4	Comp., 5.1K, 5%, 1/4 W	4010512	2	RC07GF512J	81349
R5	Comp., 2.7K, 5%, 1/4 W	4010272	2	RC07GF272J	81349
R6	Comp., 51 ohm, 5%, 1/4 W	4010510	1	RC07GF510J	81349
R7	Met Ox, 2K, 2%, 1/4 W	4130202	3	C4/2%/2K	24546
R8	Comp., 510 ohm, 5%, 1/4 W	4010511	1	RC07GF511J	81349
R9	Comp., 5.6 ohm, 5%, 1/4 W	4010569	5	RC07GF5R6J	81349
R10	R5				
R11	R9				
R12	Met Ox, 68 ohm, 2%, 1/4 W	4130680	1	C4/2%/68	24546
R13	Met Ox, 43 ohm, 2%, 1/4 W	4130430	1	C4/2%/43	24546
R14	Met Ox, 3.9K, 2%, 1/4 W	4130392	1	C4/2%/3.9K	24546
R15	R7				
R16	R4				
R17	R1				
R18	R2				
R19	Comp., 100 ohm, 5%, 1/4W	4010101	1	RC07GF101J	81349
R20	Met Ox, 56 ohm, 2%, 1/4 W	4130560	2	C4/2%/56	24546
R21	R9				
R22	R20				
R23	Comp., 360 ohm, 5%, 1/4 W	4010361	1	RC07GF361J	81349
R24	R9				
R25	Met Ox, S.A.T. (2K, 2% Nom)	4130999	1	C4/2%/XX	24546
R26	Met Ox, 39 ohm, 2%, 1/4 W	4130390	2	C4/2%/39	24546
R27	Met Ox, 200 ohm, 2%, 1/4 W	4130201	3	C4/2%/200	24546
R28	Met Ox, 270 ohm, 2%, 1/4 W	4130271	1	C4/2%/270	24546
R29	R3				
R30	Not used				
R31	Comp, 10 ohm, 5%, 1/4 W	4010100	1	RC07GF100J	81349
R32	Met Ox, 47 ohm, 2%, 1/4 W	4130470	1	C4/2%/47	24546
R33	Met Ox, 20 ohm, 2%, 1/4 W	4130200	1	C4/2%/20	24546
R34	Met Ox, 510 ohm, 2%, 1/3 W	4130511	1	C4/2%/510	24546
R35	R9				
R36	Met Ox, 1K, 2%, 1/4 W	4130102	3	C4/2%/1K	24546
R37	R26				
R38	Comp., 390 ohm, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R39 thru R42	Comp, 10 K, 5%, 1/4 W	4010103	4	RC07GF103J	81349
R43	Met Ox, 20 K, 2%, 1/4 W	4130203	4	C4/2%/20K	24546
R44	R43				
R45	R36				
R46	R43				
R47	Met Ox, 18 ohm, 2%, 1/4 W (NOM) SAT	4130999	1	C4/2%/18	24546
R48	R43				
R49	Met Ox, 240 ohm, 2%, 1/4 W	4130241	1	C4/2%/240	24546
R50	R27				
R51	R27				
R52	R36				
R53	Met Ox, 430 ohm, 2%, 1/4W	4130431	1	C4/2%/430	24546

A106 COUNT CHAIN ASSY, continued

2020136-S

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R54	R7				
R55	Comp., 1.8K, 5%, 1/4 W	4010182	1	RC07GF182J	81349
R56	Comp., 4.7K 5%, 1/4 W	4010472	1	RC07GF472J	81349
TP1 thru TP10	Conn., Pin, .040D	2620032	10	460-2970-0203	71279
U1	Dual/Diff Ampl	3043049	1	CA3049T	07263
U2	UHF, BCD, Decade Counter	3010637	1	SP8637B	58317
U2 Alt.	High Spd. Div.	3018636	Ref.	SP8636D	58317
U3	Op Amplifier	3040741	1	UA741CD	27014
U4	PST Decade Counter	3084196	1	SN74LS196N	01295
U5	4 Bit Decade Counter	3084160	1	SN74LS160N	01295
U6	6 Dec. Ctr/8 Dec. Latch	3057031	1	LS7031	01295
U7	Hex Inverter	3087404	1	SN 74LS04N	04713
U8	Decade Counter	3084490	2	74LS490N	01295
U9	U8				
U10	Periph. Interface Adapter	3086820	1	MC6820	04713

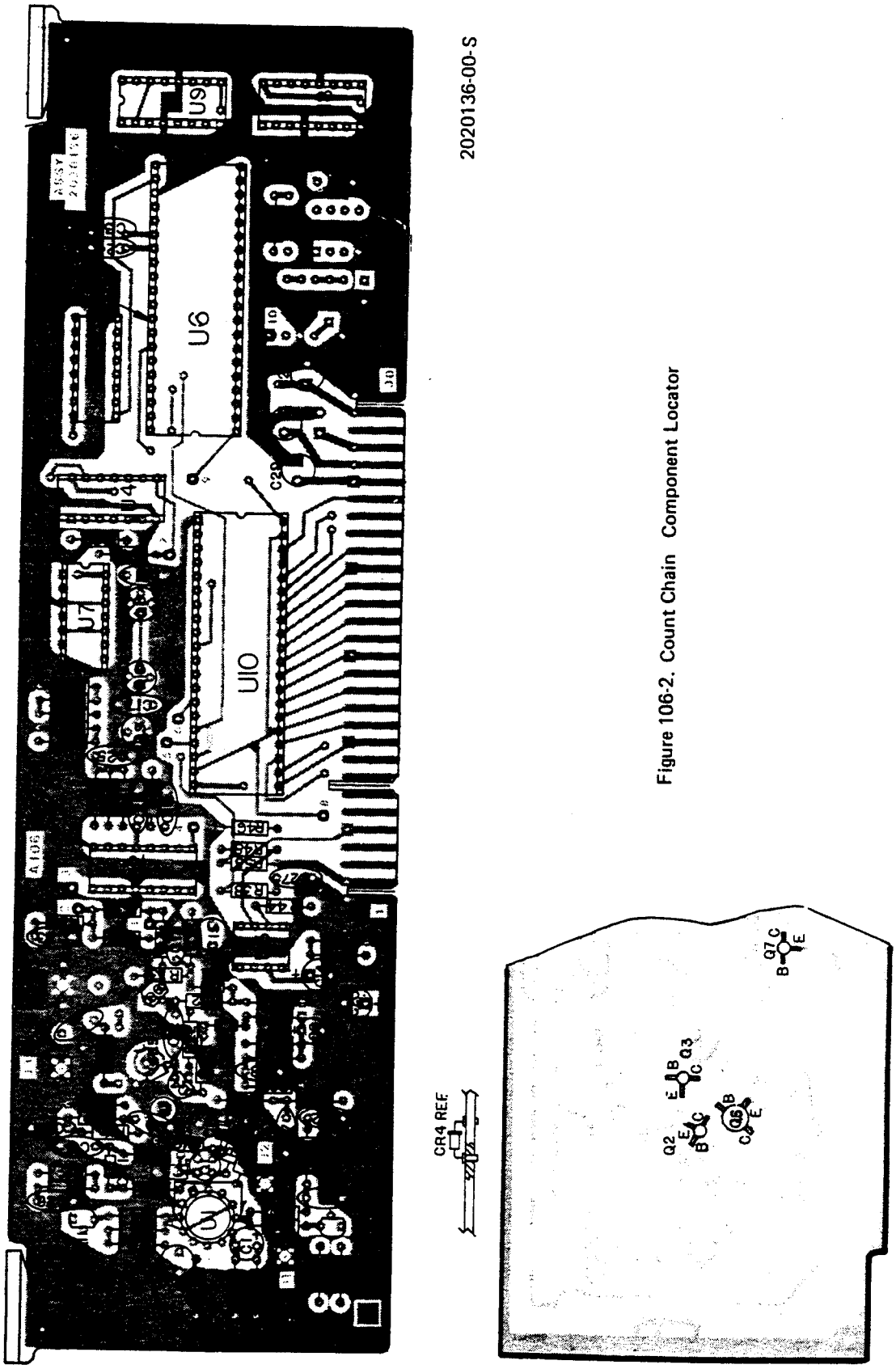


Figure 106-2. Count Chain Component Locator

A107
GATE GENERATOR
(2020197)

This assembly performs the following functions.

- Reference Oscillator Control
- Gate Generation
- Band 3 Amplitude Determination
- Power Meter Control (Option 02 only)

REFERENCE OSCILLATOR CONTROL

This circuit selects, as the time base for the counter, either the internal reference oscillator or an external 10 MHz signal applied to the rear panel. This circuit provides a 100 kHz TTL level clock signal for the gate generator, a 10 MHz TTL level clock signal for the microwave converter and, in the internal oscillator mode, a 10 MHz signal (1 volt p-p into 50 ohms) to the rear panel.

The 10 MHz internal reference signal is applied to a switchable "analog to TTL" converter (Q1, Q2, Q3). When the Ref Int/Ext line is high the TTL converter is enabled. One output goes to drive Q4, giving a square wave (1V p-p into 50 ohms) on the 10 MHz Ref line. A second output goes to NAND gate U1 (also switchable for signal isolation. The output of U1 goes to J3 to be used by the microwave converter. The output of U1 also goes to the clock input of U2. U2 is a dual decade divider that divides by 100. The output of U2 is a 100 kHz TTL clock signal to the gate generator.

When the Reference Int/Ext line is set to external (low) the TTL converter (Q1, Q2, Q3) and driver (Q4) are disabled, TTL converter (Q5, Q6, Q7) is enabled, and U1 is set to select the external input. An external reference signal applied to the 10 MHz reference line is then converted to the input of U2.

GATE GENERATOR

The Gate Generator must provide an accurate, stable, signal gate to the Count Chain. The gate must be switchable, in decade increments, between 100 micro sec and 1 sec. The gate generator consists of a programmable divide-by-N time base (U5), a dual flip-flop (U6A, U6B), and an ECL flip flop (U8). The divide ratio of U5, which determines the gate time, is set by U5 pins 12, 13, and 14 as follows.

Pin 12	Pin 13	Pin 14	Divide Ratio	Gate Time
0	0	1	10^1	100 μsec
0	1	0	10^2	1 Msec
0	1	1	10^3	10 Msec
1	0	0	10^4	100 Msec
1	0	1	10^5	1 sec

The outputs of U5 and U6 enable ECL flip-flop U8, but U8 is clocked directly from the 100kHz clock to insure gate accuracy.

When the gate is not active, U5 is permitted to free-run by holding U6B clear (T0). The gate is initialized by setting U6B. This clears U6A and clears U5 (T1). The next clock pulse sets U8 (T2). The gate is then enabled by momentarily clearing U6B (T3). The next clock sets U6A which enables U5 and U8 (T4). At T5 the gate is opened and U5 begins counting clocks (T5). Halfway through the gate, U5 pin 1 goes high (T6). After U5 has accumulated the proper number of clocks its output, pin 1, goes low. This sets U6B, which clears U6A, and sets U8 pin 7 high (T7). The next clock closes the gate (T8). The program next clears U6B (T9), which enables the gate to free-run again (T0). See figure 107-1.

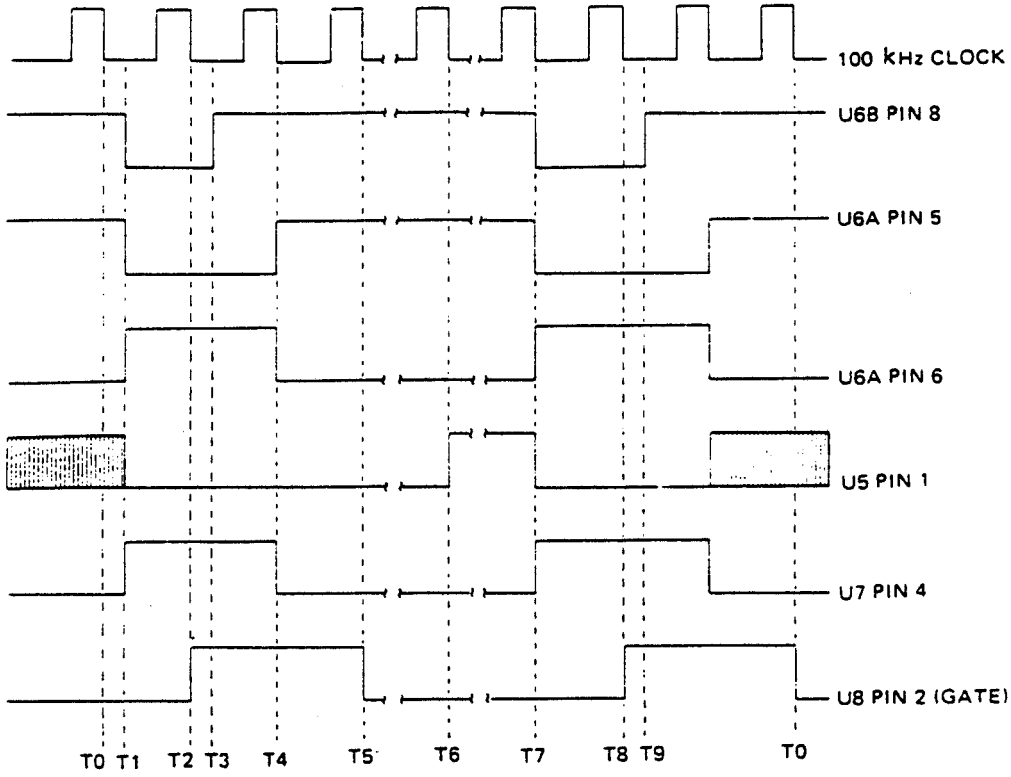


Figure 107-1. Gate Generator Timing Diagram

BAND 3 AMPLITUDE DETERMINATION

This circuit consists of three main parts.

- THE POWER METER ZERO DAC is used to automatically zero offsets in the Power Meter. It consists of two 8 bit latching DACs (U3, U4), and a comparator (U14A). All the latching DACs are driven in parallel by shift register U16, with the appropriate DAC being written to by the four write lines (U15, pins 2, 4, 6, 8). The coarse DAC (U3) has a range of ± 200 micro amps, and the fine DAC (U4) has a range of +1.5 micro amps. The Power Meter Zero DAC (U3) is adjusted so that on step 1 U14A is not set, but on the next step U14A is set. This adjusts the input to U14 to 0 volts, nulling any offsets in the power meter circuit.

- THE POWER METER consists of a 15 dB switchable gain stage (U9), an 8 bit DAC used as a variable attenuator (U10), a 100 mV comparator (U14B), and a latch (half of U17). Two variable attenuators are used, on counters equipped with the option 02 power meter, to provide greater resolution (U10, U12).

  When the detected signal from the microwave converter enters U9 the power meter is first set for maximum gain and minimum attenuation. Next the latch (U17) is reset. If the input to the comparator (U14B) is greater than 100mV, latch U17 will be set. The signal amplitude to the comparator is then reduced, and the process is repeated until latch U17 no longer gets set. The input amplitude can then be calculated from the switch and DAC settings. On counters without the power meter option the amplitude is calculated to a 3dB resolution. On counters with the power meter option the amplitude is calculated to a resolution of 0.1dB.

- The POWER METER PROM (Option 02 only) contains a logic comparator (U21), a 2K X 8 prom (U20), and a bus driver (U19). The logic comparator is connected to the microprocessor address bus, and is configured to decode the 2K address range from 4000 Hex to 47FF Hex. The comparator output drives the chip select of the Prom, and the bus driver. The prom contains the Power Meter program as well as the power correction factors. Bus driver U19 is used as a buffer for driving the microprocessor data bus.

PERIPHERIAL INTERFACE ADAPTER (PIA)

The Peripherial Interface Adapter (U18) is used as the microprocessor I/O port. It has an address range from 9900 Hex to 9903 Hex. Peripheral Port A is at address 9900, and Peripheral Port B is at address 9902.

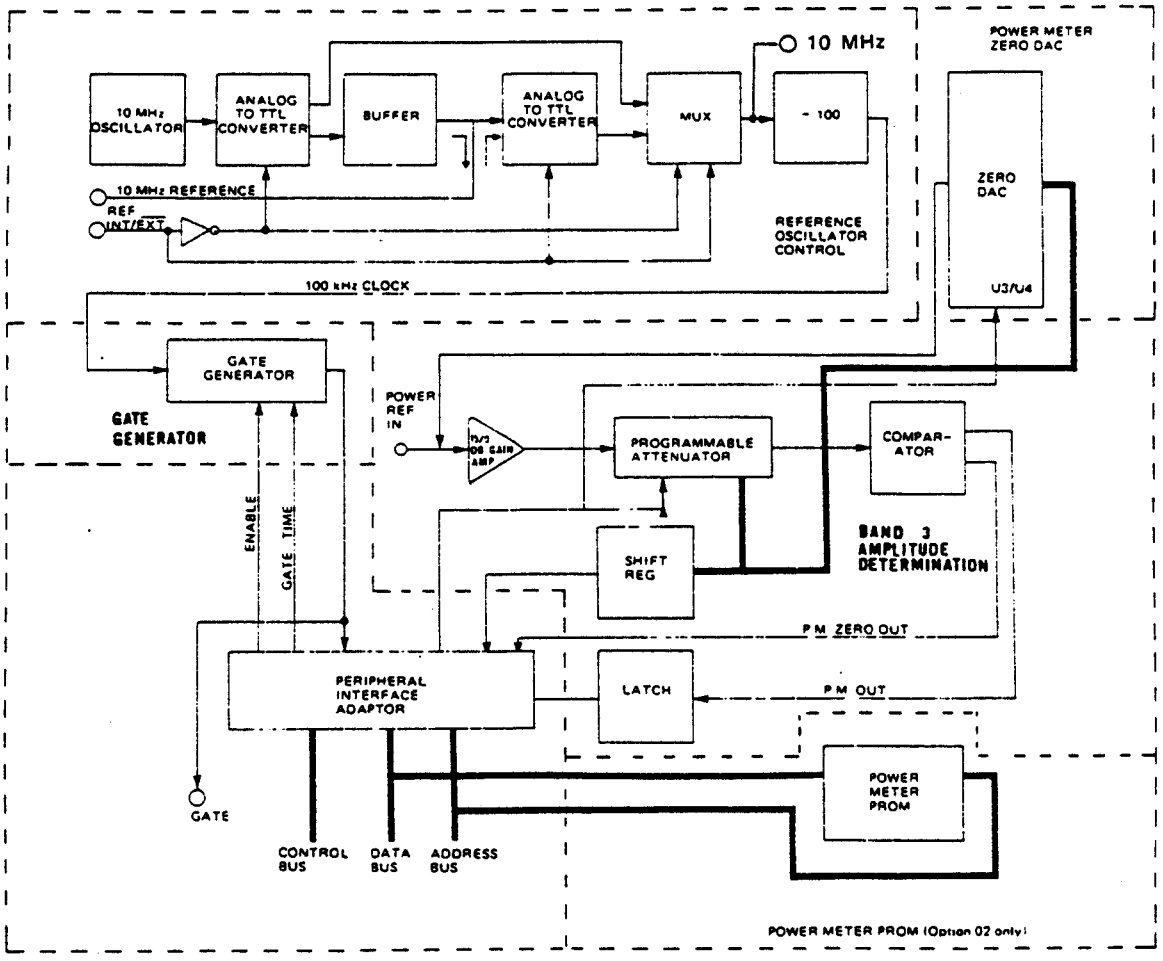


Figure 107-2. Gate Generator Block Diagram

A107 GATE GENERATOR

2020197-01/02 - L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A107	Gate Generator Assy -05/06	2020197	1	EIP	34257
	A113 Crystal Osc	2030002	Ref		
C1	Cer, .01μF, 20%, 100V	2150003	15	TG - S10	72982
C2	C1				
C3	Tant, 33μF, 20%, 10V	2300015	4	TAPA33M10	14433
C4 thru C7	C1				
C8	Mica, 22pF, 5%, 500V	2269999	1	CD10ED220J03	72136
C9	Tant, 1μF, 20%, 35V	2300008	1	TAPA 1.0M35	14433
C10	Mica, 33pF, 5%, 500V	2260021	2	CD10ED330J03	72136
C11	Mica, 100pF, 5%, 500V	2260034	1	CD10FD101J03	72136
C12	C10				
C13 thru C15	C1				
C16	Tant, 10μF, 20%, 25V	2300029	2	DF106M25S	76718
C17	C1				
C18	C3				
C19	C3				
C20	C1				
C21	C1				
C22	C3				
C23	C1				
C24	C1				
C25	C16				
C26	C1				
CR1	Hot Carrier	2710004	1	5082-2835	28480
CR2	Hot Carrier	2710006	1	5082-2800	28480
CR3	CR1 - Option only				
CR4	Zener, 6.2V	2700827	1	IN827	
R1	Comp, 10 ohm, 5%, 1/4W	4010100	2	RC07GF100J	81349
R2	Comp, 1K, 5%, 1/4W	4010102	2	RC07GF102J	81349
R3	Comp, 620, 5%, 1/4W	4010621	2	RC07GF621J	81349
R4	Comp, 2.2K, 5%, 1/4W	4010222	3	RC07GF222J	81349
R5	Comp, 220, 5%, 1/4W	4010221	2	RC07GF221J	81349
R6	Comp, 510, 5%, 1/4W	4010511	2	RC07GF511J	81349
R7	Comp, 200, 5%, 1/4W	4010201	1	RC07GF201J	81349
R8	Comp, 27, 5%, 1/4W	4010270	1	RC07GF270J	81349
R9	Comp, 300, 5%, 1/4W	4010301	1	RC07GF301J	81349
R10	Comp, 4.7K, 5%, 1/4W	4010472	6	RC07GF472J	81349
R11	R1				
R12	Comp, 2K, 5%, 1/4 W	4010202	2	RC07GF202	81349
R13	R10				
R14	R4				
R15	R5				
R16	R6				
R17	R3				
R18	Met Ox, 5.6K, 2%, 1/4W	4130562	1	C4/2%/5.6K	24546
R19	Met Ox, 3.3K, 2%, 1/4W	4130332	1	C4/2%/3.3K	24546
R20	Met Ox, 27, 2%, 1/4W	4130270	1	C4/2%/27	24546
R21	Comp, 2.7K, 5%, 1/4W	4010272	1	RC07GF272J	81349
R22	R10				
R23	R10				
R24	R2				

A107 GATE GENERATOR continued

2020197-01/02 - L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R25	R12				
R26	R4				
R27	Met Ox, 30K, 2%, 1/4W	4130303	1	C4/2%/30K	24546
R28	Met Ox, 39K, 2%, 1/4W	4130393	1	C4/2%/39K	24546
R29	Prec, 1.69K, 1%, 1/10W	4051691	1	RN55C1691F	81349
R30	Prec, 1.82K, 1%, 1/10W	4051821	1	RN55C1821F	81349
R31	Prec, 57.6K, 1%, 1/10W	4055762	1	RN55C5762F	81349
R32	Comp, 36K, 5%, 1/4W	4010363	1	RC07GF363F	81349
R33	Comp, 15K, 5%, 1/4W	4010153	1	RC07GF153F	81349
R34	Met Ox, 750, 2%, 1/4W	4130751	1	C4/2%/750	24546
R35	Prec, 6.19K, 1%, 1/8W	4056191	1	RN55C6191F	81349
R36	Prec, 100, 1%, 1/8W	4051000	1	RN55C1000F	81349
R37	R10				
R38	R10				
R39	Met Ox, 10K, 2%, 1/4W	4130103	2	C4/02/10K	24546
R40	R39				
*R41	Comp, 10K, 5%, 1/4W	4010103	1	RC07GF103J	81349
RN1	Network, 6.8K	4170005	1	4608X-101-682	80740
Q1	NPN - General Purpose	4704124	4	2N4124	
Q2	PNP - General Purpose	4704126	3	2N4126	
Q3	Q1				
Q4	Q2				
Q5	Q1				
Q6	Q2				
Q7	Q1				
Q8	DMOS, FET SW	4710031	1	SD215	18324
U1	Quad NAND	3084132	1	DM74LS132	01295
U2	Dual Decade Counter	3084490	1	SN74LS490N	01295
U3	8 Bit DAC	3057524	3	AD7524JN	
U4	U3				
U5	Digital P Chan. MOS Divider	3035009	1	MK5009P	
U6	D Type Pos Flip-flop	3087474	2	DM74LS74N	01295
U7	Quad 2-1 NP NOR Gate	3087402	1	DM74LS02N	01295
U8	Digital Dual D Flip-flop	3110131	1	MC10131L	04713
U9	Dual Low Noise Op Amp	3045534	1	NE5534N	
U10	8 Bit DAC Buff	3057525	2	AD7524LN	
U10	U3				
U11	Op Amplifier	3040308	2	LM308AN	27014
U12	U10 Buff				
U13	U11				
U14	Comparator Dual Low Pwr/Volt	3050393	1	LM393N	27014
U15	Hex Buffer/Driver	3007407	1	DM7407N	27014
U16	Dual 4 Bit Static S/R	3034015	1	MC14015B	04713
U17	U6				
U18	Periph. To MC6800	3086820	1	MC6821	01295
U19	Oct. Buffer (Option* 02 Only)	3084244	1	SN74LS244 (6400002-04)	01295
U20	PROM Set (Option* 02 Only)	2060002-03	1	TI-TM2516	04713
U21	6 Bit Comparator Bus (Option* 02 Only)	3078136	1	DM8136	27014
U22	Quad Dual Flip-flop	3084175	1	SN74LS175	01295
U23	Op Amp/Lin	3040741	1	LM741CN	27014
TP1-4	PC, Pin .040D	2626632	4	460-2976-02-03	71279

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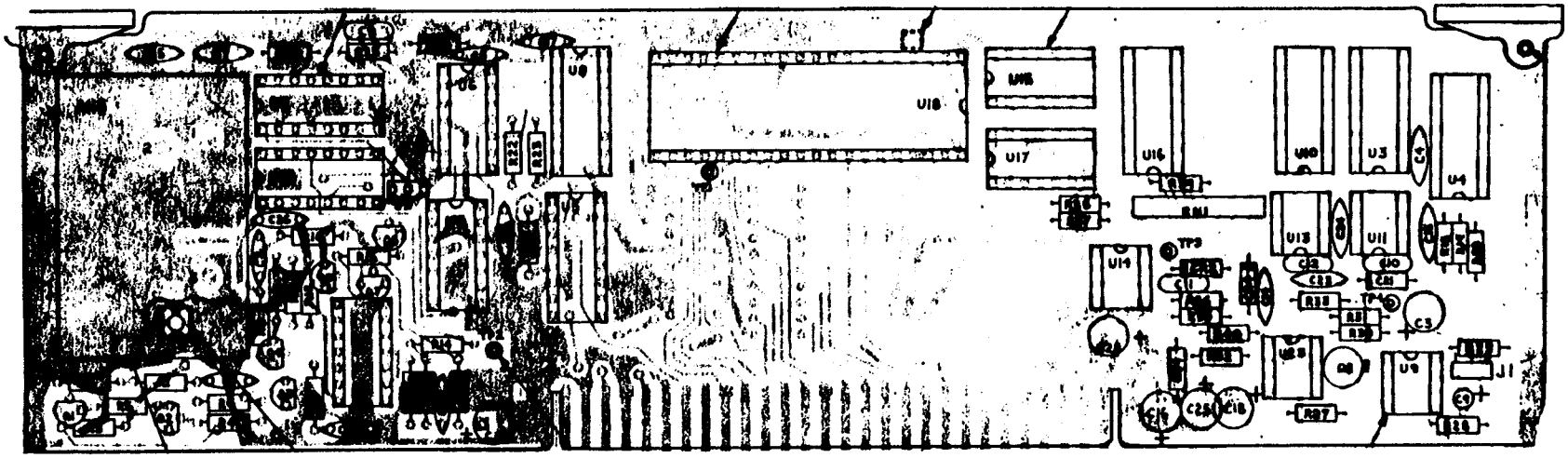

2020197-01/02-L

Figure 107-3. Gate Generator Component Locator

NOTE : If the counter contains Option 02 this board is replaced with 2020197-03/04.
Refer to Section 10, Option 02 for the 03/04 version of this assembly.

A108
CONVERTER CONTROL
(2020200)

The Converter Control performs two major functions. One of the functions is to provide a precise yig tuning current which is controlled by the microprocessor via P.I.A. U4. The other function is to phase lock the VCO in the microwave converter to a selected harmonic of a 50 kHz reference signal to provide a synthesized L.O. The converter control also permits the microprocessor to control the L.O. power amplifier and provides the microprocessor input for the I. F. threshold signal.

YIG FREQUENCY CONTROL DAC and DRIVERS

The yig tuning current is supplied by the yig driver (U3, Q1, Q2, & Q3) which is controlled by the DAC. The DAC is composed of a 12 bit monolithic DAC (U2), summing amplifier (U1) and resistors to provide a total resolution of 14 bits. PA ports 0 and 1 of the P.I.A. (U4) are used to drive the 2 least significant bits of the DAC directly. A change in the least significant bit of the DAC corresponds to a yig frequency change of 2 MHz. A voltage analog of yig current appears across R25 and is compared to the DAC output at the summing junction of U3, with resistors R1 and R19.

The slope of yig current vs DAC voltage is adjustable with R6 and the offset is adjusted with R10.

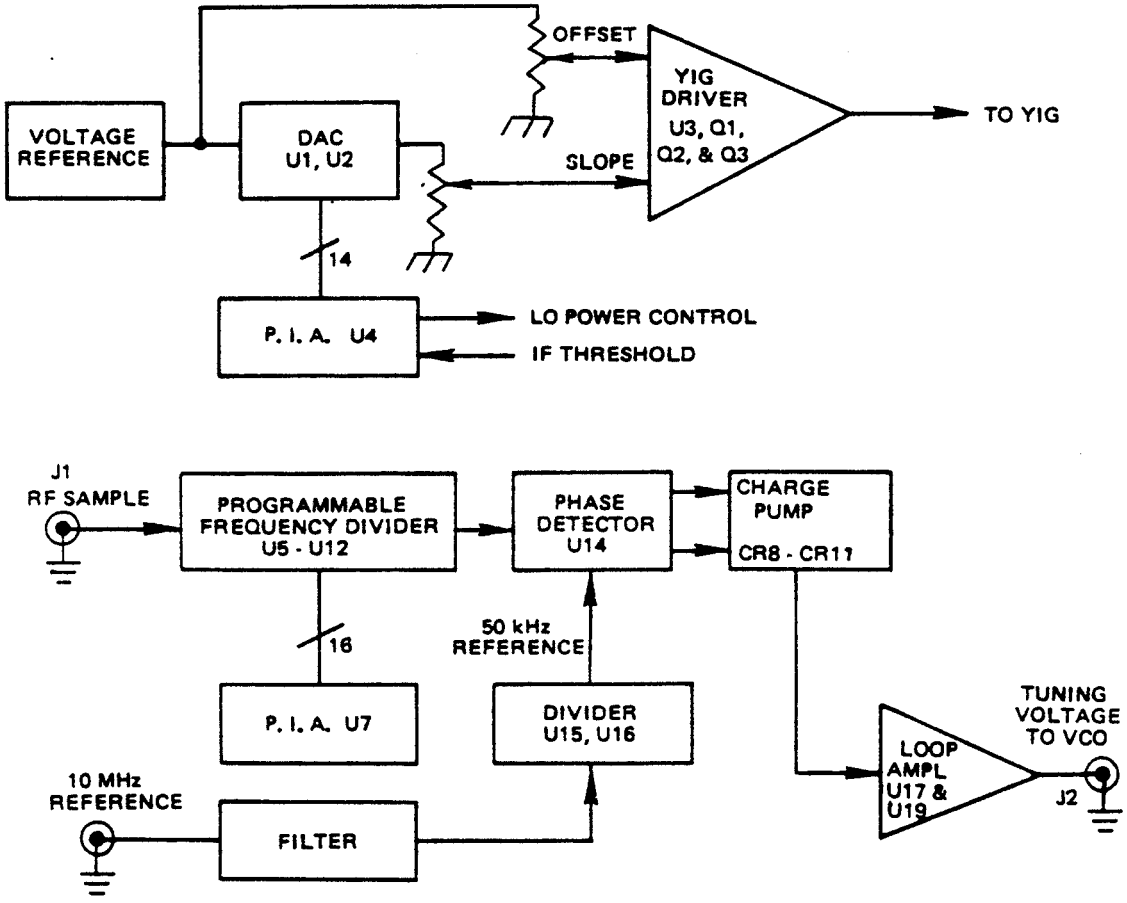

Figure 108-1. Converter Control Diagram

VCO CONTROL

The VCO control, together with the VCO, form a phase lock loop frequency synthesizer. The frequency range over which the synthesizer is used is from 370 MHz to 500 MHz.

An output of the VCO (via a buffer amplifier, U2, on the Band 2 converter board) is applied to the programmable frequency divider (U5-U13). The programmable frequency divider is programmed by the microprocessor via P.I.A. U7. The output of the programmable frequency divider is compared to the 50 kHz reference (derived from a 10 MHz clock from the gate generator board) in the phase detector U14. A phase difference between the divided down VCO and the 50 kHz reference will result in an output from the phase detector. The phase detector has two output ports, a pump-up port and a pump-down port. Pump-down is U14, pin 2. Pump-down is normally high and goes low to reduce the VCO frequency. Pump-up is U18, pin 3. Pump-up is normally low and goes high to increase the VCO frequency. The outputs of the phase detector go to the charge pump, which converts them to a single tri-state output. The charge pump output is open with no pump command, sources current with pump-up, and sinks current with pump-down. The output of the charge pumps is connected to the input of the loop amplifier U19 and U17. The loop amplifier provides the proper gain and filtering to achieve the desired loop response. The output of the loop amplifier is the VCO tuning voltage.

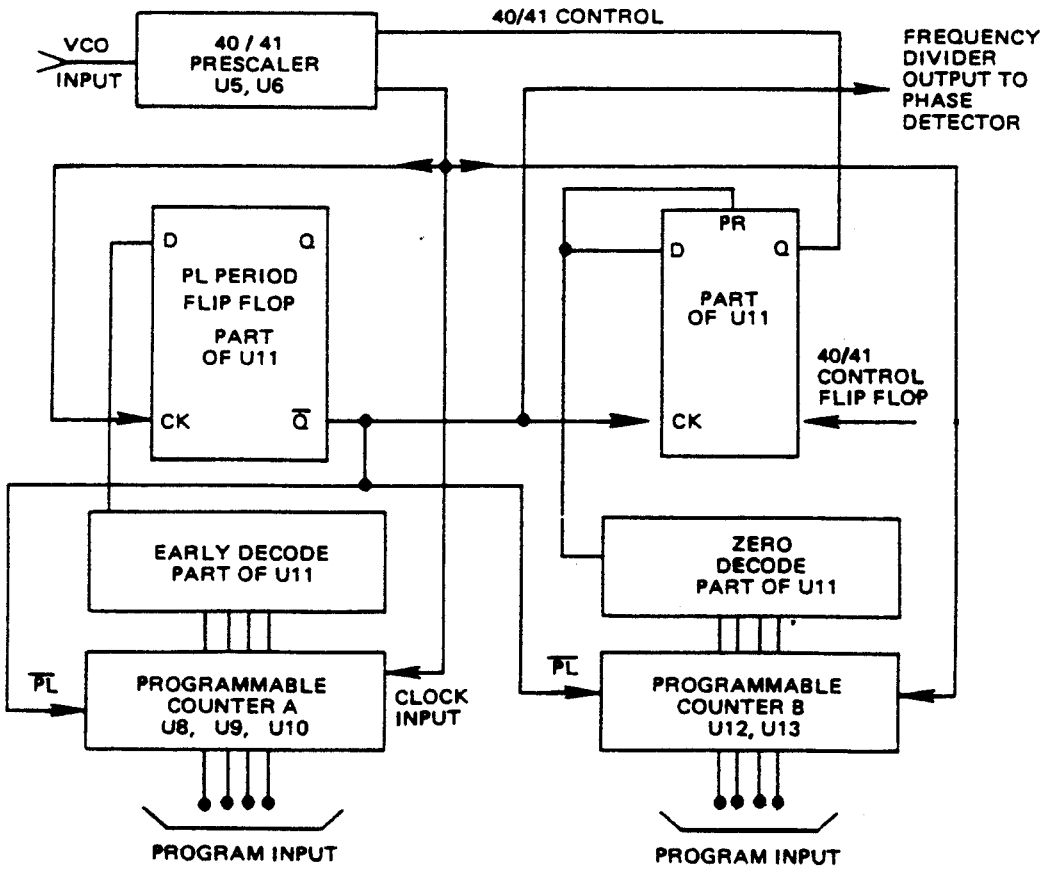

Figure 108-2. Programmable Frequency Divider Diagram

PROGRAMMABLE FREQUENCY DIVIDER

The programmable frequency divider uses a two modulus (divide number) prescaler (U5, U6) and two programmable counters (A & B). The prescaler is used to divide the VCO frequency down to a lower frequency which can be handled by low power schottky TTL programmable counters. The two modulus prescaler permits prescaling without loss of resolution. At the start of the programmable frequency divider cycle, the prescaler is set to divide by the larger modulus (41), and both programmable counters have been loaded with their respective program numbers from the PIA. The programmable counters each decrement 1 count for each output pulse from the prescaler. When programmable counter B (U12, U13) reaches the count of zero the 40/41 control flip-flop (part of U11)changes state and causes the prescaler to divide by the lower modulus (40). When programmable counter A reaches the count of 2 the D input of the PL period flip-flop (part of U11) goes high, so that on the count of 1 the flip-flop changes state, which causes both programmable counters to be reloaded with their respective program numbers and the 40/41 control flip-flop to reset (prescaler in ÷ 41 state). The very next count causes the PL period flip-flop to reset, starting the programmable frequency divider cycle over again. The equation for the divide ratio of the programmable frequency divider N_d is:

$$N_d = 40\,(N_{\text{counter A}}) + N_{\text{counter B}}$$

with the condition that:

$$N_{\text{counter B}} \text{ must not exceed } N_{\text{counter A}}$$

The weighting of the command bits is:

U9 P_1 – 400MHz	U10 P_1 – 4MHz
U9 P_0 – 200MHz	U10 P_0 – 2MHz
U8 P_3 – 160MHz	U13 P_3 – 1.6MHz
U8 P_2 – 80MHz	U13 P_2 – 0.8MHz
U8 P_1 – 40MHz	U13 P_1 – 0.4MHz
U8 P_0 – 20MHz	U13 P_0 – 0.2MHz
U10 P_3 – 16MHz	U13 P_1 – 100KHz
U10 P_2 – 8 MHz	U13 P_0 – 50KHz

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A108 CONVERTER CONTROL

2020200-02 - S

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A108	CONVERTER CONTROL ASSY	2020200-02	1	EIP	34257
C1	Disc, .005μF, 20%, 100V	2150008	1	TG-D50	56289
C2	Disc, .01μF, 20%, 100V	2150003	14	TG-S10	56289
C3	Disc, Cer, X7R, 0.047μF	2150090	1	5022EM50RD473K	24546
C4	Tant, 1μF, 10%, 35V	2300008	3	TAPA 1.0M35	14433
C5	C4				
C6	C2				
C7	Disc, .001μF, 20%, 1KV	2150001	4	5GA-D10	56289
C8	C4				
C9	Tant, 33μF, 10%, 10V	2300015	2	TAPA 33M10	14433
C10 thru C12	C7				
C13 thru C17	C2				
C18	Tant, 10pF, 20%, 25V	2300029	4	DF106M25S	72136
C19	C18				
C20	C9				
C21	C18				
C22 thru C24	C2				
C25	Disc, Cer, 560 pF, 5%, 100V	2150029	2	SR211A561JAA	14158
C26	Tant, .47μF, 20%, 35V	2300005	1	TAPA-47M35	14433
C27	Cer, 0.022μF, 15%, 50V	2350027	1	6123X7RF73KA50K	13011
C28	C18				
C29	C2				
C30	Disc, Cer, 330 pF, 10%, 100V	2150030	1	SR211A331KAA	14158
C31	Tant, 2.2μF, 50%, 16V	2300012	1	TAPA 2-2M16	14433
C32	Mica, 82pF, 5%, 500V	2260032	2	CD10ED820J03	72136
C33	C2				
C34	Mica, 470pF, NOM, SAT	2259999	1		
C35	Mica 470 pF, 500V, 5%	2250018	1	DM-15-471J	72136
C36	Mica, S.A.T.	2269999	1	30pF, NOM.	
C37	Mono, .1μF, 10%, 50V	2150028	1	RC50104KB	51406
C38	C2				
C39	Mono, 2200pF, 5%, 100V	2150026	1	SR211A222JAA	14158
C40	C25				
C41	C2				
C42	C32				
					07263
CR1	Hot Carrier	2710004-00	1	5082-2835	28480
CR2	Zener, 56V	2704758-00	1	IN4758	07263
CR3	Fast Sw	2704148	14	IN4148	07263
CR4	Zener, 6.2V	2700827	1	IN827	07263
CR5	Power Rectifier	2704001	1	IN4001	07263
CR6 thru CR18	CR3				
L1	Inductor, 100μH	3520007	1	1537-76	99800
L2	Inductor, 1μH	3510018	1	1537-12	99800
L3	Inductor, 4700μH	3510017	2	1641-475	99800
L4	L3				
Q1	PNP	4710009	1	MJE350	04713
Q2	PNP RF Amplifier	4710018	1	MPSL51	04713
Q3	NPN General Purpose	4704124	1	2N4124	04713

A108 CONVERTER CONTROL

2020200-02 -

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1	Prec., 8.45K, 1%	4120019	1	VAR-1/10C-6-1%	ACI
R2	Comp, 4.7K, 5%, 1/4W	4010472	1	RC07GF472J	81349
R3	Comp, 1K, 5%, 1/4W	4010102	6	RC07GF102T	81349
R4	Met Film, 49.9K, 1%, 1/10W	4054992	1	RN55C4992F	81349
R5	Met Ox, 390 ohm, 2%, 1/4W	4130391	2	C4/2%/390	24546
R6	Pot, WW	4280011	2	89PR-20K	73138
R7	Comp, 5.1M, 5%, 1/4W	4010515	1	RC07GF515J	81349
R8	R3				
R9	Met Ox, 10K, 2%, 1/4W	4130103	2	C4/2%/10K	24546
R10	R6				
R11	R9				
R12	Met Film, 1M, 1%, 1/10W	4051004	1	RN55C1004F	81349
R13	R5				
R14	Comp, 750, 5% 1/4W	4010751	1	RC07GF751J	81349
R15	Comp, 820K, 5%, 1/4W	4010824	1	RC07GF824J	81349
R16	R3				
R17	Met Ox, 1.6K, 2%, 1/4W	4130162	1	C4/2%/1.6K	24546
R18	Comp, 1.60K, 5%, 1/4W	4010164	1	RC07GF164J	81349
R19	Prec, 3.01K, 1%,1/10W	4120020	1	VAR-1/10C-6-1%	ACI
R20	Comp, 10K, 5%, 1/4W	4010103	3	RC07GF103J	81349
R21	Comp, 82K, 5%, 1/4W	4010823	1	RC07GF823J	81349
R22	R20				
R23	R20				
R24	R3				
R25	Wire Wound 5, 1%, 7W	4110003	1	T7 (10 PPM)	12463
R26	Comp, 2.7K, 5%, 1/4W	4010272	1	RC07GF272J	81349
R27	Comp, 51, 5%, 1/4 W	4010510	2	RC07GF510J	81349
R28	Comp, 390, 5%, 1/4W	4010391	3	RC07GF391J	81349
R29	R28				
R30	R28				
R31	R3				
R32	Comp; 100, 5%, 1/4W	4010101	3	RC07GF101J	81349
R33	R3				
R34	Comp, 2.4K, 5%, 1/4W	4010242	1	RC07GF242J	81349
R35	R32				
R36	Comp, 220K, 5%, 1/4W	4010224	1	RC07GF224J	81349
R37	R32				
R38	Comp, 4.3K, 5%, 1/4W, NOM S.A.T.	4010999	1		
R39	Comp, 2K, 5%, 1/4W	4010202	1	RC07GF202J	81349
R40	R27				
R41	Comp, 1.5M, 5%, 1/4W	4010155	1	RC07GF155J	81349
R42	Comp, 300, 5%, 1/4W	4010301	1	RC07GF301J	81349
R43	Comp, 8.2K, 5%, 1/4W	4010822	1	RC07GF822J	81349
R44	Comp, 51K, 5%, 1/4W	4010513	2	RC07GF513J	81349
R45	Comp, 5.1K, 5%, 1/4W	4010512	1	RC07GF512J	81349
R46	R44				
R47	Comp, 3.3K, 5%, 1/4W	4010332	1	RC07GF332J	
U1	Prec, J-FET Op Amp	3041016	1	OP16FJ	06665
U2	12 Bit DAC	3050012	1	HS7541-1	0000X
U3	Op Amp, Lin.	3040741	1	LM741CN	27014
U4	Peripheral Interface Adaptor	3086820	2	MC6820P	04713
U5	Two-Mod Prescaler	3112013-02	1	MC12013L	04713
U6	10K, M - S Flip-Flop	3110131	1	MC10131L	04713
U7	U4				
U8 thru U10	UP/DOWN Counter	3084192	4	DM74LS192N	27014

A108 CONVERTER CONTROL

2020200-02 - S

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
U11	Counter Control Logic	3112014	1	MC12014P	04713
U12	UP/DOWN Counter	3084193	1	DM74LS193N	27014
U13	U8				
U14	Phase Frequency Detector	3014044	1	MC4044 L	04713
U15	Quad Dual Flip-flop	3084175	1	SN74LS175	01295
U16	Decade Counter	3084490	1	SN74LS490N	01295
U17	J-FET Op Amp	3040071	2	TL071CP	01295
U18	Quad 2 INP NAND	3087400	1	DM74LS00	27014
U19	U17				

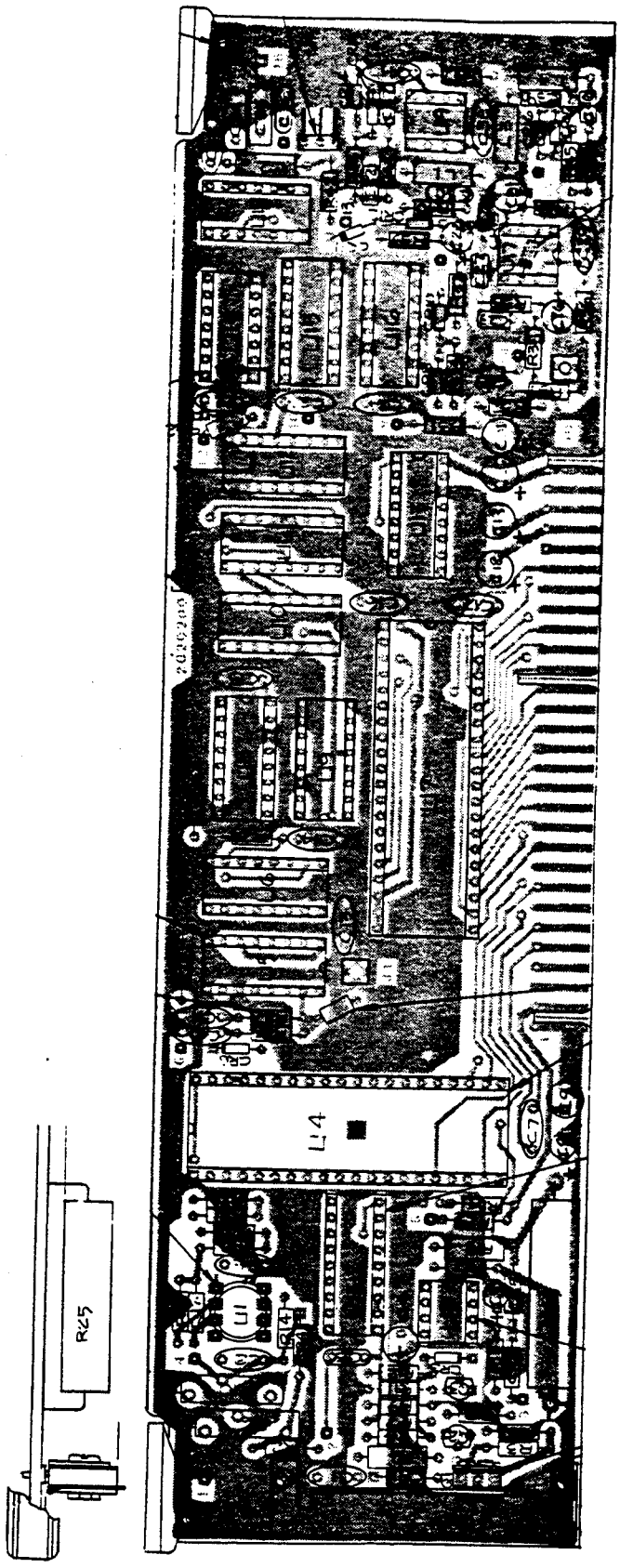

Figure 108-3. Converter Control Component Locator

A109
BAND 2 CONVERTER
(2020139)

The Band 2 Converter accepts Band 1 and Band 2 RF signals from the front panel, and local oscillator (LO) signal from the Band 3 Converter (A203). The appropriate signal is selected and processed to produce an IF signal between 10 Hz and 200 MHz. The IF signal output is sent to the Count Chain board (A106), and lock information is routed through the PIA (peripheral interface adapter) U2 to the Microprocessor (A105).

IMPEDANCE CONVERTER

Band 1 input from the front panel enters the converter at J6 and is terminated by R75. The signal is coupled to the input of a field effect transistor (FET) amplifier (Q15) through an RC network (R73, C42). Two limiter diodes (CR4, CR5) protect the FET against large input signals. The FET is a source follower with slightly less than unity gain. The FET drives a buffer amplifier (Q14) which has enough gain to increase the impedance converter overall gain to near unity. A decoupling capacitor (C39) controls the amplifiers low frequency cutoff, and C41 provides high frequency peaking to keep the gain flat to frequencies above 100 MHz.

SIGNAL SELECT

The output of the impedance converter circuit drives one input of the signal select circuitry. Signal selection is made by enabling one of three differential amplifiers, U4A, U4B, or U5A. When Band 1 is selected, a logic high signal on the PIA (U2 pin 2) turns on Q16. Q16 biases on the current source in U4A. This current source generates an 11mA current which is split between the two differential amplifier transistors in U4A. The currents from pins 5 and 6 flow through matched collector loads (R94, L7/R95, L8). R94 and R95 are equal, and are selected for the proper low frequency gain during board alignment. Inductors L7 and L8 provide peaking to give an approximate flat gain through 200MHz. Diodes CR9 and CR10 provide limiting on very strong signals to prevent the next stage from being over driven.

The next stage is a differential amplifier similar to U4A, but it is driven differentially. To generate a single ended output signal, one output of U5B (pin 12) is passed through a current mirror (Q18). The output of the current mirror is then added to the second output of U5B (pin 11) at J5. The load for this stage is a 51 ohm resistor located on the A106 Count Chain board in order to terminate the coax for RF signals. In the quiescent state, the current from Q18 equals the collector current of the differential amplifier U5B, and the output current is zero. When a signal is applied, the current will be unbalanced to generate a signal at the load resistor. To provide frequency compensation of the current mirror, an RC network (R108, C34) is connected between the emitter of Q18 and ground.

BAND 1 LOCK DETECTOR

The output signal at J5 is coupled to detector CR12. Amplifier U6 is a threshold comparator that will produce a logic low signal when the IF output from J5 is more than –6dBm. The output of U6 goes through a resistor divider network to generate a 5V TTL logic signal for the PIA. R90 provides about 1 dB of positive feedback at threshold level to prevent eratic output from the comparator.

ISOLATION AMPLIFIER

The Band 2 input signal enters on J4. This RF signal is terminated in 50 ohms by the combination of R1 and the input impedance of the amplifier. The input signal level is detected by CR1, filtered by C3, and applied to one input of the Band 2 lock detector (U1).

The isolation amplifier is a common base amplifier with a gain of −10 dB. An input signal range of +10 to −20dBm is translated to a 0 to −30dBm range into the mixer so the mixer will be in its linear range for all signal input levels. The amplifier peaks slightly near 1 GHz to overcome an increase in mixer conversion loss at these frequencies.

MIXER OPERATION

The local oscillator (LO) is applied to the IF terminal and the IF is removed from the LO terminal. This swap allows the mixer (MX1) to be unbalanced and act as a low loss attenuator for signals between 10MHz and 200MHz where no mixing is necessary. The mixer has a nominal 400MHz LO for signals between 200MHz and 600MHz; and has a nominal 800MHz LO for signals between 600MHz and 1GHz. A 980MHz LO allows operation with input signals to 1160MHz.

IF AMPLIFIER

The output of the mixer drives an IF amplifier through a 7 section, 200MHz low-pass filter. The IF amplifier is a "feedback pair" amplifier whose gain is stabilized by feedback, to be equal to 24dB. Inductor L6 is used to extend the high frequency response to 200MHz. The 1 pF capacitor (C26) between R34 and R35 is a low pass filter to reduce the 1200 to 1500 MHz LO harmonics that reach the IF amplifier.

BAND 2 LOCK DETECTOR

The IF amplifier output goes to the signal select circuit and to the Band 2 Lock Detector. The Band 2 Lock Detector has a voltage proportional to the IF level on the positive input, and a voltage proportional to the RF signal on the Negative input. The conversion gain from RF input to IF amplifier output is a +6dB for all valid signals, and less than −6dB for all spurious signals. The output of U1 is positive only when a valid IF signal is present. A small offset is added by R12 and R13 to guarantee a non lock condition when no signal is present. Resistor R90 provides about 1dB of positive feedback to prevent eratic output from noise at the point of threshold.

LO BUFFER

The VCO signal from the Band 3 Converter (A201A, J2) enters on J1. The signal goes through a 6 dB attenuator (R111, R112, R114), and a low pass filter (L1, C63, C64 to attenuate high order harmonics), and is terminated by a 51 ohm resistor (R16). Two high input impedance signal splitters (Q2, Q3) get their input signals from R16. Q2 and Q3 operate on the same basic principal. One output is taken from the emitter (acting as an emitter follower) which provides unity gain for the input signal. The AC terminating impedance on the emitter is adjusted to be 50 ohms so the amplifier will act as a unity gain amplifier for the 50 ohm load which terminates the collector when a coax cable is connected. U2 has an additional transformer (T1) in its collector lead to increase the signal output to J3 by about 4 dB.

DIVIDE-BY-TWO

The emitter output of Q3 drives the input of a divide-by-two IC (U3). The impedance is held at 50 ohms by two terminating/biasing resistors (R61, R62). The resistors keep the input bias to U3 below the emitter-coupled logic (ECL) low level (approx. −2.0V). The microprocessor enables self-test by putting a low level signal on pin 5 of the PIA (U2). This turns on Q13, and raises the voltage at U3 pin 7 to the center of an ECL signal (approx. −1.2V). This allows U3 to divide the input signal by two. The output of U3 goes to the signal select circuits.

LO SELECT

The signal from the emitter of Q2 drives the LO select circuitry. The LO provides one (of three) signals to the mixer (MX1). In Band 2A a bias current is generated to unbalance the mixer and allow signals below 190MHz to pass. In Band 2B a 370MHz or 425MHz LO signal is generated that will mix with signals of 200 to 600MHz, and provide the 10 to 200MHz IF signal desired. In Band 2C a 750MHz, 850MHz or 980MHz LO signal is generated to mix with input signals between 600MHz and 1160MHz to provide the desired IF signal.

In Band 2A, the 3ma current to bias mixer MX1 is generated when Q12 is turned on by the PIA, to apply +12V to MX1 through R57. This will allow signals to pass that are less than the cutoff frequency of the low pass filter (200MHz). The LO signal to mixer MX2 from Q2 is not allowed to pass MX2 because of the inherent balance of the mixer. No signal can enter pin 2 of MX2 because Q7 has been saturated, removing bias from buffer Q5, and shunting any RF signals to ground.

When Band 2B is selected, Q12 is turned off thus balancing mixer MX1; Q6 is turned on to unbalance mixer MX2. With MX2 unbalanced, the LO signal from Q2 can pass through MX2 and be amplified by Q10 and Q11, and be applied to mixer MX1.

When Band 2C is selected both Q6 and Q12 are off, and both mixers are balanced. In this mode Q7 is shut off and an LO signal is applied to pin 1 and 2 of MX2. The sum output of MX2 is selected by a DC blocking capacitor (C31). This sum (that is two times the incoming LO frequency) is amplified by Q10 and Q11 and applied to MX1.

The Q10 and Q11 amplifier is a series shunt pair. Q10 applies most of the RF input signal across the emitter resistor R47. This determines the transistor emitter current, which will be the collector current if the output is terminated in a low impedance. Q11 is used as a current-to-voltage converter. The output voltage of this converter is the product of the input current times the feedback resistor (R51). Since the input of this stage is a summing junction, it appears very close to zero ohms to the previous stage, Q10. The voltage gain of the two transistors can be approximated by R51/R47, which is about 3 or 10dB. Since the gain required at 800MHz is slightly greater than required at 400MHz, a low pass matching network (consisting of L2 and C20 peaks the output signal current to MX1 at 800 MHz. The remaining components around Q10 and Q11 are used to bias the transistors. Shunt biasing is used to provide collector bias voltages of 3.4V for Q10, and 4.7V for Q11.

OPTION SELECTION

Provision has been made on this assembly for a set of jumpers that will let the microprocessor know when it has the components required for a 548A (26.5 GHz) counter, and if it has an extended frequency option (Option 06). These jumpers are read by the microprocessor when the counter is turned on, and will select micro code which is applicable only when those options are available. A jumper from E1 to E3 (from pins 8 and 9 on the PIA U2) indicate that this is a 548A counter. A jumper from E2 to E4 indicates that Option 06 (Band 4) has been installed.

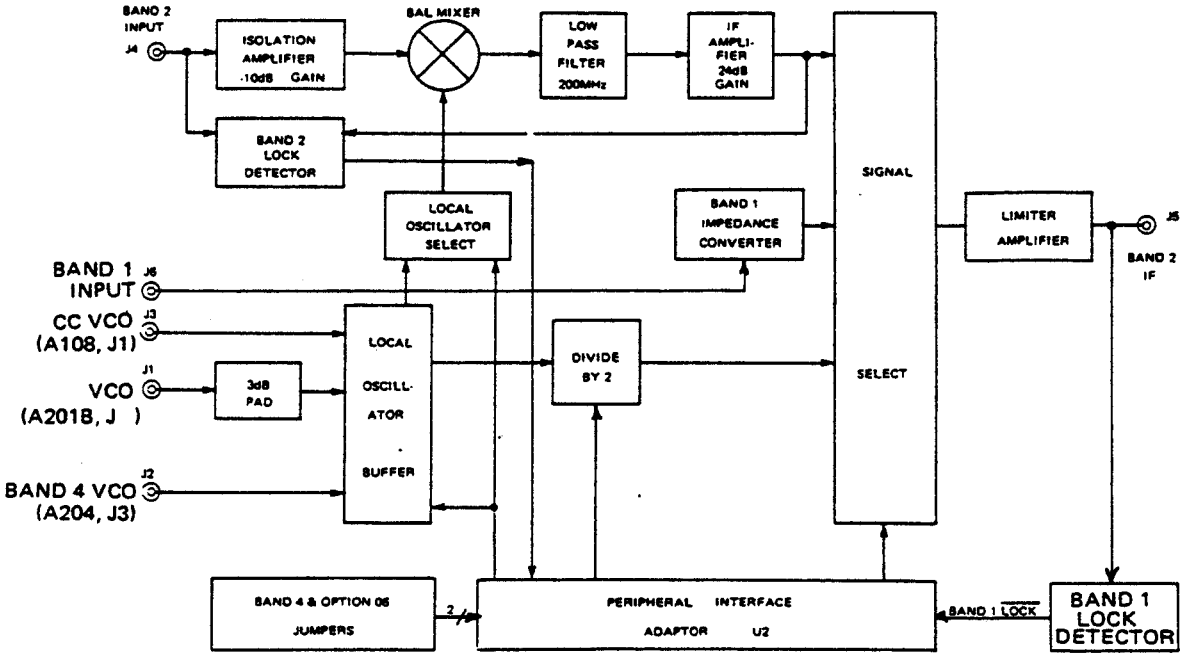

Figure 109-1. Band 2 Converter Block Diagram

A109 BAND 2 CONVERTER

2020139-03 - M

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A109	Band 2 Converter Assy	2020139-03	1	EIP	34257
C1	Cer, .01μF, 10%, 100V	2150014-00	9	6123X7R103KA100	26654
C2	C1				
C3	Cer, .001μF 10%, 100V	2150015	11	6183X7R102KA100	26654
C4 thru C6	C1				
C7	Mica, 100pF, 5%, 500V	2260034	3	FD101J03	72136
C8	Disc, .001μF, 20%, 1KV	2150001	8	SGA - D10	56289
C9	Disc, .01μF, 20%, 100V	2150003	11	TG - S10	56289
C10	C8				
C11	C8				
C12	C7				
C13	C8				
C14	C7				
C15 thru C18	C3				
C19	C8				
C20	Mica, 1pF, 5%, 500V	2260005	2	CD010C03	56289
C21	Mica, 18pF, 5%, 500V, NOM - S.A.T	2260999	1		
C22	Mica, 33pF, 5%, 500V, NOM - S.A.T.	2260999	2		
C23	C22				
C24	Mica, 27pF, 5%, 500V NOM S.A.T.	2260999	1		
C25	C1				
C26	C20				
C27	Not Used				
C28	C1				
C29	C9				
C30	C1				
C31	C3				
C32	C3				
C33	C1				
C34 thru C36	C3				
C37	C9				
C38	C3				
C39	Tant, 100μF, 20%, 6.3V	2300024	1	TAG20 - 47/6.3 - 50	14433
C40	C9				
C41	Mica, 22pF, 5%, 500V	2260017	1	ED220J03	72136
C42	Mica, 47pF, 5%, 6.3V	2260004	1	DM10 - 470J	72136
C43	Tant, 33μF,10%, 10V	2300015	6	TAG20 - 33/10 - 50	14433
C44	C9				
C45	C43				
C46	C8				
C47 thru C49	C9				
C50	Tant, 10μF, 20%, 25V	2300029	3	TAG20 - 10/25	14433
C51	C43				
C52	C9				
C53	C9				
C54	Mica, 18pF, 5%, 500V	2260015	1	CD180J03	56289
C55	C8				
C56	C8				
C57	C50				

A109 BAND 2 CONVERTER, continued

2020139-03 - M

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
C58	C43				
C59	C9				
C60	C43				
C61	C50				
C62	C43				
C63	Mica, 8pF, 13%, 500V	2660011	2	CD080J03	56289
C64	C63				
CR1	Mix UHF	2710038	3	ND4991	00005
CR2	Not Used				
CR3	CR1				
CR4	Fast Switch, GP	2704148	3	IN4148	07263
CR5	CR4				
CR6 thru CR10	Not Used				
CR11	CR4				
CR12	CR1				
L1 thru L5	Part of Board				
L6	Inductor, 0.47 μH	3510006	1	DD - 0.47	99800
L7	L1				
L8	L1				
MX1	Balanced Mixer	2030016	2	TFM-2	
MX2	MX1				
Q1	NPN, RF	4710030	8	BFR-90	04713
Q2	Q1				
Q3	Q1				
Q4	PNP, General Purpose	4704124	1	2N4124	04713
Q5	Q1				
Q6	PPNP, General Purpose	4704126	7	2N4126	04313
Q7	Q1				
Q8	Q1				
Q9	Q1				
Q10	NPN,RF, graded	4710030-02	1	BFR-90	
Q11	Q1				
Q12	Q6				
Q13	Q6				
Q14	NPN, RF	5280047	2	2N4261	01295
Q15	NN-Channel, JFET	4704416	1	2N4416	04713
Q16	Q6				
Q17	Q6				
Q18	Q14				
Q19	Q6				
Q20	Q6				
R1	Comp, 150, 5%, 1/8 W	4000151	1	RC05GF151J	81349
R2	Res, MF, 75.0, 1%, 1/8W	4067509	1	RN55D7509F	24546
R3	Res, 1.1K, 2%, 1/4W	4130112	1	C4/2%/10	24546
R4	Res, 820, 2%, 1/4W	4130820	4	C4/2%/820	24546
R5	Comp, 33, 5%, 1/8 W	4000330	1	RC05GF330J	81349
R6	Comp, 51, 5%, 1/8 W	4000510	1	RC05GF510J	81349
R7	Comp, 10K, 5%, 1/4 W	4010103	3	RC07GF103J	81349
R8	Met Ox, 8.2K, 2%, 1/4 W	4130822	2	C4/2%/8.2K	81349
R9	Met Ox, 30K, 2%, 1/4 W	4130303	1	C4/2%/30K	24546
R10	Met Ox, 43K, 2%, 1/4 W	4130433	2	C4/2%/43K	24546
R11	Comp, 43K, 5%, 1/4 W	4010433	1	RC07GF433J	81349
R12	Res, M/OX, SAT (15 NOM)	4130999	4	C4/2%/15K	24546
R13	Res, MF, 12.1, 1%, 1/8W	4061219	1	RN55D1219F	24546

A109 BAND 2 CONVERTER, continued

2020139-03 - M

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R14	Comp, 36, 5%, 1/4 W	4010360	1	RC07GF360J	81349
R15	Comp, 11, 5%, 1/4 W	4010110	2	RC07GF110J	81349
R16	Res, MF, 51.1, 1%, 1/8W	4065119	2	RN55D51R1F	24546
R17	Comp, 1K, 5%, 1/4 W	4010102	4	RC07GF102J	81349
R18	R4				
R19	R15				
R20	Res, CC, 1/4W, 5%	4010999	1		
R21	Comp, 220, 5%, 1/4 W	4010221	2	RC07GF221J	81349
R22	Comp, 20K, 5%, 1/4 W	4010203	1	RC07GF203J	81349
R23	Res, CC 820, 1/4W, 5%	4010821	2	RC07GF821J	81349
R24	Comp, 10, 5%, 1/8 W	4010100	11	RC07GF100J	81349
R25	Met Ox, 750, 2%, 1/4 W	4130751	2	C4/2%/750	24546
R26	Comp, 11k, 5%, 1/4 W	4010113	3	RC07GF113J	81349
R27	Met Ox, 4.7K, 2%, 1/4 W	4130472	1	C4/2%/4.7K	24546
R28	Res, MF, 33.2, 1%, 1/8W	4063329	2	RN55D3329F	24546
R29	Comp, 4.7K, 5%, 1/4 W	4010472	2	RC07GF472J	81349
R30	R26				
R31	Comp, 8.2K, 5%, 1/4 W	4010822	2	RC07GF822J	81349
R32	R7				
R33	R7				
R34	Res, MF, 27.4, 1%, 1/8W	4062749	1	RN55D2749F	24546
R35	Res, MF, 24.3, 1%, 1/8W	4062439	1	RN55D24R3F	24546
R36	R24				
R37	Comp, 10, 5%, 1/8 W	4000100	1	RC05F100J	81349
R38	R17				
R39	R4				
R40	R4				
R41	R24				
R42	R16				
R43	R24				
R44	Comp, 910, 5%, 1/4 W	4010911	1	RC07GF911J	81349
R45	Comp, 3.9K, 5%, 1/4 W	4010392	3	RC07GF392J	81349
R46	Comp, 27K, 5%, 1/4 W	4010273	1	RC07GF273J	81349
R47	R28				
R48	Comp, 3.3K, 5%, 1/4 W	4010332	1	RC07GF332J	81349
R49	Comp, 390, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R50	Comp, 13K, 5%, 1/4 W	4010133	1	RC07GF133J	81349
R51	Res, MF, 121, 1%, 1/8W	4061210	1	RN55D1210F	24546
R52	R24				
R53	R31				
R54	R26				
R55	R25				
R56	R24				
R57	R12 (4.3K NOM)	4130999	1	C4/2%/4.3K	
R58	R17				
R59	R45				
R60	R12 (300 or 560 NOM)				
R61	Res, MF, 82.5, 1%, 1/8W	4068259	1	RN55D82R5F	24546
R62	Res, MF, 130.0,1%, 1/8W	4061300	2	RN55D1300F	24546
R63	Comp, 510, 5%, 1/4 W	4010511	1	RC07GF511J	81349
R64	Comp, 51, 5%, 1/4 W	4010510	2	RC07GF510J	81349
R65	Comp, 200, 5%, 1/4 W	4010201	1	RC07GF201J	81349
R66	Comp, 160K, 5%, 1/4 W	4010164	1	RC07GF164J	81349
R67	Met Ox, 1.8K, 2%, 1/8 W	4130182	1	C4/2%/1.8K	24546
R68	R24				
R69	Met Ox, 510, 2%, 1/4 W	4130511	2	C4/2%/510	24546
R70	R12 (1.2K NOM)	4130999	1	C4/2%/1.2K	24546
R71	R29				
R72	R24				

A109 BAND 2 CONVERTER, continued

2020139-03 - M

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R73	Comp, 1M, 5%, 1/4 W	4010105	2	RC07GF105J	81349
R74	R64				
R75	R73				
R76	Met Ox, 2.2K, 2%, 1/4 W	4130222	3	C4/2%/2.2K	24546
R77	Met Ox, 3.9K, 2% , 1/4W	4130392	3	C4/2%/3.9K	24546
R78	Comp, 5.6K, 5%, 1/4 W	4010562	1	RC07GF562J	81349
R79	Comp, 3.6K, 5%, 1/4 W	4010362	3	RC07GF362J	81349
R80	Met Ox, 7.5K, 2%, 1/4 W	4130752	3	C4/2%/7.5K	24546
R81	R76				
R82	R24				
R83	Met Ox, 200, 2%, 1/4 W	4130201	3	C4/2%/200	24546
R84	R77				
R85	Met Ox, 330, 2%, 1/4 W	4130331	1	C4/2%/330	24546
R86	Comp, 6.8K, 5%, 1/4 W	4010682	2	RC07GF682J	81349
R87	R79				
R88	R80				
R89	R8				
R90	Comp, 75K, 5%, 1/4 W	4010753	1	RC07GF753J	81349
R91	Met Ox, 33K, 2%, 1/4 W	4130333	1	C4/2%/33K	24546
R92	Met Ox, 160, 2%, 1/4 W	4130161	1	C4/2%/161	24546
R93	R21				
R94	Res, MF, SAT., 1/8W, 1% (12.1 NOM)	4069999	2	C4/2%/12	24547
R95	R94				
R96	R83				
R97	R83				
R98	R57				
R99	R86				
R100	R79				
R101	R80				
R102	R10				
R103	R76				
R104	Comp, 180, 5%, 1/4 W	4010181	1	RC07GF181J	81349
R105	R24				
R106	Res, MF, 90.9, 1%, 1/8W	4069099	1	RN55D9099F	24546
R107	R62				
R108	R24				
R109	R69				
R110	R17				
R111	Comp, 160, 5%, 1/4 W	4010161	2	RC07GF161J	81349
R112	R111				
R113	Res, MF, 20.0, 1%, 1/8W	4062009	1	RN55D2009F	24546
R114	Met Ox, 2K, 2%, 1/4 W	4130202	2	C4/2%/2K	24546
R115	R114				
R116	Met Ox, 9.1K, 2%, 1/4 W	4130912	2	C4/2%/9.1K	24546
R117	R116				
R118	Comp, 300K 5%, 1/4 W	4010301	1	RC07GF301J	81349
R119	R45				
R120	R23				
R121	Comp, 68, 5%, 1/4 W	4010680	1	RC07GF560J	81349
R122	Comp, 100K, 5%, 1/4 W	4010101	1	RC07GF100J	81349

A109 BAND 2 CONVERTER, continued

2020139-03 - M

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
TP1 thru TP16	Conn, Pin, .040D	2620032	16	460 - 2970 - 02 - 03	71279
U1	Prec, JFET Op Amplifier	3041016	1	OP16FJ	06665
U2	Periph. Interface Adaptor	3086820	1	MC6820	04713
U3	750 MHz, D-Type Flip Flop	3001106	1	MC1690L	07263
U4	Dual/Diff. Amplifier	3043049	2	CA3049	27014
U5	U4				
U6	Op Amplifier	3040741	1	UA741CP	27014

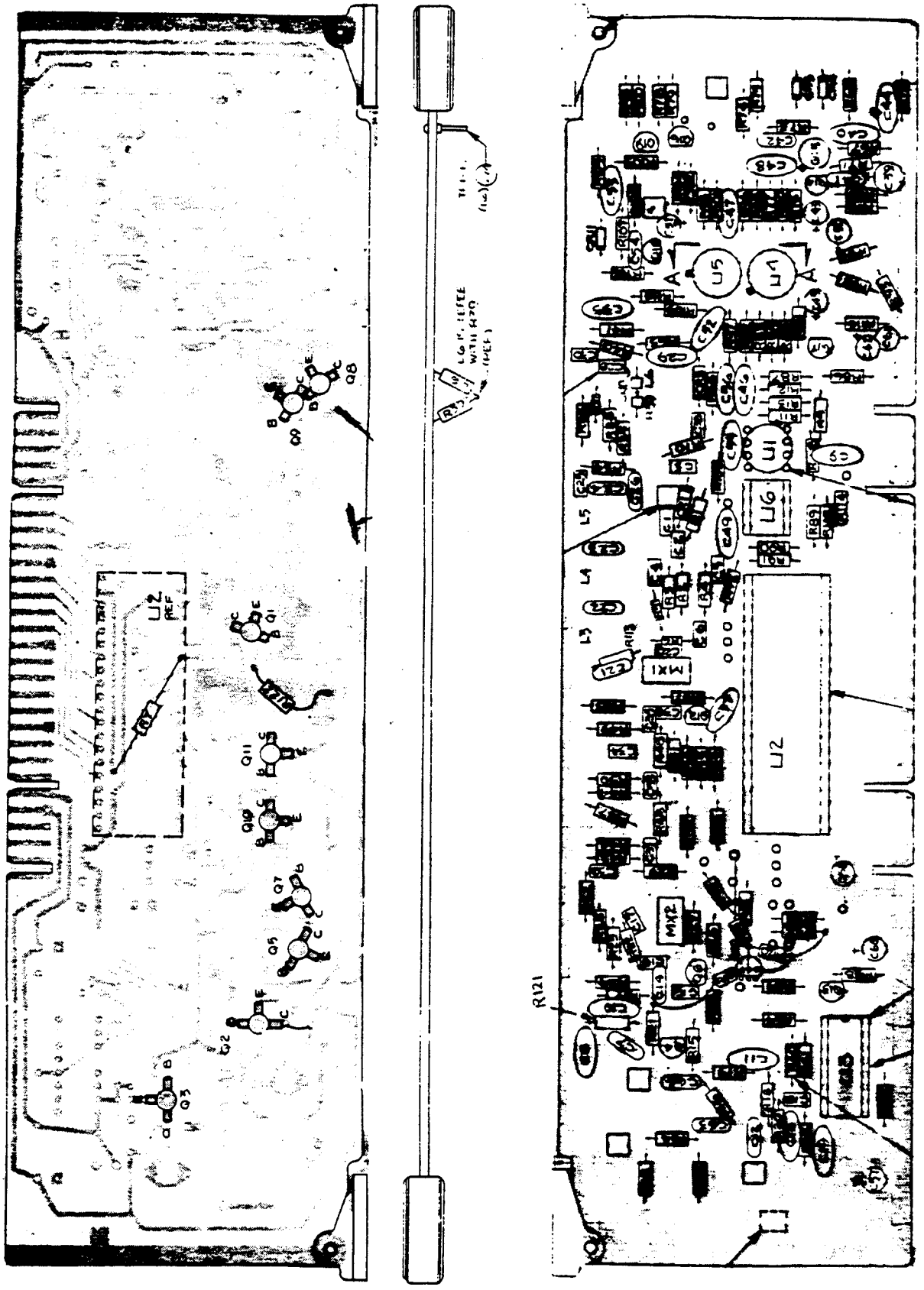

Figure 109 b. Band 2 Converter Component Locator

A110
FRONT PANEL
DISPLAY AND KEYBOARD
(2020140)

The Front Panel Display and Keyboard assembly (A110) is divided into two functional sections.

- Numeric display and annunciators
- Keyboard

NUMERIC DISPLAY AND ANNUNCIATORS

This section of the assembly contains 12 common anode seven-segment numeric display units (DS1-DS12), two green LEDs (DS37 and DS38), and a maximum of 24 yellow LEDs (DS13-DS36).

The 12 seven-segment LEDs are mounted side by side, with space between each third digit from the right. The corresponding cathode segments of the seven-segment LEDs are connected, and the drive signal come from segment drivers Q3 through Q10. The signals to drive the digits come from the digit drivers located on the Front Panel Logic board (A111).

The 24 yellow LEDs (DS13-DS36) are divided into three groups of eight LEDs each. The anodes of all LEDs in each group are connected. The cathode of each LED in a group is connected to one of the segments drivers (Q3-Q10). With this arrangement each group of annunciator lights can be regarded as similar to one seven-segment LED. The digit drives for the three groups of annunciator lights also come from the Front Panel Logic board (A111).

The two green LEDs (DS37 and DS38) are driven by Q1 and Q2. When these LEDs light, they indicate that GATE and CONVERTER SEARCH are in operation.

KEYBOARD

This section of the assembly makes provision for a maximum of 25 (single-pole double-throw) switches, of which only 21 are used. The switches are arranged in a 4 row by 6 column matrix, with the extra switch taking the row 4 column 7 position. The columns are connected to +5V through the resistor network (RN1) on the Front Panel Logic board (A111).

The keyboard is continuously scanned. The signals scanning the keyboard are derived from A111. To scan the keyboard the 4 rows are grounded sequentially. When a row is grounded, and a key in that row is pushed, one of the columns will be grounded. This information is sent to the A111 board where key debouncing is performed.

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A110 FRONT PANEL DISPLAY AND KEYBOARD

2020140-02-B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A110	Front Panel Display & Keyboard	2020140-01	1	EIP	34257
Q1 thru Q10	PNP, Amp.	4710019	10	MPS - D55	04713
R1	Comp, 4.7K, 5%, 1/4 W	4010472	2	RC07GF472J	81349
R2	Comp, 130, 5%, 1/4 W	4010131	2	RC07GF131J	81349
R3	R1				
R4	R2				
R5	Comp, 240, 5%, 1/4 W	4010241	8	RC07GF241J	81349
R6	Comp, 18, 5%, 1/4 W	4010180	8	RC07GF180J	81349
R7	R5				
R8	R6				
R9	R5				
R10	R6				
R11	R5				
R12	R6				
R13	R5				
R14	R6				
R15	R5				
R16	R6				
R17	R5				
R18	R6				
R19	R5				
R20	R6				
DS1 thru DS12	LED, Numeric, Indicator	2800024	12	TIL - 312	28480
DS13 thru DS36	LED, Lamp, Yel 0.15 x 0.25	2800020	24	MV53124	50522
DS37	LED, Lamp, Grn ,. 12 OD	2080018	2	MV5274	50522
DS38	DS37				
S1	Switch, Mon, SPDT	4500013	21	REK71882	14433
S2 thru S5	Not Used				
S6 thru S25	S1	4500013	21	REK	
P1	9 pin Recept.	2620065	1	22 - 14 - 209	0000A
P2	17 pin Recept.	2620067	1	22 - 14 - 2171	0000A
P3	13 pin Recept.	2620066	1	22 - 14 - 212	0000A

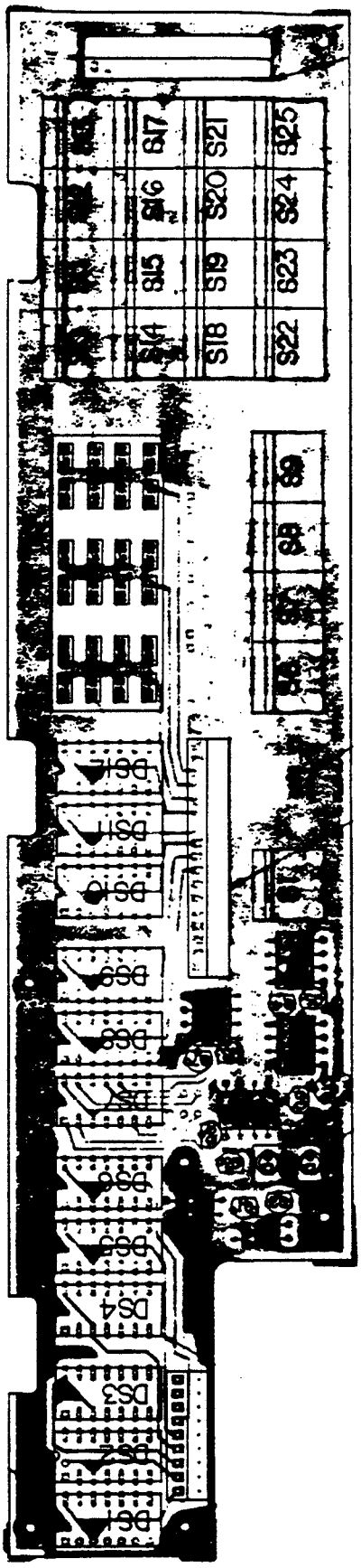


Figure 110-1. Front Panel Display and Keyboard Component Locator

A111
FRONT PANEL LOGIC
(2020191)

The Front Panel Logic assembly (A111) contains logic circuitry for control of two functions.

- DISPLAY CONTROL
- KEYBOARD CONTROL

The +5 V power supply to the front panel assemblies (A110 and A111) is regulated by a voltage regulator that is located behind the A111 board. For heatsinking purposes, this voltage regualtor is mounted on the chassis. Please refer to figure 111b. Front Panel Logic block diagram on page 111-3.

DISPLAY CONTROL

The twelve 7-segment LEDs and the three groups of annunciator lights on A110 are multiplexed. To turn on a particular segment in a digit, both the digit driver for that digit and the segment driver for that segment must be on.

The display logic is in constant operation in either the self-scan mode or the memory update mode.

SELF-SCAN MODE

This is the normal operating mode. In this mode the display scan clock is clocking the display counter (U6). The state of the display counter determines which digit will be turned on.

The state of the display counter is decoded by 4 to 16 line multiplexer (U2), and the appropriate digit driver is turned on. At this time the display memory (U7 and U8) is read, and the on/off information (stored in the display memory for that specific digit), turns the segment drivers (A110) on or off.

The display intensity is controlled by varying the duty cycle of the multiplexing. This is done by varying the resistance of the potentiometer (R4) which, in turn, varies the length of time the decoder (U2) and the display memories (U7, U8) are disabled between each scan clock cycle.

At the start of each gate operation the GATE light control is triggered, and the GATE LED lights for the length of the GATE.

MEMORY UPDATE MODE

In this mode the multiplexer logic is disabled by setting the display scan/$\overline{\text{update}}$ control line (PA4) to logic 0. The microprocessor controlled clock ($\overline{\text{clock}}$, PA1) is used to clock the display counter(U6).

Before updating the display memory (U7 and U8), the display counter is cleared by setting the clear/load control line (PA5) to logic 1, and clocking the clock input of U6. Update mode timing is illustrated in figure 111a.

KEYBOARD CONTROL

When the keyboard is not being read by the microprocessor, the Keyboard READ/$\overline{\text{SCAN}}$ control line (PA0) is at logic 0. All the outputs of the shift register are at logic 0. If no key on the keyboard is pushed, all the inputs to the 8-input NAND gate (U13) are at logic 1 level. When a key is pushed, the column containing that key will be grounded. The output of U13 goes to logic 1 and C7 (in the debounce circuit) starts to discharge. When the voltage across C7 reaches approximately +0.7 V above ground, the debounce circuit will trigger the interrupt input on the PIA (U11, pin 18) indicating that a key is being pushed.

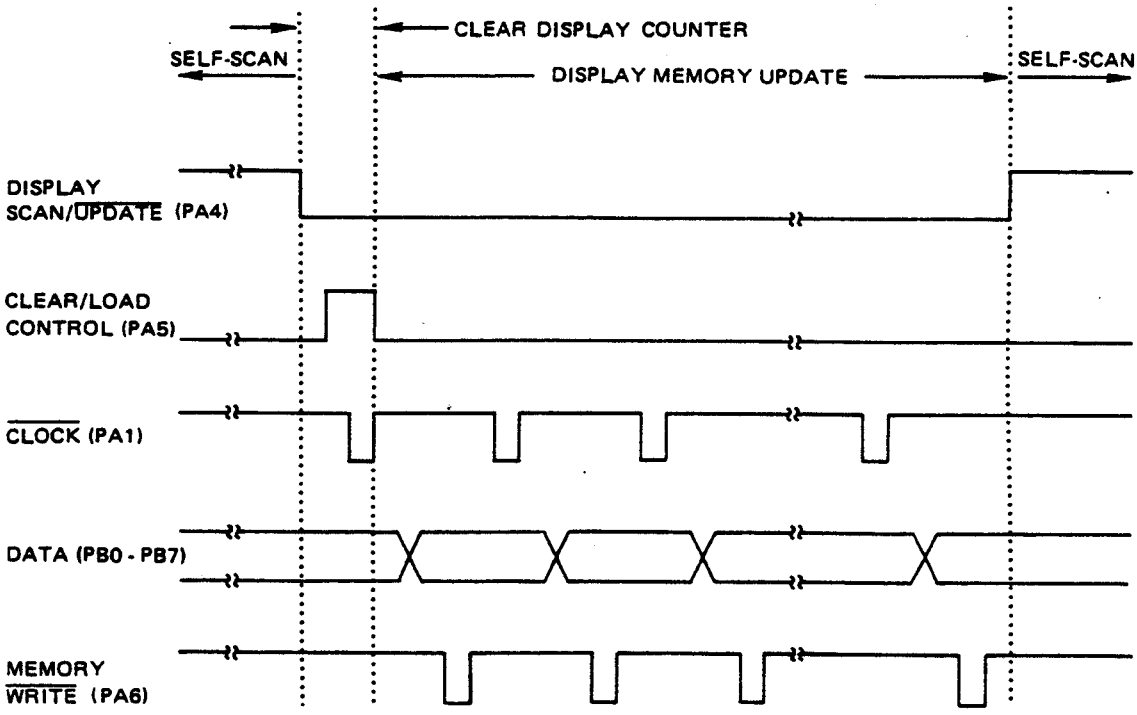


Figure 111-1. Memory Update Mode Sequence

READ KEYBOARD

When the microprocessor needs to read the keyboard, a logic 1 is put on the keyboard READ/$\overline{\text{SCAN}}$ control line (PA0). This enables the data buffer (U9). A 0111 is then loaded into the shift register (U3) by putting a logic 1 on the CLEAR/LOAD control line (PA5) and clocking the clock input of U3. The logic 0 at the output of the shift register (U3) is shifted through the shift register once. The microprocessor reads the keyboard row and column information with the logic 0 at each of the 4 outputs of U3 to determine the coordinate of the key pushed. After the keyboard is read, the keyboard READ/$\overline{\text{SCAN}}$ line is returned to logic 0.

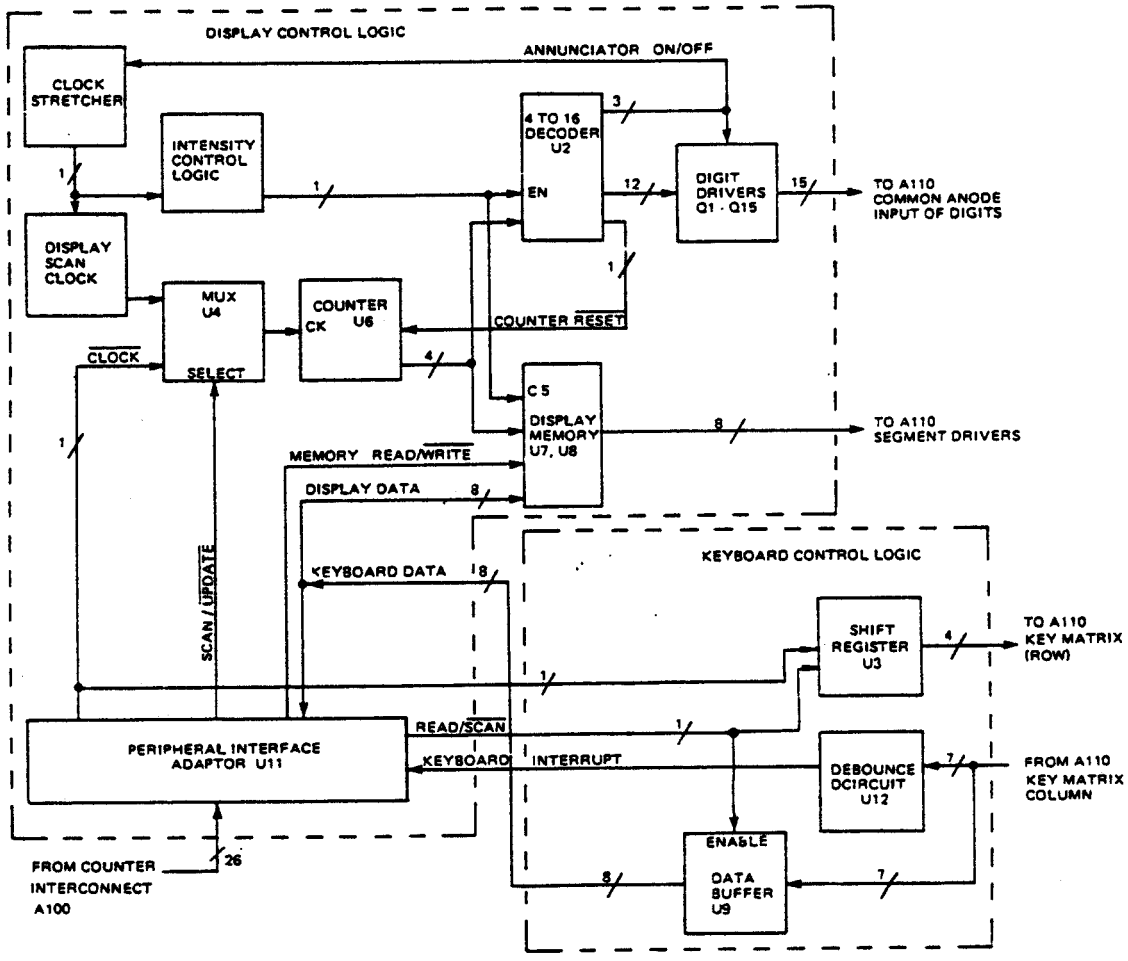


Figure 111-2. Front Panel Logic Block Diagram

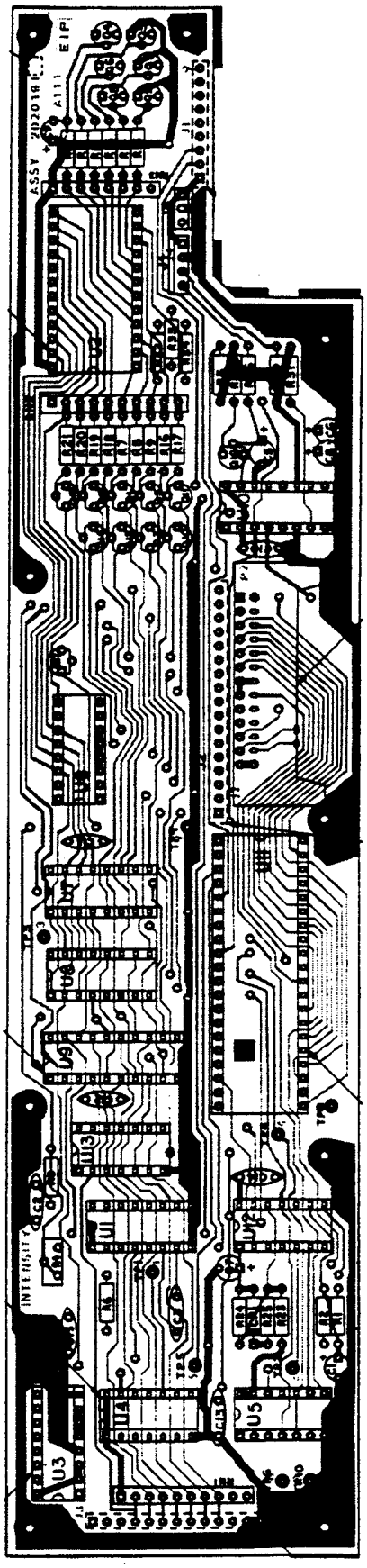
A111 FRONT PANEL DRIVER

2020191 - G

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A111	Front Panel Driver Assy	2020191	1	EIP	34257
C1	Tant, 0.1μF, 10%, 35V	2300020	1	TAPA .10M35	14433
C2	Cer., .002μF, 20%, 1KV	2150005	2	TG - S20	56289
C3	C2				
C4	Not Used				
C5	Tant, 47μF, 20%, 16V	2300025	1	TAPA 47M16	14433
C6	Tant, 2.2μF, 20%, 16V	2300012	1	TAPA 2.2M16	14433
C7	Tant, 22μF, 20%, 16V	2300030	1	TAPA 22M16	14433
C8	Tant, .33μF, 20%, 35V	2310031	1	TAPA .33M16	14433
C9	Tant, 33μF, 20%, 10V	2300015	1	TAPA 33M16	14433
C10 thru C15	Cer., .01μF, 20%, 100V	2150003	6	TG - S10	56289
CR1	General Purpose	2704148	1	IN4148	07263
J1	9 Pin Male	2620062	1	22 - 03 - 2091	0000B
J2	17 Pin Male	2620064	1	22 - 03 - 2171	0000B
J3	13 Pin Male	2620063	1	22 - 03 - 2131	0000B
J4	4 Pin, FR. LOCK	2620068	1	640456-4	74868
J5	3 Pin	2620121	1	640456-3	74868
P2	26 Pin, Right Angle	2620131	1	3493 - 1002	76381
Q1 thru Q15	PNP, Power , Darlington	4710027	15	MPS - D54	04713
Q16	NPN, General Purpose	4704124	2	2N4124	04713
Q17	Q16				
R1	Comp, 10K, 5%, 1/4W	4010103	2	RC07GF103J	81349
R2	Comp, 220, 5%, 1/4W	4010221	1	RC07GF221J	81349
R3	Comp, 75K, 5%, 1/4W	4010753	1	RC07GF753J	81349
R4	Variable, Cer., 200K, KT05, 0.5W	4250022	1	72XR200	73138
R5	Comp, 120K, 5%, 1/4W	4010124	1	RC07GF124J	81349
R6	Comp, 2.4K, 5%, 1/4W	4010242	1	RC07GF242J	81349
R7 thru R21	Comp, 1K, 5%, 1/4W	4010102	15	RC07GF102J	81349
R22	Not Used				
R23	Comp, 15K, 5%, 1/4W	4010153	1	RC07GF153J	81349
R24	Comp, 390, 5%, 1/4W	4010391	1	RC07GF391J	81349
R25	Comp, 200, 5%, 1/4W	4010201	1	RC07GF201J	81349
R26	Comp, S.A.T., 1K, NOM , 1/4W, 5%	4010999	1		
R27	R1				
R28	Not Used				
R29	Comp, 2.2K, 5%, 1/4W	4010222	1	RC07GF222J	81349
R30	Not Used				
R31	Comp, 27K, 5%, 1/4W	4010273	1	RC07GF273J	81349
R32 thru R34	Comp, 39K, 5%, 1/4W	4010393	3	RC07GF393J	81349
RN1	Network, 9 x 10K, 0.2W, 2%	4170003	2	785-1-R10K	32997
RN2	RN1				
RN3	Network, 7 x 10K, 0.3W, 2%	4170004	1	784-1-R10K	32997

A111 FRONT PANEL DRIVER continued

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
TP1 thru TP6	.040D Pin , Gold	2620032	9	460-2970-02-03	71279
TP7	Not Used				
TP8 thru TP10	TP1				
U1	TTL, Monostable, MV	3084123	2	DM74LS123N	0000X
U2	4-16 Line Decoder	3074154	1	DM74154N	0000X
U3	4 Bit Shift Register	3084195	1	DM74LS195N	0000X
U4	AND - OR - INVERT Gates	3087451	1	SN74LS51N	01295
U5	Quad, 2 INP NAND Gate	3084132	1	DM74LS132N	0000X
U6	Binary Sync Clear	3084163	1	SN74LS163	01295
U7	Bipolar RAMS	3057489	2	DM74LS189	0000X
U8	U7				
U9	Oct Bus Trans	3084244	1	SN74LS244N	01295
U10	U1				
U11	Periph, Interface Adaptor	3086820	1	MC6820	04713
U12	Hex Inverter	3087414	1	SN74LS14N	01295
U13	8INP NAND Gates	3087430	1	DM74LS30N	0000X
U14	Pos. Voltage Regulator (reference only - U14 part of front panel power supply)	3057805	1	MC7805CT	04713



2020191 - G

Figure 111c. Front Panel Component Locator

A201A
VOLTAGE CONTROL OSCILLATOR
(2020199)

The VCO assembly contains three functional subassemblies as shown in Figure 201A-1. The VCO consists of transistor oscillator Q1-2 (whose frequency is determined by inductor L13), variable capacitor C2, and varactor CR2. The capacitance of CR2 is determined by the applied tuning voltage at J3. The oscillator is buffered by Q3 and the output is split two ways using T1.

The second subassembly is a single-stage common emitter amplifier that is broadly tuned and loaded with 50 ohm. The output level is approximately +9 to +12 dBm over the range of 370 to 500 MHz. This output is the VCO reference.

The third subassembly is a three-stage power amplifier consisting of a common emitter amplifier (Q5) and two class C stages (Q6 and Q5). This amplifier provides approximately 20 dB of gain and 0.8 watts output over the tuning range of 400 to 500 MHz. The variable capacitor C24 and C25 are adjusted to optimize output power and flatness. Output power is switched on or off by applying bias to Q5 and Q9, which are controlled by Q8. On-to-off power ratio exceeds 50 dB.

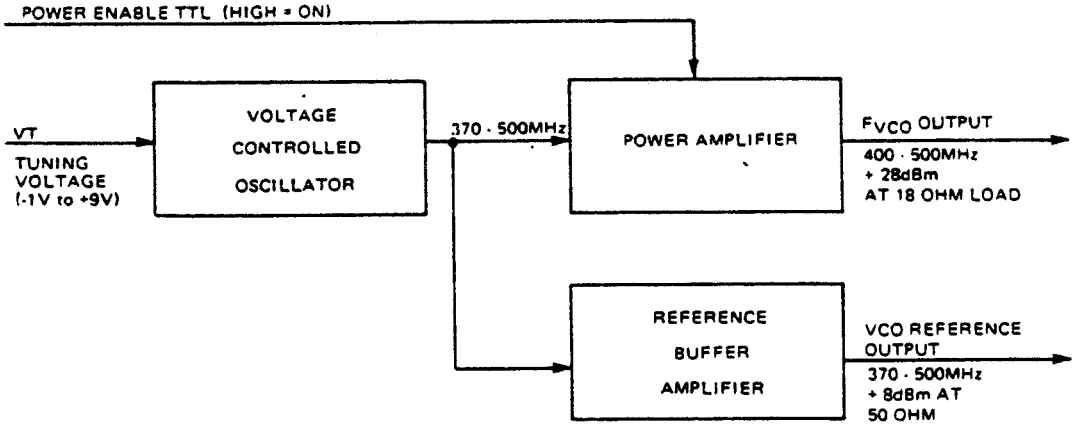


Figure 201A-1. VCO Block Diagram

A201A VOLTAGE CONTROL OSCILLATOR

2020199-00 H

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A201A	VCO Assembly	2020199	1	EIP	
	P/O Band 3 Converter Assy (A203)	2010241	REF		
C1	Cer., .001 μF, 10%, 100V	2150015	12	6183X7R102KA100	80031
C2	Cer, 3-15 pF, 25V	2350036	5	DVS3A15A	JFD
C3	Cer., .01 μF, 10%, 25V	2150014	2	6123X7R103KA100	80031
C4	Chip, 6.2 pF, 8%, 50V	2100021	2	100A6R2D50XC	29990
C5	Tant, 10 μF, 20%, 25V	2300029	2	DF106M25S	72136
C6	Cer., 33pF, 10%, 100V	2150069	1	6113X7R470KA100	80031
C7	C1				
C8	C5				
C9	C4				
C10	Cer, 1.5-6 pF, 25V	2350035	1	DVS3A6A	JFD
C11	Disc, NPO, 56pF, 5%, 100V	2150072-00	2	100-100- X7R-560J	51642
C12	C1				
C13	Cer, 47 pF, 10%, 100V	2150039-00	1	5018EM100RD470K	29938
C14	C2				
C15	C2				
C16 thru C18	C1				
C19	C11				
C20 thru C22	C1				
C23	Chip, 15 pF, 5%, 50V	2100022	1	100A150J50XC	29990
C24	C2				
C25	C2				
C26	C1				
C27	C3				
C28	Cer., 15 pF, 10%, 100V	2150033	1	6113X7R150KA100	80031
C29	Not Used				
C30	C1				
C31	Not Used				
C32	Disc, Cer , 4.7 pF, 10%, 100V	2150086	1	6113COG479DA1000480LG	13011
C33	C1				
CR1	Tuning UHF/VHF	2710046	1	HA154	18518
L1	Inductor, 1.0 μH	3510003	5	DD-1.00	
L2	Inductor, .033 μH	3520013	2	551-5172-03	72259
L3	L1				
L4	Inductor, .056 μH	3520016	1	1026-08	71895
L5	Not Used				
L6	L2				
L7	Inductor, 0.027μH	3520012	2	551-5172-02	71279
L8	L1				
L9	L1				
L10	Part of Board , Inductor, Spiral				
L11	L7				
L12	Not Used				
L13	L10				
L14	L1				
Q1	NPN, Microwave	4710032-01	1	NE02137	72136
Q2	NPN, Microwave	4710032-00	5	NE02137	33297
Q3 thru Q6	Q2				
Q7	NPN, UHF/VHF Power	4710029	1	NE050391-12	72136

A201A VOLTAGE CONTROL OSCILLATOR, continued

2020199-00 H

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
Q8	NPN, General Purpose	4704124	1	2N4124	04713
Q9	PNP, General Purpose	4704126	1	2N4126	04713
R1	Met Ox, 1K, 2%, 1/4 W	4130102	3	C4/2%/1K	24546
R2	Met Ox, 10K, 2%, 1/4 W	4130103	2	C4/2%/10K	24546
R3	Met Ox, 100 K, 2%. 1/4 W	4130104	1	C4/2%/100K	24546
R4	Met Ox, 1.8K, 2%, 1/8 W	4130182	1	C4/2%/1.8K	24546
R5	Met Ox, 300 ohm, 2%, 1/4 W	4130301	1	C4/2%/300	24546
R6	Met Ox, 1.5K, 2%, 1/4 W	4130152	2	C4/2%/1.5K	24546
R7	Met Ox, 510 ohm, 2%, 1/4 W	4130511	2	C4/2%/510	24546
R8	Met Film, 15.0 ohm, 1%, 1/8W	4061509	4	RN55D1509F	24546
R9	Met Ox, 150 ohm, 2%, 1/4 W	4130151	1	C4/2%/150	24546
R10	R8				
R11	Met Film, 68.1 ohm, 1%, 1/8W	4066819	2	RN55D4759F	24546
R12	R6				
R13	R7				
R14	Met Film, 121 ohm, 1%, 1/8W	4061210	1	RN55D210F	24546
R15	Met Ox, 470 ohm, 2%, 1/4 W	4130471	3	C4/2%/470	24546
R16	Met Ox, 560 ohm, 2%, 1/4 W	4130561	1	C4/2%/560	24546
R17	Met Ox, 430 ohm, 2%, 1/4 W	4130431	1	C4/2%/430	24546
R18	R1				
R19	R1				
R20	R15				
R21	Met Ox, 1.1 K, NOM, 2%, 1/4 W, SAT	4130999	1		
R22	Met Film, 100.1 ohm, 1%, 1/8W	4061000	1	RN55D1000F	24546
R23	20 ohm Nom, 5%, 2.5 W, S.A.T.	4119999	1		
R24	Not Used				
R25	Met Film, 30.1 ohm, NOM 1%, 1/8W, SAT	4069999	2		
R26	R25				
R27	Met Film, 27.4 ohm, NOM 1%, 1/8W	4069999	1	C4/2%/SAT	24546
R28	R8				
R29	R8				
R30	R11				
R31	Met Ox, 4.7K, 2%, 1/4 W	4130472	1	C4/2%/4.7K	24546
R32	R2				
R33	R15				
R34	Comp, 5.6, 5%, 1/4 W	4010569	1	RC07GF5R6J	81349
T1	Transformer, RF	4910002	1	EIP	34257

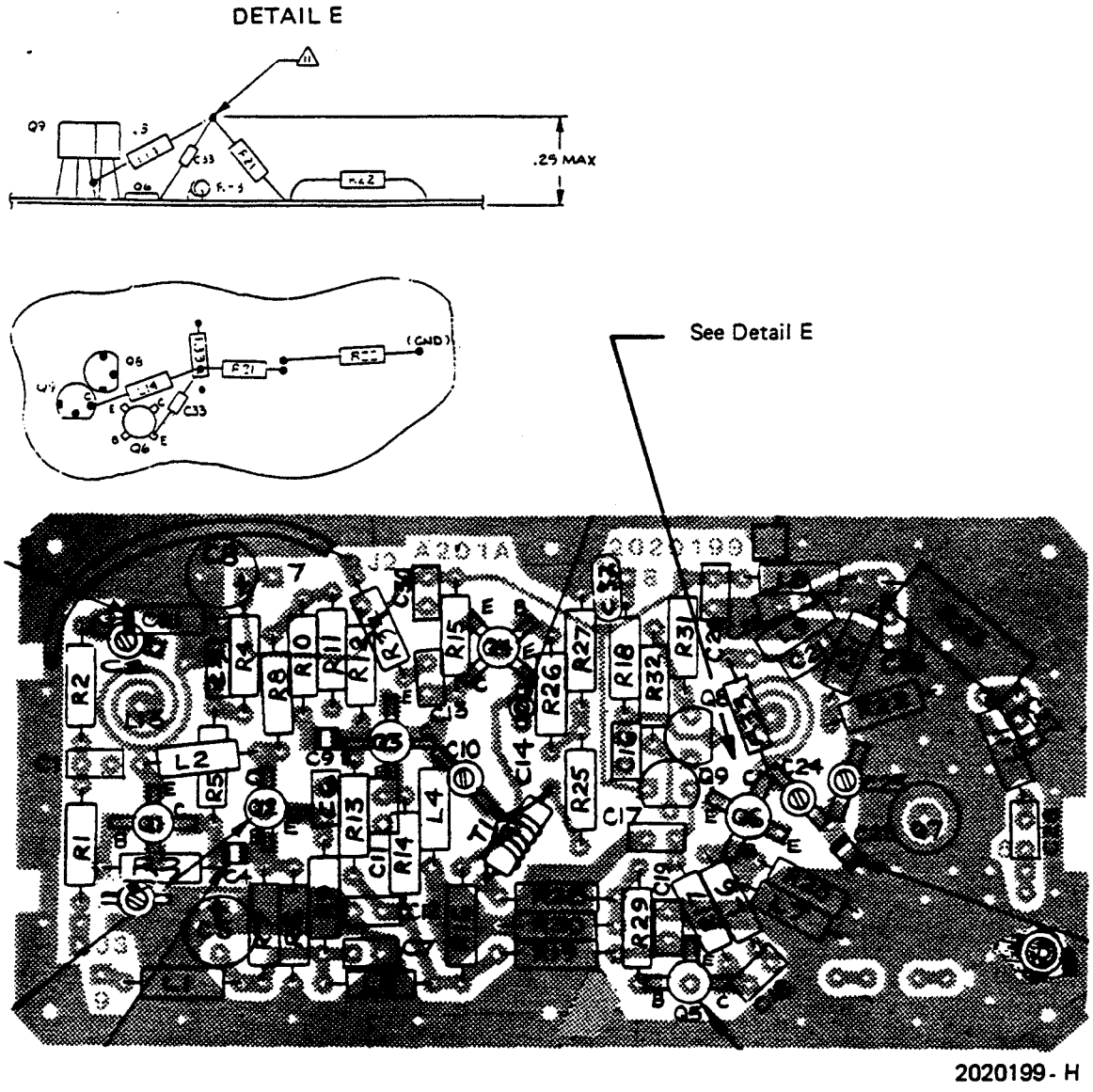


Figure 201A-2. Voltage Controlled Oscillator Component Locator

A201B
IF AMPLIFIER
(2020143)

The IF Amplifier performs three major functions.

- Amplifies the down-converted intermediate IF frequency to ± 0dBm.
- Provides a digital threshold output when the IF power exceeds -3dBm.
- Provides an analog signal that is proportional to the total power at the Band 3 input. A gain scaling control alters the output by 15dB (=X30).

The Microwave assembly mixer output is the input to the IF board. The IF goes through a high pass filter to three similar amplifier stages. Stage 1 consists of transistors Q1 and Q2 operating under closed loop feedback via R4. Resonant peaking of the output at 125MHz using L4 and C8 gives a power gain of 23dB. Successive stages are similar except that stagger tuning is used for optimum response shape. Inductors L4, L5, and L7 are printed on the circuit board and are adjusted by means of shorting bars placed across portions of the spiral. The IF output signal is sampled by a detector CR3. It's level is compared to a voltage corresponding to –3dBm. When this level is exceeded, the IF threshold output goes low.

The low frequency signal from the mixer is the current caused by rectification of the input power. This is converted to a voltage in U2. To provide a larger dynamic range, a gain change is made by switching the Field Effect Transistor (FET) Q7, thus lowering the feedback resistor. Assemblies used in –02 converters (26.5 GHz) also include transistors Q8 & Q9 to translate a TTL input to ± 12V necessary to drive FET Q10. This circuit sets the mixer bias current to 0 when the VCO power amplifier is enabled.

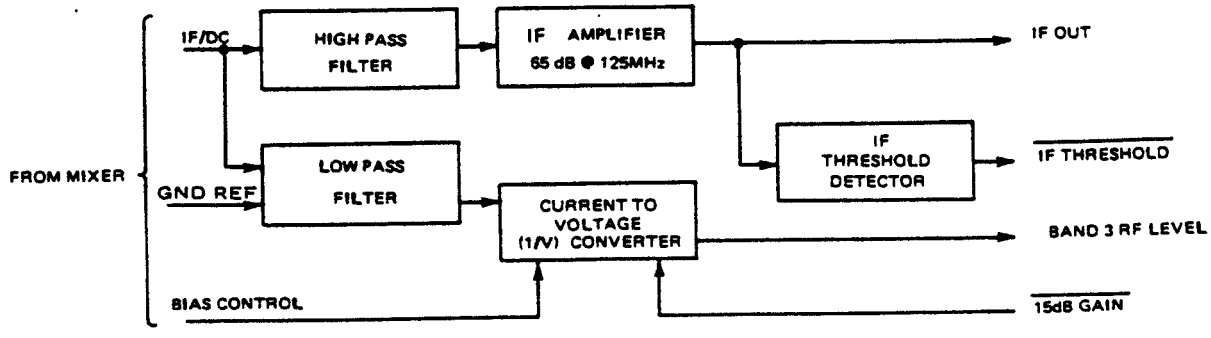


Figure 201B-1. IF Amplifier Functional Diagram

A201B IF AMPLIFIER

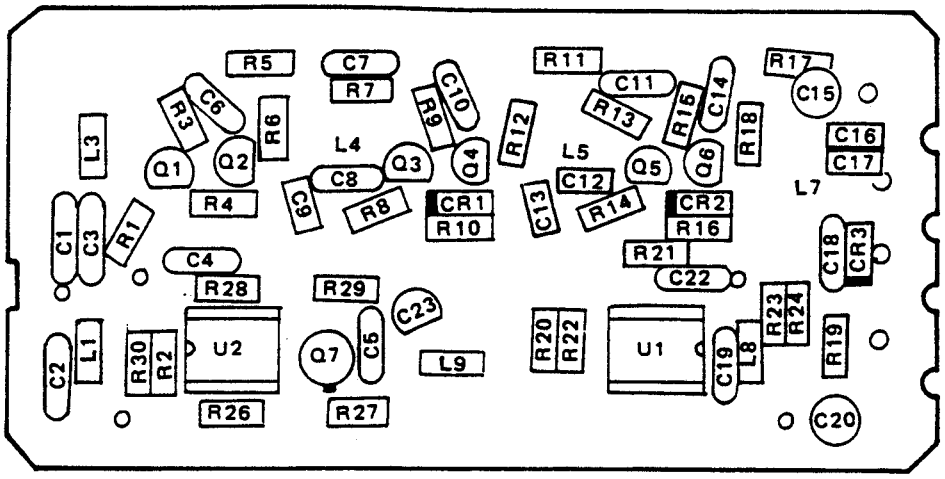
2020143-01-AH

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A201B	IF Amplifier Assy	2020143-01	1	EIP	34257
	P/O VCO/IF Mod Assy	2010142	Ref		
C1	Mica, 8pF, 13%, 500V	2260011	1	CD080C03	56289
C2	Mica, 100pF, 5%, 500V	2260034	6	FD101J03	72136
C3	Mica, 15pF, 5%, 500 V NOM S.A.T.	2269999	3		
C4	Cer, .01μF, 20%, 100V	2150003	7	TG - S10	56289
C5	Not Used				
C6	C4				
C7	C4				
C8	C3				
C9	C2				
C10	C4				
C11	C4				
C12	C3				
C13	C2				
C14	C4				
C15	Tant, 10μF, 20%, 25V	2300029	2	TAG20 - 10/25(M)	14433
C16	Mica, 39pF, 5%, 500V	2260023	1	CD10ED390J03	56289
C17	C2				
C18	C2				
C19	C4				
C20	C15				
C21	Not Used				
C22	C2				
C23	Cer, .001μF, 10%, 100V	2150015	1	UR2020S100X7R102K	80031
CR1	Hot Carrier	2710004	2	5082-2835	07263
CR2	CR1				
CR3	Mixer, UHF Schottky	2710038	1	ND4991	21843
L1	Inductor, .68μH	3520017	2	1641-475	72259
L2	Not used				
L3	L1				
L4	Part of Board				
L5	Part of Board				
L6	Not Used				
L7	Part of Board				
L8	Inductor, 1μH	3510003	2	DD - 1.00	72259
L9	L8				
Q1 thru Q6	NPN, RF	4710026-02	6	NE73432B	0000S
Q7	D - MOS FET Switch	4710031	1	SD215	18324
R1	Res, MF, 47.5, 1%, 1/8W	4064759	3	RN55D759F	91637
R2	Res, MF, 1.82K, 1%, 1/10W	4051821	1	RN55C821F	81349
R3	Comp, 1K, 5%, 1/4 W	4010102	3	RC07GF102J	81349
R4	Met Ox, 560, 2%, 1/4 W	4130561	1	C4/2%/560	24546
R5	Comp, 10, 5%, 1/4 W	4010100	5	RC07GF100J	81349
R6	Met Ox, 82, 2%, 1/4 W	4130820	2	C4/2%/82	24546
R7	R5				
R8	R1				

A201B IF AMPLIFIER

2020143-01-AH

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R9	Comp, 2K, 5%, 1/4 W	4010202	1	RC07GF202J	81349
R10	Met Ox, 470, 2%, 1/4 W	4130471	2	C4/2%/470	24546
R11	R5				
R12	Met Ox, 75, 2%, 1/4 W	4130750	1	C4/2%/75	24546
R13	R5				
R14	R1				
R15	R3				
R16	R10				
R17	R5				
R18	R6				
R19	Comp, 20K, 5%, 1/4 W	4010203	1	RC07GF203J	81349
R20	Prec, 1%, 4.12K, NOM, S.A.T	4059999-00	1		
R21	Met Flm, 681K, .5%, 1/8W	4056813-00	1	RN55C6813D	81349
R22	Met Flm, 470K, .5%,1/8 W	4054703-00	1	RN55C4703D	81349
R23	Met Ox, 6.8K, 2%, 1/4 W	4130682-00	1	C4/2%/6.8K	24546
R24	Met Ox, 4.7K, 2%, 1/4 W	4130472-00		C4/2%/4.7K	24546
R25	Not used				
R26	Precision, 57.6K, 1%, 1/10 W	4055762-00	1	RN55C5762F	81349
R27	Met Ox, 100 ohm, 2%, 1/4 W	4130101	1	C4/2%/100	24546
R28	Comp, 100K, 5%, 1/4 W	4010104	1	RC07GF104J	81349
R29	Comp, 15K, 5%, 1/4 W	4010153	1	RC07GF153J	81349
R30	R3				
U1	Dual Comp, Low Power	3050393	1	LM393	0000X
U2	Dual Op Amp.	3045532	1	NE5532	0000X



2020143 -01 AH

Figure 201B-2. IF Amplifier Component Locator

A203
BAND 3 MICROWAVE CONVERTER

The A203 Microwave Converter consists of three sub-assemblies.

- A201A Voltage Control Oscillator
- A201B IF Amplifier
- A202 Microwave (yig)

CAUTION

Disassembly of the A202 Microwave assembly, or removal of it from the A201A VCO or A201B IF Amplifier will void the EIP warranty.

The assembly drawing and schematic for both the VCO and IF circuits are included only for reference. The entire A203 assembly must be tested as a complete unit to ensure proper performance of the counter. Repair of the A202 Microwave assembly can only be done at the factory. The VCO and IF Amplifier boards require special test equipment, therefore field repair is not recommended.

The Band 3 Converter is a complete microwave subsystem (see Figure 203-1) which converts an input signal in the 1 to 18 (26.5) GHz range down to an IF of 125MHz. Down conversion is achieved in this heterodyne system by combining the input signal with a harmonic of a precisely known reference signal (F_{VCO}). The mixer then produces a signal (F_{IF}) equal to the difference between the input and reference harmonic. If this difference is close to 125MHz, it is amplified to a level of about 0dBm and then counted. The input signal is then determined from the equation $F_{IN} = NF_{VCO} + F_{IF}$. F_{VCO} is set by the instrument program via a phase locked loop located on the converter control board (A108) and is thus known exactly. Harmonics of the VCO are produced by the comb generator and coupled to the mixer. The frequency ranges of the VCO and IF are such that for any VCO frequency and any input frequency, only one harmonic can produce an IF frequency. The YIG filter located between the RF input and the mixer is used to approximately determine the input frequency and from this information the desired values of N, F_{VCO} and +/– are determined.

Two other outputs are obtained from the Band 3 Converter. The first is an analog signal which is a measure of input RF power. The second is a digital signal $\overline{\text{(IF THRESHOLD)}}$ which indicates that an IF signal exists at a level of –3dBm or greater.

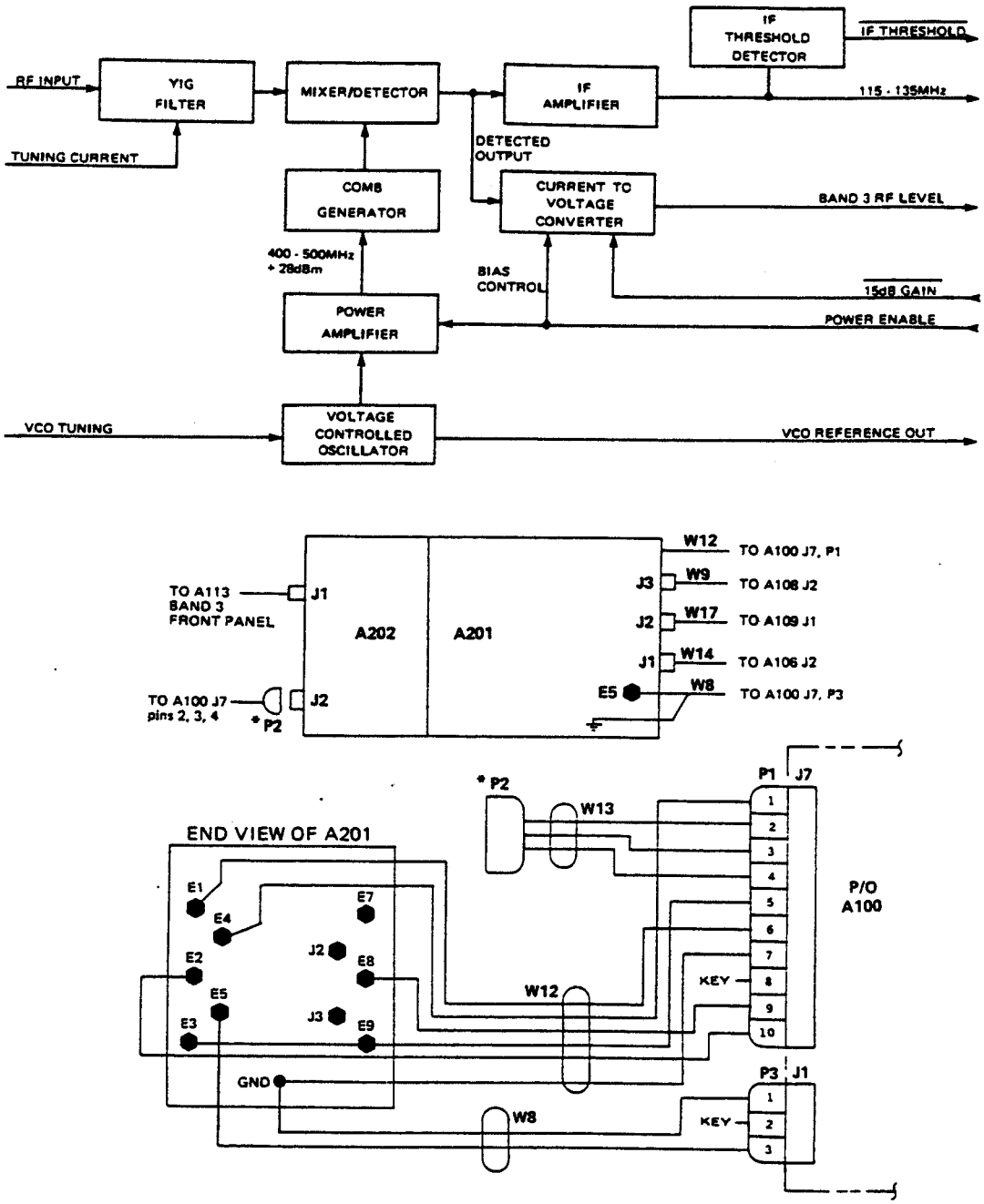


Figure 203-1. Band 3 Microwave Converter Diagram

Section 10
Options

Section 10 provides descriptions, specifications (where applicable), schematic diagrams and component locators for the options available for use with the Model or 548 counter.

OPTION

01 D TO A CONVERTER

DAC will convert any three consecutively displayed digits into an analog voltage output on rear panel.

02 POWER MEASUREMENT

1 to 18/26.5 GHz will measure sine wave amplitude to 0.1 dBm resolution and display simultaneously with frequency.
Power offset to 0.1 dB resolution, selectable from front panel.
Option will not degrade the basic performance of the counter.

03 TIME BASE OSCILLATOR $< 5 \times 10^{-9}$ (2010143-03).

04 TIME BASE OSCILLATOR $< 1 \times 10^{-9}$ (2010143-04).

05 TIME BASE OSCILLATOR $< 5 \times 10^{-10}$ (2010143-05).

06 EXTENDED FREQUENCY CAPABILITY - 548A
Use in conjunction with model 590 Frequency Extension Cable Kit
and optional Remote Sensors models 91 thru 95.

07 REMOTE PROGRAMMING/BCD output

08 GENERAL PURPOSE INTERFACE BUS (GPIB)

09 REAR PANEL INPUT

10 CHASSIS SLIDES

OPTION 01
DIGITAL TO ANALOG CONVERTER

Option 01 will convert three consecutive digits to an analog voltage, available on the rear panel. The output will reflect the display, and substitute zeros for any non-numeric characters that appear. The output will be updated after every display update.

SPECIFICATIONS

Output Voltage	0.000 V to 0.999 V
Accuracy (25° C)	± 0.5 % ±1 mV
Temp. Stability (0-50° C)	± 0.01 % / °C
Resolution	1 mV
Load Impedance	1 K ohm minimum
Connector	BNC female (on rear panel)
Protection	± 10 V or dc applied to output connector will not cause damage. No damage will occur by any load.

OPERATION

On power up the DAC is in off state.

LOCAL OPERATION WITH KEYBOARD

A three key sequence selects the location of the three digits desired, by entering the most significant digit wanted. Digits are numbered 01 through 12.

PRESS : DAC [ ] [X] [X] XX can vary from 01 to 12.

EXAMPLES :

DAC [ ] [0] [1] 1 Hz digit selected

DAC [ ] [0] [2] 10 Hz, 1 Hz digits selected

DAC [ ] [0] [3] 100 Hz, 10 Hz, 1 Hz digits

DAC [ ] [0] [4] 1 kHz, 100 Hz, 10 Hz digits

•
•
•

DAC [ ] [1] [2] 100 GHz, 10 GHz, 1 GHz digits

After pressing DAC [ ] , the display will show the present DAC status, e.g., DAC OFF or DAC XX, and three decimal points will show the locations of the currently selected digits (if DAC is on).

After pressing the first [X], the display will show the temporary entry, e.g., DAC X , but the three decimal points will still show the previous DAC status.

After pressing the second [X], the display will show the new entry, e.g., DAC X X , and the three decimal points will move to the new places. The DAC output will start to be updated accordingly. Release of the button pressed will return the display back to normal frequency display.

Any wrong key pressed will result in displaying ERROR 10. The operator must restart the key sequence to enter the correct data.

To clear display from DAC data, ERROR display, or ignoring half-sequence entered, press [CLEAR DISPLAY]. Display will return to normal and DAC status will not be changed.

To shut off DAC press [DAC] [DATA CLEAR] or [DAC] [0] [0]

REMOTE OPERATION

For remote operation through GPIB, refer to the GPIB (Option 08) section of this manual.

For remote operation through BCD/RMT, refer to the BCD/RMT (Option 07) section of this manual.

THEORY OF OPERATION

A simplified block diagram of the DAC board is shown in figure 01-1.

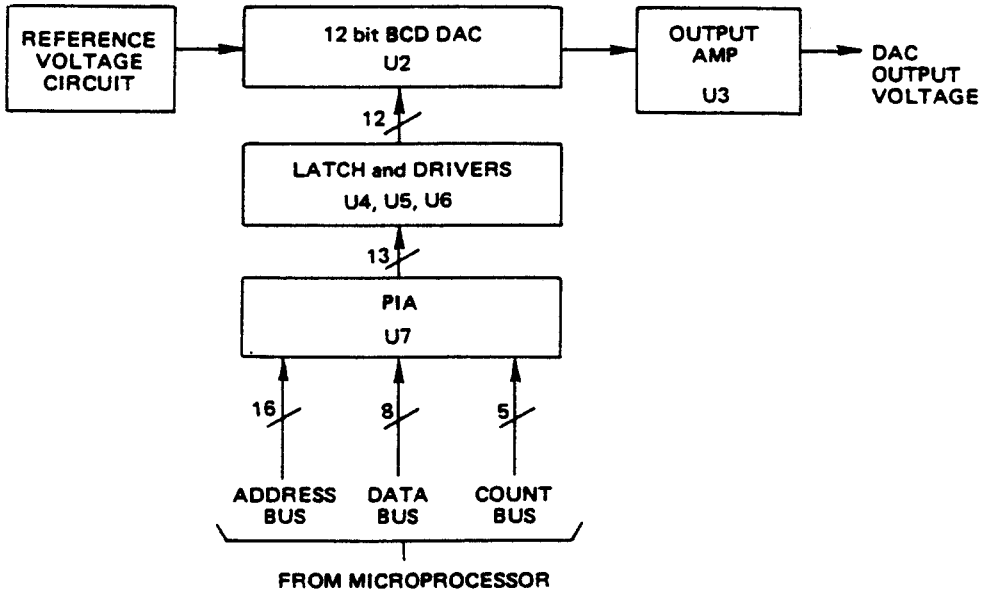


Figure 01-1. DAC Board, Simplified

HARDWARE

PIA AND LATCH DRIVER BLOCKS

The three selected digits are manipulated by the program and sent to the PIA. First the two LSD's are sent to port A, then the third digit (MSD) plus a positive-going pulse (on pin 14 of U7) that triggers the latch U6 so that the complete 12 bit word appears to the DAC inputs (U2). U4 and U5 are level translators from T^2L to CMOS for the DAC.

ANALOG BLOCKS

The DAC is referenced to a 1 volt reference voltage that is generated by CR1 zener and U1 Operational Amplifier. Gain adjustment is provided to calibrate the reference voltage. The DAC U2 converts the 12 bit digital inputs to an analog voltage (0.000V – 0.999V). The output amplifier U3 provides the necessary I/V conversion, output isolation and protection. Zero offset adjustment is provided for calibration purposes, also.

SOFTWARE

The DAC software is described in figures 01-2 and 01-3.

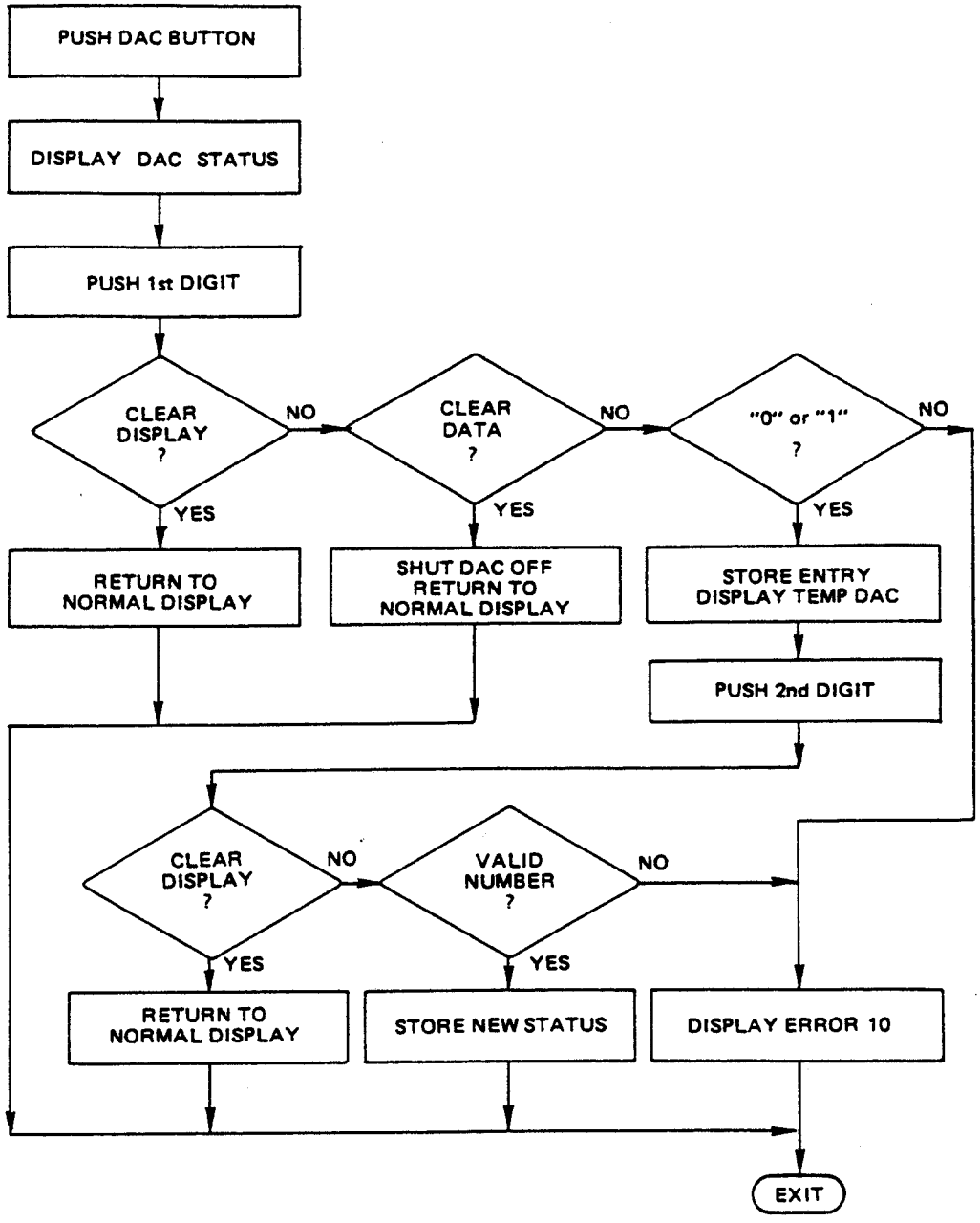


Figure 01-2. Keyboard Control

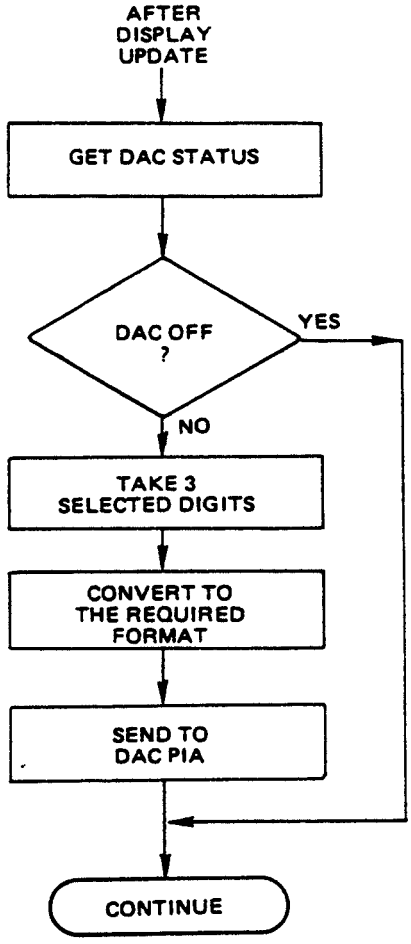


Figure 01-3. DAC Board Update

CALIBRATION

The following instruments or their equivalents are required to perform calibration of the DAC board. Calibration is required every six months or after the board has been repaired.

BRAND	MODEL	TYPE	SPECIFICATIONS
Fluke	8050A	DVM	4 ½ digit resolution

ZERO OFFSET CALIBRATION

1. Turn on the counter with no input, so that the display shows all zeros.
2. PUSH [DAC] [0] [3]
3. Connect digital volt meter to the rear DAC output.
4. Adjust R6 to reach 0.000 volts on the DVM display.

FULL SCALE CALIBRATION

1. Short TP3 to TP4.
2. Adjust R4 to reach 1.000 volts on the DVM display.
3. Remove the short.

The calibration for the DAC board is complete.

PERFORMANCE TESTS

Refer to the instruments table in Calibration for the required test equipment.

Connect the DVM to the DAC output (rear panel). Connect rear 10 MHz output to Band 1 input.

ENTER : [BAND] [1] [RESOL] [2] Display shows 10.000 0 MHz.

ACCURACY TEST

ENTER : [DAC] [0] [6] DVM should read 0±1mV.

ENTER : [FREQ OFFSET] [•] [9] [9] [9] [MHz] DVM should read 0.999±0.006 V.

Repeat the second test in accuracy for entries between .888 and .111. DVM should read the entry ± 1 mV ± 0.5 % of entry.

TROUBLESHOOTING

1. If zero offset calibration cannot be achieved, check that all digital inputs to U2 (pins 3 to 15) are at "low" levels (+ 0.5 V). If they are not, replace U2 or U3.

2. If full scale calibration cannot be achieved, check that voltage at TP1 is 6.2 volts. If voltage is wrong, replace CR1 or R1 after verifying the +12 V supply. If the voltage at TP1 is 6.2 volts, check TP2. The voltage at TP2 should be 1.000 volts. If it is not, the failure is in U1 or the resistors R2, R3, or R4. If TP2 voltage is still not 1.000 volts, replace U2.

3. The digital lines in the DAC board can be checked in three ways.

   - With a static test implemented by connecting the rear time base 10 MHz output to Band 1 input.

     ENTER : [BAND] [1] [RESOL] [2] Display shows 10.000 0 MHz

     ENTER : [DAC] [0] [6]

     Now entering [FREQ OFFSET] [.] [X] [X] [X] [MHz] will cause a display of 10.XXX0 MHz.

     The XXX are selected to the DAC board, so the three BCD's should appear on U7, pins 2 to 13 (pin 2 is the LSB). On pin 14 there should be positive pulses. Checking two combinations like 777 and 888 can locate a fault in the digital path between U7 outputs and U2 inputs.

   - A dynamic test that is provided with the DAC option.

     ENTER : [TEST] [1] [1]

     A continuous count ramp from 000 to 999 is sent to the DAC board, regardless of DAC status or display.

     Connect the DAC rear output to an oscilloscope. A ramp should be observed going from 0 to .999 volts. The ramp is built with 1 mV amplitude steps. Any failure in one or more digital lines in the board will cause either breaking in the ramp or a multiple amplitude steps (2mV, 4 mV, ect.). Careful analysis will show the bad line or lines.

   - Signature analysis while operating in the dynamic test just described, and checking the following signatures.

DAC OPTION SIGNATURES

	START	STOP	CLOCK
CONNECTIONS	A106 TP5	A106 TP5	A105 TP8
BUTTONS	OUT ↑	IN ↓	IN ↓

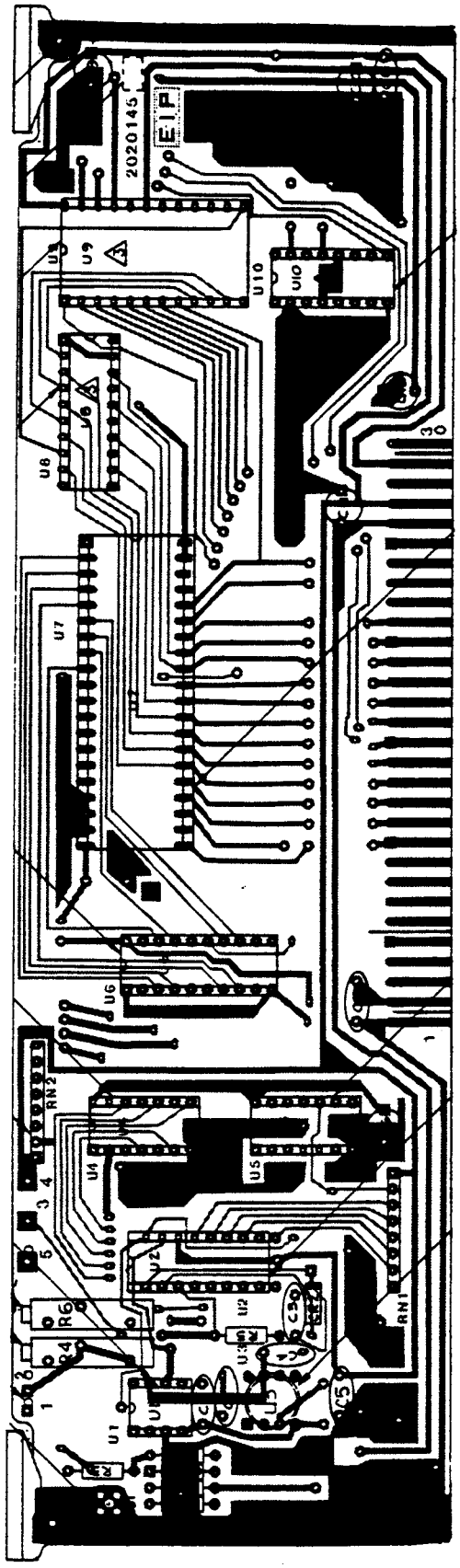
LINE	SIGNATURE
U4 pin – 2	46F0
4	79HH
6	7U60
8	4F30
10	9115
12	17HP
+5 V	1915
U5 pin – 2	2597
4	7P0U
6	U8A9
8	P1C0
10	7808
12	7C4C
U6 pin – 2	2597
5	7P0U
6	U8A9
9	P1C0
12	7808
15	7C4C
16	46F0
19	79HH

LINE	SIGNATURE
+5 V	1915
U7 pin – 2	0F91
3	7F31
4	4CA3
5	3241
6	U738
7	5UPU
8	0659
9	5HHF
10	7U60
11	4F30
12	9115
13	17HP
14	30UC

OPTION 01 – DIGITAL TO ANALOG CONVERTER

2020145 - K

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A104	Digital to Analog Converter Assy	2020145-02	Ref.	EIP	
C1	Cer, .01 μ F, 20%, 100V	2150003	6	TG-S10	56289
C2	C1				
C3	Mica, 100pF, 5%, 500V	2260034	1	CD10FD101J03	56289
C4	C1				
C5	C1				
C6	Tant, 33 μ F, 20%, 10V	2300015	3	TAG20-33/10-50	14433
C7	C1				
C8	C1				
C9	C6				
C10	Tant, 10 μF, 20%, 25V	2300029	2	TAG20-10/25-20	14433
C11	C10				
C12	C6				
CR1	Zener, 6.2V	2700827	1	IN827 or IN827A	
CR2	Shottky, Barrier	2710004	1	FH1100	07263
R1	Comp, 750, 5%, ¼ W	4010751	1	RC07GF751J	81349
R2	Prec, 20K, 1%, ¼W	4052002	1	RN55C 2002F	81349
R3	Prec, 6.19K, 1%, ¼ W	4062871	1	RN55D2871F	81349
R4	Variable, 500 ohm ,10%	4280009	1	89PR500	
R5	Comp, 10K, 5%, ¼ W	4010103	1	RC07GF103J	81349
R6	Variable, 10K ohm, 10%	4280006	1	89PR10K	
R7	Comp, 1K, 5%, ¼ W	4010102	1	RC07GF102J	81349
RN1	Network of 7,10K	4170004	2	4308R-101-103	32997
RN2	RN1				
U1	Op Amplifier	3040741	1	LM741CN	0000X
U2	DAC	3050752	1	AD7525KN	0000X
U3	Prec, Op Amplifier, JFET	3041016	1	OP16FP	06665
U4	Hex Buffer	3007407	2	DM7407N	0000X
U5	U4				
U6	8 Bit Latch	3034373	1	MM74C373N	
U7	PIA	3086820	1	MC6821	04731
U8	Oct. Driver	3084244	1	SN74LS244N	01295
U9	PROM Set	2060001-04	1	6300001-09	01295
U10	6 Bit Comparator	3078131	1	DM8131	0000X



2020145 -00-K

U8, U9, U10 are not used in models 545A/548A

Figure 01-4. DAC Component Locator

OPTION 02
POWER MEASUREMENT

Option 02 measures the power of signals applied to Band 3. The power is displayed (to 0.1 dB resolution) simultaneously with frequency (to 100 kHz max. resolution). For A M and F M averaging purposes, gate time is controllable in the power meter mode, through the resolution function. Power gate time mirrors frequency gate time. For example, in resolution 0 the frequency gate time is 1 second, and the power gate time is 1 second. In resolution 1 the frequency gate time is 100 msec., and the power gate time is 100 msec. Option 02 allows power offsets from -99.9 dB to 99.9 dB, with a 0.1 dB resolution and will not degrade the basic performance of the counter.

SPECIFICATIONS

ACCURACY	± 1.2 dB Typical 0-50° C ± 0.5 dB Typical 25° C
TIME ADDED	1 GATE TIME + 50 msec.
RESOLUTION	0.1 dB POWER, Sensitivity to -10 dBM; 0.2 dBm to overload, Selectable 100 KHz -1 GHz Frequency
RANGE	Entire Operating Range of Band 3

KEYBOARD OPERATION

To turn the power meter ON or OFF, PRESS: POWER METER ON/OFF

If the power meter option is off, pushing the POWER METER ON/OFF key will turn the power meter on. Pushing that key again will turn the power meter off. If the counter is displaying only frequency it will begin displaying frequency and power. If the counter is displaying frequency and power it will begin displaying frequency only.

Turn the power meter on. Observe the display. Frequency is displayed on the left, and power is displayed on the right. The dBm annunciator lights to indicate power meter operation. If the power of the signal is too small to measure, the display will show EE.E in the power meter digits. (Since 0 dBm is a valid power. 00.0 cannot be used as a no-power indicator.)

When the power meter option is on, the frequency measurements displayed on the front panel are to a maximum resolution of 100 kHz. The last selected time will be retained.

Power meter offset function enables the entry of a positive or negative power offset to 0.1 dB resolution. The offset will be incorporated into the power measurement after the next gate.

TO INPUT POWER OFFSETS

PRESS: POWER METER OFFSET — Notice flashing annunciator and power offset last entered.

PRESS: [#] — Number keys corresponding to desired power offset.

PRESS: dB — To terminate input sequence. Notice OFFSET PWR annunciator solidly lit after terminator key is released.

TO RECALL STORED OFFSETS

PRESS: POWER METER OFFSET — Stored offset is displayed.

PRESS: CLEAR DISPLAY — Returns counter to display measurements.

TO REMOVE POWER OFFSETS

PRESS: POWER METER OFFSET DATA CLEAR OR POWER METER OFFSET 0 dB OR POWER METER OFFSET dB

GPIB OPERATION

PA – Power Active. Turns POWER METER option on.

PP – Power Passive. Turns POWER METER option off.

PO – Power Offset. Enables entry of positive or negative power offsets to 0.1 dB resolution. Take a new reading after data entry if counter is not in HOLD.

THEORY OF OPERATION

The power meter uses the Schottky diode in the microwave converter as its power sensor. The output of the diode detector is connected to a programmable gain attenuator, which consists of two switchable gain stages (one is in the IF Amplifier A201B and one is on the Gate Generator A107) and two 8 bit attenuators. A comparator, set to 100 mV, and a TTL latch provide output information to the microprocessor. See figure 02-1.

After the counter has a signal, and has taken a frequency reading, it starts the power meter task. This triggers the gate time counter, resets the TTL power latch, moves the yig ±50 MHz (to insure that the signal peak is passed through), then checks the TTL power latch. If the latch is set, the attenuation is increased in 3 dB steps (until the signal is attenuated below the level of the comparitor), then back one step. If maximum attenuation is reached, and the latch is still being set, the word OVERLOAD is displayed and the task is exited.

When the latch is first checked, if it is still reset, the attenuation is decreased in 3 dB steps until the comparator level is reached. If minimum attenuation (maximum gain) is reached, the display is set to EE.E, and the task is exited.

After the attenuation is adjusted to a 3 dB resolution a successive approximation is performed to find the attenuation to a 0.1 dB resolution. The attenuation is stored, and if the gate time counter is not finished, the cycle is repeated. When the gate time counter is finished all the readings are averaged to eliminate the effects of AM on the signal.

The "power vs power" and "power vs frequency" corrections are added, and the sum is displayed. A detailed flowchart of the power meter is shown is figure 02-2.

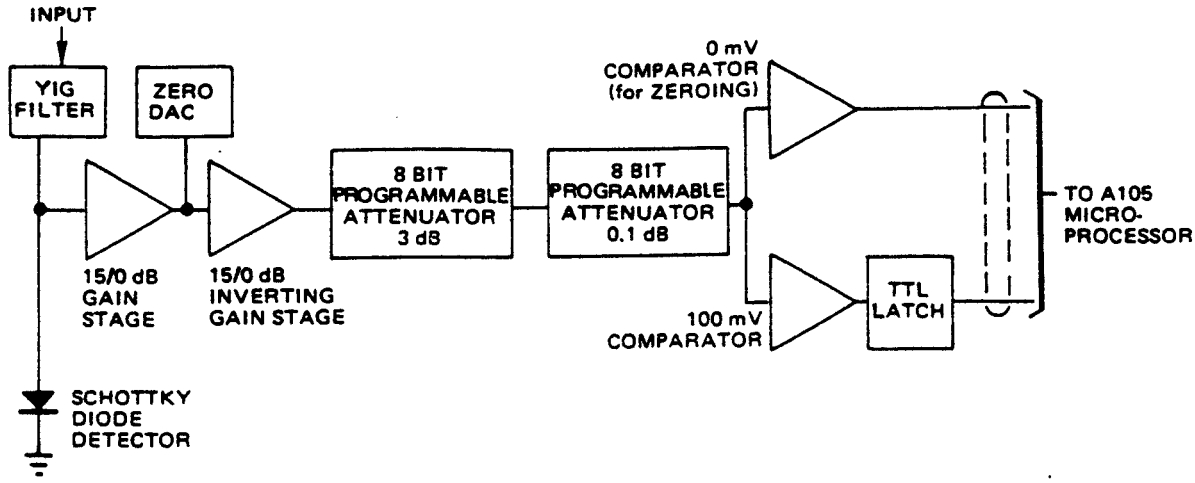


Figure 02-1. Power Meter Hardware

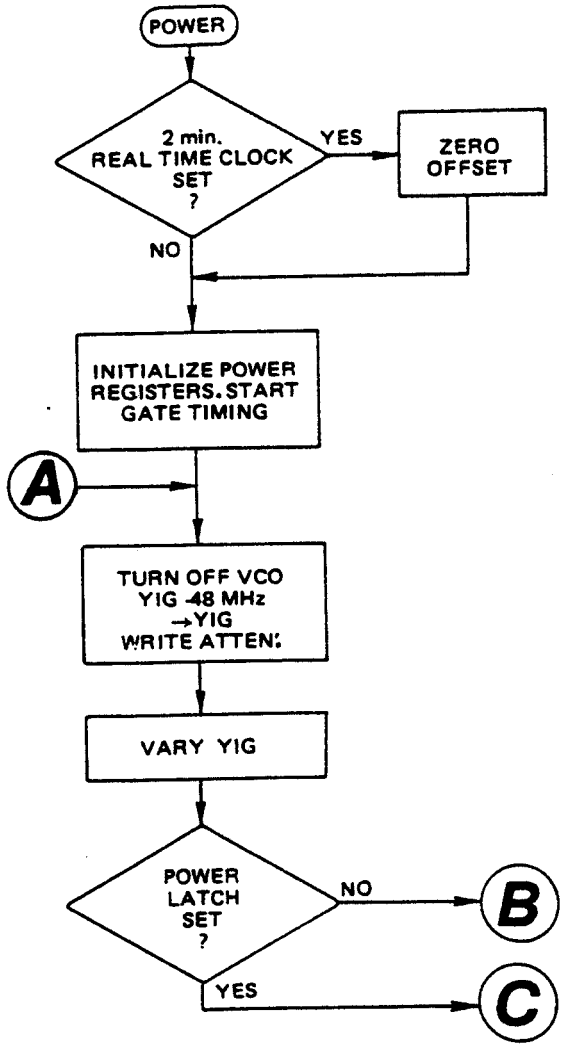


Figure 02-2. Power Meter Task

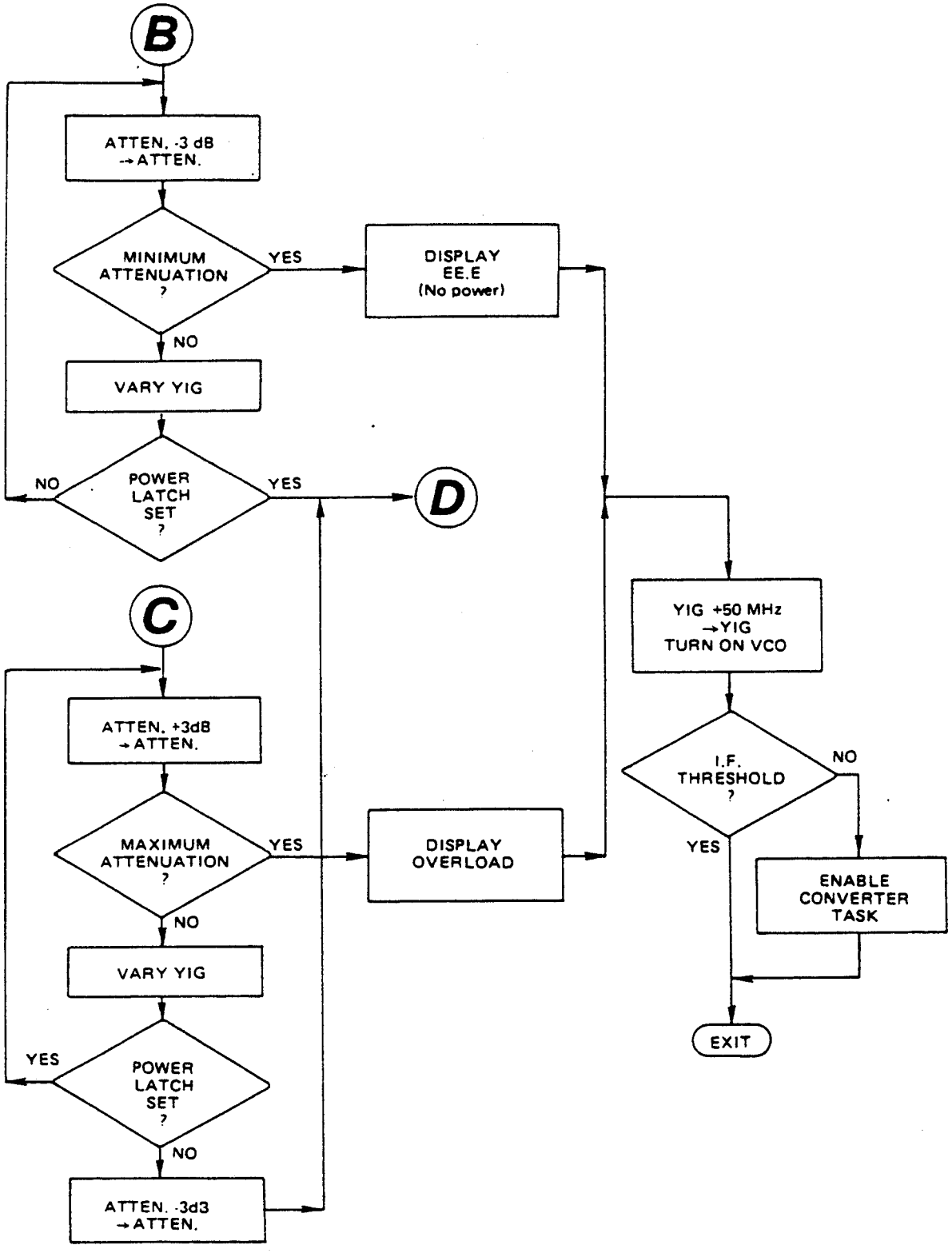


Figure 02-2. Power Meter Task, continued

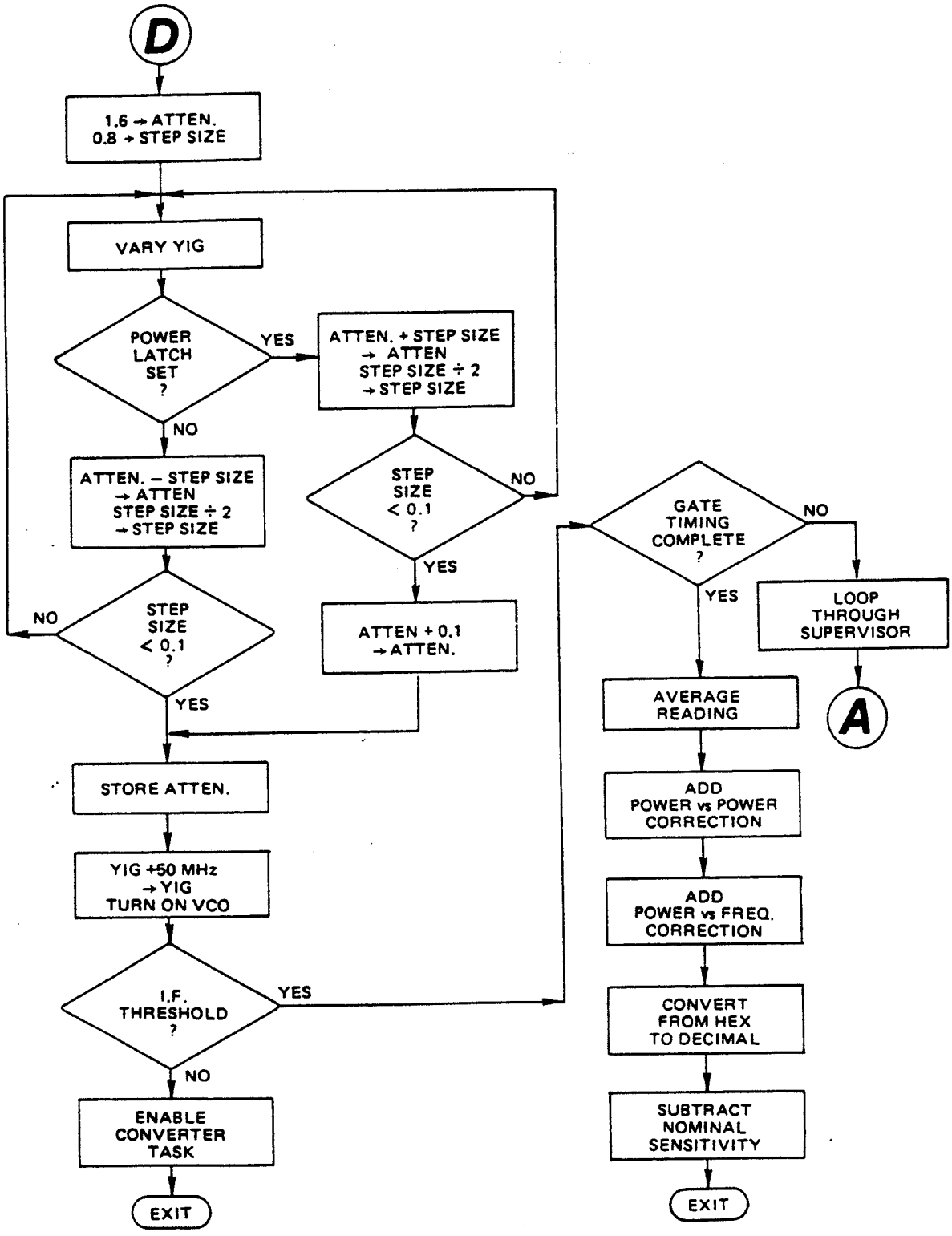


Figure 02-2. Power Meter Task, continued

CALIBRATION

The power meter contains 690 correction factors, stored in PROM.

The 150 "power vs power" correction factors compensate for variations from square law in the detector and power meter circuits. They are divided into three tables. The first table corrects variations below 10 GHz. The second corrects variations between 10 and 20 GHz. The third corrects variations above 20 GHz.

The 540 "power vs frequency" correction factors compensate for variations in the detector output at different frequencies. "Power vs frequency" corrections cover 0-27 GHz every 50 MHz.

The power meter is calibrated at the factory using specialized automatic test equipment. Because of the accuracy required, recalibration in the field is not recommended. If, however, recalibration is required, use the procedures given herein.

The test equipment required for calibration is:

MFG	MODEL	DESCRIPTION	CRITICAL PARAMETERS
H.P.	435A	Power Meter	Measures -30 to +15 dBm
Wavetek	2002	Sweeper	950 MHz - 2 GHz
EIP	928	Microwave Source	1 GHz -18.6 GHz
HP	8690A 8696A	Microwave Sweeper	18 GHz - 26.5 GHz
E.H.		PROM Programmer	Programs TI 2516 PROMS and performs check sums

CAUTION

Be sure all connections are clean
and tight. Loose or dirty connections
will cause calibration errors.

1. Duplicate the power meter PROM, zeroing all corrections (address 0000-02EC in the PROM) and setting address 02F6 to FF. Install the uncorrected PROM in the counter.

2. Set the Wavetek to 2 GHz ±1 MHz. Connect the Wavetek to band 3 of the counter. Adjust the output until the counter reads -35 dBm.

3. Connect Wavetek to the power meter. Subtract the counter reading from the power meter reading. Round the result (R_1) to 0.1 dBm.

4. Using the following formulas, justify the correction to a number between 10 and 20.

$$\text{int}(R_1) - 1 = N \; ; \; (\text{int}(R_1) = \text{Whole number portion of } R_1)$$

$$10(R_1 - N) = \text{CORR}_{10}$$

$$\text{Convert CORR}_{10}\text{ (decimal)} \rightarrow \text{CORR}_{16}\text{ (hexadecimal)}$$

(R_1 is the result of step 3.)

5. Program the correction in these locations.

   0000 - 0005 inclusive
   0032 - 0037 inclusive
   0064 - 0069 inclusive

6. Connect the Wavetek to the counter. Increase power until the counter reads 1 dB higher.

7. Connect the Wavetek to the power meter. Subtract the counter reading from the power meter reading. Round the result (R_2) to 0.1 dBm.

8. Using the following formulas, calculate the correction.

$$10 (R_2 - N) = CORR_{10}$$

$$\text{Convert } CORR_{10} \rightarrow CORR_{16}$$

(R_2 is the result of step 7, and N was found in step 4.)

9. Program the correction in the 3 addresses found by the following formulas.

$$40 + P = Add\ 1_{10},\ Add\ 1_{10} \rightarrow Add\ 1_{16}$$

$$40 + P + 50 = Add\ 2_{10},\ Add\ 2_{10} \rightarrow Add\ 2_{16}$$

$$40 + P + 100 = Add\ 3_{10},\ Add\ 3_{10} \rightarrow Add\ 3_{16}$$

(P is the power the counter was set at in step 6.)

10. Repeat steps 6 through 9 until overload is reached on the counter.

11. Install the partially corrected PROM in the counter.

12. Set the Wavetek to 950 MHz, about -15 dBm.

13. Measure the power on the counter and power meter. Subtract the counter reading from the power meter reading. Round the results to 0.1 dBm. Multiply the results by 10 and convert to hex.

14. Program the correction in the address found by the following formula.

$$\frac{FREQ\ (MHz)}{50} + 150 = Add_{10}$$

$$Add_{10} \rightarrow Add_{16}$$

15. Increase frequency by 50 MHz. Repeat steps 13 and 14. Change the sweepers as necessary, until the upper frequency limit of the counter is reached.

Refer to section 9, pages 107-5 through 107-9, for parts list and schematic diagram. The counter recalibration is now complete.

16. Perform a check sum on the corrected PROM.

17. Calculate the program number by the following formula:

FE (hexadecimal) - M = Program number

M = Last two digits of the check sum found in Step 16.

18. Program address 02F6 with the program number found in Step 17.

19. Calibration is now complete.

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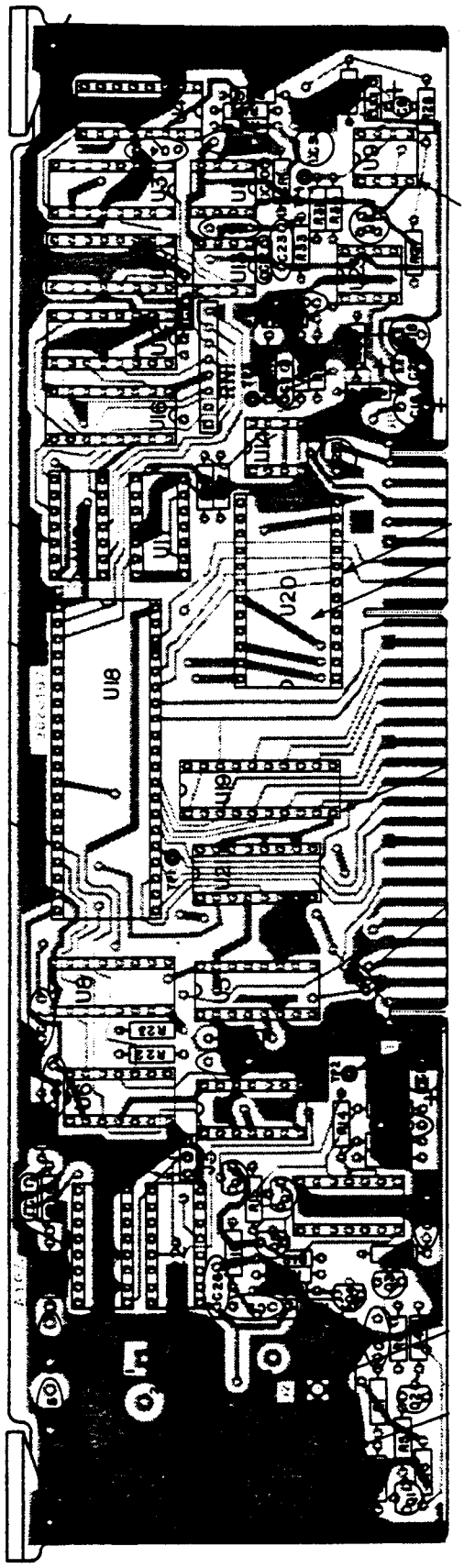


2020197 -03/04 - L

Figure 02-3. Gate Generator Component Locator

OPTIONS 03, 04, 05
TIME BASE OSCILLATORS

Three Time Base Oscillators are available as options for either the model 545A or 548A. These high stability options enhance the accuracy of the counter by the addition of oven stabilized crystal oscillators. These oscillators improve counter operation by reducing both time temperature variations.

When any one of these options is installed, the TCXO is removed from the Gate Generator board (A107) and the following components are added.

- One of three Oven Oscillators (A114) mounted on the chassis.
- 28 VDC Power Supply board (A112) , assembly part number 2010226
- Power Supply Transformer T1 (part number 4900006) mounted on A112.
- Time Base Adjustment Pot J2 (part number 2010190) mounted on the rear panel.
- Related interconnecting cable harnesses.

	OPTION 03	OPTION 04	OPTION 05
CHARACTERISTIC	2030010 - 01	2030010 - 02	2030010 - 03
AGING RATE/24 HOURS (After 72 hour warm-up)	$< \lvert 5 \times 10^{-9} \rvert$	$< \lvert 1 \times 10^{-9} \rvert$	$< \lvert 5 \times 10^{-10} \rvert$
SHORT TERM STABILITY (1 second average)	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms
0° to + 50° C TEMPERATURE STABILITY	$< \lvert 6 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$
± 10% LINE VOLTAGE CHANGE	$< \lvert 5 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$

Figure 03/04/05-1. Time Base Oscillator Option Specifications

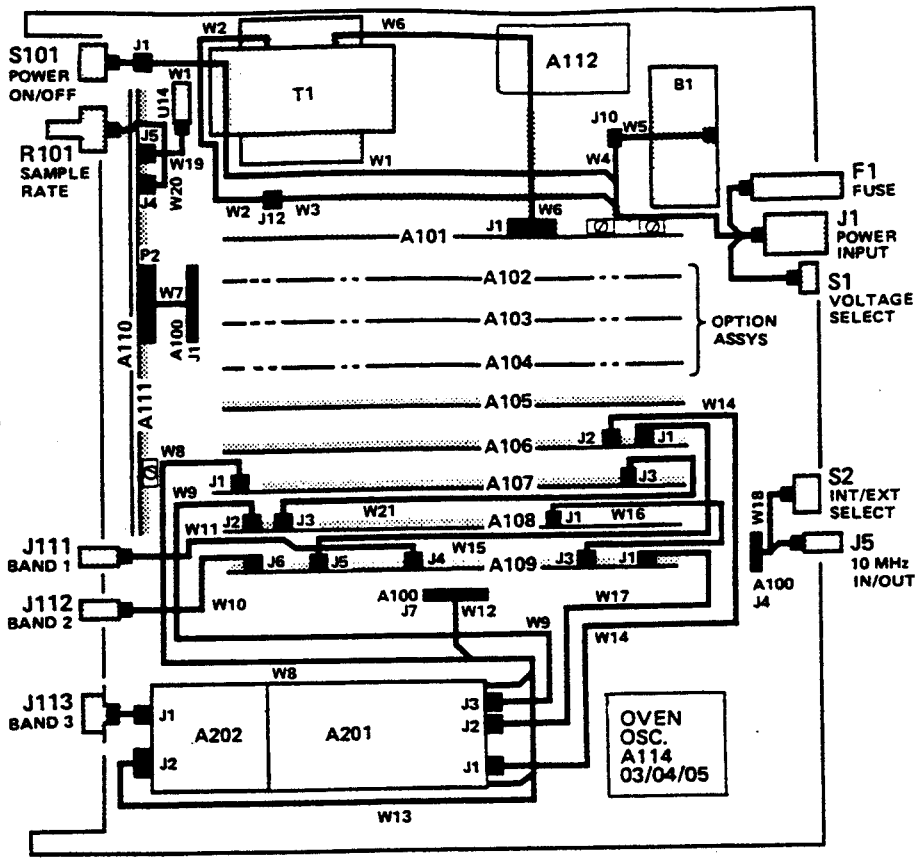


Figure 03/04/05-2. Component Location, Time Base Option

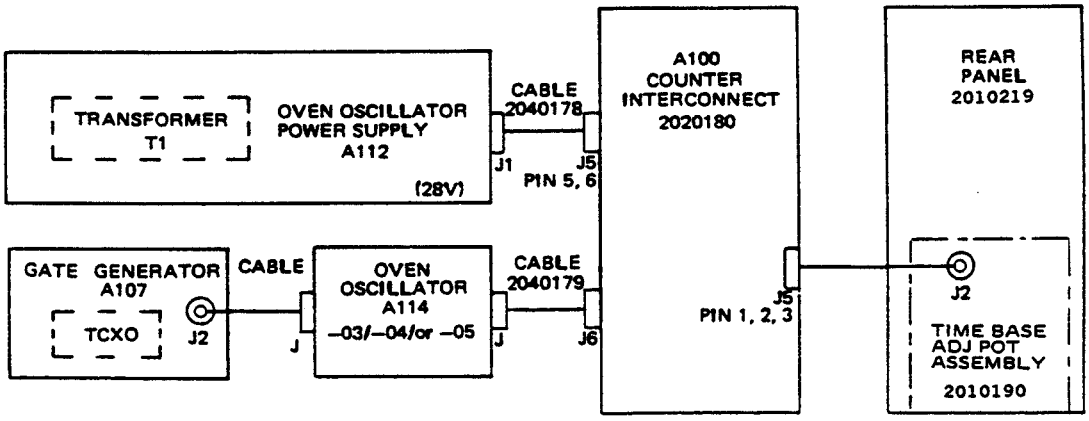


Figure 03/04/05-3. Time Base Option, Interconnection Diagram

OVEN OSCILLATOR POWER SUPPLY

The Oven Oscillator Power Supply board (A112) is a simple 28V regulated, current limited power supply. U1 and U2 provide voltage regulation, thermal protection and current limiting.

The transformer T1, CR1, C1 and C2 provide a 40V nominal unregulated DC voltage. The output voltage is set by voltage divider R5, R3 and R4. These resistors were selected so that 28V out provides 2.23V at U2 pin 2 (to U2 pin 1). Diode CR2 protects the supply from being pulled more negative than ground. See the schematic in figure 03/04/05-6.

The power supply (A112) is on and operating as long as the counter is connected to an active AC power source. The counter's POWER ON/OFF switch on the front panel does not control this assembly.

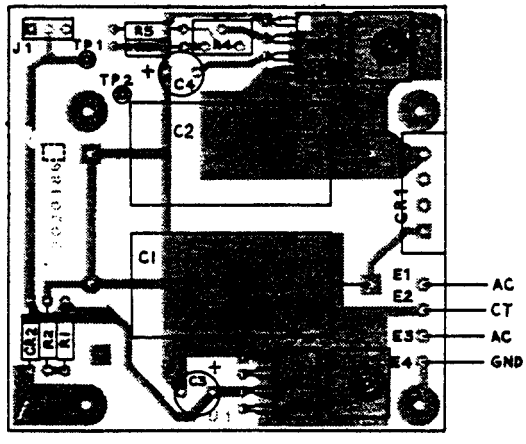


Figure 03/04/05-4. Oven Oscillator Power Supply (A112) Component Location

OVEN OSCILLATOR CALIBRATION

When options 03, 04 or 05 are installed in the counter, the effects of temperature perturbations and aging must still be considered, although the magnitude of the inaccuracies associated with each oscillator are greatly reduced.

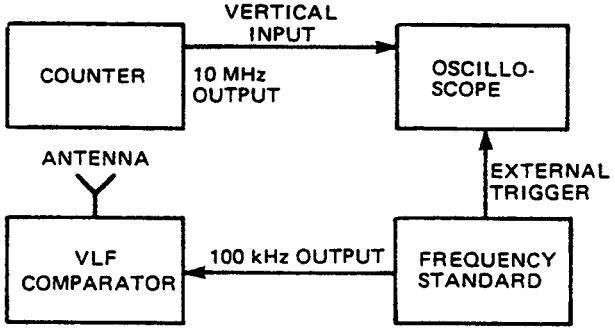
Full benefit of the oven stabilized oscillator characteristics can only be realized if the oscillator is running continuously (with counter always connected to a source of AC power). Under these conditions the perturbations in frequency will generally be in the positive direction for either an increase or decrease in temperature from + 25° C. The aging characteristic is also generally in the positive direction.

How frequently the oscillator is adjusted is determined by the level of accuracy required. To adjust the oscillator to an inaccuracy of less than 1 X 10^{-9} parts, relative to a standard, use this procedure. The test is illustrated in figure 03/04/05 - 5.

Observe the drift of the oscilloscope pattern. The fractional frequency offset is computed from:

$$\frac{T_{\text{drift of zero crossing}}}{T_{\text{observation time of drift}}} = \frac{\Delta f}{f}$$

If the pattern drifts, at a rate of .01 microsecond every 10 seconds, the frequency is in error by 1 part in 10^9.



OVEN OSCILLATOR A114

Figure 03/04/05-5. Time Base Calibration.

All frequency checks and adjustments should be made only after the oscillator has been connected to its power source for 24 hours. If the oscillator has been disconnected from its power source for more than 24 hours it may require 72 hours of continuous operation to achieve the specified frequency aging rate.

To measure oscillator frequency:

1. Connect the counter's internal oscillator output signal from the 10 MHz IN/OUT connector (on the rear panel of the counter) to the vertical input of the oscilloscope.

2. Trigger oscilloscope externally with the frequency standard. The VLF Comparator is used to determine the absolute frequency of the standard.

3. Set oscilloscope sweep rate to 0.1 μ sec/cm and expand X10; this results in a sweep rate of .01 μ sec/cm.

4. Adjust oscilloscope vertical controls for maximum gain.

5. Determine the frequency difference (see page 6-24).

6. Horizontal drift of oscilloscope display in μ sec/sec, is a measure of the difference between the frequency standard and the counter oscillator frequency. If the difference is excessive for the desired counter application, vary the TIME BASE ADJUST control on the rear panel of the counter until the pattern stops drifting.

NOTE

For highest accuracy, the counter should be operated
for 72 hours prior to adjustment.

OPTION 03/04/05 - TIME BASE OSCILLATOR PCB ASSYs 2020186 - B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A112	OSCILLATOR POWER SUPPLY	2020186	1	EIP	
C1	Elec, 680 uF, 40V	2200021	2	3074JH681T040JPB	80031
C2	C1				
C3	Tant, 10 uF, 25V	2300029	2	DF106M25S	NEC
C4	C3				
CR1	Bridge Rectifier	2710019	1	SBMB1	14099
CR2	Rectifier	2704001	1	IN4001	
R1	Met Ox, 3.3K, 2%	4130332	1	C4/2%/3.3K	24546
R2	Met Ox, 2K, 2%	4130202	1	C4/2%/2K	24646
R3	Met Ox, 560, 2%	4130561	1	C4/2%/560	24546
R4	Variable, Cer, 500, 10%	4250014	1	72XR500	73138
R5	Met Ox, 3.6K, 2%	4130362	1	C4/2%/3.6K	24546
U1	Positive Voltage Regulator	3040780	1	uA78MGUIC	07263
U2	Negative Voltage Regulator	3040790	1	uA79MGUIC	07263

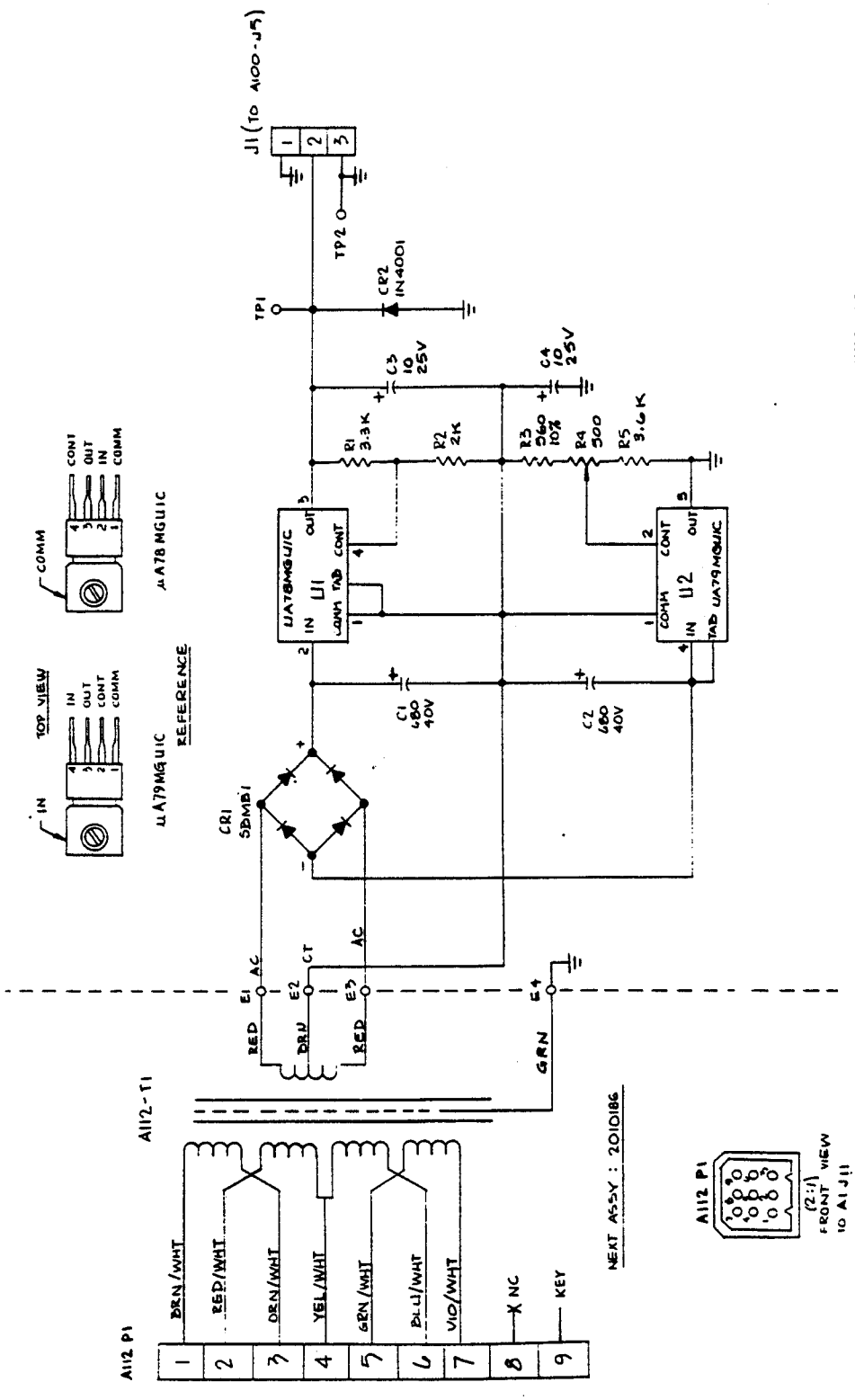


Figure 03/04/05-6. Time Base Option Schematic

OPTION 06
EXTENDED FREQUENCY CAPABILITY

The frequency range extension option is available on the 548A counter. This option, when used with the model 590 Frequency Extension Cable kit and one of the optional remote sensors, enables the counter to count signals above 26.5 GHz. The option consists of:

- Band 4 Converter Module, A204
- Band 4 Software
- Coax Cable, Front panel to A204 J1 - P/N 2040232
- Coax Cable, Front panel to A204 J2 - P/N 2040231

SPECIFICATIONS

BAND	FREQUENCY RANGE	SENSITIVITY (TYPICAL)	MAX. INPUT	REMOTE SENSOR MODEL
41	26.5-40 GHz	{ -25 dBm typ. } { -20 dBm min. }	+5 dBm	91
42	40-60 GHz	-25 dBm	+5 dBm	92
43	60-90 GHz	-25 dBm	+5 dBm	93
44	90-110 GHz	-25 dBm	+5 dBm	94

OPERATION

To operate the counter in the 26.5 - 40 range, connect the short cable (supplied with the frequency extension kit) from the lower output jack on the front panel, to the Band 3 input. Connect the long cable from the upper outjack to the remote sensor.

PRESS:	BAND	BAND annunciator blinks
PRESS:	4	BAND 4 annunciator blinks
PRESS:	1	BAND 4 annunciator lights stays on

The counter is now in the proper mode for operation.

NOTE: Before connecting the remote sensor to the frequency source, verify that the power level is within the limits specified for the sensor. When you connect the sensor the counter will automatically display the reading.

THEORY OF OPERATION – HARDWARE

When measuring a signal frequency greater than 26.5 GHz the 548A using the Option 06 Frequency Extension with a model 590 kit and a 91 remote sensor, down converts the input to approximately 1.0 GHz. This signal is then fed to the Band 3 input, where a second conversion produces a 125 MHz IF.

A multiplier chain increases the VCO output frequency to the 5.28–6 GHz range, which is referenced to the time base. See Figure 06-1. This signal provides the local oscillator (LO) power, which is transmitted to the remote sensor, an external harmonic mixer. When the input frequency and harmonics of the LO, (generated in the mixer) combine, a first IF is generated in the range of 1.00–1.35 GHz.

A diplexer separates the LO and IF signals received from the harmonic mixer. The level of the IF is then increased to a minimum of -25 dBm via the IF amplifier, then supplied to the Band 3 converter input.

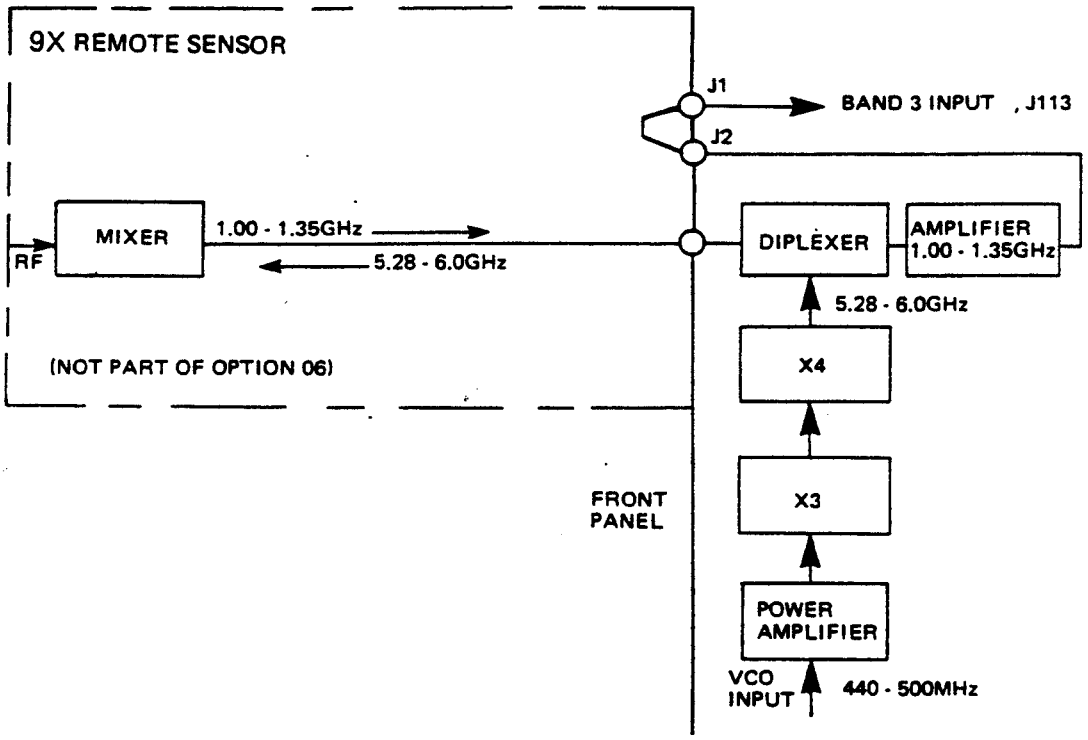


Figure 06-1. Frequency Extension Block Diagram

THEORY OF OPERATION – SOFTWARE

Band 4 acquires a signal by using a double conversion process. The microprocessor has control over the YIG filter and the VCO, thus making it possible to compute the approximate RF input signal, and down-convert the IF signal so it can be counted.

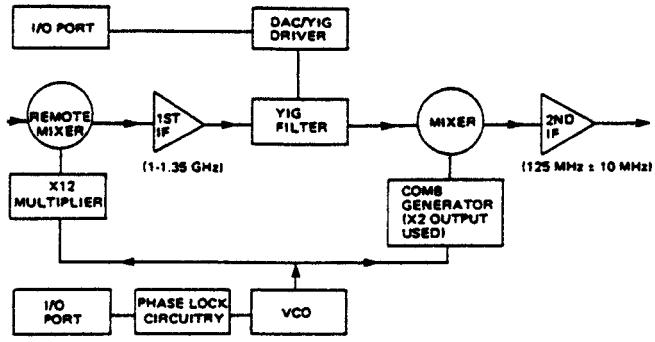


Figure 06-2. Down-conversion of Band 4 Signal

The following equations characterize this process.

$$\text{RF INPUT} = 12\,N\,F_{VCO} \pm \text{1st IF}$$

$$\text{1st IF} = 2\,F_{VCO} + \text{2nd IF}$$

therefore:

$$\text{RF INPUT} = \underbrace{F_{VCO}}_{\text{Controlled by Processor}}\ \underbrace{(12N \pm 2)}_{\text{calculated}}\ \underbrace{\pm \text{2nd IF}}_{\text{IF counted}}$$

Sign depends on hi/low side mixing to produce 1st IF.

Where N = the harmonic number which is mixing with the RF to produce the first IF.

There are two main functions that the Band 4 program performs. It locks on to an incoming RF signal, and tracks an RF signal once it is locked.

The locking routine is called by the supervisor when any of the following conditions are met.

1. Selection of Band 4
2. Loss of IF threshold after being locked
3. Any reset condition

The tracking routine is used under the following two conditions.

1. After locking, the tracking routine is used to "fine tune" the locked signal.
2. When the RF signal is moving, the tracking routine is used to give a constant update of corrected parameters so that the YIG filter and VCO can stay locked onto the signal.

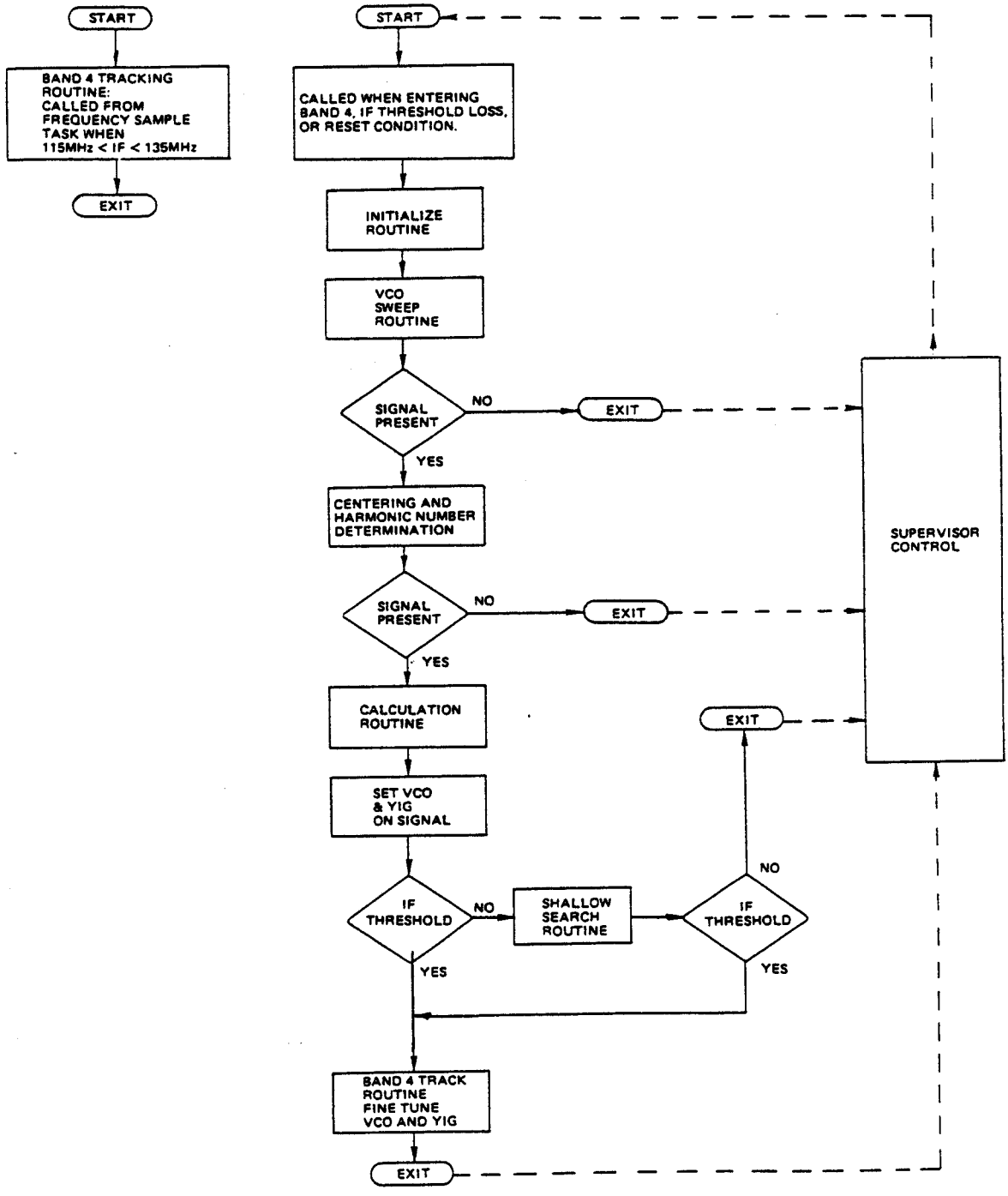


Figure 06-3. Band 4 Program, Flow Diagram

The process by which the program locks onto an RF signal is defined in the next six sections. Refer to Figure 06-3.

INITIALIZATION – The working table (BANDTP) for band 4 is cleared and the appropriate table of constants, used by the program for the particular Band 4 that has been selected, are loaded from PROM in this area. BANDTP is an area in RAM that is 27 bytes long.

VCO SWEEP – This routine steps the VCO frequency by a step size stored in BANDTP. After each step, the VCO frequency is checked for three stop points.

1. Top VCO frequency limit (500 MHz)
2. Wraparound frequency
3. Lockout frequency

If the top VCO frequency has been reached and no signal has been found, the program will return to the supervisor. If the top frequency is reached, and a signal has been detected, then the VCO is set to its low limit and the bottom range is searched until the wraparound frequency is reached.

If the wraparound frequency has been reached (the frequency at which the last VCO frequency has produced the strongest IF frequency), then the program will stay at this frequency, and will perform the centering and harmonic number determination routines.

If a lockout frequency (a VCO frequency at which erroneous locking results) is detected, the VCO frequency will be incremented by:

13 * STEP SIZE = NEW VCO FREQUENCY

and the program will continue from this frequency.

After each VCO step the YIG filter is swept to see if a signal is detected by the power DAC attenuator. If a signal was detected, the YIG is swept back and forth, and the attenuation is increased until the signal is lost. At this point a new VCO frequency is stepped and the process of signal detection continues, thus leaving the power DAC at the last setting to detect the next highest signal.

CENTERING AND HARMONIC NUMBER DETERMINATION – This routine will determine the harmonic number of the VCO which is causing the mix product to be in the proper range. (Refer to Figure 06-4).

First we obtain the proper step size for the calculation of the harmonic number (N). After the VCO sweep routine is complete and the VCO frequency is set, the incoming signal is mixed with a harmonic of the VCO frequency to produce a signal in a predetermined passband region. This signal is stepped to the outer edge of the passband (± step depending on whether the signal is high or low side mixed) by the following process.

1. Increment the VCO
2. Power level the IF signal
3. Center on the signal
4. Test for band limits

These steps are repeated until the edge of the passband is reached.

Harmonic Number N	Input Frequency Ranges	
	High Side Mixing (MHz)	Low Side Mixing (MHz)
5	25,395 – 28,875	27,405 – 31,125
6	30,675 – 34,875	32,685 – 37,125
7	35,955 – 40,875	37,965 – 43,125
8	41,235 – 46,875	43,245 – 49,125
9	46,515 – 56,875	48,525 – 55,125
10	51,795 – 58,875	53,805 – 61,125
11	57,075 – 64,875	59,085 – 67,125
12	62,355 – 70,875	64,365 – 73,125
13	67,635 – 76,875	69,645 – 79,125
14	72,915 – 82,875	74,925 – 85,125
15	78,195 – 88,875	80,205 – 91,125
16	83,475 – 94,875	85,485 – 97,125
17	88,755 – 100,875	90,765 – 103,125
18	94,035 – 106,875	96,045 – 109,125
19	99,135 – 112,875	101,325 – 115,125

Figure 06-4. Harmonic Mixing Ranges

Next the VCO is stepped back into the passband and a new centering takes place. This second center frequency is stored for later calculation of the harmonic number. Next the signal is stepped to the edge of the passband position it had just left, and it is centered. This center frequency is now compared to the first edge of the passband center frequency, and must be within 8 MHz. If it is not within 8 MHz it will be assumed that the signal is moving, and the Band 4 program is exited.

The IF frequency step size, caused by the VCO frequency step, is used to determine the harmonic number by the following equation.

$$\frac{\Delta \text{ IF FREQ. DUE TO VCO STEP}}{\text{HARMONIC SPACING}} = \text{HARMONIC \#(N)}$$

Where harmonic spacing = VCO step size X 12

CALCULATION ROUTINE – The calculation routine is used to find the approximate RF frequency Fin in the following manner.

1. Compute $F' = 12\,N * F_{VCO}$
2. Center the YIG filter on the first IF
3. Convert the binary YIG frequency to BCD
4. Compute $F_{IN} = F' \pm F_{YIG}$ (where F_{YIG} gives the approximate value for the first IF).
5. Compute a corrected VCO frequency using the equation:

$$F_{VCO} = (F_{IN} \pm 125) / (12N \pm 2)$$

Then tune the VCO with the corrected frequency and center the first IF frequency in the yig passband.

SHALLOW SEARCH – This routine tests for a signal in the IF passband. If a signal is present, the routine is exited. If a signal is not present, the routine will search an RF range of ±60 MHz (in steps of 200 kHz), for the signal, and continues if a signal is found. If a signal is not found, the Band 4 program returns control to the supervisor.

BAND 4 TRACKING – The tracking routine centers the second IF in the following range.

115 MHz <2nd IF SIGNAL <135 MHz

This routine is called from outside of the Band 4 program to track a signal. A test is first made to determine if an IF threshold is present. If IF threshold is present it continues, if not the program returns to the supervisor to start the locking process from the beginning.

This routine reads the second IF frequency and computes the new VCO frequency so that the second IF is in the range given above. A new YIG frequency is calculated and the VCO and YIG are "tuned" to produce a new IF. A new FLO (frequency added to the second IF to produce the displayed frequency), is calculated. The equation for this process is:

$$F_{LO} = F_{VCO} (12\ N \pm 2)$$

The YIG frequency is: NEW F_{YIG} = 2 (NEW VCO) + 125 MHz.

PERFORMANCE TESTS

The Band 4 converter module is not field repairable. When a malfunction is suspected, its operation can be checked from the front panel as follows:

IF AMPLIFIER — Apply a -50 dBm signal to the diplexer port (upper output jack) from 1.0 to 1.35 GHz. Output should be greater than -13 dBm as checked on a spectrum analyzer connected to the IF output (lower jack).

LO SIGNAL — Connect a spectrum analyzer to the diplexer port (upper output jack). Using the following formula, set the VCO frequency between 440 and 500 MHz. The spectrum analyzer should show the 12th harmonic of the VCO frequency (5.28-6 GHz). The spectrum analyzer signal should be +8 dBm minimum, and free of breakup and spurious signals to -30 dBc.

To convert from the desired VCO frequency to the PIA program number:

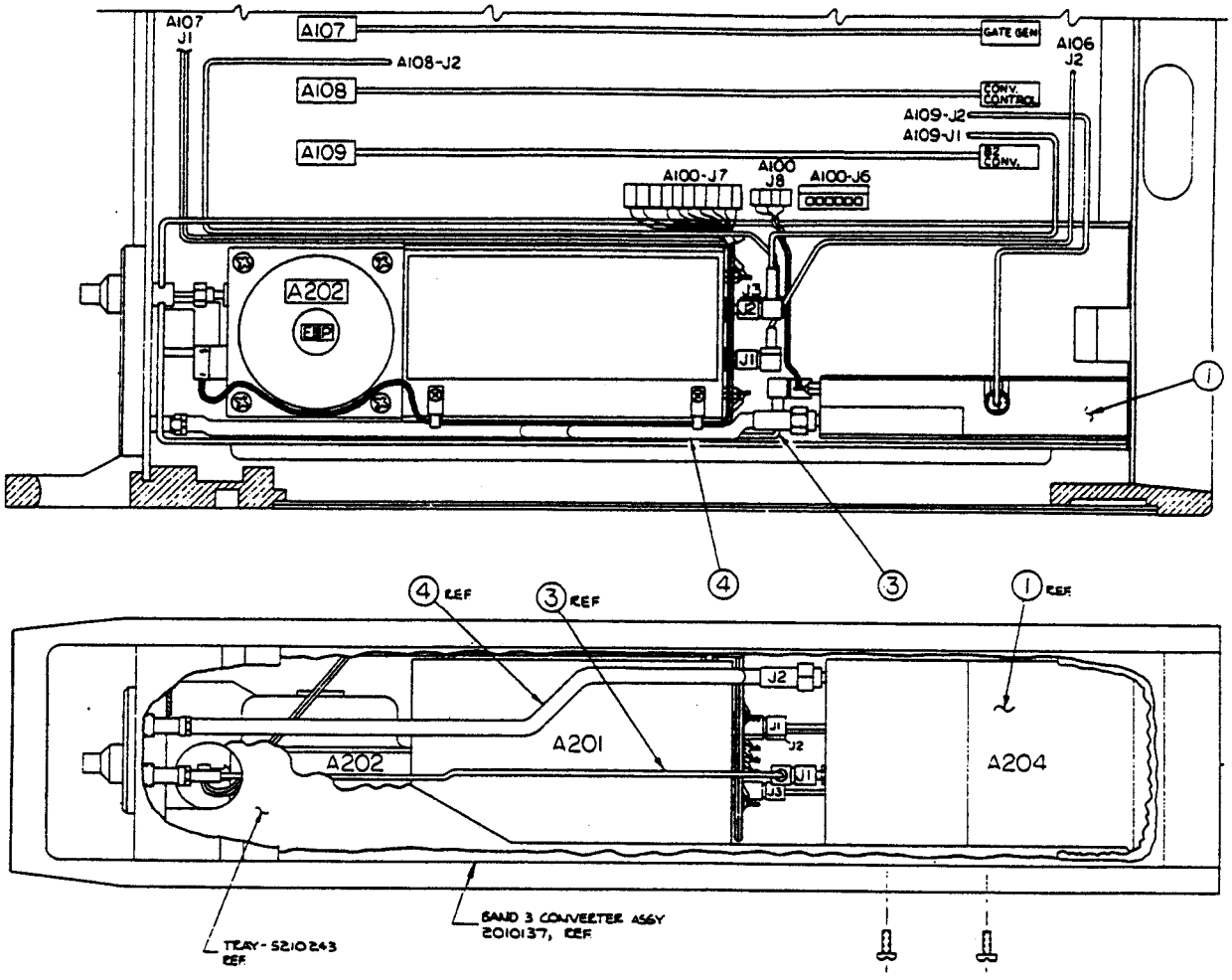
EXAMPLE (440.75 MHz)

1. Round the desired frequency to a multiple of 50 KHz (The resolution of the VCO frequency is 50 KHz).
2. Multiply the desired frequency (in MHz) by 5 . . . . . 440.75 X 5 = 2203.75
3. If the result contains no fractional part, go to step 8.
4. Multiply only the fractional part by 16 . . . . . .75 x 16 = 12
5. Add the result to the most significant digit from step 2 . . . . . MSD of 2203.75 = 2 – 2 + 12 = 14
6. Convert the result to hexadecimal . . . . . $14_{10} = E_{16}$
7. Replace the MSD from step 2 with the result from step 6 and drop the fractional part . . . . . 2203.75 → E203
8. The two most significant digits are programmed to address 9822, and the two least significant digits are programmed to address 9820.

To remove a defective converter:

1. Remove the line cord and both the top and bottom cover of the counter.
2. Remove the two screws holding the converter in place from the bottom.
3. Remove coaxial cables and unplug DC harness.
4. Lift the converter out of the counter.

To replace, proceed in the reverse order. See Figure 06-5 for location of the converter in the counter.



① Band 4 Converter – 2010229

③ Cable (FP to A204J1) – 2040232-01

④ Cable (FP to A204J2) – 2040231-01

Figure 06-5. Location of Installed Band 4 Converter (A204)

OPTION 07
REMOTE PROGRAMMING/BCD OUTPUT

This option makes it possible to use a conventional printer or other readout device, and remotely program the functions that are normally done on the front panel of the counter.

SPECIFICATIONS

BCD OUTPUT

FORMAT	11 digits plus sign in parallel
"0" STATE	0.4 Volts at 4mA
"1" STATE	2.7 Volts at -400μA
NEGATIVE REF.	Ground
POSITIVE REF.	+5 Volts at 2K Ω Source Impedance
PRINT COMMAND	20 μs wide TTL Low level logic signal
INHIBIT INPUT	2 to 50 Volts High level logic signal

REMOTE PROGRAMMING

INPUT LOADING	1 low power SchottkyTTL load plus 10K pull up to +5 Volts
FUNCTIONS	All front panel controls except: Power ON/OFF, Sample rate, Clear Display, and test functions greater than 01.
OUTPUT LEVEL	Refer to "0" State and "1" State for BCD.

OPERATION

BCD OUTPUT

This binary-coded decimal (BCD) output (plus sign information) represents any numerical data that would normally be displayed by the eleven digits on the front panel of the counter. When the information being displayed represents the frequency alone the minus sign refers to the frequency. When the information being displayed represents frequency and power the minus sign refers to the power.

A 20 microsecond print command is provided to indicate when the data is valid. An inhibit command is provided that will prevent the data from being altered.

BCD OUTPUT PIN CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	10^1 A	16	10^8 B	31	10^3 D	46	10^0 C
2	10^1 B	17	10^9 A	32	10^4 C	47	10^0 D
3	10^2 A	18	10^9 B	33	10^4 D	48	Print Command
4	10^2 B	19	10^{10} A	34	10^5 C	49	Minus Sign
5	10^3 A	20	10^{10} B	35	10^5 D	50	Ground
6	10^3 B	21	10^0 A	36	10^6 C		
7	10^4 A	22	Inhibit	37	10^6 D		
8	10^4 B	23	10^0 B	38	10^7 C		
9	10^5 A	24	–Ref.	39	10^7 D		
10	10^5 B	25	+Ref.	40	10^8 C		
11	10^6 A	26	10^1 C	41	10^8 D		
12	10^6 B	27	10^1 D	42	10^9 C		
13	10^7 A	28	10^2 C	43	10^9 D		
14	10^7 B	29	10^2 D	44	10^{10} C		
15	10^8 A	30	10^3 C	45	10^{10} D		

NOTE

The 10^0 bit is the least significant digit, and corresponds to the 1 Hz output.

A, B, C, and D are the 1, 2, 4, and 8 bits of each binary coded decimal output digit.

REMOTE PROGRAMMING

All front panel functions can be remotely programmed except the Power on/off, Sample Rate, Clear Display, and test functions greater than 01. All the inputs are activated by a ground contact closure, or a "0" level TTL signal (0 = true). The input load is equal to one low power Schottky TTL load plus a 10 KΩ pullup to +5 volts.

CONTROL LINE FUNCTIONS

REMOTE ENABLE – A low level on this line transfers counter control from the front panel keyboard to the rear panel remote programming connector.

INPUT DATA – A low level on this line initiates a data read cycle to read the function/program data contained on the 22 data input lines. If this line is held low the counter will continuously poll the input data.

DATA ACCEPTED – This signal is output from the counter to the controller. The line goes high when data is being read by the counter, and goes low upon completion of a data read cycle.

PROGRAM DATA – A low level on this line indicates that the 22 data lines will be interpreted as program data. A high level on this line indicates that these lines will be interpreted as function data.

DATA LINE FUNCTIONS

RESET COUNTER – A low level on this line will reset the counter and initiate a new search for a valid signal.

UPDATE READING – A low level on this line will cause the counter to take a new reading, update the front panel display, and update the BCD output.

BAND SELECT (3 lines) – These lines select the band, or Test 01, in accordance with the following:

C	B	A	BAND
0	0	0	Test 01
0	0	1	Band 1
0	1	0	Band 2
0	1	1	Band 3
1	0	0	Band 4.1*
1	0	1	Band 4.2*
1	1	0	Band 4.3*
1	1	1	Band 4.4*

*In counters that do not have Option 6, the C bit does not apply.

RESOLUTION (4 lines) – These lines program the remote resolution. A four digit BCD number (0 through 9) will indicate the number of digits that are blanked.

DAC SELECT (4 lines) – These lines select the most significant digit of the DAC option (01), when it is installed in the counter. A hexadecimal number (1 to B) will select digit 1 to 11 as the MSD of the 3 digits output to the DAC. Any other digit disables the DAC option.

HOLD MODE – A low level on this line will place the counter in the hold mode (data not updated until the counter is reset).

FAST CYCLE – A low level on this line will place the counter in the fast cycle mode (no display time).

POWER METER – A low level on this line will enable the power meter on counters with Option 02.

VIEW FUNCTION LINES (5 lines) – A low level on one of these lines will cause the counter to display the indicated function on the front panel and the BCD output. If more than one line is enabled at a time, the counter will display the first one found in the following order.

1. DAC Select
2. Frequency Limit Low
3. Frequency Limit High
4. Frequenty Offset
5. Power Offset

PROGRAM LINE FUNCTIONS

PROGRAM SELECT (2 lines) – These two lines select one of four functions to be programmed by the program data in accordance with the following.

SELECT b	BIT a	FUNCTION PROGRAMMED
0	0	Frequency limit low
0	1	Frequency limit high
1	0	Frequency Offset
1	1	Power Offset

MINUS SIGN – When this line is low the four digits of programming data are interpreted as a negative number.

EXPONENT (3 lines) – These three lines are interpreted as a BCD number (0 to 7). This number is the power of 10 that is to be multiplied, times the four digits of data (data X 10^X). This multiplier is used for all frequency input data, and is ignored for the power input data.

DIGIT 1 TO DIGIT IV (4 lines each) – These are four BCD digits that represent the input data. Digit 1 is the MSD and Digit IV is the LSD. For power input, a decimal point is located between Digit II and Digit III, and Digit IV is not used.

DATA ENTRY

Preceeding any data entry sequence, the counter must be placed in the remote mode (remote enable line low). Once in remote mode, the input data line is brought low to initiate a data read sequence. The data read is normally function data. When the program data line is brought low, the data read will be interpreted as program data. The data accept line will go high to indicate that the data has been latched in, and will remain high while the counter processes this data.

Figure 07-1 shows the data entry timing sequence. The input data line debounce time (1) is typically 16 to 18 ms. Data is latched into the counter 48 μs before the data accept line goes high (2). As soon as the data accept line goes high, all data (except remote enable) can be removed. The data accept line stays high while the counter processes the input data. This process is data dependent, and can take from 1 to 140 ms (3). To prevent the counter from setting the poll mode, the input data line must go high within 100 μs after the data accept line goes low (4). If poll mode is set, the next data read cycle will occur between 0 and 100 ms after the high to low transition of the data accept line. After this first data read cycle, all subsequent data read cycles will occur at 100 ms intervals.

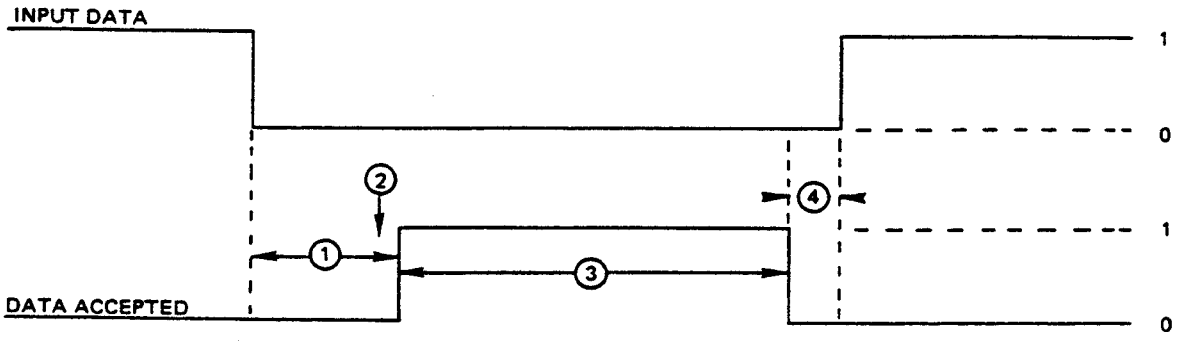


Figure 07-1. Data Entry Timing

DATA ENTRY EXAMPLE

The following example remotely programs the counter to be in Band 3 with 1 kHz resolution, and a -160 MHz frequency offset.

1. Put counter in remote mode by bringing the remote enable line low.
2. Set the program data to be entered by bringing the program data line low.
   a. Set digit 1=1
      Set digit 2=6
      Set digit 3=0
      Set digit 4=0
   b. Set the exponent =5 (1600×10^5)
   c. Set program select A=0, B=1 (frequency offset)
   d. Set minus sign low (negative offset)
3. Enter program data by bringing the input data line low until the data accept line goes high.
4. Set the remote function data.
   a. Return all lines high except the remote enable line.
   b. Set the resolution A and B lines low (resolution 3).
   c. Set the Band select C line low (Band 3).

   NOTE: Counters that do not have Option 06 (Band 4) will set Band 3, even with the select line C high.
5. Enter function data by bringing the input data line low until the data accept line goes high.

REMOTE PROGRAMMING PIN CONNECTIONS

PIN	FUNCTION DATA	PROGRAM DATA
1-5	BCD Data (Do not use these pins)	
6-12	Ground	
13	DAC Select A	Digit II A
14	DAC Select B	Digit II B
15	DAC Select C	Digit II C
16	DAC Select D	Digit II D
17	Resolution A	Digit I A
18	Resolution B	Digit I B
19	Resolution C	Digit I C
20	Resolution D	Digit I D
21-24	No connection	
25	Program Data)	Program Data)
26	Remote Enable) Control Lines	Remote Enable) Control Lines
27	Input Data)	Input Data)
28	Data Accepted)	Data Accepted)
29	View Power Offset	Digit IV A
30	View Frequency Offset	Digit IV B
31	View Frequency Limit High	Digit IV C
32	View Frequency Limit Low	Digit IV D
33	View DAC Select	Digit III A
34	Power Meter Enable	Digit III B
35	Fast Cycle Mode	Digit III C
36	Hold Mode	Digit III D
37	Ground	Ground
38-44	No connection	
45	Band Select A	Exponent A
46	Band Select B	Exponent B
47	Band Select C	Exponent C
48	(No function)	Minus Sign
49	Update Reading	Program Select A
50	Reset Counter	Program Select B

THEORY OF OPERATION

The BCD/REMOTE programming board takes data from the display and formats it as parallel data output for the rear panel. It also receives counter control and programming information from the 26 line input on the rear panel to provide for remote control of the counter.

BCD THEORY OF OPERATION

During each update cycle, the counter checks for the existence of the BCD/RMT board. If the board exists, the program checks the state of the inhibit input. If the inhibit input is true (+2 to +50V on the input), the program jumps past the BCD output but the counter continues to update the display. If the input is low, the program scans through each of the 11 digits (LSB to MSB). Each digit is checked, and any non-numerical digit is replaced by a zero. The resulting BCD digit is then sent to U2 through 4 bits of port B of the PIA (U14). After each digit is made available to U2, 4 clock pulses (BCD Clock) are sent to U2 (through U7) to shift all the data in the shift registers to the right by 4 bits (1 digit). At the end of these data shift pulses, a BCD load pulse enters the new data into U2. When the last digit (MSB) is entered into U2, the sign bit is simultaneously entered into U1. After all the data has been entered into the shift register, the program sends out a 20 microsecond print command.

REMOTE PROGRAMMING THEORY OF OPERATION

When the remote enable line is high, none of the other remote programming lines can effect the counter. When the remote enable line is brought low, the counter changes from local to remote operating conditions and switches control for the counter from the front panel keyboard to the rear panel remote programming connector. When in the remote mode, the counter waits for an input from the INPUT DATA request line. When the input data line is brought low, the data direction control line is sent low to put U9 in the low impedance buffer mode. The RMT LOAD line is then toggled to load all remote input data into the input registers (U8-U12). The counter then changes the data accepted output from a low to a high to indicate that the data has been read. The 8 bits of data into U14 (from U8 and U10), are read by the microprocessor. Groups of 4 clock pulses are then sent out (on the RMT CLOCK line), to shift the input data into U10 where the data is read by the microprocessor through U14. When all the data has been read, the data direction control line is returned to a high level, and the data accept line is returned to low, indicating the data has been accepted by the counter.

When the INPUT DATA line is held low, the counter sets a flag and returns to read the input data at approximately 100 millisecond intervals. This continues until the INPUT DATA line is returned to high, at which time the counter returns to the condition where it is waiting for a high to low transition on the INPUT DATA line.

When the remote enable line is returned to the high state (local mode), the counter exercises a clear display function and then returns to the (previous) local mode condition.

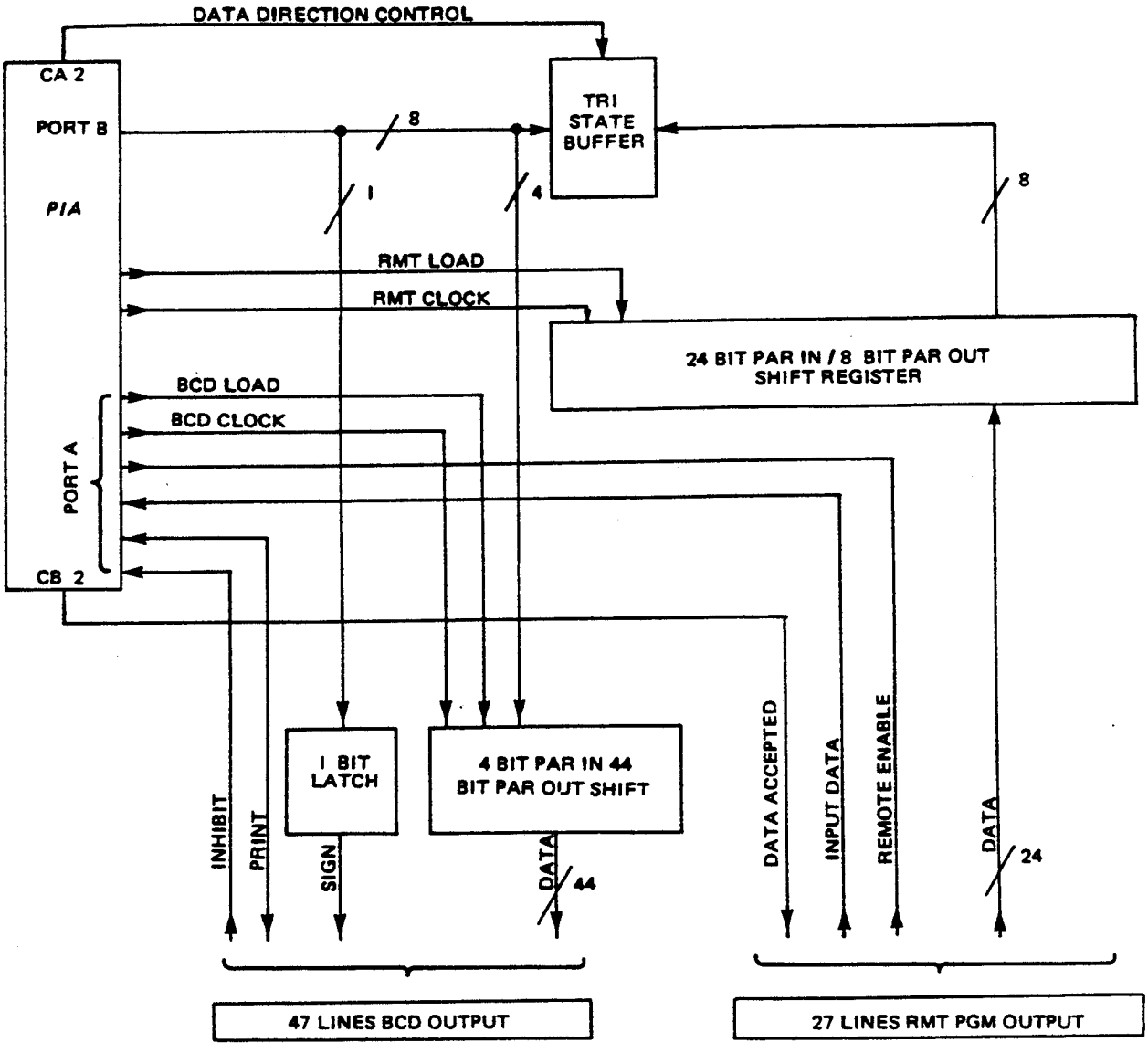


Figure 07-2. Remote Programming/BCD Output Simplified Block Diagram

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OPTION 07 - REMOTE PROGRAMMING / BCD OUTPUT

2020132 - E

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
07	REMOTE PROGRAMMING / BCD , PCB	2020132		EIP	34257
-1	Bail Mount Kit	5000195	1	3475-1	76381
-2	Cable, Flat Ribbon (to A100 J2, J3)	2040176-01	2		
-3	PCB Assy, A102 A	2020132	1	EIP	
C1	Tant, 33uF, 10%, 10V	2300015	1	TAG-20-33/10-50	14433
C2 thru C5	Cer, .01uF, 20%, 100V	2150003	4	TAG-S10	56289
Q1	Transistor, NPN	4704401	1	2N4401	04713
R1	Comp, 1 K, 5 %, ¼ W	4010102	1	RC07GF102J	81349
R2	Comp, 5.6K, 5%, ¼ W	4010562	4	RC07GF562J	81349
R3	Comp, 10K, 5%, 1/8 W	4010103	1	RC07GF103J	81349
R4	R2				
R5	Comp, 2.7K, 5%, ¼ W	4010272	2	RC07GF272J	81349
R6	R5				
R7	R2				
R8	R2				
RN1 thru RN3	Network, 10 pin , 10K, 2%, 1.25W	4170003	3	4310R-102-56	32997
TP1 thru TP11	.040 Dia. Conn. Pin	2620032	11	460-2970-02-03	71279
U1	4 bit Shift Register	3084195	4	DM74LS195	01295
U2	U1				
U3 thru U7	8 Bit Parallel OUT Register	3074164	5	DM74164	01295
U8	U1				
U9	Line Driver/Octal Buffer Inverter	3084244	1	SN74LS244N	01295
U10	U1				
U11	8 bit Shift Register	3084166	2	74LS166	01295
U12	U11				
U13	Hex Inverter/Schmitt Trig.	3087414	1	DM74LS14N	01295
U14	P.I.A.	3086821	1	MC6821	04713

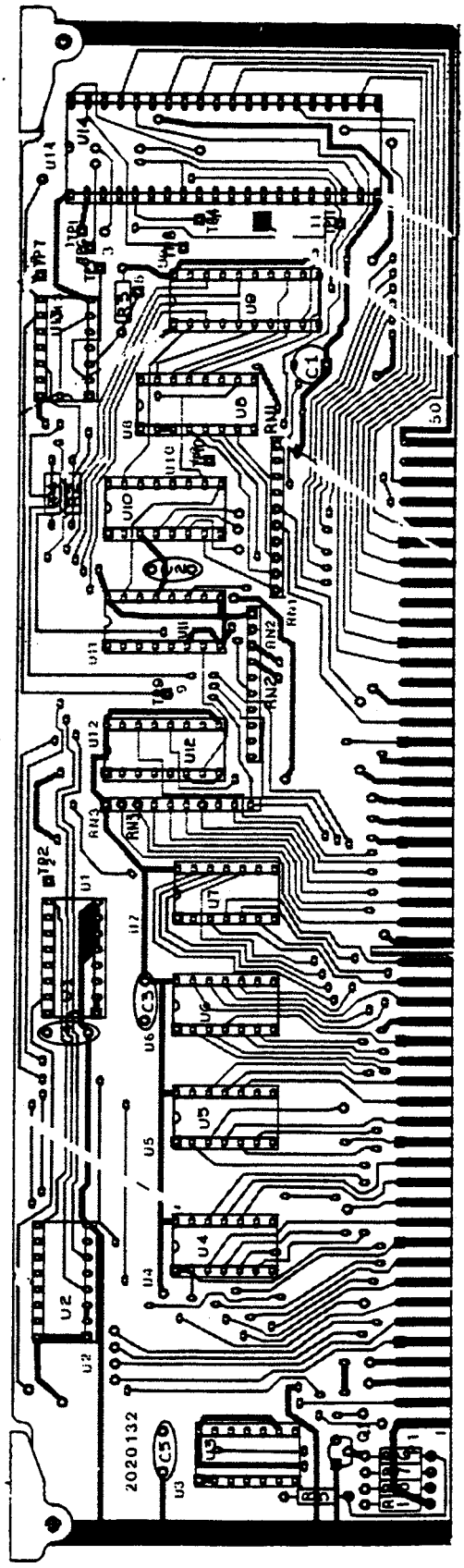


Figure 07-3. Remote Programming / BCD Output, Component Locator

OPTION 08

GENERAL PURPOSE INTERFACE BUS

Option 08 makes 545A/548A microwave counters fully compatible with the General Purpose Interface Bus (GPIB). With this option the counter can respond to remote control instructions and can output measurement results via the IEEE 488-1978 Bus interface. At the simplest level the counter can output data to other devices such as the HP 5150A Thermal Printer. In more sophisticated systems a calculator or other system controller can remotely program the counter, trigger measurements, and read results. Of course, a calculator or computer adds other benefits to a GPIB based measurement system. The calculator can manipulate data to compute the mean and standard deviation, check for linearity, and compare results to limits, or perform many other functions.

GPIB FUNCTIONS IMPLEMENTED

The GPIB interface function subsets implemented are:

SH1	complete capability
AH1	complete capability
T5	basic talker, serial poll, Talk Only mode, unaddress if MLA
L3	basic listener, Listen Only mode, unaddress if MTA
SR1	complete capability
RL1	complete capability
DC1	complete capability
DT1	complete capability

NOTE

When DEVICE CLEAR or SELECTED DEVICE CLEAR GPIB bus command is received, the counter will revert to the power on state. When DEVICE TRIGGER GPIB bus command is received, the counter will initiate a new frequency reading cycle. The converter will not be reset. When counter is in REMOTE the RESET key, on the front panel keyboard, acts as the RETURN to LOCAL key.

SETTING ADDRESS SWITCH

The counter employs a decimal address switch locate on the top edge of A102. It is set for decimal address 19 at the factory. To verify the switch setting without removing the top of the counter, simply initiate test 10; enter 9C04 and read the address on the display. A description of test 10 can be found on page 6-7. After reading the address, terminate the test by pushing the clear display key.

The address switch is also used to put the counter in the Talk Only (TO) or Listen Only (LO) mode. To put the counter in the Listen Only mode simply set the address switch to 41 or any number higher.

The counter can be put in four different modes of operation in the Talk Only mode. The following is a list of the address settings for entering these modes.

ADDRESS	MODE OF OPERATION
32	Continuous output determined by SAMPLE RATE control. Exponent in scientific format.
33	Continuous output - fast active. SAMPLE RATE control inactive. Exponent in scientific format.
34	Continuous output determined by SAMPLE RATE control. Exponent in zero output format.
35	Continuous output - fast active. SAMPLE RATE control inactive. Exponent in zero output format.

NOTE

In the Talk Only or the Listen Only mode, the address of the counter is always automatically set to decimal 0.

DEVICE DEPENDENT DATA INPUT

It takes a specific amount of time for the counter to process the input data (error checking, formatting, changing the mode of operation, etc.). To prevent the data rate of the bus from slowing down while the counter is doing input data processing, the data is accepted as soon as it is available on the bus, and it is temporarily stored in memory. The size of the storage memory is 100 characters.

The users of the GPIB option need to be aware that there is a difference between accepting data and complying with it. If the counter is asked to output a reading before it has finished processing the input data, the output will be in error if the operator makes the assumption that the counter is in the mode that was just programmed. To prevent this, sufficient programmed delays must be provided, or use must be made of the counter's Service Request status byte. See Service Request (SR) command description.

GPIB INSTRUCTION FORMAT

<OP CODE> <NUMBER> <TERMINATOR>

OPERATION CODE or OP CODE can take any of the following formats:

<LETTER> <LETTER> or <LETTER> <DIGIT>

Example: FH (Frequency limit high) or B3 (band 3)

The NUMBER portion of the statement can take the form of any of the following:

<SIGN> <DIGIT STRING>

Example: −2457

<SIGN> <DIGIT STRING> • <DIGIT STRING>

Example: −3.483

NOTE: Spaces within the <OP CODE> and <NUMBER> portions of the instructions are always ignored.

The TERMINATOR allows the operator to choose the scale of an input number as well as implement special functions.

TERMINATOR = G/M/K/H/D/P/C

G, M, K, H, represent GHz, MHz, kHz and Hz respectively.
D = dB, P = clear data, (equivalent to "clear data" key on keyboard)
C = clear display (equivalent to "clear display" key on keyboard)

FORMAL DEFINITION OF INSTRUCTIONS

<OP CODE> <NUMBER> <TERMINATOR>

<OP CODE> ::= <LETTER> <LETTER> | <LETTER> <DIGIT>

<NUMBER> ::= <SIGN> <DIGIT STRING> |
<SIGN> <DIGIT STRING> • <DIGIT STRING> |
NULL

<TERMINATOR> ::= G | M | K | H | D | P | C | NULL

<SIGN> ::= + | − | NULL

<DIGIT STRING> :: <DIGIT> <DIGIT> <DIGIT>·····

<LETTER> ::= A | B | C | D | E | F | G | H | I | J | K | L | M | N |
O | P | Q | R | S | T | U | V | W | X | Y | Z

<DIGIT> :: = 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0

PROGRAM CODE SET

Codes underlined indicate start-up conditions. These conditions are set by the device clear or selected device clear, or power on.

DISPLAY

DA – Display Active: Output Frequency Reading to Front Panel and Bus
DP – Display Passive: Output Frequency Reading to Bus only
DN – Display Normal

BAND

B1 – Band 1: 10Hz - 100MHz
B2 – Band 2: 10MHz - 1GHz
B3 – Band 3: 1GHz - 18GHz (Model 545A) / 26.5GHz (Model 548A)
B4 – Band 4: (Model 548A / Option 06)

RESOLUTION

R0 – Resolution 0 = 1Hz
R1 – Resolution 1 = 10Hz
R2 – Resolution 2 = 100Hz
R3 – Resolution 3 = 1KHz
R4 – Resolution 4 = 10KHz
R5 – Resolution 5 = 100KHz
R6 – Resolution 6 = 1MHz
R7 – Resolution 7 = 10MHz
R8 – Resolution 8 = 100MHz
R9 – Resolution 9 = 1GHz

MEASUREMENT FUNCTIONS

FA – Fast Active (Ignore sample rate Pot)
FP – Fast Passive (Terminates FA)
RS – Reset Basic Counter and Converter. Take a new reading after reset.
HA – Hold Active
HP – Hold Passive

DATA MANIPULATION FUNCTIONS

FO – Frequency Offset. Take a new reading after data entry if counter not in hold.
PO – Power Offset. Take a new reading after data entry if counter not in hold.
*OA – Offset Active:
—Add Frequency Offset to Frequency Reading
—Add Power Offset to Power Reading if Power Meter Function is active
OP – Offset Passive (Terminates OA)
ML – Multiplier. Multiplies frequency readings by an integer number.

*In Start-up Condition, although OA is Active, "0" (zero) Frequency and Power Offsets are programmed.

POWER METER

PA – Power Meter Option Active. Initiate a new gate.
PP – Power Meter Option Passive (Terminates PA)

***MEASUREMENT PARAMETERS**

FH – Frequency Limit High. Basic counter and converter will be reset after data entry.
FL – Frequency Limit Low. Basic counter and converter will be reset after data entry.

SELF-TEST FUNCTIONS

TA – Test Active.
TP – Test Passive. (clear test function)

DATA FORMAT

EZ – Exponent Zero
ES – Exponent Scientific

DATA OUTPUT

BR – Output both frequency and power readings
FR – Output frequency readings only
PR – Output power readings only

SERVICE REQUEST

SR – Service request enable

DAC OPTION

DC – Select DAC option

*Measurement parameters: Standard Software
Limits of 950MHz (LOW) and 18.5GHz (HIGH) (27GHz for Model 548A) are featured in each counter at turn on.

DESCRIPTION OF AVAILABLE COMMANDS

DISPLAY

DA - Display Active - Outputs readings to both front panel and GPIB bus

DP – Display Passive - Outputs readings to GPIB bus only. It will decrease the cycle time of the counter.

DN – Display Normal - Resets display only; used for clearing error messages on the display. Cannot be used after verifying preprogrammed data such as Frequency Offsets or Frequency Limits. This OPCODE affects only the display.

BAND

B1 – Selects Band 1

B2 – Selects Band 2

B3 – Selects Band 3

B4 – Selects Band 4. Requires an additional digit input to designate individual remote sensors.

Example: B41 = remote sensor 1 which covers range of 26.5 to 40GHz.

RESOLUTION

R0 thru
R9 – Resolution 0 thru 9 - Picks the front panel resolution from 1Hz to 1GHz. Also chooses gate time which is related to resolution: 1Hz = 1 Sec, 10Hz = 100 Sec. 100Hz = 10 msec. 1kHz to 1GHz = 1 msec.

MEASUREMENT FUNCTIONS

FA – Fast Active - Causes the counter to go into the fast cycle mode of operation. In this mode, the front panel sample rate/hold control is inactive and the fastest sample rate is attained. The counter will not go into the Fast Active mode of operation until Hold Active is disabled.

FP – Fast Passive - Terminates FA.

RS — Reset Basic Counter and Converter - Re-acquires input signal and takes a new reading. Has the same function as manual reset button.

HA — Hold Active - The counter stops taking readings and the last frequency and power readings are displayed and held. The counter can be directed to take one reading when it is in this mode by sending Device Trigger or Selected Device Trigger GPIB bus command to the counter. It will also update the reading if the RS mnemonic is received.

HP — Hold Passive - Terminates HA.

DATA MANIPULATION FUNCTIONS

FO — Frequency Offset - Enables entry of frequency offsets. (1 Hz resolution available.) A new gate will be initiated after data entry if counter is not in HOLD.

PO — Power Offset - Enables entry of power offsets. Take a new reading after data entry if counter is not in HOLD.

OA — Offset Active - Add frequency offset to frequency readings. Add power offset to power readings if power meter function is active.

OP — Offset Passive - Does not add frequency and power offset to readings.

ML — Multiplier - Enables entry of a 2-digit frequency readings multiplier. The multiplier must be an integer between 00 and 99. The results are to 1kHz resolution. A new reading will be initiated after the data entry if the counter is not in HOLD. If the results of the multiplications are larger than, or equal to 999.999999999GHz, the counter will output 999.999999999GHz to the bus if asked to output readings.

POWER METER

PA — Power Active - Enables power meter option.

PP — Power Passive - Terminates power meter option.

MEASUREMENT PARAMETERS

FH — Frequency Limit High - Enables entry of frequency limit high (10 MHz resolution available). The basic counter and converter will be reset after the data entry.

FL — Frequency Limit Low - Enables entry of frequency limit low (10 MHz resolution available). The basic counter and conveter will be reset after the data entry.

SELF-TEST FUNCTIONS

TA — Test Active - Enables the counter to perform the selected test function by entering the mnemonic TA followed by two digits. When Test 05, 08, 09, or 10 is active and the counter is being asked to output data, the data that is displayed on the front panel is the data being output.

The output data format is as follows:

XXXXXXXXXXXXCRLF

X = alpha-numeric
CR = carriage return
LF = line feed

For detailed descriptions of tests 01 through 09 and test 11, see the section on Keyboard Controlled Circuit Tests.

Test 10 operates in the following manner:

1. To activate Test 10 input TA10.
2. To read the data stored in a specific memory location, input the address of the memory location in a four digit hexadecimal number. Enable the counter to talk and then read data from the counter.
3. To alter the data stored in a certain memory location:

   If 2. has been performed - input the desired data for that memory location.

   If 2. has not been performed - input the memory address, followed by a two digit hexadecimal number.

TP — Test Passive - Terminates test function.

DATA FORMAT

EZ – Exponent Zero - output format.

ES – Exponent Scientific - output format.

DATA OUTPUT

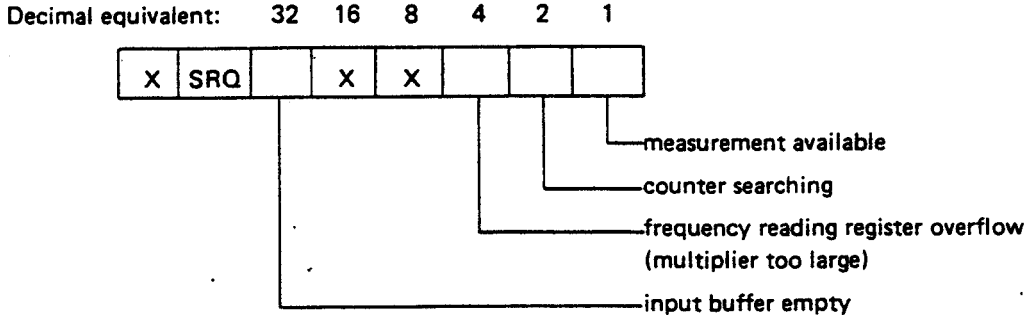
BR – Output both frequency and power readings. (See section on output data format.)

FR – Output frequency readings only. (See section on output data format.)

PR – Output power readings only. (See section on output data format.)

SERVICE REQUEST

SR – Service Request Enable - Enables the counter to send Service Request to the bus when a certain event has taken place in the counter. To enable the function, input SR followed by two decimal digits. The two digits are the decimal equivalent of the content of the eight bit status register. More than one bit of the status register can be set.



To disable the Service Request function, input SR00.

NOTE

Even when the Service Request function is disabled, the Service Request status byte will still be continuously altered to reflect the internal states of the counter.

EXAMPLE: To enable service request on measurement available or input buffer empty, send SR33.

DAC OPTION

DC – DAC Option - Enables the DAC option to convert three consecutive digits to an analog voltage, available on the rear panel. The output will reflect the display, and zeros are substituted for any non-numeric characters that appear. The output will be updated after every display update.

DC00 – turns DAC option off
DC01 – selects 1 Hz digit
thru
DC12 – selects 100 GHz, 10GHz and 1 GHz digits.

DATA OUTPUT FORMAT

The 545A/548A transmit the following string of characters to output a measurement.

Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Format																		
EZ (Exponent Zero)	␣	±	D	D	D	D	D	D	D	D	D	D	D	D	E	0	CR	LF
ES (Exponent SCI)*	±	D	D	D	D	D	D	D	D	D	D	D	D	D	E	D	CR	LF
Power**	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	±	D	D	D	.	D	CR	LF

Freq. + Power

- FREQ in EZ mode: ␣ ± D D D D D D D D D D D E 0 , ␣␣␣␣␣␣␣␣␣␣ ± D D D . D CR LF
- FREQ in ES mode: ± D D D D D D D D D D D D E D , ␣␣␣␣␣␣␣␣␣␣ ± D D D . D CR LF

When the counter is in Test 05, 08, 09, or 10, the output will reflect the data on the display. The format is as follows:

XXXXXXXXXXXXCRLF.

␣ = Blank
D = Digit
X = Alpha-numeric
CR = Carriage Return
LF = Line Feed

*in Exponent Scientific one digit represents the position of the decimal point. Exponent digit can be either 0, 3, 6, or 9.

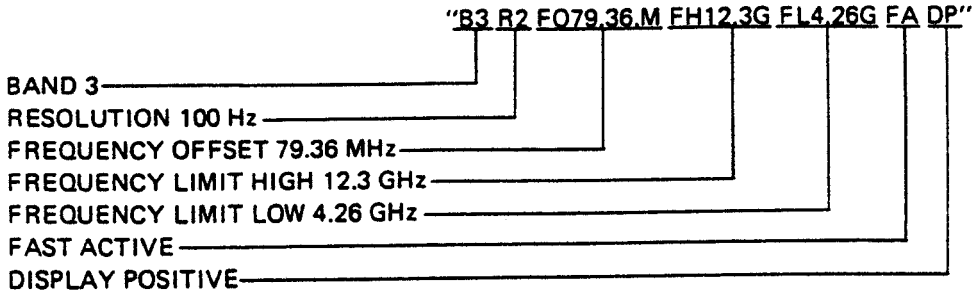
**The power information always have the decimal point fixed for 0.1dB resolution.

Under different output modes, the following counter outputs can be expected by a listener.

OUTPUT MODE	COUNTER OPERATING MODE	OUTPUT
BR	PA	FREQ + PWR
	PP	FREQ
	TA01	FREQ
FR	PA	FREQ
	PP	FREQ
	TA01	FREQ
PR	PA	PWR
	PP	–999.9
	TA01	–999.9
BR, FR or PR	TA 05, 08, 09, or 10	Data on front panel display

PROGRAM EXAMPLES

The examples given here assume an address setting of decimal 19 or ASCII talk address "S" and listen address "3" for the counter. By addressing the counter to listen and sending the following program string, it sets up the following measurement conditions.



The following programs illustrate how controllers function with the counter. These programs cause the counter to make a series of frequency measurements. The calculators read the measurements into memory and print the results. The programs assume the counter Talk and Listen address is decimal "19."

```
HP 9825A    0:   dim A (10)
            1:   rem 7
            2:   wrt 719, "B3R2FO-4.55M"
            3:   wait 300
            4:   for I = 1 to 10
            5:   red 719, A (I)
            6:   prt A (I)
            7:   next I
            8:   end
HP 9845A    10:  output 719, "B3R2FO-4.55M '
            15:  wait 300
            20:  input 719, A
            30:  print "Frequency minus offset equals," A
            40:  Go to 20
TED 4051    10:  print @19: "B3R2FO-4.55M"
            20:  input @ 19: A
            30:  print "Frequency minus offset equals," A
            40:  Go to 20
```

The 9825A program will cause the counter to take a series of ten readings, print them on the 9825A paper tape and stop. Notice that an offset of 4.55 MHz is subtracted from each reading.

The program shown for the 9845A and TEK 4051 cause the counter to make a frequency measurement and print that measurement. To end the program, initiate a "STOP" command. This is accomplished on the 9845A with the key labeled "STOP." On the TEK 4051 use the key labeled "BREAK." To restart the program enter the RUN statement followed by the line number that is printed in the INTERRUPT message.

READING A MEASUREMENT

To read a measurement from the counter to a calculator, the counter must first be addressed to talk and the calculator to listen. The examples below indicate how a calculator may read a measurement from the counter.

HP 9825A

```
10 red 719, A
20 prt A
```

TEK 4051

```
10 input @ 19:A
20 print A
```

HP 9845A

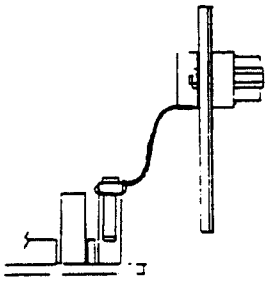
```
10 enter 719, A
20 print A
```

The EIP counters can use two different modes. HA which takes one reading then waits for a reset command or a Device Trigger GPIB Bus Command. In this condition the counter is sent a reset or Device Trigger and (when addressed to talk) a new reading is output to the BUS. The counter will hold that particular reading on the display until another reset command or Device Trigger command is received. The other mode is HP or HOLD PASSIVE. In this mode data is read out in a normal BUS fashion. The display automatically updates corresponding to the sample rate chosen. In this condition successive readings can be output without generating a reset or Device Trigger command each time.

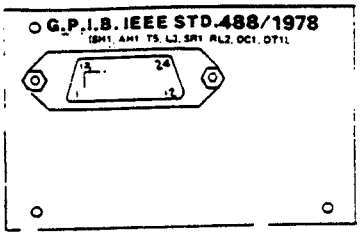
ADDRESS CHARACTERS		ADDRESS CODES					
Listen	Talk	binary 5	4	3	2	1	decimal *
SP	@	0	0	0	0	0	00
!	A	0	0	0	0	1	01
"	B	0	0	0	1	0	02
#	C	0	0	0	1	1	03
$	D	0	0	1	0	0	04
%	E	0	0	1	0	1	05
&	F	0	0	1	1	0	06
'	G	0	0	1	1	1	07
(	H	0	1	0	0	0	08
)	I	0	1	0	0	1	09
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
,	L	0	1	1	0	0	12
–	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
0	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26
;	[	1	1	0	1	1	27
<	/	1	1	1	0	0	28
=	]	1	1	1	0	1	29
>	^	1	1	1	1	0	30

* Decimal Talk/Listen Address is provided as a cross reference for those controllers which use decimal address.

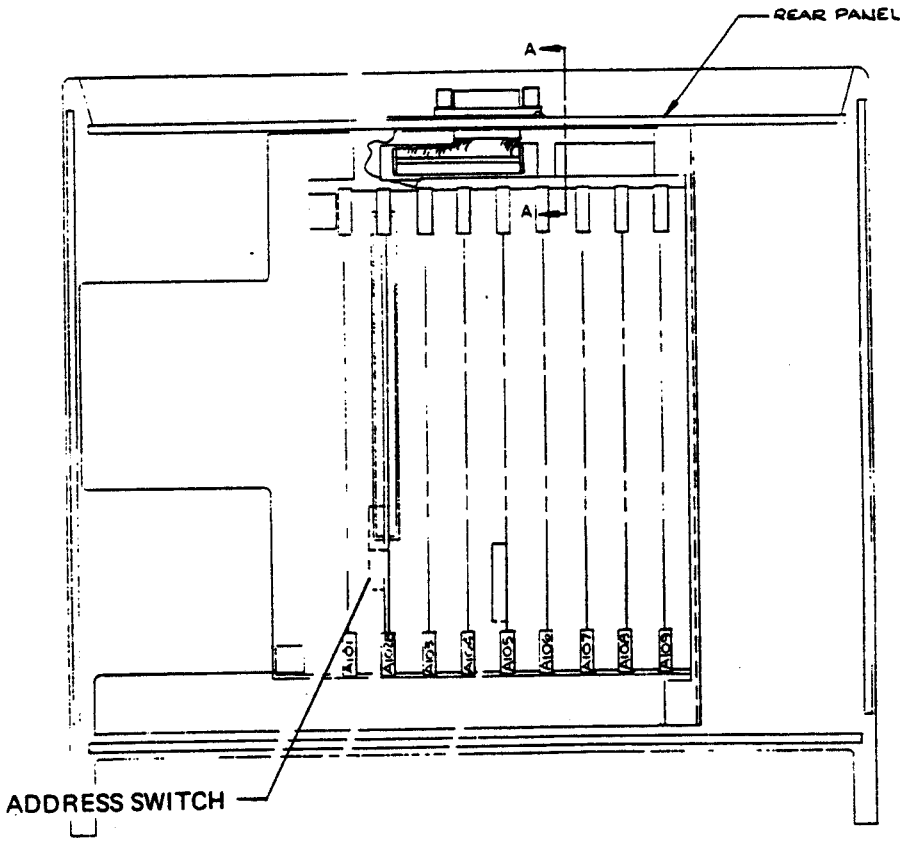
Figure 08-1. Allowable Address Codes



DETAIL A-A



CONTACT	SIGNAL LINE	CONTACT	SIGNAL LINE
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	GND. (6)
7	NRFD	19	GND. (7)
8	NDAC	20	GND. (8)
9	IFC	21	GND. (9)
10	SRQ	22	GND. (10)
11	ATN	23	GND. (11)
12	SHIELD	24	GND. LOGIC



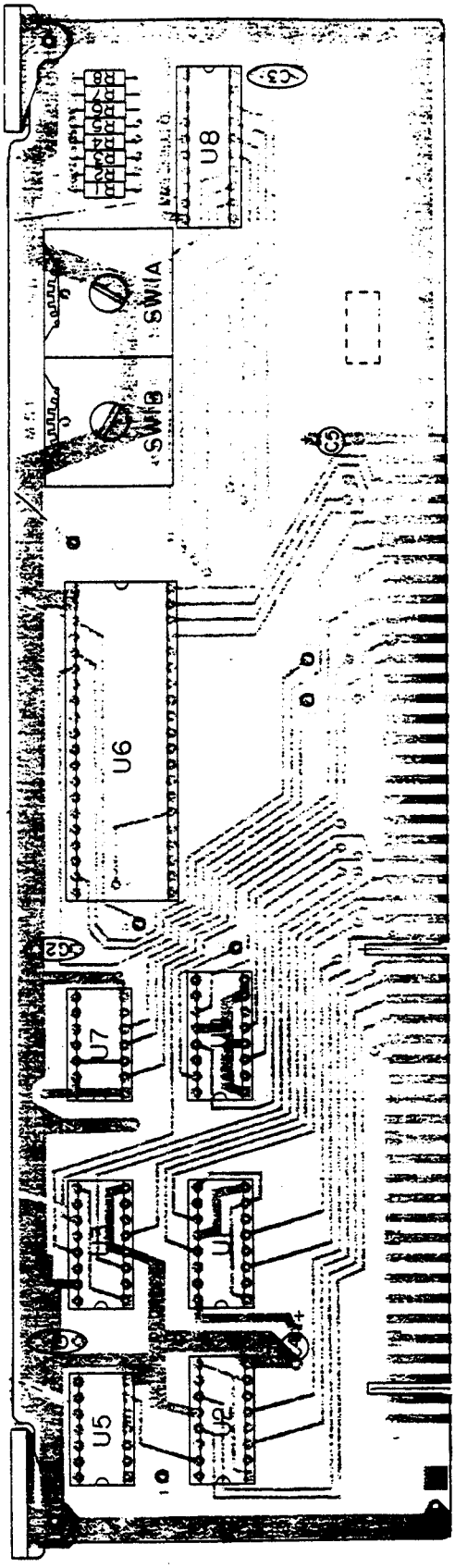
SEE G.P.I.B MANUAL FOR ADDRESS SETTING INSTRUCTIONS.

Figure 08-2. Location of GPIB in Counter

OPTION 08—GENERAL PURPOSE INTERFACE BUS

2020133-B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
08	GPIB Option	2010232		EIP	34257
-1	PCB Assy, GPIB (A102B)	2020133	1	EIP	34257
C1	Cer, .01μF, 20%, 100V	2150003	3	TG - S10	56289
C2	C1				
C3	C1				
C4	Tant, 33μF, 20%, 10V	2300015	2	TAG20 - 33/10 - 50	14433
C5	C4				
R1 thru R8	Comp, 5.6K, 5%, 1/4W	4010562	8	RC07GF562J	81349
SW1A and SW1B	Thumbwheel Switch	4540004	2	1X2270 - 0000	
TP1 thru TP6	P.C. pin 0 .040 diameter	2620032	6	460-2970-02-03	71279
U1 thru U4	Quad 3-state Bus Transciever	3053448	4	MC3448	04713
U5	Hex Inverter	3087404	1	74LS04	27014
U6	General Purpose Interface Adaptor	3058488	1	MC68488	04713
U7	Tri Input NAND Gate	3087410	1	74LS10	27014
U8	Oct Bus Transciever	3084245	1	74LS245	27014



2020133 - B

Figure 08-3. GPIB Component Locator

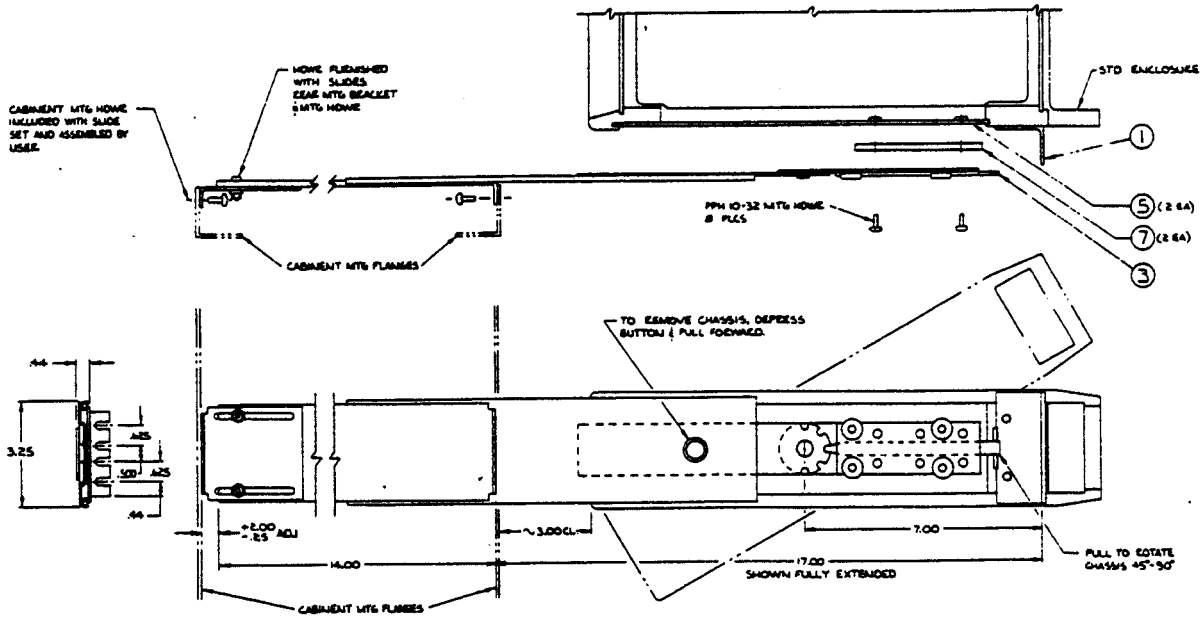
OPTION 10
CHASSIS SLIDE

Option 10 equips your counter with the hardware required to mount the unit in a standard 19" wide console. With the chassis slide installed the counter can be serviced without removing it from the rack.

The option consists of:

OPTION 10 – 2010147

①	Rack Mount Kit	– 2010008-01
③	Slide Set	– 5000189
⑤	Side Panels	– 5210179
⑦	Spacers	– 5210249



1. All MTG HDWR and hole spacing conforms to MIL-STD-189.
2. To install slides in field; Remove top cover and top frame; Mount special side panels (5210179) on Std. enclosure.
3. Item numbers within ◯ symbol are on P/L 2010147. All other items assembled or exploded are shown for clarification or reference only.

Side View of Counter With Option 10 Installed

Appendix A
Accessories

FURNISHED ACCESSORIES

Line Cord
Manual

ACCESSORIES AVAILABLE FOR PURCHASE

REMOTE SENSOR OPTIONS (FOR EXTENDED FREQUENCY, OPTION 06)

BAND NUMBER	PART NUMBER	FREQUENCY RANGE
91	2030022-00	26.5–40 GHz
92	2030029-00	40–60 GHz
93	2030030-00	60–90 GHz
94	2030031-00	90–110 GHz
95	2030038-00	50–75 GHz
96	2030059-00	33–50 GHz

SPECIFICATIONS

TABLE A-1. SPECIFICATIONS

BAND 4
Used with 548A Counter and 590 Frequency Extension Kit

OPTION	91	92	93	94	95	96
SELECT BAND	41	42	43	44	42 or 43	41 or 42
Waveguide Band	Ka	U	E	W	V	Q
Range	26.5–40 GHz	40–60 GHz	60–90 GHz	90–110 GHz	50–75 GHz	33–50 GHz
Sensitivity (typ)	-25dBm (-20 dBm min.)	-25 dBm	-25 dBm	-25 dBm	-25 dBm	-25 dBm
Waveguide Size	WR-28	WR-19	WR-12	WR-10	WR-15	WR-22
Waveguide Flange	UG-599/U	UG-383/U	UG-387/U	UG-387/U	UG-385/U	UG-383/U
Max. Input (typ)	+5 dBm	+5 dBm	+5 dBm	+5 dBm	+5 dBm	+5 dBm
Damage Level	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+10 dBm
Aquisition Time (typ)	<2.5 sec	<2.5 sec	<2.5 sec	<2.5 sec	<2.5 sec	<2.5 sec

EXAMPLE: If desired measurement is 60 - 90 GHz, the required equipment is:

Model 548A with Option 06 - Extended Frequency and
Model 590 - Extended Frequency Cable Kit with Option 93 - Remote Sensor

INSTALLATION

Before connecting the remote sensor to the frequency source, verify that the power level is within the limits specified for the sensor.

Connect the long LO cable from the upper jack to the remote sensor. When using the sensor option 91, use the SMA-TNC adapter in the 590 kit. Connect the short IF cable from the lower jack to the Band 3 input.

CAUTION

Static discharge or ground loops can damage or destroy the diode in a remote sensor. Always connect the LO cable to the counter first, then touch the shield to the body of the sensor before connecting.

Be sure that the counter and waveguide port to which the sensor will connect have a common ground. If in doubt, connect with a ground strap before connecting the remote sensor.

OPERATION

After connection, select band 41,42,43, or 44 on the 548A counter (equipped with option 06). Select the band by:

This counter is identified by two sets of numbers, the model number 545A or 548A and a serial number that is located on a label affixed to the rear panel. Both numbers must be mentioned in any correspondence regarding this counter.

Press BAND [4] [1] or 42, 43, or 44.

Be certain that the band selected coincides with the remote sensor in use. See specifications in Table A-1.

NOTE

Frequency limits (low/high) and power meter function (Option 02) only operate to 26.5 GHz.

REPAIR

If loss of sensitivity occurs, the diode may be damaged. the 91 sensor diode can be replaced; all others require factory repair.

To replace the 91 sensor diode, unscrew the knurled cap and pull out the diode. Replace it with a !N53B type diode that can be ordered from EIP by part number 2730053-00 or directly from the manufacturer:

Alpha Industries, Inc.
20 Sylvan Road
Woburn MA 0-807

EIP has an assembly exchange program for rapid repair of damaged units. Consult factory for details.

SERVICE KIT

The service kit for the 545A/548A counter contains the following items and the kit itself is useful as a carrying case.

2000017-01	Calibration Kit
2020147-01	GPIB/BCD Extender Board
2020184-01	Standard Extender Board
2020185-01	Band 2 Extender Board
2040221-01	Cable, BNC to Select
2040222-01	Cable, BNC to PC JK
2610054-00	Test Cable, BNC E/Z Hook
5000094-00	IC Extractor Tool

SERVICE KIT

The service kit for the 545A/548A counter will contain the following items.

2000017 – SERVICE KIT
2020147 – GPIB/BCD EXTENDER CARD
2020184 – STANDARD EXTENDER BOARD
2020185 – BAND 2 EXTENDER BOARD
2040221 – CABLE, BNC TO SELECT
2040222 – CABLE, BNC TO PC JK
2610054 – TEST CABLE, BNC E/Z HK
5000094 – IC EXTRACTOR TOOL

This kit is useful as a carrying case.

Appendix B
List of Manufacturers

FSCM	MANUFACTURER
0000X	Any Manufacturer of this product.
00656	Aerovox Inc., 740 Belleville Ave, New Bedford, MA 02741
00809	Croven Ltd., Whitby, Ontario, Canada
01121	Allen-Bradley Co., South Milwaukee, WI 53204
01295	Texas Instruments Inc., Dallas, TX 75222
02660	Amphenol Connector Div., Bunker Ramo Corp., Broadview, IL 60153
02735	Solid State Div. RCA Corp., Somerville, NJ 08876
04618	American Pamcor Inc., Paoli, PA 19301
04713	Motorola Inc., Semiconductor Div., Phoenix, AZ 85008
06665	Precision Monolithic Inc., 1500 Space Park Drive, Santa Clara, CA 95050
07263	Fairchild Semiconductor, Mountain View, CA 94040
08717	Sloan Company, Sun Valley, CA 91352
09353	C & K Components Inc., Watertown, MA 02172
11236	CTS of Berne Inc., Berne, IN 46711
11237	CTS, Keen, Paso Robles, CA 93446
12463	Optronics Mfg., 2420 S. 60th St., Omaha, NE 68106
14158	AVX, Filters, 10080 Willow Creek Rd., San Diego, CA 92131
14298	American Components Inc., Conshohocken, PA 19428
14433	ITT Semiconductor Div., West Palm Beach, FL 33401
14455	Quality Hardware Mfg. Co., 12605 Daphine, Hawthorn, CA 90250
14655	Cornell Dubilier, Dept. 150, Ave. L, Newark, NJ 07101
18324	Signetics Corp., Sunnyvale, CA 94086
23880	Stanford Applied Engineering Inc., Santa Clara, CA 95050
23036	Pamotor Inc., Burlingame, CA 94010
24546	Corning Glass Works, Bradford, PA 16701
26654	Varadyne Ind., Santa Monica, CA 90404
27014	National Semiconductor Corp., Santa Clara, CA 95051
28480	Hewlett-Packard Co., Palo Alto, CA 94304
29990	ATC Div., Phase Ind., Huntington Station, NY 11746
34257	EIP Microwave Inc., Santa Clara, CA 95134
34649	Intel Corp., 3585 SW 198th Ave., Aloha, OR 97005
51406	Murata Corp. of America, 1148 Franklin Rd., Marietta, GA 30068
56289	Sprague Electric Co., North Adams, MA 01247
59660	Tusonix Inc., 2155 Forbes Bldg., Tucson, AZ 85705
70903	Belden Corp., Chicago, IL 60644
71590	Centralab Div., Globe-Union Inc., Milwaukee, WI 53201
72136	Electro Motive Corp., Sub. of Int. Elect. Corp., Florence, Santa Clara, CA 95050
72259	Nytronics Inc., Pelham Manor, NY 10803
72982	Erie Technological Products Inc., Erie, PA 16512
73445	Amperex Electronic Corp., Hicksville, NY 11802
80031	Mepco/Electra Inc., Morristown, NJ 07960
80740	Beckman Instruments Inc., Fullerton, CA 92634
81349	Military Specification
86797	Rogan Bros. Inc., Skokie, IL 60076
91637	Dale Electronics Inc., Columbus, NE 68601
95275	Vitramon Inc., Bridgeport, CT 06601
98291	Sealectro, Mamaroneck, NY 10544
99800	Delavan Div. American Precision Industries, East Aurora, NY 14052