"The fact that we are here today to debate raising America's debt limit is a sign of leadership failure. It is a sign that the U.S. government can't pay its own bills. It is a sign that we now depend on ongoing financial assistance from foreign countries to finance our government's reckless fiscal policies.

Increasing America's debt weakens us domestically and internationally. Leadership means that 'the buck stops here.' Instead, Washington is shifting the burden of bad choices today onto the backs of our children and grandchildren.

America has a debt problem and a failure of leadership. Americans deserve better."

--- Quote from then–Senator Barack Hussein Obama on the increasing the debt limit, which he voted against in 2006, as recorded in the Congressional Record for the Senate S. 2237–8 March 16, 2006. He never even bothered to vote on the debt limit in 2007 or 2008. Change!

(rpc.senate.gov/public/_files/alternativestothedebtlimitincreasev20.pdf)
Fig. 4—Directory Number Translator
**Fig. 5—Example of Mobile DN Assignment**

<table>
<thead>
<tr>
<th>INDEX</th>
<th>NON-DOC</th>
<th>NON-NON</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**NOTE 1:**
NOC 1 IS FOR MWX-222, NGN 1 IS ASSIGNED FOR 222-SXXX, AND NGN 127 IS CHOSEN ARBITRARILY FOR THIS EXAMPLE

**LEGEND:**
- DN = DIRECTORY NUMBER
- MTSO = MOBILE TELEPHONE SWITCHING OFFICE
- NGN = NUMBER GROUP NUMBER
- NOC = NORMALIZED OFFICE CODE
Fig. 6—Line Equipment Number Translator
Fig. 7—Trunk Group Number Translator Auxiliary Block

Fig. 8—Trunk Group Number Translator Auxiliary Block for Loop-Around Trunks
Fig. 9 — Trunk Network Number to Trunk Group Number Translator Auxiliary Block for Loop-Around Trunks

Fig. 10 — Trunk Group Number Supplementary Table Translator
Fig. 11—Trunk Network Number to Trunk Group Number Translator Auxiliary Block for Cell Site Trunks

Legend:
- TCC - TRUNK CLASS CODE
- TGN - TRUNK GROUP NUMBER
- VR - VOICE RADIO NUMBER
- VRCNHNL - RADIO CHANNEL NUMBER
- WRON - NUMBER OF WORDS IN AUXILIARY BLOCK

Fig. 12—Pseudo Route Index Expansion Tables for PRI 045, 057, 058, 059, 060, and 061

Legend:
- PRI - PSEUDO ROUTE INDEX
- TGN - TRUNK GROUP NUMBER

Fig. 13—Route Index Expansion Table for RI 131

Legend:
- RI - ROUTE INDEX
- RS - RETURN SUPERVISION
- TGN - TRUNK GROUP NUMBER

Page 50
Fig. 14—Directory Number to Serial Number Translator
<table>
<thead>
<tr>
<th>WORD</th>
<th>WRON</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td><strong>0</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>0</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>1</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>2</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>3</strong></td>
</tr>
</tbody>
</table>

**CELL SITE TRUNKING TRANSLATOR**

**CELL MASTER STATUS TRANSLATOR**

**CELL MASTER EQUIPAGE TRANSLATOR**

**CELL MASTER LOCATION TRANSLATOR**

Fig. 15 — Cell Site Translator
AUTOPLEX System 100 Feature Document / #1A ESS – Part 3

Fig. 16.—Cell Site Trunking Translator
Fig. 17—AMPS Miscellaneous Information Translator (Sheet 1 of 2)
LEGEND:

- CMAX - MAXIMUM NUMBER OF ACCESS CHANNELS THE MOBILE HAS TO SCAN
- CPA - COMBINED PAGING AND ACCESS
- CPT - CELLSITE PROCESS COUNTER THRESHOLD
- DCT - DIVERSITY COUNTER THRESHOLD
- DTX - DISCONTINUOUS TRANSMISSION
- FGDIFF - FRAME GAIN DIFFERENTIAL
- GCSCF - GLOBAL CELL SITE POWER CONTROL FLAG
- GMPCF - GLOBAL MOBILE POWER CONTROL FLAG
- LOCREQ - LOCATION REQUEST LIMIT
- LPCF - LONG PAGE BUNDLING
- MPCT - MOBILE PROCESS COUNTER THRESHOLD
- N-1 - NUMBER OF PAGING CHANNELS THE MOBILE HAS TO SCAN
- NEWACC - NEW ACCESS CHANNEL
- NO. B - NUMBER OF BYTES (8 BITS)
- NO. C - NUMBER OF CELLS
- OVALI - ORIGIN VOLUME LOCATION IDENTIFIER
- POLC - PAGING CELL IDENTIFIER
- RCF - READ CONTROL FILLER WORD
- RSV - ROAMER SERVICE VALIDATION
- STD - SAT DETECT THRESHOLD
- SUI - SYSTEM IDENTIFICATION NUMBER
- SLPP - SKIP LOCATE PERIOD VALUE
- SNM - SERIAL NUMBER
- TEF - TRAFFIC EVENT FAILURE
- TEVT - TRAFFIC EVENT SUCCESS
- WNN - NUMBER OF WOES IN THE AUXILIARY BLOCK

Fig. 17—AMPS Miscellaneous Information Translator (Sheet 2 of 2)
NOTE:
1. FOUR I/O FRAMES PER I/O GROUP

LEGEND:
IOMP - INPUT/OUTPUT MICROPROCESSOR
IDUC - INPUT/OUTPUT UNIT CONTROLLER
IDUS - INPUT/OUTPUT UNIT SEPARATOR

Fig. 19—I/O Member Configuration (Note 1)
Fig. 20—I/O Processor Member Number Translator (Sheet 1 of 2)
LEGEND:
- ABO-ABQ - INDICATES WHETHER PORT 0-2, RESPECTIVELY, IS EQUIPPED WITH ANSWER BACK (HANDSHAKING)-O
- ACU - INDICATES WHETHER AN AUTOMATIC CALL UNIT IS CONNECTED TO THE CHANNEL-0
- AP - INDICATES WHETHER AN APPLICATION IS CONTROLLING THE LINK-1
- CNLSPD - CHANNEL SPEED OF THE CHANNEL
- CNTRLPT - INDICATES WHETHER THE CONTROL PULSE POINT IN A CC-GCP POINT OR ANOTHER TYPE OF POINT-0 OR 1
- CPADR - CONTROL PULSE POINT OCTAL ADDRESS
- DSO-DSZ - DATA SET INDICATOR FOR PORT 0-2, RESPECTIVELY
- DSTYPE - TYPE OF DATA SET ON THE CHANNEL
- FXD - INDICATES WHETHER THE CHANNEL IS HALF OR FULL DUPLEX-1
- IDCTYPE - TYPE OF I/O CONTROLLER ON THE CHANNEL-7
- IDCO-IDCT5 - EQUIPAGE FIELDS FOR I/O UNIT CONTROLLERS 0-15, RESPECTIVELY
- IDGRP - I/O GROUP
- IFO - I/O FRAME
- IOUS - I/O UNIT SELECTORS
- IQDSPTYPE - TYPE OF IQDS CURRENTLY BEING USED-001
- LCI - HARDWARE LDI NUMBER
- MDPT - UNIPOLAR CDP POINT ADDRESS OF THE FIRST OF EIGHT SIGNAL DISTRIBUTOR POINTS NEEDED PER I/O FRAME
- MPD-MP1 - EQUIPAGE STATUS OF MICROPROCESSOR 1 OR 2, RESPECTIVELY
- MMN - OTHER I/O MEMBER NUMBER IN THE I/O FRAME
- PPAD - PULSE POINT ADDRESS
- PIPSOURCE - INDICATES THE FORMAT OF THE IOUS PULSE POINT SOURCE-1
- PT0-PT12 - EQUIPAGE OF PORT 0-3, RESPECTIVELY
- PUBSPLNT - ADDRESS OF THE SET OF SCAN POINTS FOR THE PUB TO THE I/O FRAME
- PUBSCPT - ADDRESS FOR THE SET OF SCAN POINTS OF THE PUB SERVING THIS FRAME
- SC - TYPE OF TRANSMISSION ON THE CHANNEL-0
- SCNPT - SUPERVISORY MASTER SCANNER OCTAL SCAN POINT ADDRESS OF THE POWER CONTROL SWITCH
- WROWN - NUMBER OF WORDS IN AUXILIARY BLOCK

Fig. 20—I/O Processor Member Number Translator (Sheet 2 of 2)
(a) ITEMS SCOPT AND PUBSCOPT SPECIFY THE SCAN POINT ADDRESS OF THE POWER CONTROL SWITCH ASSIGNED TO EACH IOSU AND THE SCAN POINT ADDRESS OF THE PUB (PERIPHERAL UNIT BUS) SERVING THIS FRAME, RESPECTIVELY. THE SCOPT AND PUBSCOPT LEAD DESIGNATIONS ARE AS FOLLOWS:

<table>
<thead>
<tr>
<th>POINT</th>
<th>LEAD DESIGNATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>SC0</td>
<td>OSCBP (POSITIVE LEAD)\nSCBN (NEGATIVE LEAD)</td>
</tr>
<tr>
<td>SC1</td>
<td>OSCAP\nOSCAN</td>
</tr>
<tr>
<td>SC2</td>
<td>ASCBP\nASCBN</td>
</tr>
<tr>
<td>SC3</td>
<td>ASCAP\nASCAN</td>
</tr>
<tr>
<td>SC4</td>
<td>1SCBP\n1SCBN</td>
</tr>
<tr>
<td>SC5</td>
<td>1SCAP\n1SCAN</td>
</tr>
<tr>
<td>SC6</td>
<td>BSACP\nBSBON</td>
</tr>
<tr>
<td>SC7</td>
<td>BSACP\nBSSCAN</td>
</tr>
</tbody>
</table>

Fig. 21—I/O Processor Frame Scan Point Assignment and Lead Designations (Sheet 1 of 3)
(b) ITEMS MDPNT AND PUPMPNT SPECIFY THE BIPOLAR CPS (CENTRAL PULSE DISTRIBUTOR) POINT ADDRESS OF THE SIGNAL DISTRIBUTOR POINTS NEEDED PER I/DGS AND THE SET OF BIPOLAR POINTS FOR THE PUB TO I/O FRAME, RESPECTIVELY. THE MDPNT AND PUPMPNT LEAD DESIGNATIONS ARE AS FOLLOWS:

<table>
<thead>
<tr>
<th>POINT</th>
<th>LEAD DESIGNATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>MD0</td>
<td>DCOSP</td>
</tr>
<tr>
<td></td>
<td>DCOSN</td>
</tr>
<tr>
<td>MD1</td>
<td>GCACKP</td>
</tr>
<tr>
<td></td>
<td>GCACKN</td>
</tr>
<tr>
<td>MD2</td>
<td>ACOSP</td>
</tr>
<tr>
<td></td>
<td>ACSN</td>
</tr>
<tr>
<td>MD3</td>
<td>AACKP</td>
</tr>
<tr>
<td></td>
<td>AACKN</td>
</tr>
<tr>
<td>MD4</td>
<td>1COSP</td>
</tr>
<tr>
<td></td>
<td>1COSN</td>
</tr>
<tr>
<td>MD5</td>
<td>1CACKP</td>
</tr>
<tr>
<td></td>
<td>1CACKN</td>
</tr>
<tr>
<td>MD6</td>
<td>BDOSP</td>
</tr>
<tr>
<td></td>
<td>BDOSN</td>
</tr>
<tr>
<td>MD7</td>
<td>BCACKP</td>
</tr>
<tr>
<td></td>
<td>BCACKN</td>
</tr>
</tbody>
</table>

Fig. 21—I/O Processor Frame Scan Point Assignment and Lead Designations (Sheet 2 of 3)
(c) Item CPADR Specifies a Unipolar CPD Point. The CPD Points are Assigned in Consecutive Order for the Entire Group of I/O Processors (0-63). The Lead Designations are as follows:

For An Even Numbered CPD

<table>
<thead>
<tr>
<th>CPD Point</th>
<th>Lead Designations</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONTROL POINTS FOR IDUS A</td>
<td>XXXX N</td>
</tr>
<tr>
<td></td>
<td>XXXX P</td>
</tr>
<tr>
<td>CONTROL POINTS FOR IDUS B</td>
<td>XXXX N</td>
</tr>
<tr>
<td></td>
<td>XXXX P</td>
</tr>
</tbody>
</table>

For An Odd Numbered CPD

<table>
<thead>
<tr>
<th>CPD Point</th>
<th>Lead Designations</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONTROL POINTS FOR IDUS A</td>
<td>XXXX N</td>
</tr>
<tr>
<td></td>
<td>XXXX P</td>
</tr>
<tr>
<td>CONTROL POINTS FOR IDUS B</td>
<td>XXXX N</td>
</tr>
<tr>
<td></td>
<td>XXXX P</td>
</tr>
</tbody>
</table>

XXX is the 4-digit number representing CPD points in the CPD assignment tables, representing (from left to right) Half, Group, Row, and Column.

Fig. 21—I/O Processor Frame Scan Point Assignment and Lead Designations (Sheet 3 of 3)

<table>
<thead>
<tr>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>13</th>
<th>12</th>
<th>7</th>
<th>6</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>NTPI = 27</td>
<td>UTYN = 59</td>
<td>MEMN = EVEN NUMBERED MEMBER NUMBER</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- MEMN = MEMBER NUMBER
- NTPI = NONTRUNK PROGRAM INDEX
- UTYN = UNIT TYPE NUMBER

Fig. 22—Master Scanner Number and Central Pulse Distributor Subtranslator Word
LEGEND:

CSN - CELL SITE NUMBER
CSN - END OF NUMBER INDICATOR
WRNO - NUMBER OF WORDS IN AUXILIARY BLOCK
HRNO - LENGTH OF HEAD TABLE

Fig. 23 — Cell Dialup Channel Translator
Fig. 24 — Cell Master Status Translator
<table>
<thead>
<tr>
<th>MOBILE ATTENUATION CODE</th>
<th>MOBILE-STATION POWER CLASS</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>0  4  8</td>
</tr>
<tr>
<td>001</td>
<td>4  4  8</td>
</tr>
<tr>
<td>010</td>
<td>8  8  8</td>
</tr>
<tr>
<td>011</td>
<td>12 12 12</td>
</tr>
<tr>
<td>100</td>
<td>16 16 16</td>
</tr>
<tr>
<td>101</td>
<td>20 20 20</td>
</tr>
<tr>
<td>110</td>
<td>24 24 24</td>
</tr>
<tr>
<td>111</td>
<td>28 28 28</td>
</tr>
</tbody>
</table>

Fig. 25—Interpretation of Mobile Attenuation Codes and Mobile Station Power Class
Fig. 26—Cell Master Equipage Translator (Sheet 1 of 2)
Overview

This is my version of the analog–to–digital converter for Scotty Sprowls’ Modularized Spectrum Analyzer (MSA) project. The original analog–to–digital converter design is SLIM–ADC–16.

The spectrum analyzer’s Analog–to–Digital Converter (ADC) stage is based around (two) 16–bit Analog Devices AD7685 serial ADCs There is no need for any external (manual) reference adjustment to set the ADC conversion range and it’ll still obtain excellent resolution in the MSA/VNA systems. Each ADC will digitize its input of 0 to 5 volts into a binary serial stream equal to 0 to 65,535. This equates to approximately 76.3 µV per bit resolution. Only one AD7685 will be used in this spectrum analyzer design. The second AD7685 for the VNA phase detector will be constructed and discussed in a future article.

The "MAGVOLTS" magnitude output from the logarithmic detector is connected to the ADC’s input. This voltage range should be from +0.4 volts to +2.4 volts (over the AD8306’s 100 dB range). The AD7685 will then convert +0.4 volts to a bit value of 5,243. The +2.4 volts will convert to a bit value of 31,457. The overall dynamic bit range is equal to 26,214 bits (31,457 – 5,243). Therefore, the conversion factor for the MSA’s combination of logarithmic detector and 16–bit ADC is: 100 dB / 26,214 bits = 0.0038 dB per bit resolution. This is what determines the final displayed RF power magnitude on the spectrum analyzer.

Both ADCs will capture and clock–out their data simultaneously. The MSA software commands both ADCs to begin conversion with a single toggle of the CONVERT line. 16 toggles of the SERCLOCK line causes the AD7685 to output a serial stream of 16 bits. The Serial Data Output (SDO) of the AD7685 (pin 7) has a limited current (500 µA) capability. Therefore, a 2N2222 transistor provides buffering and current sinking to drive the WAIT and ACK lines on the controlling computer’s parallel port (LPT). The computer’s LPT port is normally a TTL–compatible input with an internal pull–up resistor to +5V. Having two pull–up resistors shouldn’t hurt and should help make the circuit compatible with different computers. You may have to experiment with different BIOS settings for your computer’s parallel port if you encounter problems.

To control the AD7685, two main control lines are used: CONVERT and SERCLOCK. Both AD7685 chips are controlled simultaneously. Before conversion, these lines are held low. To begin conversion, the CONVERT line is commanded high. This initiates the AD7685’s in–chip sample–and–hold circuit. While CONVERT is high, any voltage changes on the analog input(s) will be disregarded. Also, the SDO output will be high impedance (WAIT and ACK will be high impedance).

It takes approximately 2 µS for the 16–bit conversion (sample) to take place. When complete, the 16–bit data word will be stored in the AD7685’s buffer (hold). After conversion is complete, the CONVERT signal is brought low. The Most Significant Bit (MSB) D15 will be present on the SDO pin (there is a logic inversion by the 2N2222 on the line back to the computer, WAIT or ACK). Each time the SERCLOCK is brought low, the data word is shifted by one bit.

The data is valid 15 nanoseconds after the negative edge of SERCLOCK. It takes sixteen SERCLOCKs to shift out the 16–bit data word. If no data is clocked out of the buffer, the next CONVERT signal will overwrite the buffer.
MSA Software

The MSA software works in this way:

1.) It begins with CONVERT and SERCLOCK lines held low.

2.) CONVERT to high. This initiates the A-to-D conversion process.

3.) CONVERT to low. High-to-low takes about 5 µS, allowing the minimum 2 µS conversion time requirement.

4.) SERCLOCK to high. D15 MSB is valid on SDO, and is read by the computer.

5.) SERCLOCK to low. Next data word bit is shifted.

6.) SERCLOCK to high. D14 bit is valid on SDO, and is read by the computer.

7.) SERCLOCK to low. Next data word bit is shifted.

8.) SERCLOCK to high. D13 bit is valid on SDO, and is read by the computer.

9.) SERCLOCK to low. Next data word bit is shifted.

10.) SERCLOCK to high. D12 bit is valid on SDO, and is read by the computer.

11.) SERCLOCK to low. Next data word bit is shifted.

12.) SERCLOCK to high. D11 bit is valid on SDO, and is read by the computer.

13.) SERCLOCK to low. Next data word bit is shifted.

14.) SERCLOCK to high. D10 bit is valid on SDO, and is read by the computer.

15.) SERCLOCK to low. Next data word bit is shifted.

16.) SERCLOCK to high. D9 bit is valid on SDO, and is read by the computer.

17.) SERCLOCK to low. Next data word bit is shifted.

18.) SERCLOCK to high. D8 bit is valid on SDO, and is read by the computer.

19.) SERCLOCK to low. Next data word bit is shifted.

20.) SERCLOCK to high. D7 bit is valid on SDO, and is read by the computer.

21.) SERCLOCK to low. Next data word bit is shifted.

22.) SERCLOCK to high. D6 bit is valid on SDO, and is read by the computer.

23.) SERCLOCK to low. Next data word bit is shifted.

24.) SERCLOCK to high. D5 bit is valid on SDO, and is read by the computer.
25.) **SERCLK** to low. Next data word bit is shifted.

26.) **SERCLK** to high. D4 bit is valid on SDO, and is read by the computer.

27.) **SERCLK** to low. Next data word bit is shifted.

28.) **SERCLK** to high. D3 bit is valid on SDO, and is read by the computer.

29.) **SERCLK** to low. Next data word bit is shifted.

30.) **SERCLK** to high. D2 bit is valid on SDO, and is read by the computer.

31.) **SERCLK** to low. Next data word bit is shifted.

32.) **SERCLK** to high. D1 bit is valid on SDO, and is read by the computer.

33.) **SERCLK** to low. Next data word bit is shifted.

34.) **SERCLK** to high. D0 bit is valid on SDO, and is read by the computer.

35.) **SERCLK** to low. SDO is high impedance.

36.) Subsequent **SERCLKs** do nothing and the conversion process repeats.

**Video Filter**

This magnitude ADC circuit is designed with an optional input video bandwidth filter based around an Analog Devices ADG704 4-channel multiplexer. This will allow a selection of additional capacitance to be placed in parallel with the AD7685’s input.

The ADG704 can be used to select four different integration times (video bandwidths) for the final displayed magnitude signal. The capacitor values for the video filter were chosen arbitrarily and you may wish to experiment with different values.

The video filter helps to remove excessive noise before the analog-to-digital conversion process and is a simple way to “narrow” to the response of the spectrum analyzer.

The MSA software video filter selections:

<table>
<thead>
<tr>
<th>V0</th>
<th>V1</th>
<th>Filter Selection</th>
<th>Video Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>S1 – 1000 pF</td>
<td>Wide</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>S2 – 0.01 µF</td>
<td>Medium</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>S3 – 0.1 µF</td>
<td>Narrow</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>S4 – 1.0 µF</td>
<td>Extra Narrow</td>
</tr>
</tbody>
</table>

Scotty’s software video filter controls may still be experimental at this point.

The video bandwidth determines the spectrum analyzer’s capability to discriminate between two different power levels. This is because a narrower video bandwidth will remove noise in the logarithmic detector output. This filter is used to “smooth” the final display by removing any noise from the signal envelope.

([wikipedia.org/wiki/Spectrum_analyzer#Video_bandwidth](https://wikipedia.org/wiki/Spectrum_analyzer#Video_bandwidth))
Overview of the ADG704 video filter (right) and AD7685 16–bit ADC (left).

Both the AD7685 and the ADG704 are in 10–pin MSOP packages, so MSOP–to–DIP converters were used for soldering convenience.

Polystyrene capacitors are used in the video filter section and the large non–polarized orange capacitor (1 µF) is for the "extra narrow" video filter selection.

The 2N2222 transistor buffer is on the lower–left.

The SOT–89 device is a Sieko S–81250SG precision 5 volt regulator.

The "reference" voltage (pin 1) for the AD7685 should be very well filtered and regulated for maximum performance and magnitude resolution.
The capacitors for the video filters should be low-leakage, non-microphonic, high-quality film types (polystyrene, Teflon, etc.). Otherwise, switching in the video filters could cause a small shift in the magnitude voltage.

The selectable video bandwidths are somewhat arbitrary. The wide video bandwidth is for the highest sweeping speed, medium for general speed, and narrow for very slow sweeping or to get the most accurate magnitude/phase data.

The ADG704 video filter is optional and if not used, a single 1000 pF capacitor should be added across the input (pin 3) of the AD7685.

This corresponds to a "wide" video filter as you do want a little bit of low-pass filtering here to keep the noise out, but not too much.
Completed overview of the analog-to-digital converter with video filter.

It's mounted inside an old 800 MHz cellular phone receive pre-amplifier case.

The SMA jack on the left is used for the MAGVOLTS input.

A 1000 pF feed-through capacitor (lower-left) is used for the +12 VDC power input.

180 pF feed-through capacitors are used for the ADG704 and AD7685 control lines. These should be low-value capacitors to avoid distorting the control waveforms.
Alternate overview.

AD7685 voltage conversions:

<table>
<thead>
<tr>
<th>Analog Input (Volts)</th>
<th>Digital Output (Hexadecimal – Binary)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.999924</td>
<td>FFFF 1111111111111111</td>
</tr>
<tr>
<td>2.500076</td>
<td>8001 1000000000000000</td>
</tr>
<tr>
<td>2.500000</td>
<td>8000 1000000000000000</td>
</tr>
<tr>
<td>2.499924</td>
<td>7FFF 0111111111111111</td>
</tr>
<tr>
<td>0.000076</td>
<td>0001 0000000000000000</td>
</tr>
<tr>
<td>0.000000</td>
<td>0000 0000000000000000</td>
</tr>
<tr>
<td>0.400000</td>
<td>147B 0001010001111011</td>
</tr>
<tr>
<td>2.400000</td>
<td>7AE1 0111101011110001</td>
</tr>
</tbody>
</table>

The two Least Significant Bits (LSB) are somewhat noisy which yields a more realistic 14-bit resolution. Therefore, with this circuit, the magnitude resolution of the MSA is actually around 0.01 dB.
Finished case overview.

The MAGVOLTS input of this module will then be connected back to the Logarithmic Detector stage. Be sure to use coaxial cable for this connection.

The CONVERT, SERCLOCK, MAGDATA, V0, and V1 lines go back to their respective latches on the Control Board.

CONVERT goes to latch P3D7.

SERCLOCK goes to latch P3D6.

MAGDATA goes to WAIT (DB25 pin 11).

V0 goes to latch P4D0.

V1 goes to latch P4D1.
Scotty’s Spectrum Analyzer
Analog-to-Digital Converter with Video Filter
MSA Equiv. SLIM-ADC-16

+5 VDC to ADC704

10 μF

S-81250

22 μF

10kΩ

S-81250SGY is Sieko precision 5V regulator.

Video filter capacitors should be low-leakage & not polarized.

PxDx lines go to the corresponding outputs on the Control Board.
"You didn’t build that!"

How the fuck do you close a hole in the ground? LOL! Change!
Jon Gibson of Lake Lincolndale, New York posted a sign in his yard protesting the anti–Second Amendment "NY SAFE Act."

After someone stole four of his signs, he decided to put up a motion–activated trail camera...
Well, well, well... It's the Somers, New York Police Department in action.

Change!
The U.S. Marine Corps War Memorial in Washington D.C. closed because of Obongo and the Democrats failure to make a budget which doesn't bankrupt the entire country.

These memorials cost very little to run, and a troop of Boy/Girl Scouts could (should) manage them while the federal government "shuts down."
Uh–oh!

Looks like someone knocked over the barricades and are now illegally trespassing on federal government property!

Don't let Obama know or he'll send a Predator drone after you!
Don't worry, it was just the Syracuse Honor Flight showing Obama what they think of his "change."
The "shutdown" World War 2 memorial in Washington D.C. has better security than our borders!
Remember when Americans could park their own cars without the government’s help?